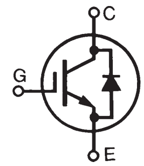
IXYS

High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

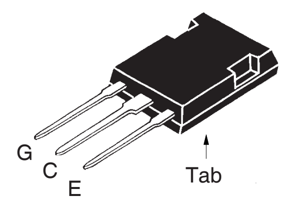
IXBX25N250

V_{CES} = 2500V
I_{C90} = 25A
$V_{CE(sat)}$ ≤ 3.3V



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	2500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	2500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	55	A
I_{C90}	T_C = 90°C	25	A
I_{CM}	T_C = 25°C, 1ms	180	A
SSOA	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 4.7Ω	I_{CM} = 80	A
(RBSOA)	Clamped Inductive Load	V_{CES} ≤ 2000	V
P_C	T_C = 25°C	300	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) From Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
F_C	Mounting Force	20..120 / 4.5..27	N/lb.
Weight		6	g

PLUS247™



G = Gate   E = Emitter
C = Collector   Tab = Collector

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)		Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V		2500			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}		2.5		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V				50	μA
		T_J = 125°C			3	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V				±100	nA
$V_{CE(sat)}$	I_C = I_{C90}, V_{GE} = 15V, Note 1				3.3	V
		T_J = 125°C		3.4		V

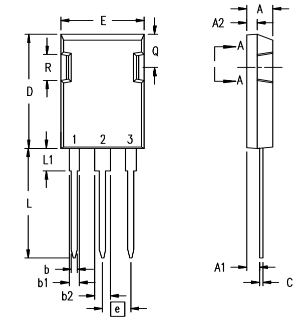
Features
- High Blocking Voltage
- International Standard Package
- Low Conduction Losses

Advantages
- Low Gate Drive Requirement
- High Power Density

Applications
- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generator
- Capacitor Discharge Circuit
- AC Switches

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Min.	Typ.	Max.	
g_{fS}	I_C = 25A, V_{CE} = 10V, Note 1	11	18		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		2450		pF
C_{oes}			96		pF
C_{res}			35		pF
Q_g	I_C = 25A, V_{GE} = 15V, V_{CE} = 1000V		103		nC
Q_{ge}			17		nC
Q_{gc}			43		nC
$t_{d(on)}$	**Resistive Switching times, T_J = 25°C**		55		ns
t_r	I_C = 25A, V_{GE} = 15V		240		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 4.7Ω		145		ns
t_f			640		ns
$t_{d(on)}$	**Resistive Switching times, T_J = 125°C**		54		ns
t_r	I_C = 25A, V_{GE} = 15V		640		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 4.7Ω		140		ns
t_f			510		ns
R_{thJC}				0.42	°C/W
R_{thCS}			0.15		°C/W

PLUS 247™ (IXBX) Outline



Terminals: 1 - Gate
2 - Collector
3 - Emitter

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Min.	Typ.	Max.	
V_F	I_F = 25A, V_{GE} = 0V			2.3	V
t_{rr}	I_F = 25A, $-di_F/dt$ = 100A/μs		1.6		μs
I_{RM}	V_R = 100V, V_{GE} = 0V		37.2		A

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

*Additional provisions for lead to lead voltage isolation are required at V_{DS} > 1200V.

Fig. 1. Output Characteristics @ T_J = 25ºC

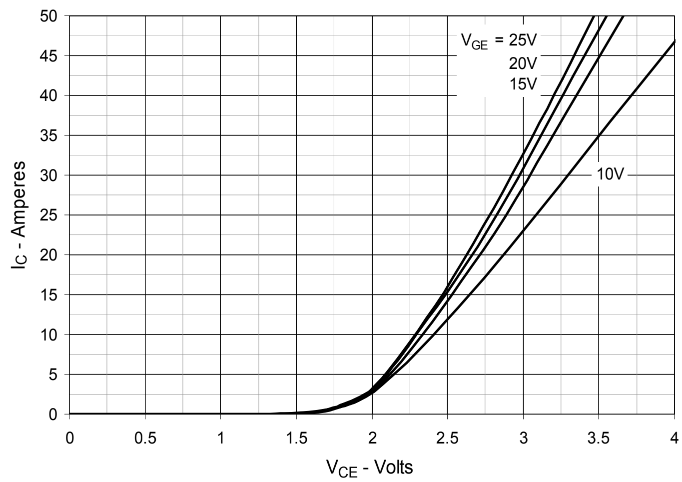


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

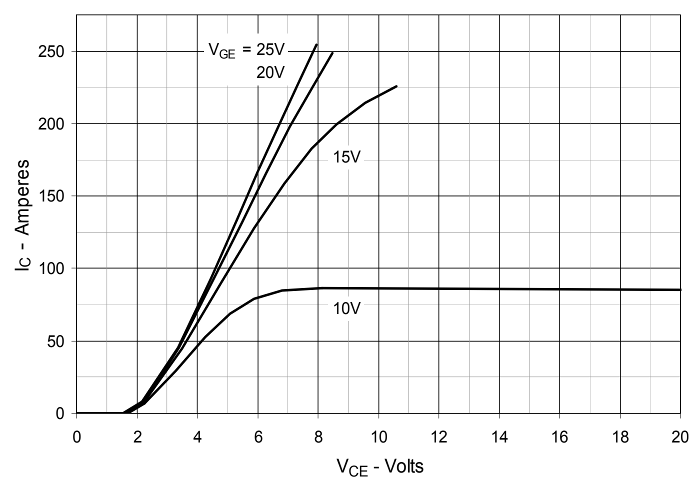


Fig. 3. Output Characteristics @ T_J = 125ºC

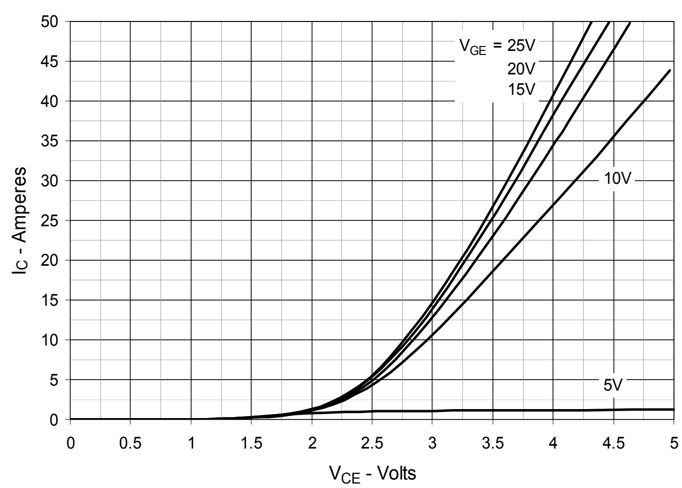


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

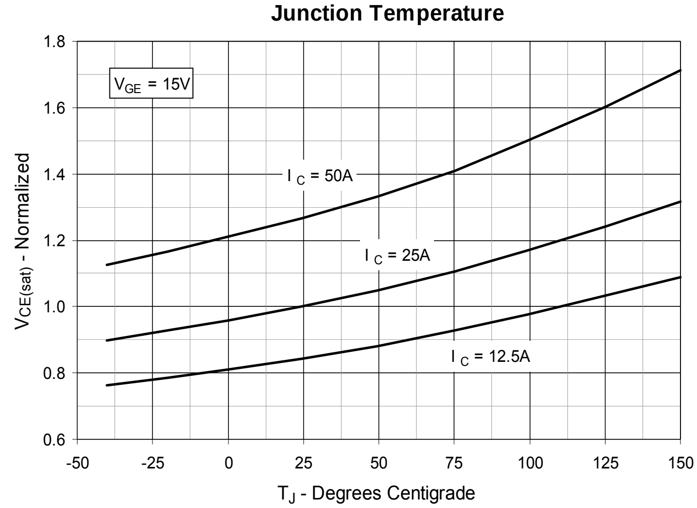


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

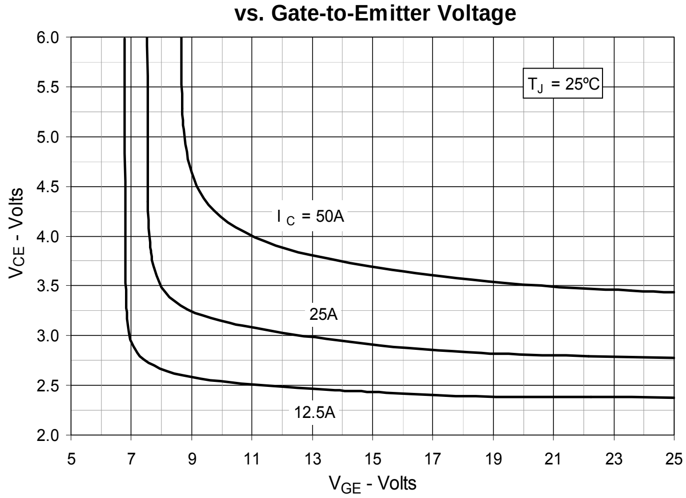


Fig. 6. Breakdown & Threshold Voltages vs. Junction Temperature

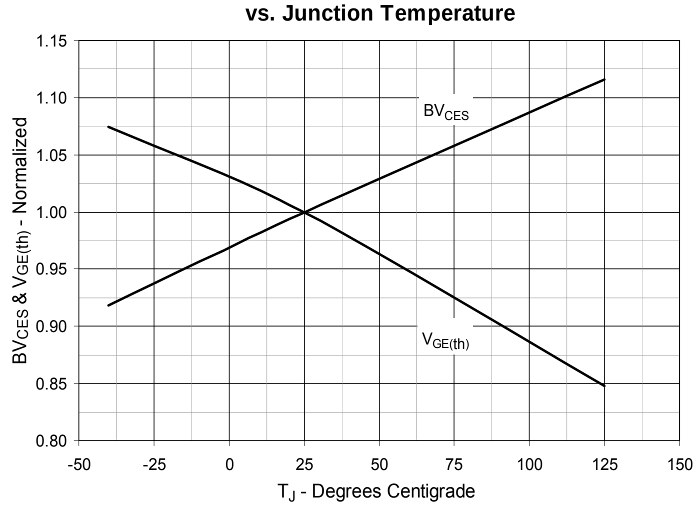


Fig. 7. Input Admittance

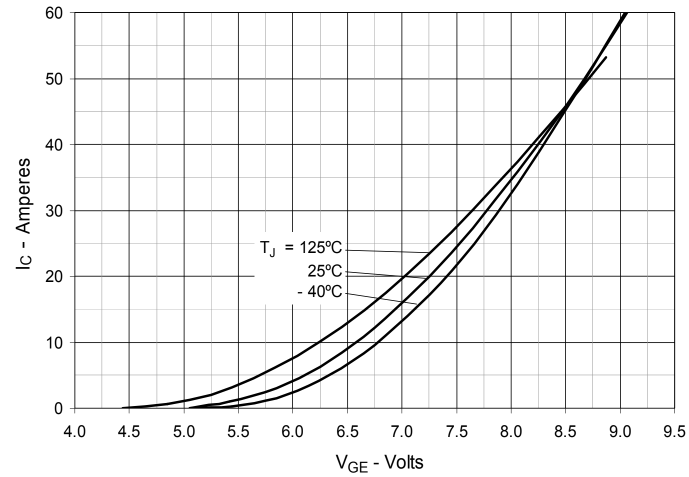


Fig. 8. Transconductance

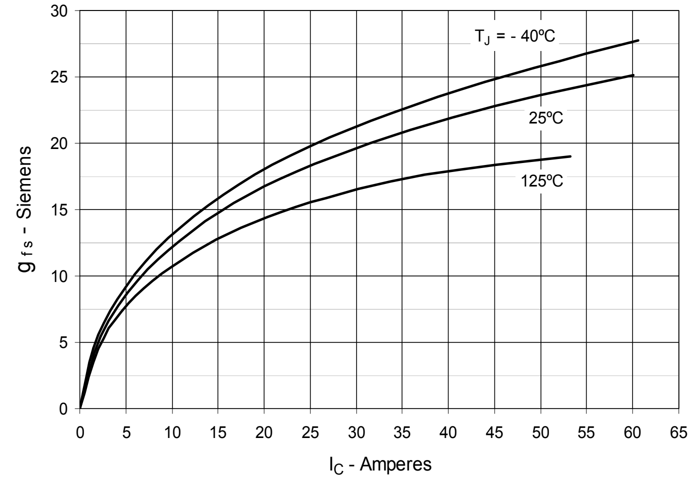


Fig. 9. Forward Voltage Drop of Intrinsic Diode

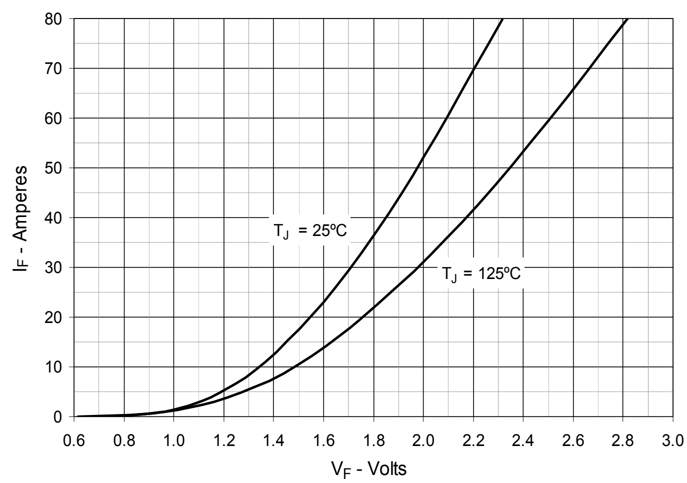


Fig. 10. Gate Charge

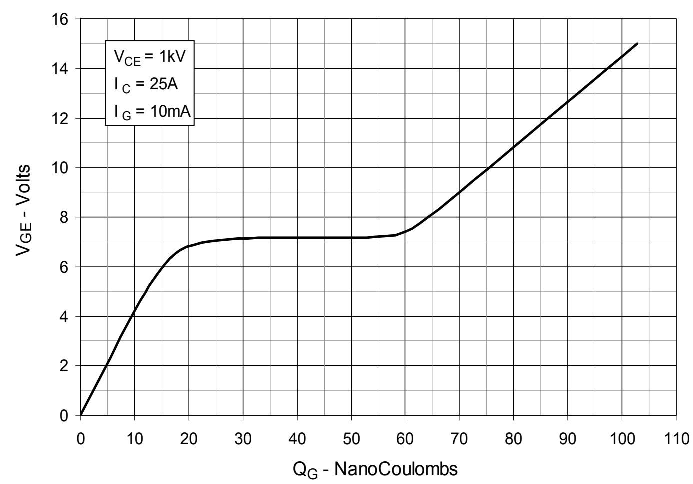


Fig. 11. Capacitance

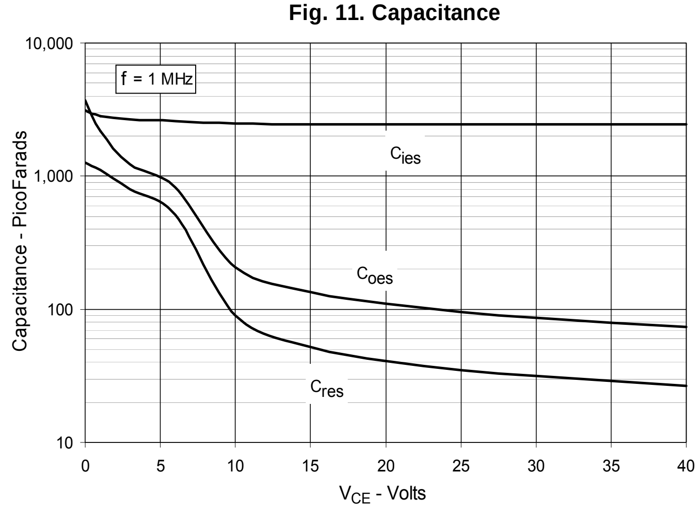


Fig. 12. Reverse-Bias Safe Operating Area

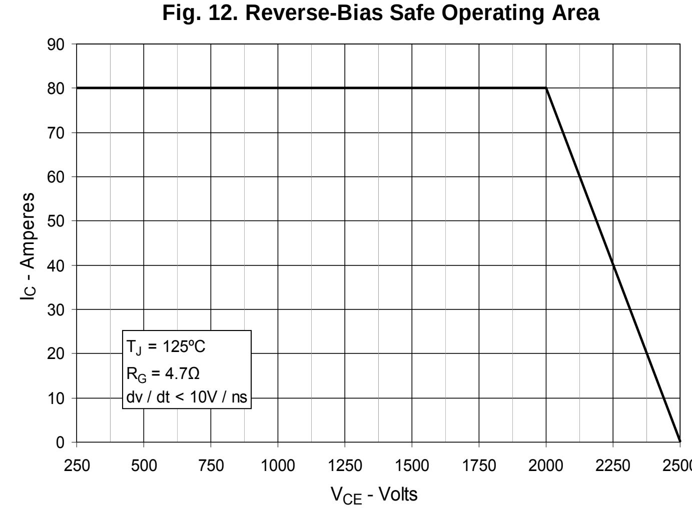


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

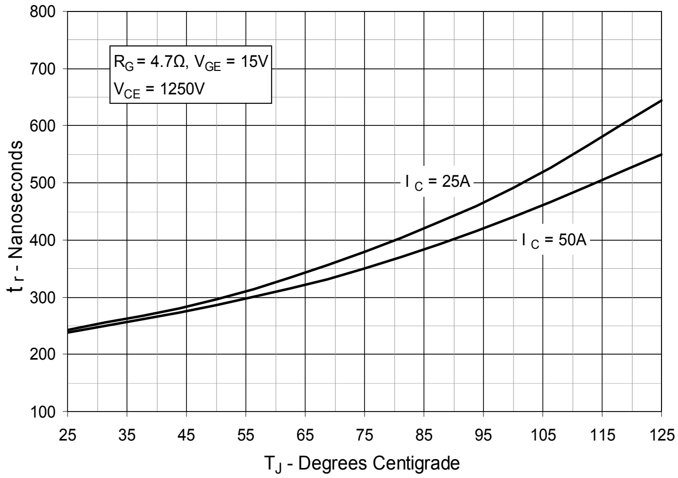


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

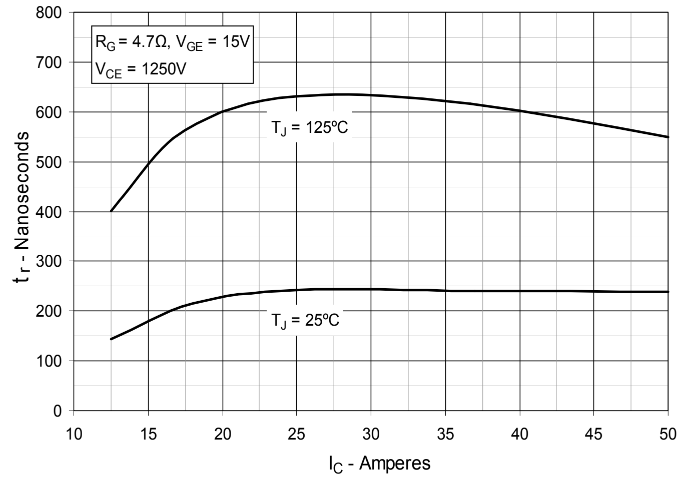


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

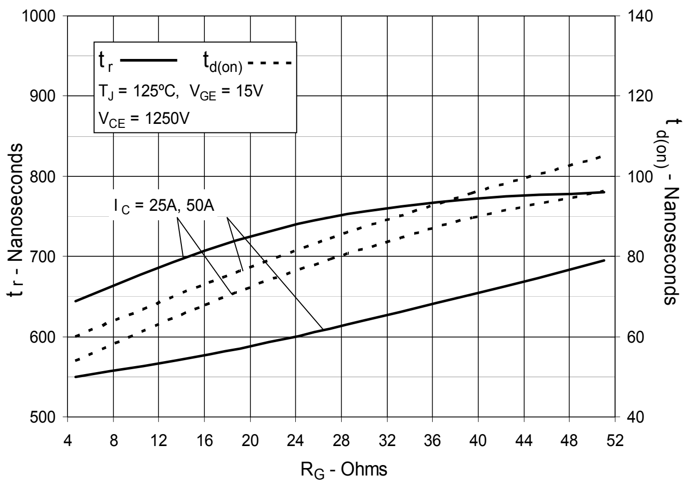


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

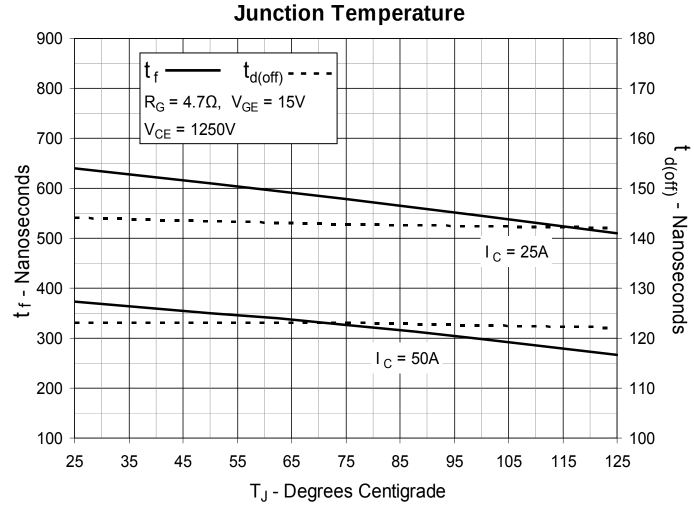


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

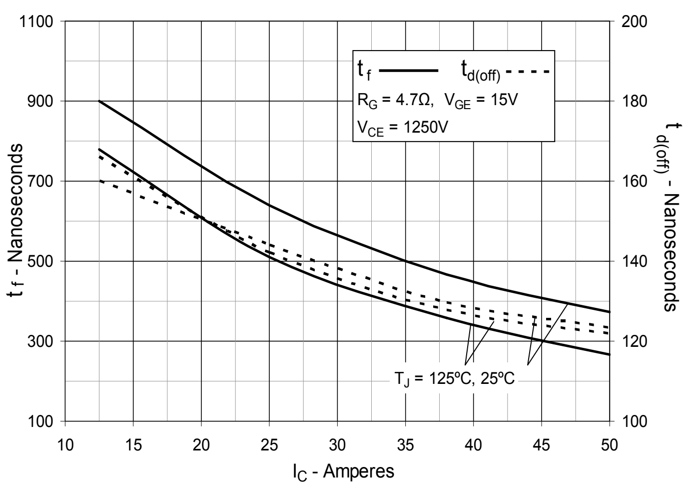


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

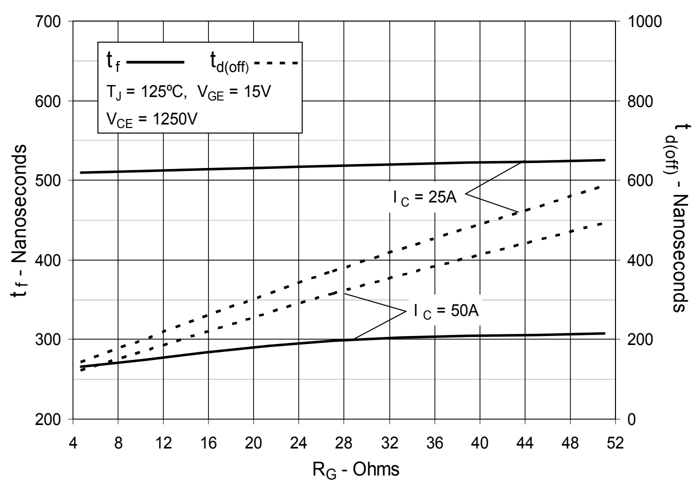


Fig. 19. Maximum Transient Thermal Impedance