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NOT RECOMMENDED FOR NEW DESIGNS

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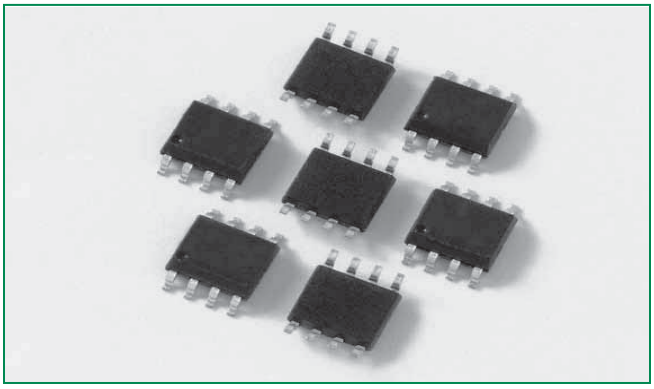
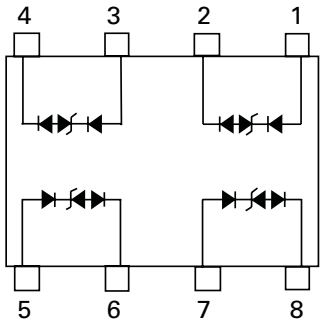
GREEN

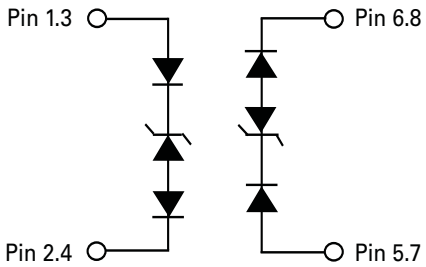
SPLV2.8-4 Series 2.8V 40A TVS Array



Pinout



Functional Block Diagram



Description

The SPLV2.8-4 was designed to protect low voltage, CMOS devices from ESD and lightning induced transients. There is a compensating diode in series with each low voltage TVS to present a low loading capacitance to the line being protected. These robust structures can safely absorb repetitive ESD strikes at ±30kV (contact discharge) per IEC61000-4-2 standard and each structure can safely dissipate up to 40A (IEC61000-4-5, t_P=8/20µs) with very low clamping voltages.

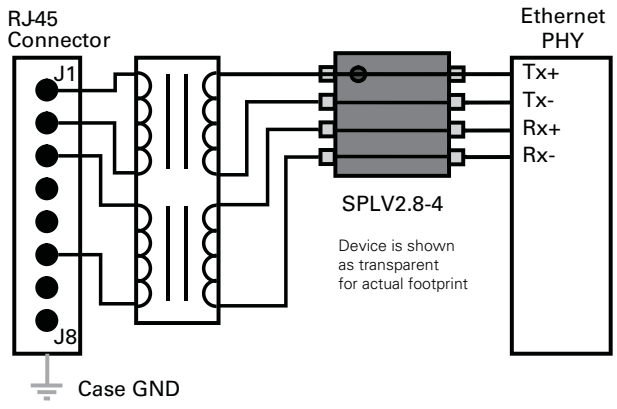
Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 40A (8/20µs)
- Low capacitance of 2pF per line
- Low leakage current of 1µA (MAX) at 2.8V
- SOIC-8 pin (JEDEC MS-012) configuration allows for simple flow-through layout

Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Switching Systems
- Desktops, Servers, and Notebooks
- Analog Inputs
- Base Stations

Application Example



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Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			2.8	V
Reverse Breakdown Voltage	V_{BR}	I_T=2μA	3.0			V
Snap Back Voltage	V_{SB}	I_T=50mA	2.8			V
Reverse Leakage Current	I_{LEAK}	V_R=2.8V (Each Line)			1	μA
Clamping Voltage[1]	V_C	I_{PP}=5A, t_P=8/20μs (Each Line)		7.0	8.5	V
Clamping Voltage[1]	V_C	I_{PP}=24A, t_P=8/20μs (Each Line)		13.9	15.0	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±30			kV
		IEC61000-4-2 (Air)	±30			kV
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$ (Each Line)		0.4		Ω
Diode Capacitance[1]	C_D	V_R=0V, f=1MHz (Each Line)		2.0	2.5	pF

Note: [1]Parameter is guaranteed by design and/or device characterization.

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Power (t_P=8/20μs)	600	W
Peak Pulse Current (t_P=8/20μs)	40	A
Operating Temperature	-40 to 85	°C
Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Figure 1: Capacitance vs. Reverse Voltage

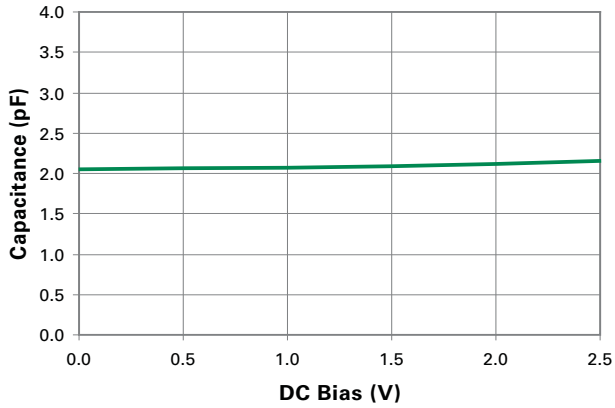


Figure 2: Clamping Voltage vs. I_{PP}

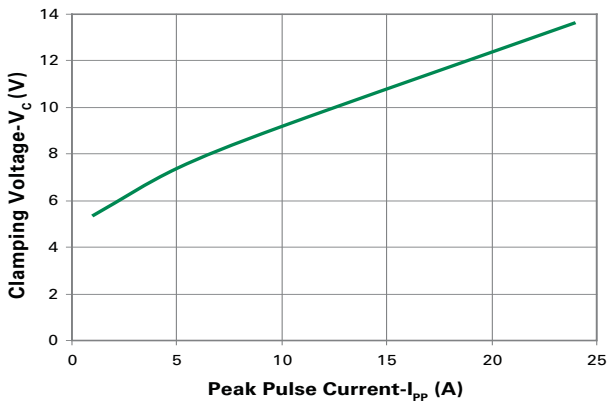
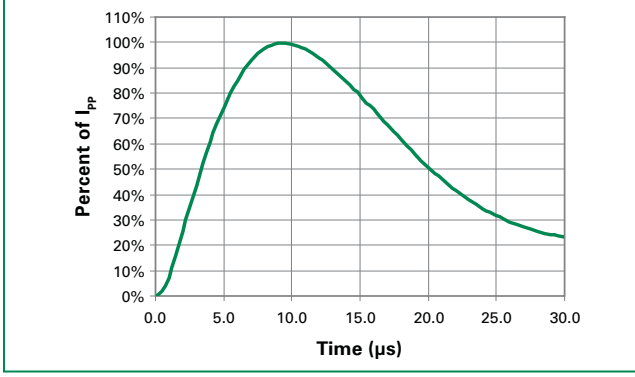


Figure 3: Pulse Waveform



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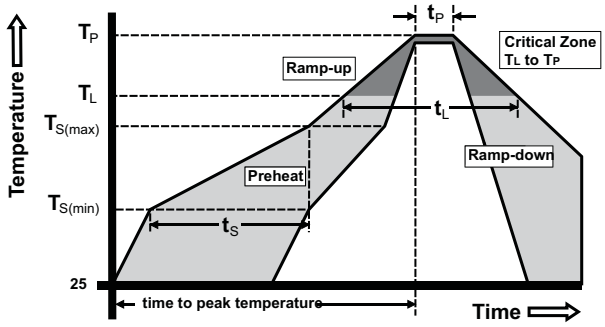
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

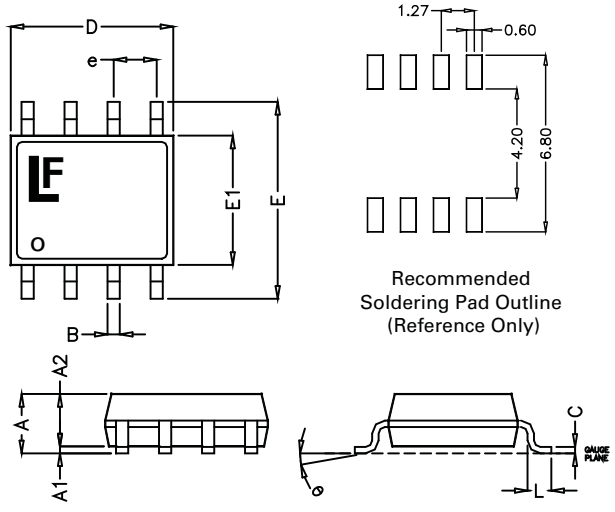
Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — Mechanical Drawings and Recommended Solder Pad Outline



Package	SOIC			
Pins	8			
JEDEC	MS-012			
	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
B	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

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Part Numbering System

SP LV2.8 -4 B T G

- SP: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- LV2.8: Series
- -4: No. of channels
- B: Package, B = SOIC-8
- T: Tape & Reel
- G: G= Green

Part Marking System

U 2.8 -4

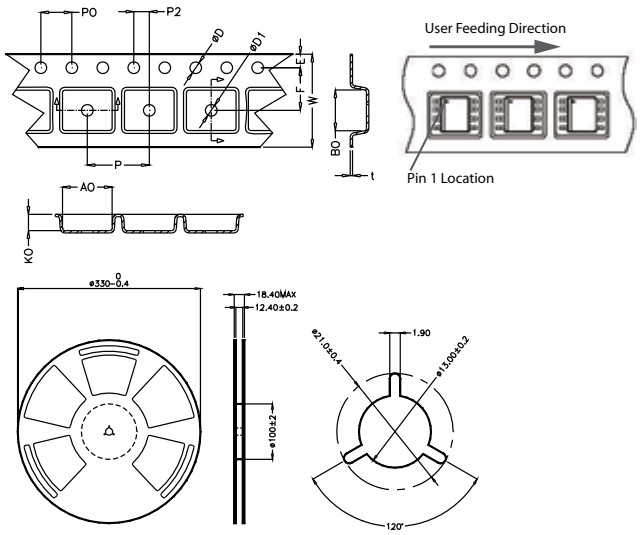
U2.8-4

- U: **Product Series**, U = SPLV2.8
- 2.8: **Voltage Level**
- -4: **No. of channels**

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SPLV2.8-4BTG	SOIC-8	U2.8-4	2500

Embossed Carrier Tape & Reel Specification — SOIC Package



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

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SPLV2.8-4BTG SPLV2.8-4BTG-T SPLV2.8HTG