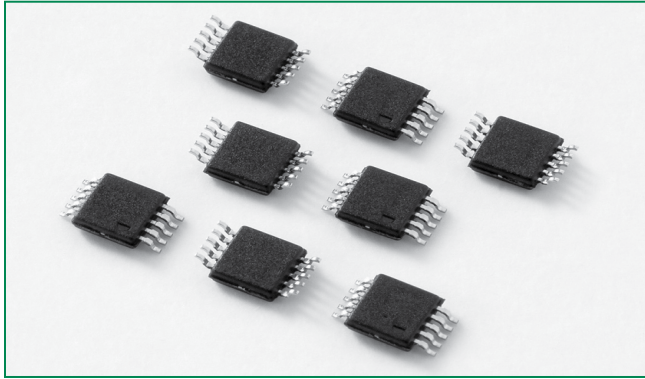


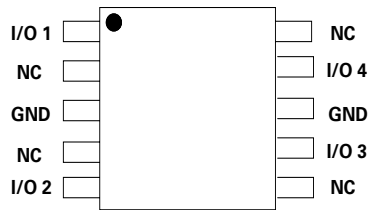
**SP4045 Series 1.5pF 24A Diode Array (HDBaseT)**



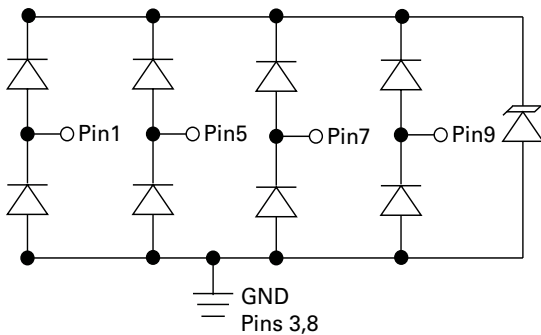
**Description**

The SP4045 integrates low capacitance diodes with an additional zener diode to protect each I/O pin against ESD and high surge events. This robust device can safely absorb up to 24A per IEC 61000-4-5 2<sup>nd</sup> edition ( $t_p=8/20\mu s$ ) without performance degradation and a minimum  $\pm 30kV$  ESD per IEC 61000-4-2 International Standard. Their low loading capacitance also makes them ideal for protecting high speed signal pins.

**Pinout**



**Functional Block Diagram**



**Features**

- Signal-integrity-preserving straight through routing
- Low leakage current of 1 $\mu A$  (MAX) at 3.3V
- ESD, IEC 61000-4-2,  $\pm 30kV$  contact,  $\pm 30kV$  air
- EFT, IEC 61000-4-4, 40A (5/50ns)
- Lightning, IEC 61000-4-5
- 2<sup>nd</sup> edition, 24A (8/20 $\mu s$ )
- Low capacitance of 1.5pF (TYP) per I/O
- AEC-Q101 qualified
- Halogen free, Lead free and RoHS compliant
- Moisture Sensitivity Level (MSL Level-1)

**Applications**

- HDBaseT Protector
- 10/100/1000 Ethernet
- 2.5 and 5 Gigabit Ethernet
- T1/E1 Secondary Protection
- T3/E3 Secondary Protection
- A/V Equipment
- Automotive Ethernet

**Additional Information**



Datasheet



Resources



Samples

Life Support Note:

**Not Intended for Use in Life Support or Life Saving Applications**

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$I_{PP}$	Peak Current ( $t_p=8/20\mu s$ )	24	A
$P_{PK}$	Peak Pulse Power ( $t_p=8/20\mu s$ )	600	W
$T_{OP}$	Operating Temperature	-40 to 125	°C
$T_{STOR}$	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

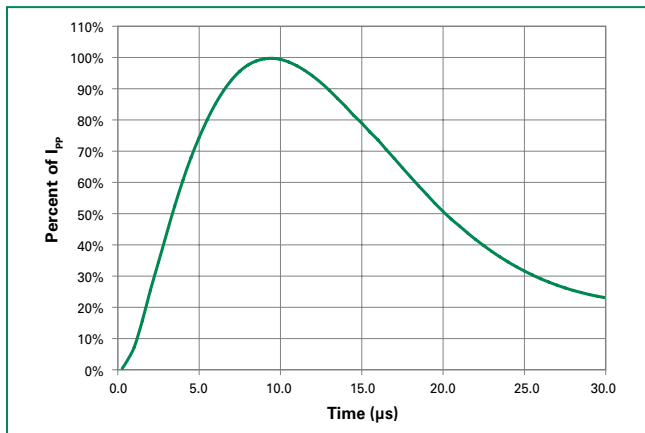
### Electrical Characteristics ( $T_{OP}=25^\circ C$ )

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	$V_{RWM}$				3.3	V
Snap Back Voltage	$V_{SB}$	$I_{SB}=50mA$	2.8			V
Reverse Leakage Current	$I_{LEAK}$	$V_R=3.3V$ , I/O to GND		0.5	1.0	$\mu A$
Clamp Voltage <sup>1</sup>	$V_C$	$I_{PP}=1A$ , $t_p=8/20\mu s$ , Fwd		6.0		V
		$I_{PP}=2A$ , $t_p=8/20\mu s$ , Fwd		7.0		V
Dynamic Resistance <sup>2</sup>	$R_{DYN}$	TLP $t_p=100ns$ , Pin 1 to Pin 2		0.3		$\Omega$
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC61000-4-2 (Contact)	$\pm 30$			kV
		IEC61000-4-2 (Air)	$\pm 30$			kV
Diode Capacitance <sup>1</sup>	$C_{I/O-GND}$	Reverse Bias=0V		1.5		pF

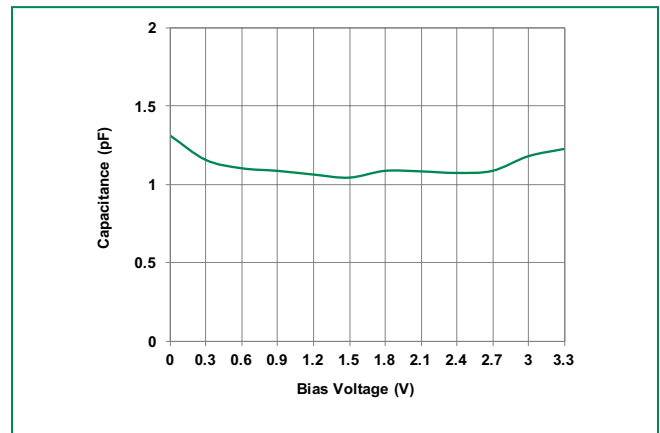
Note: 1. Parameter is guaranteed by design and/or device characterization.

2. Transmission Line Pulse (TLP) test setting : Std.TDR(50 $\Omega$ ),  $t_p=100ns$ ,  $tr=0.2ns$  ITLP and VTLP averaging window: star  $t1=70ns$  to end  $t2=80ns$

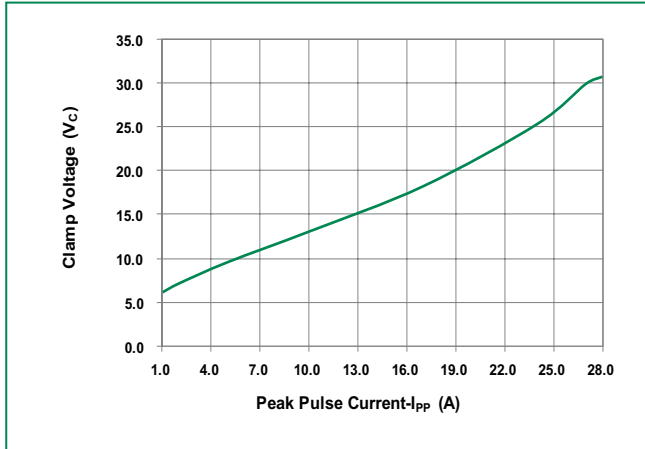
### 8/20 $\mu s$ Pulse Waveform



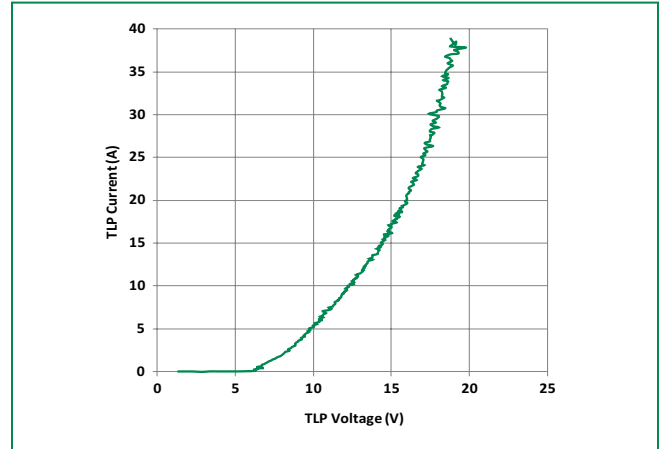
### Capacitance vs. Reverse Bias



**Clamping Voltage vs.  $I_{PP}$**

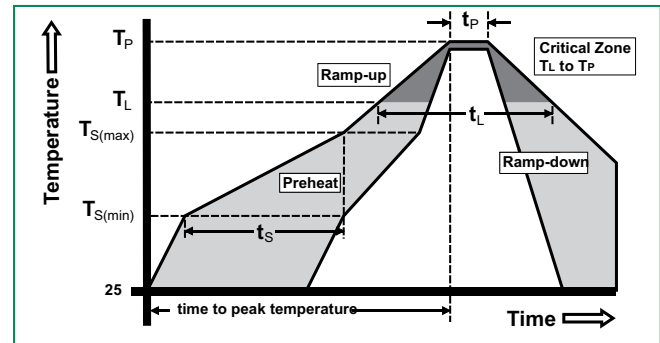


**Transmission Line Pulsing (TLP) Plot (Pin 1 to Pin2)**



**Soldering Parameters**

Reflow Condition		Pb – Free assembly
Pre Heat	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
Average ramp up rate (Liquidus) Temp ( $T_L$ ) to peak		3°C/second max
$T_{s(max)}$ to $T_L$ - Ramp-up Rate		3°C/second max
Reflow	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
Peak Temperature ( $T_p$ )		260 <sup>+0/-5</sup> °C
Time within 5°C of actual peak Temperature ( $t_p$ )		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature ( $T_p$ )		8 minutes Max.
Do not exceed		260°C



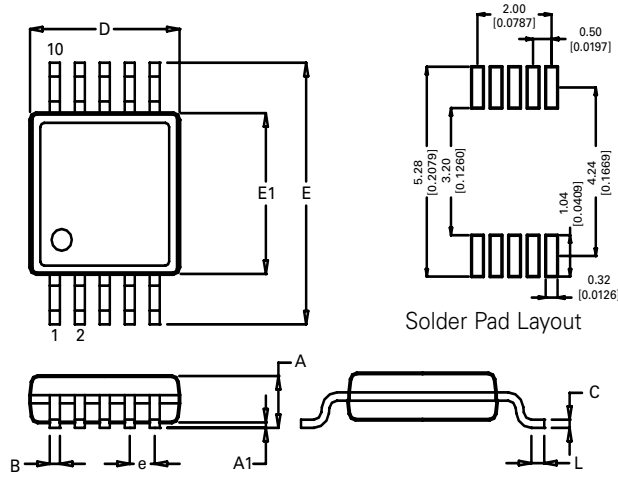
**Product Characteristics**

<b>Lead Plating</b>	Pre-Plated Frame
<b>Lead Material</b>	Copper Alloy
<b>Lead Coplanarity</b>	0.0004 inches (0.102mm)
<b>Substrate material</b>	Silicon
<b>Body Material</b>	V-0 per UL 94 Molded Epoxy

Notes :

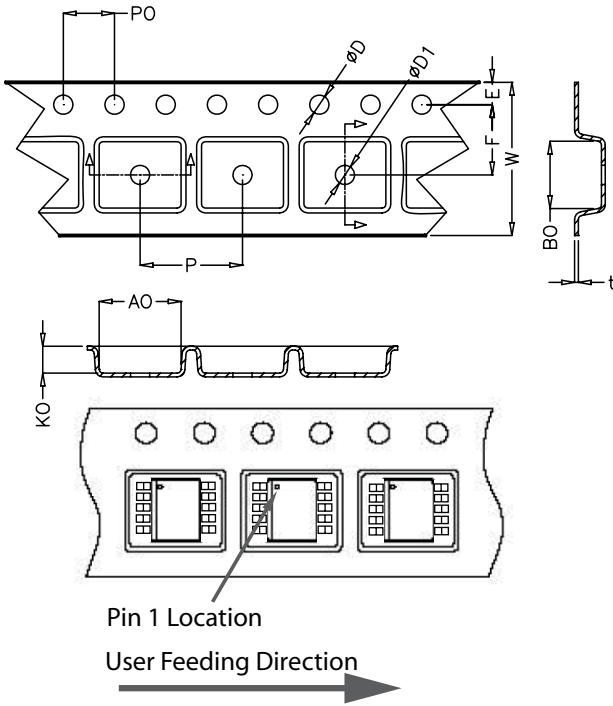
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

**Package Dimensions – MSOP-10**



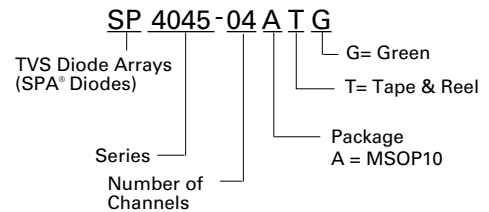
Package	MSOP			
Pins	10			
JEDEC	MO-187			
	Millimeters		Inches	
DIM	Min	Max	Min	Max
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
B	0.17	0.27	0.007	0.011
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.67	5.10	0.184	0.200
E1	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
L	0.40	0.80	0.016	0.032

**Embossed Carrier Tape & Reel Specification – MSOP-10**

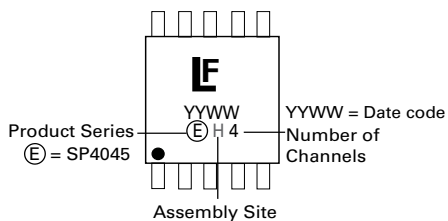


	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.40	5.60	0.213	0.220
D	1.50	1.60	0.059	0.063
D1	1.50 Min		0.059 Min	
PO	3.90	4.10	0.154	0.161
W	11.70	12.30	0.460	0.484
P	7.90	8.10	0.311	0.319
AO	5.20	5.40	0.205	0.213
BO	3.20	3.50	0.126	0.138
KO	1.20	1.50	0.047	0.059
t	0.30 +/- 0.05		0.012 +/- 0.002	

**Part Numbering System**



**Part Marking System**



**Ordering Information**

Part Number	Package	Marking	Min. Order Qty.
SP4045-04ATG	MSOP-10	ⓔ H4	4000

# Mouser Electronics

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