

TVS Diode Arrays (SPA[®] Diodes) Lightning Surge Protection - SP2502L Series

SP2502L Series 3.3V 75A Diode Array

Pinout



SOIC-8 (Top View)

Note: Pinout diagrams above shown as device footprint on circuit board.

Functional Block Diagram



Additional Information



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Description

The SP2502L provides overvoltage protection for applications such as 10/100/1000 Base-T Ethernet and T3/ E3 interfaces. This device has a low capacitance of only 5pF making it suitable for PHY side Ethernet protection and the capability to protect against both longitudinal and differential transients. Furthermore, the SP2502L is rated up to 100A (tp=2/10 μ s) making it suitable for line side protection as well against lightning transients as defined by GR-1089 (intra-building), ITU, YD/T, etc. The application schematic provides the connection information for a PHY side protection scheme of a single differential pair.

Features

- Lightning protection, IEC 61000-4-5, 75A (8/20µs)
- Low clamping voltage
- Low insertion loss, loglinear capacitance
- Combined longitudinal and metallic protection
- Clamping speed of nanoseconds

Applications

- T1/E1 Line cards
- 10/100/1000 BaseT Ethernet
- T3/E3 and DS3 Interfaces

SOIC-8 surface mount

· Lead-Free and RoHS-

Compliant

package (JEDEC MS-012)

GREEN

RoHS

• STS-1 Interfaces

Application Example



The schematic shows protection for a single differential pair as part of a larger high-speed data interface such as Ethernet. The SP2502L provides both metallic (differential) and longitudinal (common mode) protection from lightning induced surge events as specified by regulatory standards such as Telcordia's GR-1089 CORE and ITU K.20 and 21.

The SP2502L protects against both positive and negative induced surge events while the TeleLink fuse provides overcurrent protection for the long term 50/60 Hz power fault events.

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Current (8/20µs)	75	А
Peak Pulse Power (8/20µs)	2100	W
IEC 61000-4-2, Direct Discharge	30	kV
IEC 61000-4-2, Air Discharge	30	kV
Telcordia GR 1089 (Intra-Building) (2/10µs)	100	А
ITU K.20 (5/310µs)	20	А

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
SOIC Package	170	°C/W
Operating Temperature Range	-40 to 125	°C
Storage Temperature Range	–55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOIC - Lead Tips Only)	260	°C
(SUIC - Lead Tips Unly)		

Electrical Characteristics (T _{op} = 25°C)						
Parameter	Symbol	Test Conditions	Min	Тур	Мах	Units
Reverse Stand-Off Voltage	V _{RWM}	I _τ ≤1μA	-	-	3.3	V
Reverse Breakdown Voltage	V _{BR}	l _τ = 2μA	3.3	-	-	V
Snap Back Voltage	V _{SB}	I _T = 50mA	3.3	-	-	V
Reverse Leakage Current	I _R	V _{RWM} = 3.3V	-	-	1	μA
Clamping Voltage, Line-Ground ¹	V _c	I _{pp} = 40A, t _p =8/20 μs	-	-	14	V
Clamping Voltage, Line-Ground ¹	V _c	I _{pp} = 75A, t _p =8/20 μs	-	-	20	V
Clamping Voltage, Line-Ground ¹	V _c	I _{pp} = 100A, t _p =2/10 μs			20	V
Dynamic Resistance, Line-Ground ¹	R _{DYN}	(V _{C2} -V _{C1})/(I _{PP2} -I _{PP1})	-	0.2	-	Ω
Clamping Voltage, Line-Line ¹	V _c	I _{pp} = 40A, t _p =8/20 μs	-	-	20	V
Clamping Voltage, Line-Line ¹	V _c	I _{pp} = 75A, t _p =8/20 μs	-	-	30	V
Clamping Voltage, Line-Line ¹	V _c	I _{pp} = 100A, t _p =2/10 μs			30	V
Dynamic Resistance, Line-Line ¹	R _{DYN}	(V _{C2} -V _{C1})/(I _{PP2} -I _{PP1})	-	0.3	-	Ω
Junction Capacitance ¹	C,	Line to Ground V _R =0V, f= 1MHz	-	5	8	pF
	,	Line to Line, $V_{\mu}=0V$, f= 1MHz	-	2.5	5	pF

1. Parameter is guaranteed by design and/or device characterization.



Pulse Waveform



Capacitance vs. Reverse Bias at 1MHz



Mon-Repetitive Peak Pulse Power vs. Pulse Time

Clamping Voltage vs. I_{PP}



Current Derating Curve





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Soldering Parameters

Reflow Cond	Pb – Free assembly		
	- Temperature Min (T _{s(min)})	150°C	
Pre Heat	- Temperature Max (T _{s(max)})	200°C	
	-Time (min to max) (t _s)	60 – 180 secs	
Average ram	p up rate (Liquidus) Temp (T_L) to peak	3°C/second max	
$T_{S(max)}$ to T_{L} -	3°C/second max		
Deflerer	- Temperature (T _L) (Liquidus)	217°C	
nellow	- Temperature (t _L)	60 - 150 seconds	
Peak Temperature (T _p)		260 ^{+0/-5} °C	
Time within 5°C of actual peak Temperature (t _p)		20 – 40 seconds	
Ramp-down Rate		6°C/second max	
Time 25°C to peak Temperature (T _P)		8 minutes Max.	
Do not exceed		260°C	



Part Marking System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL Recognized compound meeting flammability rating V-0

Part Numbering System



Ordering Information					
Part Number Package Marking Min. Order Qty.					
SP2502LBTG	SOIC-8	SP2502	2500		



Package Dimensions – Mechanical Drawings and Recommended Solder Pad Outline



Package	SOIC				
Pins	8				
JEDEC		MS-012			
Symbol	Millimetres Inches			hes	
Symbol	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A1	0.10	0.25	0.004	0.010	
A2	1.25	1.65	0.050	0.065	
В	0.31	0.51	0.012	0.020	
С	0.17	0.25	0.007	0.010	
D	4.80	5.00	0.189	0.197	
E	5.80	6.20	0.228	0.244	
E1	3.80	4.00	0.150	0.157	
е	1.27 BSC 0.050 BSC) BSC	
L	0.40	1.27	0.016	0.050	

Embossed Carrier Tape & Reel Specification - SOIC Package







Course has l	Millimetres		Inches	
Symbol	Min	Max	Min	Мах
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 ± 0.20		1.574 ± 0.008	
w	11.9	12.1	0.468	0.476
Р	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
К0	2	2.2	0.079	0.087
t	0.30 ± 0.05		0.012 ± 0.002	

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