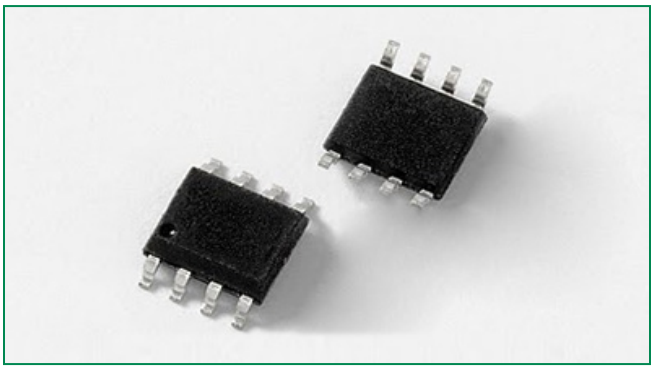
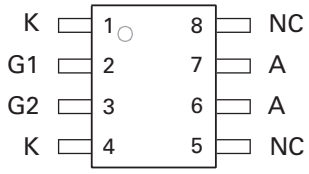
B9110DF, Single Port, ± polarity tracking SLIC protector



Agency Approvals

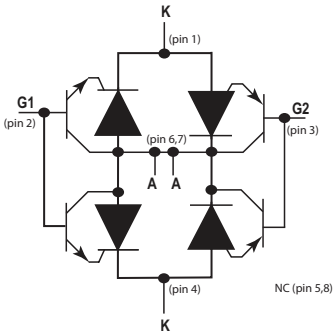
Agency	Agency File Number
	E133083

Pinout



Pin #	Pin Name	Description
1, 4	K	Connect to subscriber lines (Tip or Ring)
2	G1	Connect to battery ($-V_{BAT}$)
3	G2	Connect to battery ($+V_{BAT}$)
6, 7	A	Connect to ground (earth)
5, 8	NC	Not connected

Schematic Symbol



Description

This single port polarity programmable B9110DF protector is specifically designed to protect smart ringing SLICs with dual power supplies. This B9110DF will protect the SLIC interface against lightning induced surges and power fault events. It contains fast switching crowbarring structures that are compatible with the Basic levels outlined in ITU K.20, K.21. For compliance with the Enhanced levels, an additional resistor in series with tip and ring may be required. This programmable protector may also be beneficial for YD/T 950, TIA-968-B, GR-1089-Core Issue 6 and UL/EN/IEC 60950-1 compliance.

The SLIC chipset voltage reference may change as the on-hook/off-hook line condition changes. Therefore, this protector is referenced to the $+V_{BAT}$ and $-V_{BAT}$ references so that its protection thresholds follow these reference voltage changes by approximately 1.4V. The B9110DF gates utilize transistor gain networks so that a low 5 mA current level will activate these four separate protection structures. This allows for easier turn on during slow rising ac power fault events.

Features

- High performance protection for SLICs with $+V_{BAT}$ and $-V_{BAT}$ references and with changing V_{BAT} references
- Wide -110V to +110V programming range
- Low gate current triggering
- ESD Immunity(HBM): JESD22 Class 3B, ≥8KV
- MSL: Level 1 - unlimited
- tracking crowbarring component
- Fails short circuit when surged in excess of its ratings to protect SLIC chipset
- Surge capability does not degrade after multiple surge events within its ratings
- RoHS compliant and lead-free

Applications

- Wireless In the Local Loop (WLL)
- Voice applications which require regenerated POTS
- VoIP applications
- PBX
- FXS applications
- Digital Pair Gain systems (DPG) and Digital Loop Carrier systems (DLC)
- Small Office Home Office (SOHO)

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Absolute Maximum Ratings (T_A =25°C)

Symbol	Parameter	Test Conditions		Value	Unit
V_{DRM}	Repetitive peak off-state voltage	$V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V		-120	V
		$V_{G2(Line)}$ = 0, V_{G1} ≥ -5 V		+120	
I_{PPSM}	Non-repetitive peak impulse current (see Notes 1, 2, 3 and 4)	2/10 µs (Telcordia GR-1089-CORE)		±100	A
		5/310 µs (K.20, K.21 open-circuit voltage wave shape 10/700 µs)		±45	
		10/1000 µs (Telcordia GR-1089-CORE)		±30	
		8/20 µs (IEC 61000-4-5, 2nd Edition)		±110	
I_{TSM}	Non repetitive peak on-state current	50Hz / 60Hz (see Notes 1, 2, 3, 5 and 6)	0.2s	9.0	A
			1s	5.0	
			900s	1.7	
V_{G1M}	Maximum negative battery supply voltage			-110	V
V_{G2M}	Maximum positive battery supply voltage			+110	V
$\Delta V_{(BAT)M}$	Maximum differential battery supply voltage			220	V
T_{STG}	Storage temperature range			-65-150	°C
T_J	Junction temperature			-40-150	°C
T_L	Maximum lead temperature for soldering during 10s			260	°C
$R_{\theta JA}$	Junction to ambient thermal resistance			55	°C /W

NOTES:

1. Initially the component must be in thermal equilibrium with T_J = 25 °C. The surge may be repeated after the component returns to its initial conditions.
2. The rated current values may be applied to either of the Line to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of a single terminal pair).
3. Rated currents only apply if pins 6 & 7 (Ground) are connected together.
4. Applies for the following bias conditions: V_{G1} = -20 V to -110 V, V_{G2} = 0 V to +110 V.
5. EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.
6. Please refer to "I_{TSM} Rating vs Current Duration" table on page 3.

Electrical Characteristics

Symbol	Parameter	Test Conditions		Max	Unit
I_D	Off-state current	V_D=V_{DRM}, $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V (see Note 1)	T_A=25°C	-5	µA
			T_A=85°C	-50	
		V_D=V_{DRM}, $V_{G2(Line)}$=0, V_{G1} ≥ -5V (see Note 1)	T_A=25°C	+5	
			T_A=85°C	+50	
$I_{G1(Line)}$	Negative-gate Leakage current	$V_{G1(Line)}$ = V_{G1M}		-5	µA
$I_{G2(Line)}$	Positive-gate Leakage current	$V_{G2(Line)}$ = V_{G1M}		+5	µA
$V_{G1L(BO)}$	Gate-Line impulse breakover voltage	V_{G1}=-100V, I_T=-100A (see Note 2)	2/10µs	-15	V
			10/100µs	-11	
$V_{G2L(BO)}$	Gate-Line impulse breakover voltage	V_{G2}=+100V, I_T=+100A (see Note 2)	2/10µs	+15	V
			10/100µs	+11	
I_H	Holding current	V_{G1}=-60V, I_T=-1A, di/dt=1A/ms		-150 (min)	mA
I_{G1T}	Negative-gate trigger current	I_T=-5A, $t_{p(g)}$≥20µs, V_{G1}=-60V		+5	mA
I_{G2T}	Positive-gate trigger current	I_T=+5A, $t_{p(g)}$≥20µs, V_{G2}=+60V		-5	mA
V_{GT}	Gate trigger voltage	I_T=-3A, $t_{p(g)}$≥20µs, V_{GG}=-100V		1.4	V
C_O	Line-ground off-state capacitance	f=1MHz,V_D=-3V, G1 & G2 open circuit		110	pF

NOTES:

1. V_D is the supply voltage during test
2. Voltage measurements should be made with an oscilloscope with limited bandwidth (20 MHz) to avoid high frequency noise.

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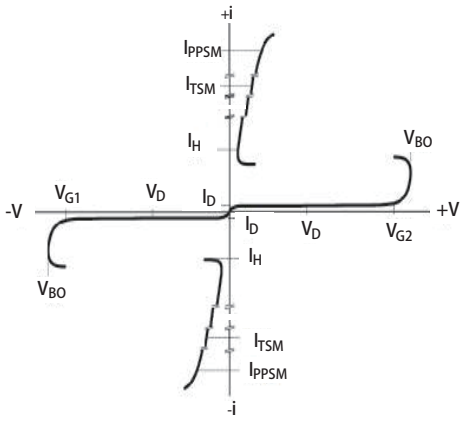
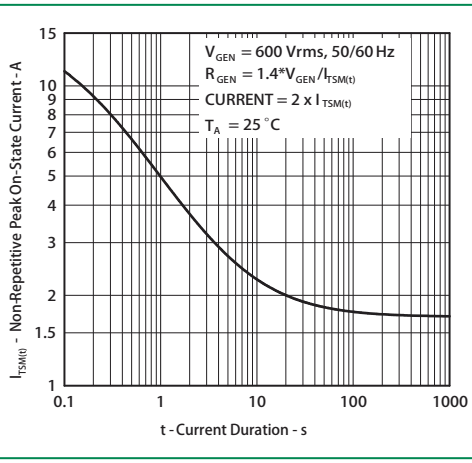
SIDACtor® Protection Thyristors
Programmable tracking Protection

V-I Characteristics



Parameter	Symbol
Off-state current	I_D
Repetitive peak off-state voltage	V_D
Holding current	I_H
Non-repetitive peak impulse current	I_{PPSM}
Non repetitive peak on-state current	I_{TSM}
Breakover voltage	V_{BO}
Gate-Line impulse breakover voltage	V_{G1}, V_{G2}

I_{TSM} Rating vs Current Duration(T_A=25°C)



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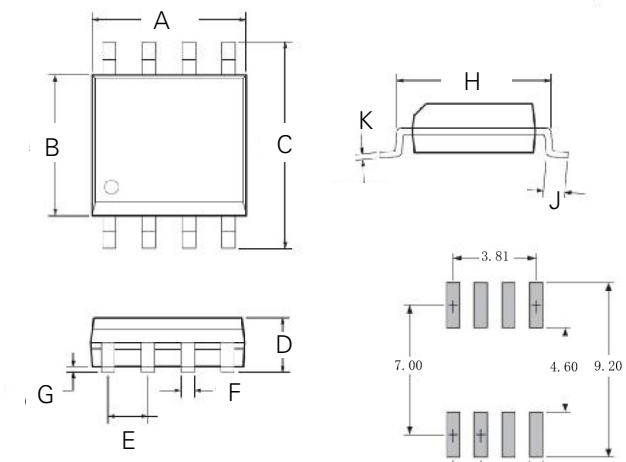
SIDACtor® Protection Thyristors
Programmable tracking Protection

Dimensions — MS-012 (Wide Body)



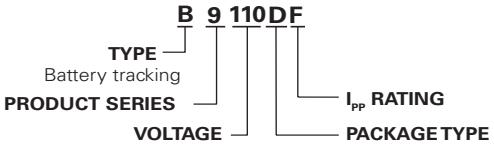
Layout Pattern

Dimensions are in Millimeters

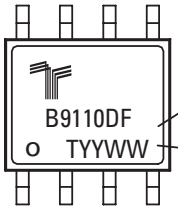
Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.205	0.217	5.20	5.50
B	0.205	0.217	5.20	5.50
C	0.287	0.315	7.30	8.00
D	0.067	0.083	1.70	2.10
E	0.050 BSC		1.27 BSC	
F	0.014	0.020	0.36	0.51
G	0.002	0.010	0.05	0.25
H	0.244	0.260	6.20	6.60
J	0.022	0.043	0.55	1.10
K	0.007	0.009	0.18	0.22

* BSC = **B**asic **S**pacing between **C**enters

Part Numbering



Part Marking



Part Number Code

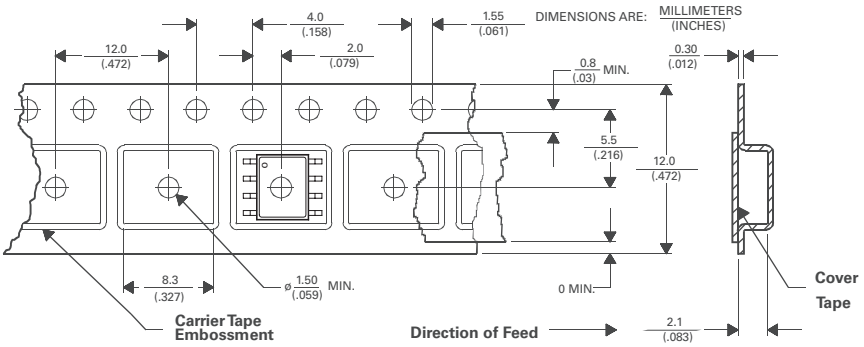
Date Code

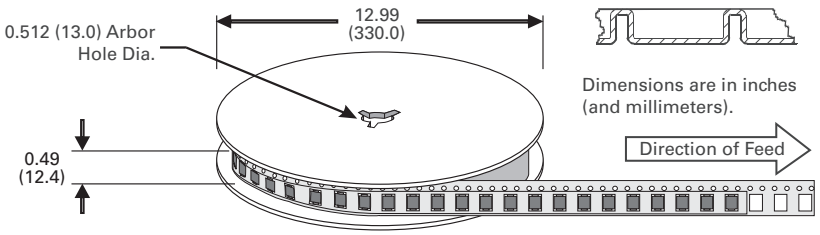
T: Assembly code
YY: Yearly code
WW: Weekly code

Product Selector

Part Number	Part Marking	Package Type	Description	Quantity	Industry Standard
B9110DF	B9110DF	D	MS-012 SMT 8-pin SOIC Tape and Reel Pack	2000	EIA-481-D

Tape and Reel Specifications — MS-012 (Wide Body)





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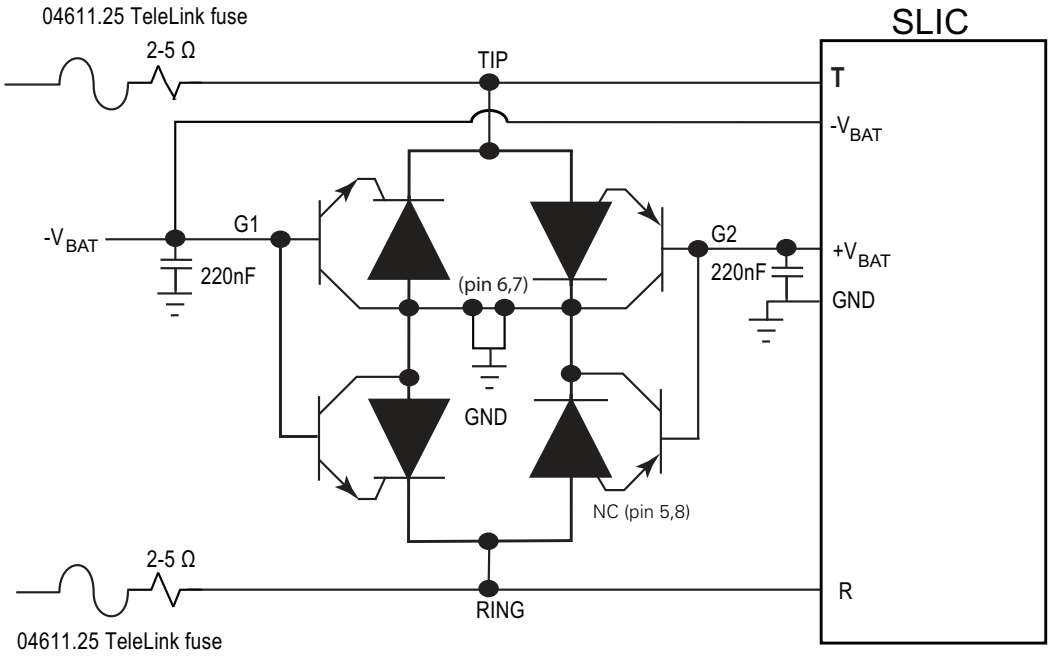
Operating and schematic explanation

The MS-012 SMT (SOIC-8) Dual Polarity Battrax® is specifically designed to provide surge protection for SLIC (Subscriber Line Interface Circuit) cards implementing positive and negative ringing, which are used in many telecommunication applications. This single 8-pin component provides protection for both line conductors (TIP & RING) by shunting positive and negative surges to the ground reference.

The surges are diverted to ground through the SCRs which are connected between the TIP/RING conductors and the ground reference. These SCRs have a transistor buffered gate that provides a low current magnitude trigger level; typically 5 mA or less. The SCRs will reset when the magnitude of the loop current drops below the component's holding current parameter I_H.

This component's turn-on threshold tracks with both the positive and negative reference voltages of the SMART SLIC component. As the line conditions change from on-hook to off-hook, the SLIC reference voltage levels will also change in an effort to conserve energy. This tracking protection component will typically operate at +1.4V above $+V_{BAT}$ and at -1.4 V below $-V_{BAT}$ during either surge conditions or power fault events. The buffered gate reduces the gate current needed to activate this component to approximately 5 mA.

The gate capacitors, which act as a charge reservoir, supply the needed current to trigger this component to the on-state and should be physically located in close proximity to the B9110DF gate leads. During slow rising ac power fault events, the discharge current of the capacitor (I_C = C dv/dt) easily achieves the 5 mA threshold to activate the SCR. This solution below will comply with the power fault and surge requirements of GR-1089 Intra-building Port Type and the Basic level of ITU K20/21. For GR-1089 Port Type 3 and Enhanced level of ITU K20/21, the series resistor value may need to be increased. The TeleLink fuse complies with both GR-1089 intra-building and inter-building requirements and both Basic and Enhanced levels of the ITU Recommendations.



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