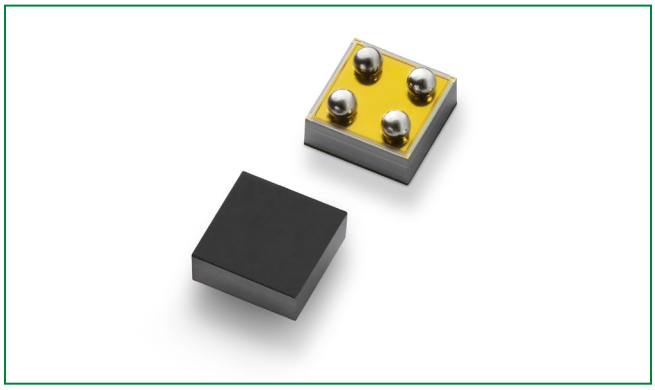
LQ05021QCS4

5 V, 2 A Ultra Low Consumption Load Switch With Slew Rate Control

RoHS Pb



Description

The LQ05021QCS4 is an ultra-efficiency, 2.0 A rated, load switch with integrated slew rate control. The best in class efficiency makes it an ideal choice for use in IoT, mobile, and wearable electronics.

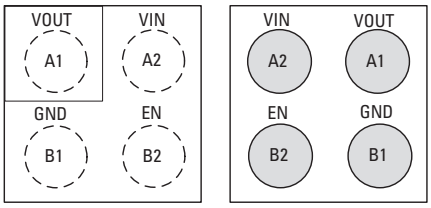
It supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The LQ05021QCS4 integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

The LQ05021QCS4 load switch device supports an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

The LQ05021QCS4 load switch device is small utilizing a wafer level chip scale package with 4 bumps in a 0.77 mm x 0.77 mm x 0.46 mm die size and a 0.4 mm bump pitch.

Pinout Designation



Pin Description

Pin #	Pin Name	Description
A1	V_{OUT}	Switch output
A2	V_{IN}	Switch input. Supply voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch. The EN pin has an internal pull-down resistor

Features and Benefits

- Ultra-low I_Q: 1 nA Typ @ 5.5 V_{IN}
- Ultra-low I_{SD}: 19 nA Typ @ 5.5 V_{IN}
- Low R_{ON} = 34 mΩ Typ @ 5.5 V_{IN}
- I_{OUT} max = 2.0 A
- Wide input range: 1.1 V to 5.5 V, 6 Vabs max
- Controlled rise time: 430 µs at 3.3 V_{IN}
- Internal EN pull-down resistor
- Integrated output discharge switch
- Ultra small: 4 bumps in a 0.77 mm x 0.77 mm x 0.46 mm WLCSP

Applications

- Mobile devices
- Data storage, SSD
- IoT devices
- Wearables
- Low power subsystems

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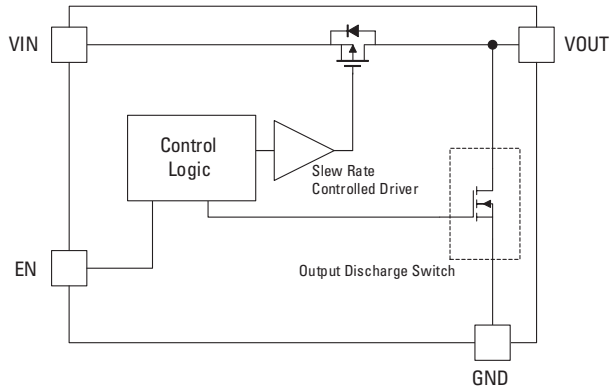
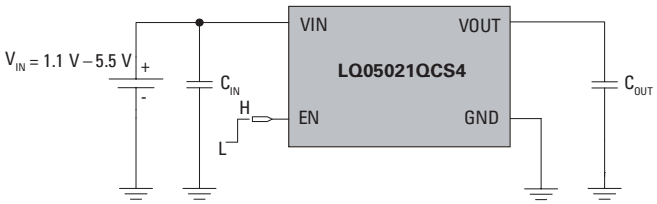
Functional Block Diagram



Typical Applications



Absolute Maximum Rating

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
P_D	Power Dissipation at T_A = 25 °C			1	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_J	Maximum Junction Temperature			150	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (board dependent)			110	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		kV

Note: Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Recommend Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.1	5.5	V
T_A	Ambient Operating Temperature	-40	85	°C

Note: The device is not guaranteed to function outside of the recommended operating conditions.

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Electrical Characteristics (Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Basic Operation							
V_{IN}	Supply Voltage			1.1		5.5	V
I_Q	Quiescent Current	$V_{IN} = V_{EN}$ =5.5 V, I_{OUT} = 0 mA			520		nA
		$V_{IN} = V_{EN}$ =5.5 V, I_{OUT} = 0 mA[1]			1		nA
		$V_{IN} = V_{EN}$ = 5.5 V, I_{OUT} = 0 mA, T_A = 85 °C[1]			12		nA
I_{SD}	Shutdown Current	EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.1 V			3		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.8 V			4		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.3 V			6		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 4.5 V			9		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 5.5 V			19	50	nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 5.5 V, T_A = 55 °C			110		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 5.5V, T_A = 85 °C			600		nA
R_{ON}	On-Resistance	V_{IN} = 5.5 V, I_{OUT} = 500 mA	T_A = 25 °C		34	47	mΩ
			T_A = 85 °C		40		mΩ
		VI_{IN} = 3.3 V, I_{OUT} = 500 mA	T_A = 25 °C		42	56	mΩ
			T_A = 85 °C		50		mΩ
		V_{IN} = 1.8 V, I_{OUT} = 300 mA	T_A = 25 °C		68		mΩ
		V_{IN} = 1.2 V, I_{OUT} = 100 mA	T_A = 25 °C		125		mΩ
		V_{IN} = 1.1 V, I_{OUT} = 100 mA	T_A = 25 °C		155		mΩ
R_{DSC}	Output Discharge Resistance	E_N = Low , I_{FORCE} = 10 mA		70	85	100	Ω
V_{IH}	EN Input Logic High Voltage	V_{IN} = 1.1 V - 1.8 V		0.9			V
		V_{IN} = 1.8 V - 5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 1.1 V - 1.8 V				0.3	V
		V_{IN} = 1.8 V - 5.5 V				0.4	V
R_{EN}	EN Internal resistance	Internal Pull-down Resistance:		7	10.1	13	mΩ
I_{EN}	EN Current	E_N = 5.5 V				0.8	µA
Switching Characteristics [2]							
t_{dON}	Turn-On Delay	R_L = 150 Ω, C_{OUT} = 0.1 µF			275		µs
t_R	V_{OUT} Rise Time				430		µs
t_{dON}	Turn-On Delay[4]	R_L = 500 Ω, C_{OUT} = 0.1 µF			245		µs
t_R	V_{OUT} Rise Time[4]				410		µs
t_{dOFF}	Turn-Off Delay[3,4]	R_L = 10 Ω, C_{OUT} = 0.1 µF			0.38		µs
t_F	V_{OUT} Fall Time[3,4]				1.32		µs
t_{dOFF}	Turn-Off Delay[4]	R_L = 500 Ω, C_{OUT} = 0.1 µF			1.1		µs
t_F	V_{OUT} Fall Time[3,4]				18		µs

Notes:

1. I_Q does not include enable pull down current through the pull-down resistor RPD.
2. $t_{ON} = td_{ON} + t_R$, $t_{OFF} = td_{OFF} + t_F$
3. Output discharge path is enabled during off.
4. By design; characterized, not production tested.

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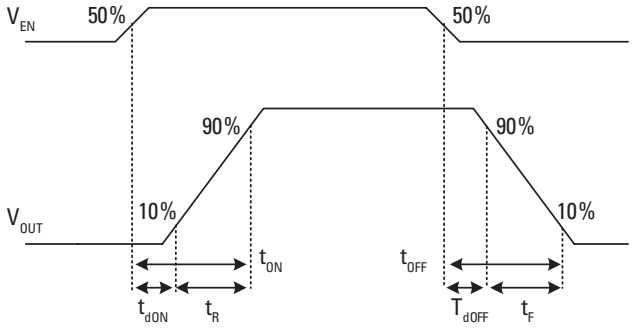
Timing Waveforms



Typical Performance Characteristics

Figure 1 - On-Resistance vs. Supply Voltage

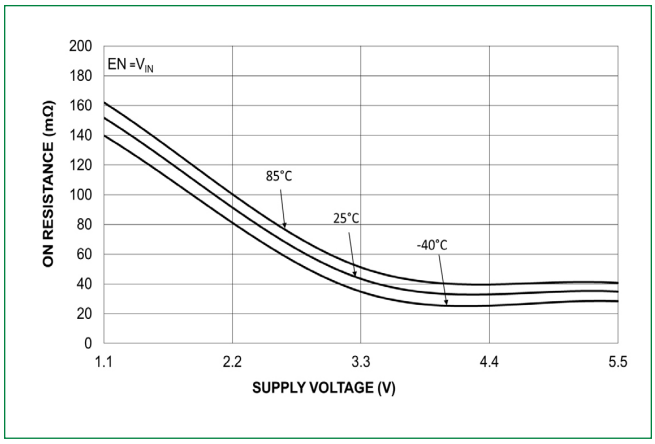


Figure 2 - On-Resistance vs. Temperature

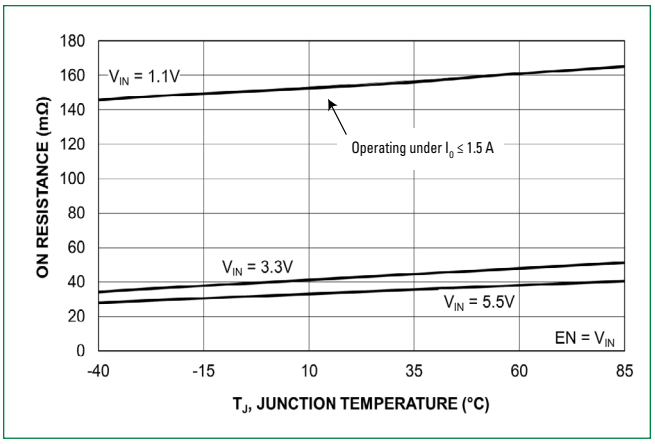


Figure 3 - Quiescent Current vs. Supply Voltage

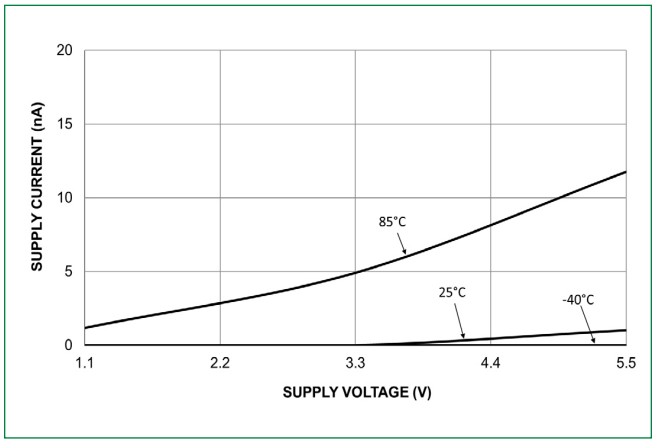


Figure 4 - Quiescent Current vs. Temperature

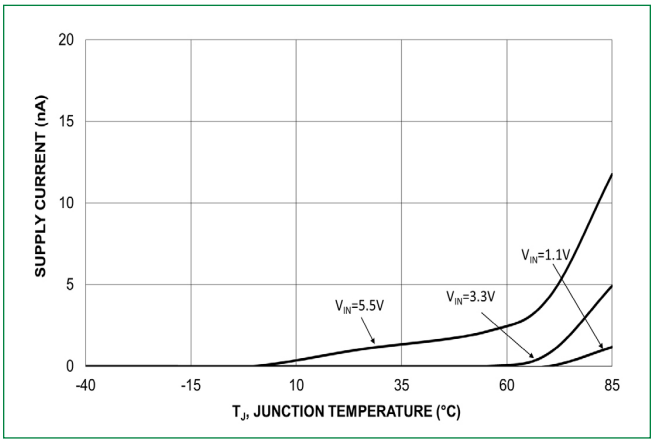


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Figure 5 - Shutdown Current vs. Supply Voltage

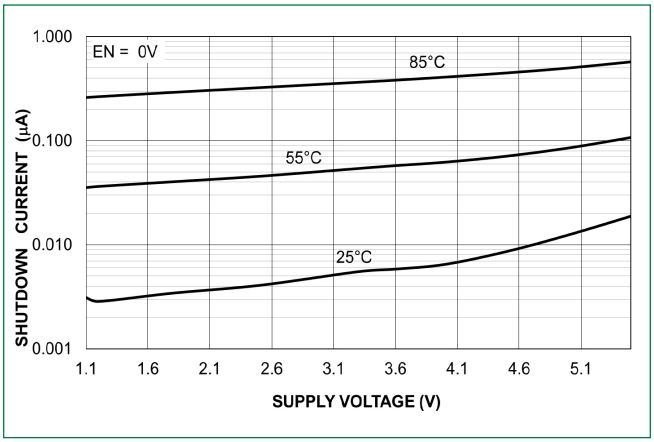

Figure 6 - Shutdown Current vs. Temperature

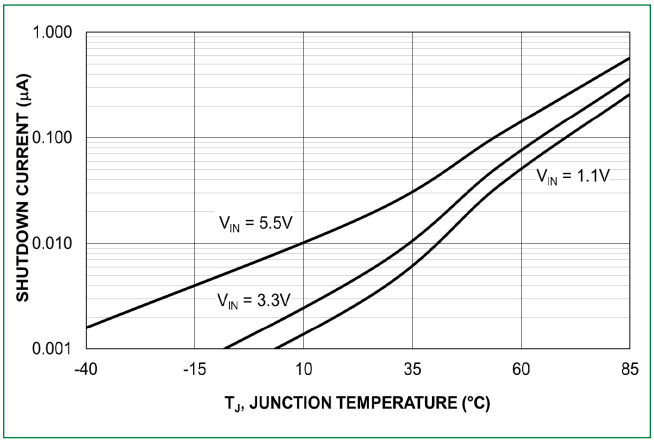

Figure 7 - EN Input Logic High Threshold

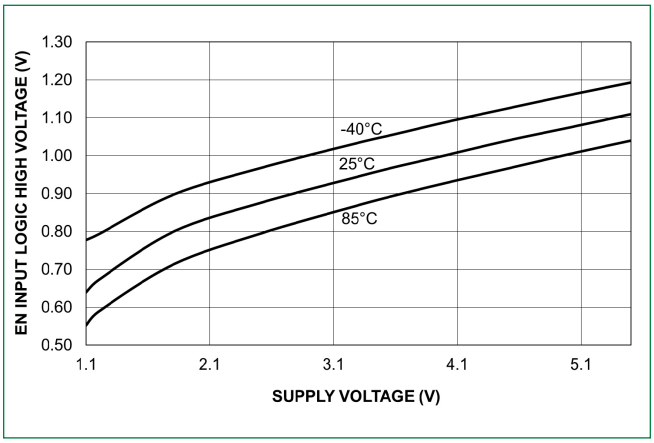

Figure 8 - EN Input Logic High Threshold Vs. Temperature

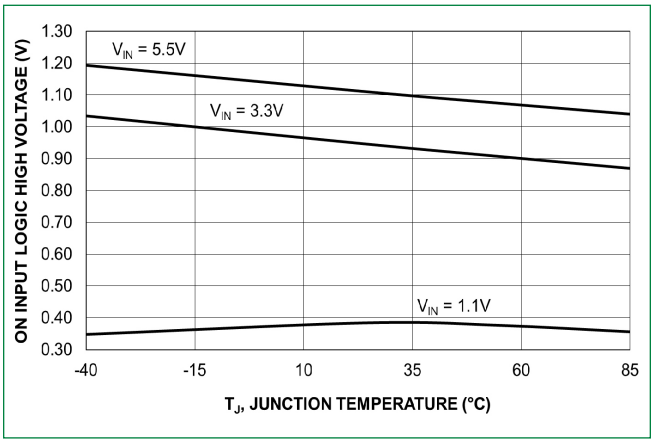

Figure 9 - EN Input Logic Low Threshold

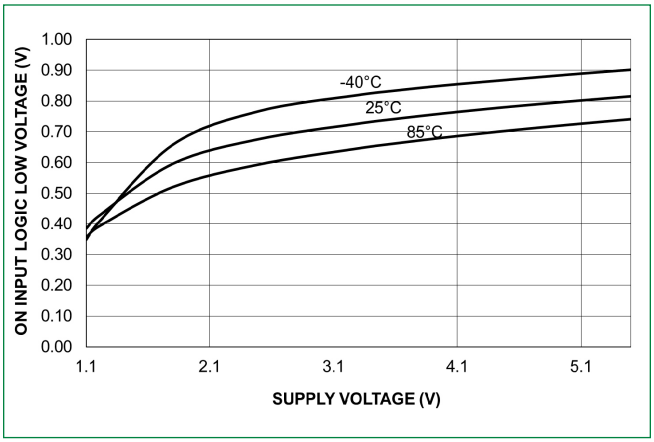

Figure 10 - EN Input Logic Low Threshold Vs. Temperature

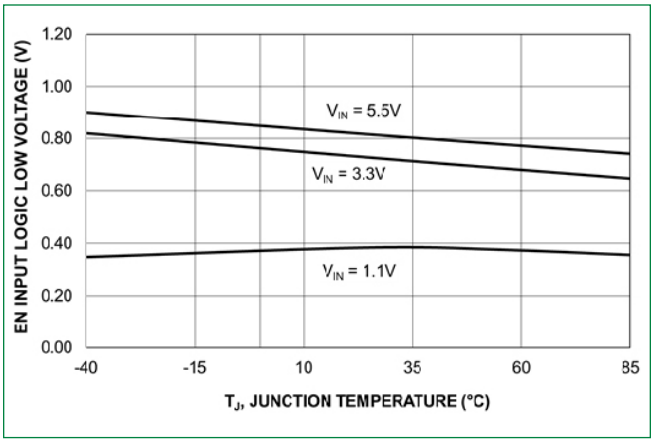

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Figure 11 - V_{OUT} Rise Time vs. Temperature

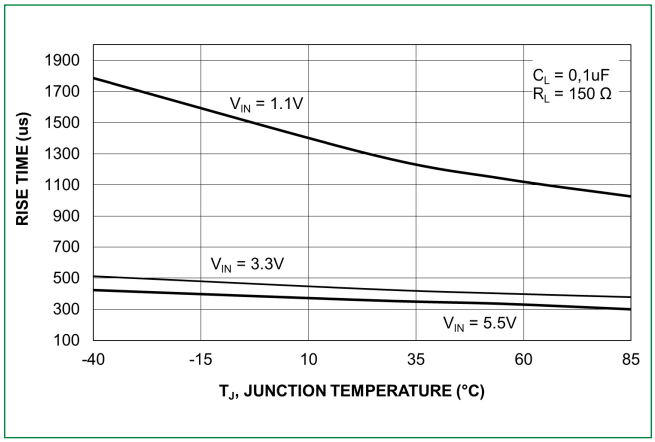

Figure 12 - Turn-On Delay Time vs. Temperature

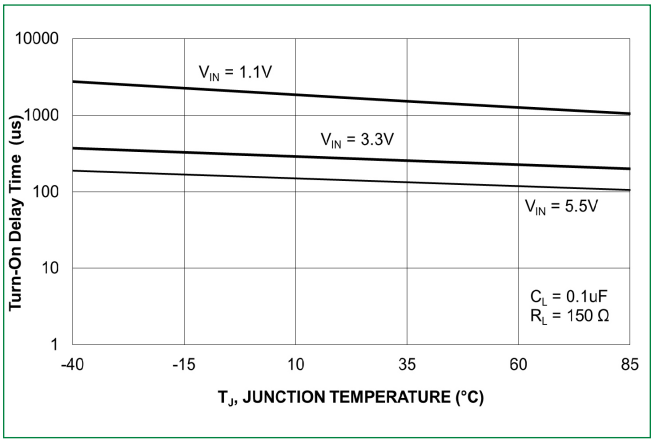

Figure 13 - Pull-down Resistance vs. Temperature

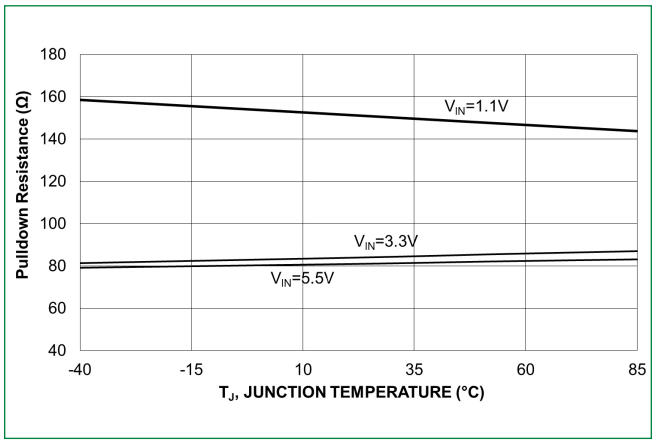

Figure 14 - Enable Input Current vs. Temperature

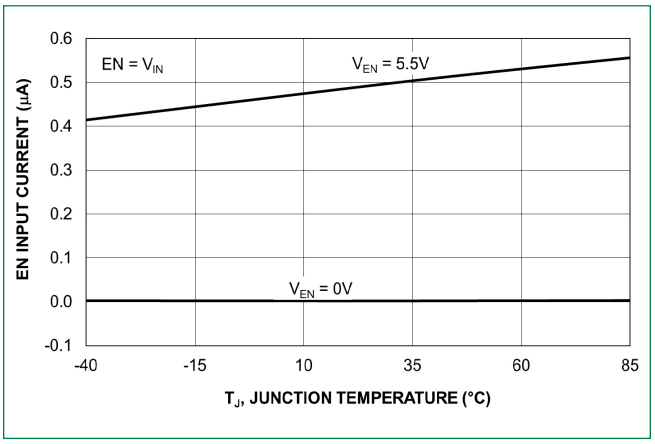

Figure 15 - Turn-On Response
V_{IN} = 3.3 V, C_{IN} = 1.0 µF, C_{OUT} = 0.1 µF, R_L = 150 Ω

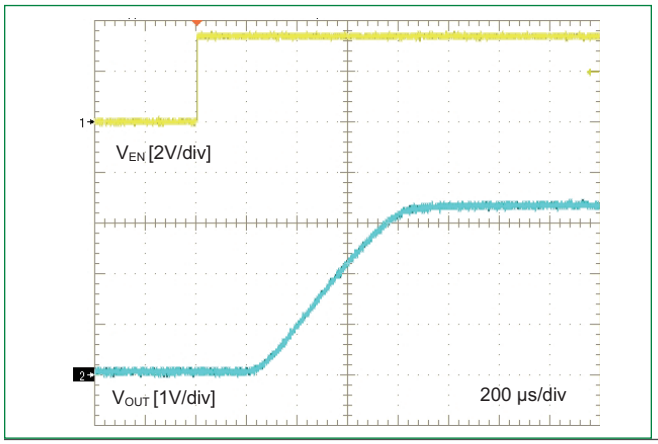

Figure 16 - Turn-On Response
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT} = 0.1 µF, R_L = 500 Ω

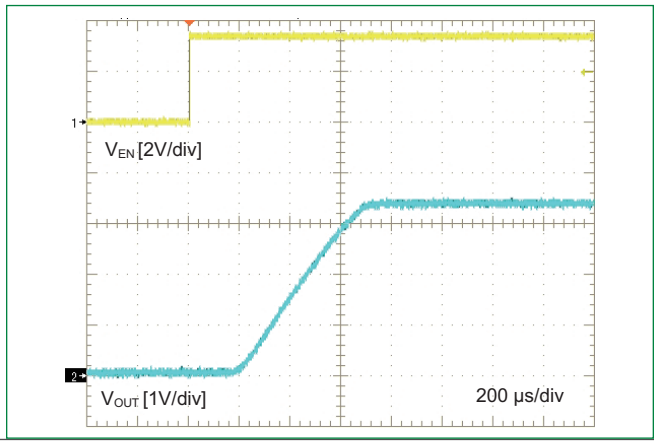

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Figure 17 - Turn-Off Response, Output Discharge
V_{IN} = 3.3 V, C_{IN} = 1.0 µF, C_{OUT} = 0.1 µF, R_L = 150 Ω

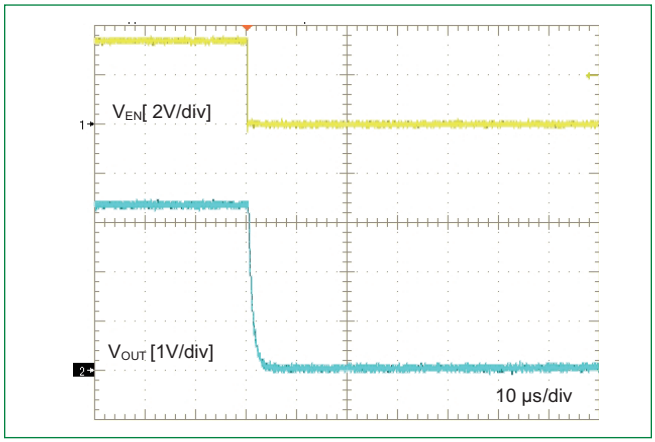
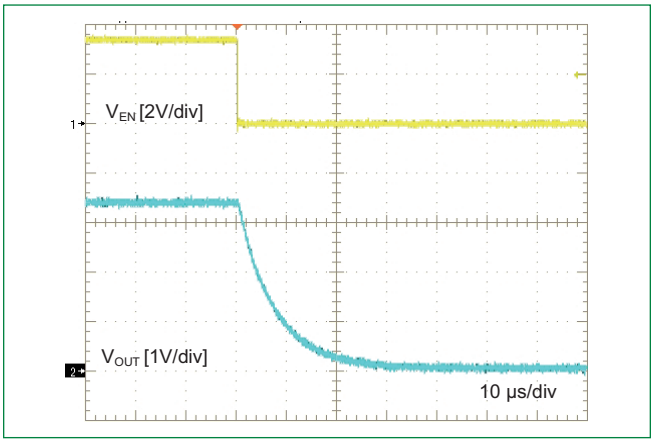


Figure 18 - Turn-Off Response, Output Discharge
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT} = 0.1 µF, R_L = 500 Ω



Application Information

The LQ05021QCS4 integrated 2.0 A, ultra-efficient load switch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.77 mm x 0.77 mm x 0.46 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.4 mm pitch for manufacturability.

Input Capacitor

A capacitor is recommended to be placed close to the VIN pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The LQ05021QCS4 can be activated by EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

Output Discharge Function

The LQ05021QCS4 has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce voltage drops and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

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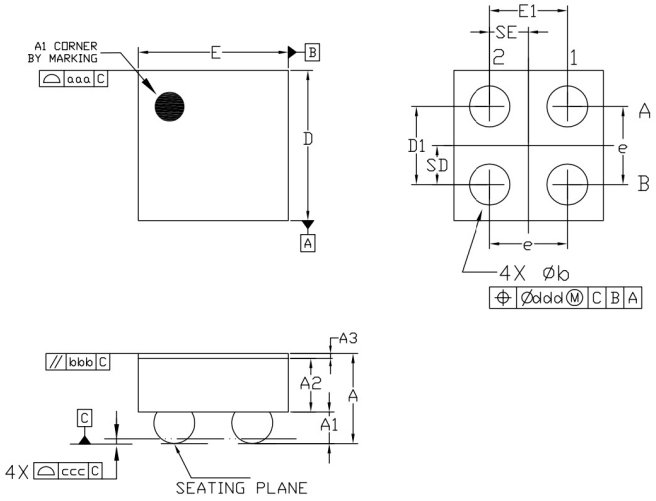
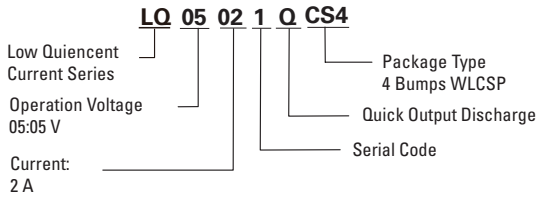
Dimensions

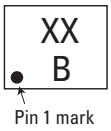


Dimension	Millimeters		
	Min	Nom	Max
A	0.410	0.460	0.510
A1	0.135	0.160	0.185
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	0.755	0.770	0.785
E	0.755	0.770	0.785
D1	0.350	0.400	0.450
E1	0.350	0.400	0.450
B	0.170	0.210	0.250
E	0.400 BSC		
SD	0.200 BSC		
SE	0.200 BSC		
Tol. of Form & Position			
aaa	0.100		
bbb	0.100		
ccc	0.050		
ddd	0.050		

Part Numbering



Part Marking



B = Device Code
XX = Lot Run Code

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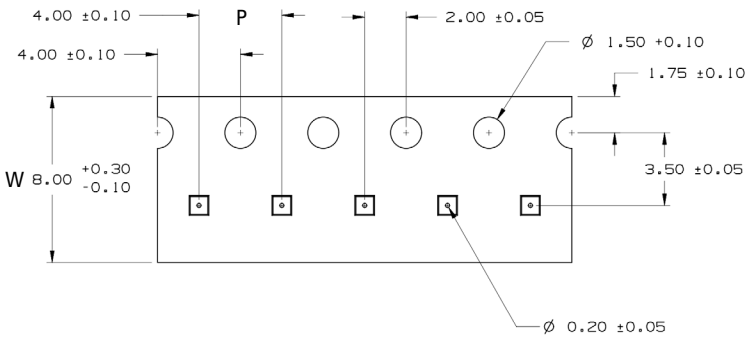
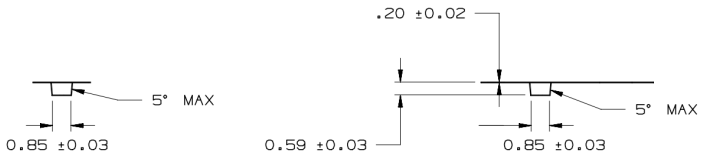
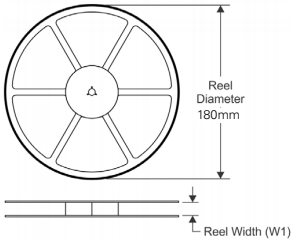
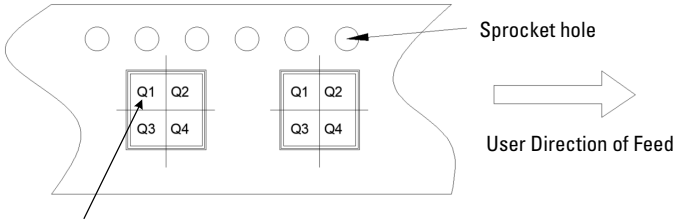
Carrier Tape & Reel Specification









Quandrant assignments pin 1 orientation
Dimensions are in millimeters

Device	Package	Pins	SPQ	Reel Diameter	Reel Width W1	A0	B0	K0	P	W	Pin1
LQ05021QCS4	4 Bumps WLCSP	4	4000	180	9	0.85	0.85	0.59	4	8	Q1

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