



LEOPARD IMAGING INC

Rev. 1.1

LI-IMX265-MIPI-M12

Data Sheet

Key Features

- Sony Diagonal 8.9 mm (Type 1/1.8) CMOS Image Sensor IMX265
- Active pixels: 2064H x 1544V
- Pixel size: 3.45 μm x 3.45 μm
- Color sensor
- Interface: MIPI output
- Support M12 lens
- Global Shutter
- Weight: 15 g
- Part#: **LI-IMX265-MIPI-M12**

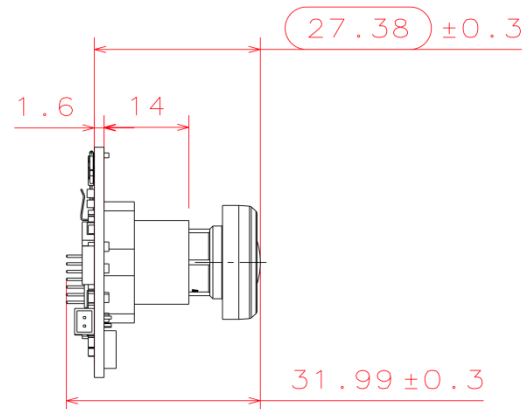
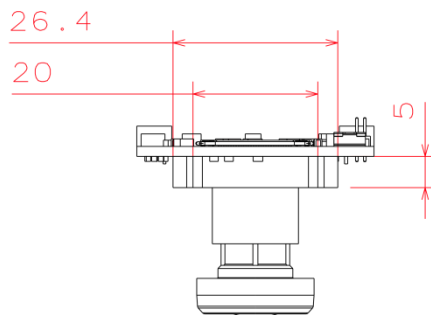
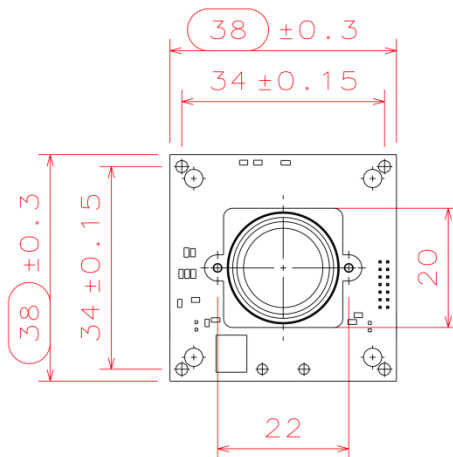


Lens Spec

- Model: N118B05518W
- Focal length: 5.5 mm
- Aperture, F/#: 1.8
- Built in 650nm IR cut filter
- FOV (H): 64.5 °
- TV Distortion: 2.2 %
- Mount: M12 x P0.5



Dimensions



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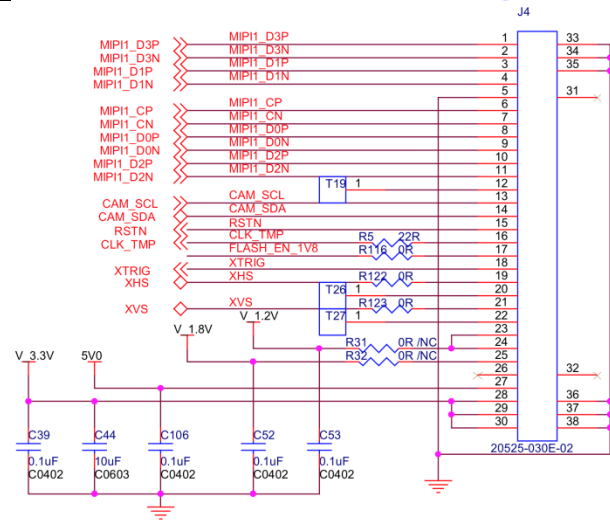
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Interfaces

Interfaces

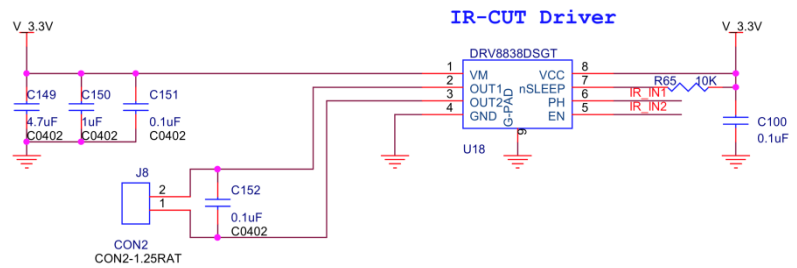
Interface J4:

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: LI-FAW-1233-T1 (200mm)



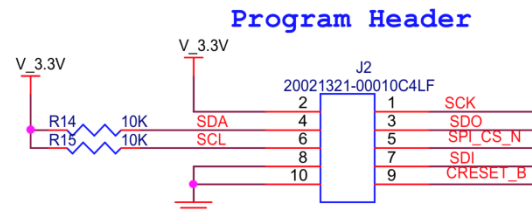
Interface J8:

- Part#: 1734829-2
- Number of Positions: 2
- Pitch: 1.25mm



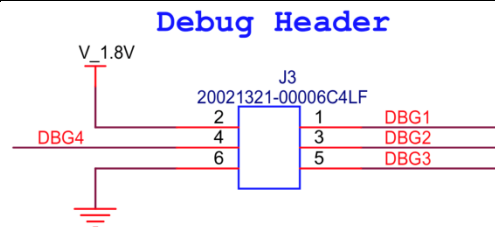
Interface J2:

- Part#: 20021321-00010C4LF
- Number of Positions: 10
- Pitch: 1.27mm



Interface J3:

- Part#: 20021321-00006C4LF
- Number of Positions: 6
- Pitch: 1.27mm



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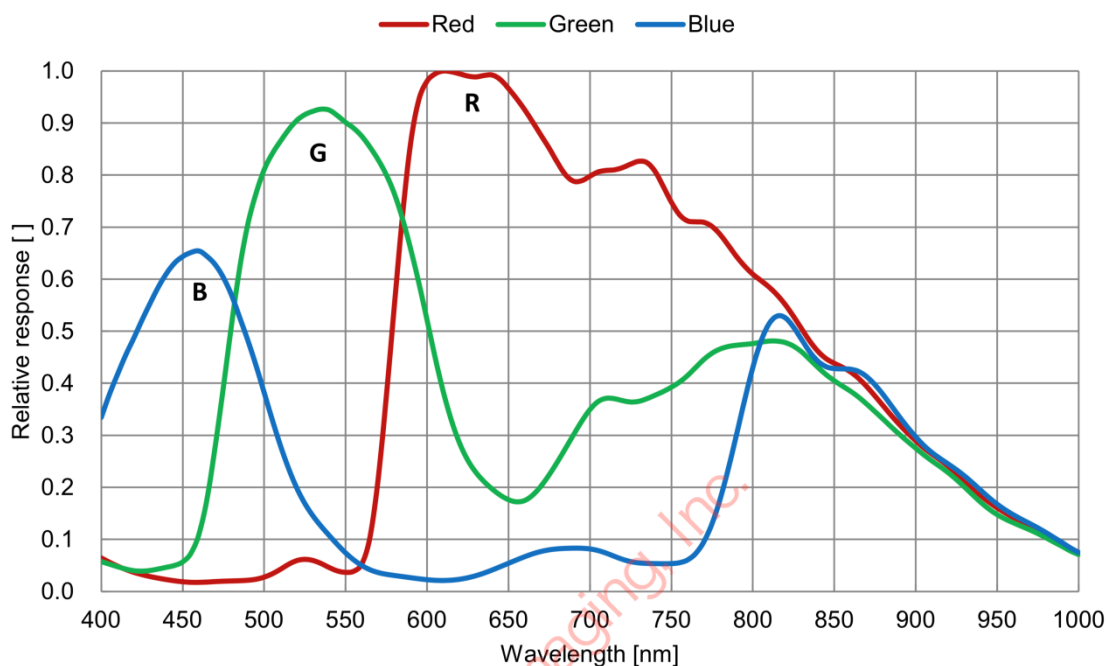
Absolute Maximum Ratings

Item	Symbol	Rating			Unit	Remarks
Supply voltage (Analog 3.3 V)	AV _{DD}	-0.3	to	+4.0	V	
Supply voltage (Interface 1.8 V)	OV _{DD}	-0.3	to	+3.3	V	
Supply voltage (Digital 1.2 V)	DV _{DD}	-0.3	to	+2.0	V	
Input voltage	VI	-0.3	to	OV _{DD} +0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	to	OV _{DD} +0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	to	+75	°C	
Storage temperature	Tstg	-40	to	+85	°C	
Performance guarantee temperature	Tspec	-10	to	+60	°C	

Recommended Operating Conditions

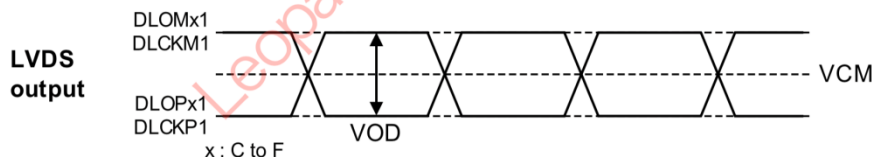
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Analog 3.3 V)	AV _{DD}	3.15	3.30	3.45	V
Supply voltage (Interface 1.8 V)	OV _{DD}	1.70	1.80	1.90	V
Supply voltage (Digital 1.2 V)	DV _{DD}	1.10	1.20	1.30	V

Spectral Sensitivity Characteristics



DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V _{DDHx}	AV _{DD}	—	3.15	3.30	3.45	V
	Interface	V _{DDMx}	OV _{DD}	—	1.70	1.80	1.90	V
	Digital	V _{DDLx}	DV _{DD}	—	1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE	VIH	XVS / XHS in Slave mode	0.8 × OV _{DD}	—	—	V
		SCK SDI XCE XTRIG	VIL		—	—	0.2 × OV _{DD}	V
Digital output voltage		DLOPx1 DLOMx1 DCKP1	VCM	Low voltage LVDS (termination resistance: 100 Ω)	—	OV _{DD} /2	—	V
		DCKM1 x: C to F	VOD		100	150	210	mV
		XHS XVS SDO	VOH	XVS / XHS in Master mode	OV _{DD} -0.4	—	—	V
		TOUT1 TOUT2	VOL		—	—	0.4	V



Power Consumption

Item	Pins	Symbol	Typ.	Max.	Unit
Operating current Serial LVDS 4 ch 12 bit 55.6 frame/s	V _{DDH}	IAV _{DD}	120	175	mA
	V _{DDM}	IOV _{DD}	11	20	mA
	V _{DDL}	IDV _{DD}	120	180	mA
Standby current	V _{DDH}	IAV _{DD_STB}	—	0.5	mA
	V _{DDM}	IOV _{DD_STB}	—	0.5	mA
	V _{DDL}	IDV _{DD_STB}	—	20	mA

Operating current:

(Typical value condition) : Supply voltage: 3.30 V / 1.80 V / 1.20 V, T_j = 25 °C

(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, T_j = 60 °C

Worst state of internal circuit operating current consumption.

Standby current:

(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, T_j = 60 °C, INCK = 0 V,

The device in the light-obstructed state.



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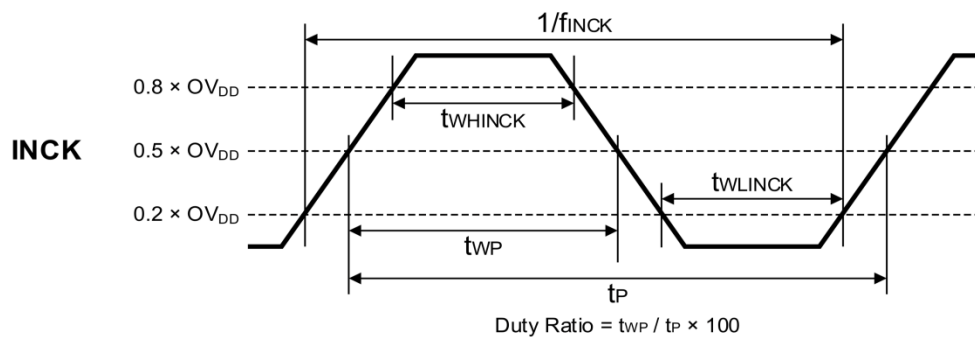
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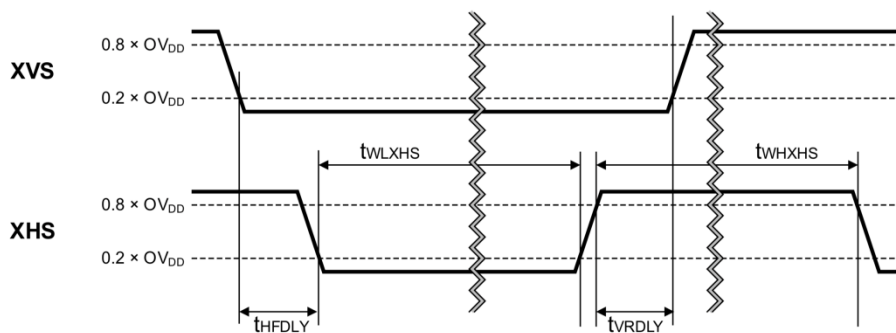
AC Characteristics



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	$f_{INCK} \times 0.96$	f_{INCK}	$f_{INCK} \times 1.02$	MHz	$f_{INCK} =$ 37.125 MHz, 74.25 MHz, 54 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45.0	50.0	55.0	%	Define with $0.5 \times OV_{DD}$

* The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)



Item	Symbol	Min.	Typ.	Max.	Unit
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns
XVS - XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns
XHS - XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns

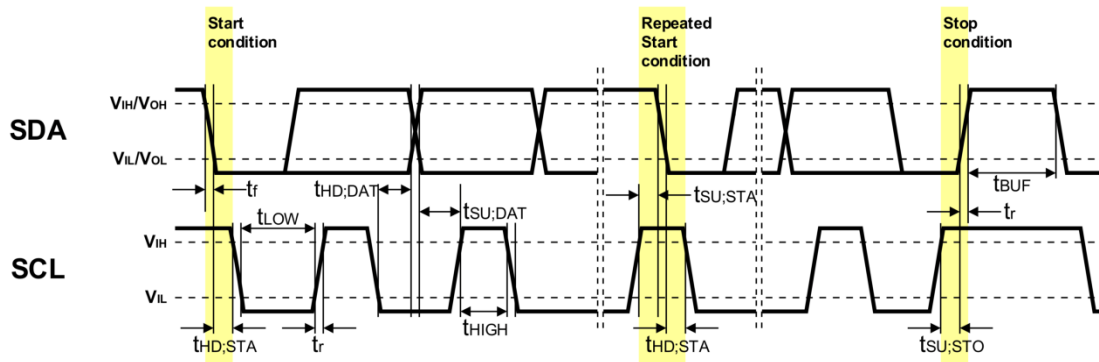
Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.



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I²C Communication



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	$0.3 \times OV_{DD}$	V	
High level input voltage	V_{IH}	$0.7 \times OV_{DD}$	—	1.9	V	
Low level output voltage	V_{OL}	0	—	$0.2 \times OV_{DD}$	V	$OV_{DD} < 2$ V, Sink 3 mA
High level output voltage	V_{OH}	$0.8 \times OV_{DD}$	—	—	V	
Output fall time	t_{of}	—	—	250	ns	Load 10 pF – 400 pF, $0.7 \times OV_{DD} - 0.3 \times OV_{DD}$
Input current	I_i	-10	—	10	μ A	$0.1 \times OV_{DD} - 0.9 \times OV_{DD}$
Capacitance for SCK (/SCL) , SDI (/SDA)	C_i	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	μ s
Low period of the SCL clock	t_{LOW}	1.3	—	—	μ s
High period of the SCL clock	t_{HIGH}	0.6	—	—	μ s
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	μ s
Data hold time	t_{HDDAT}	0	—	0.9	μ s
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	μ s
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	μ s



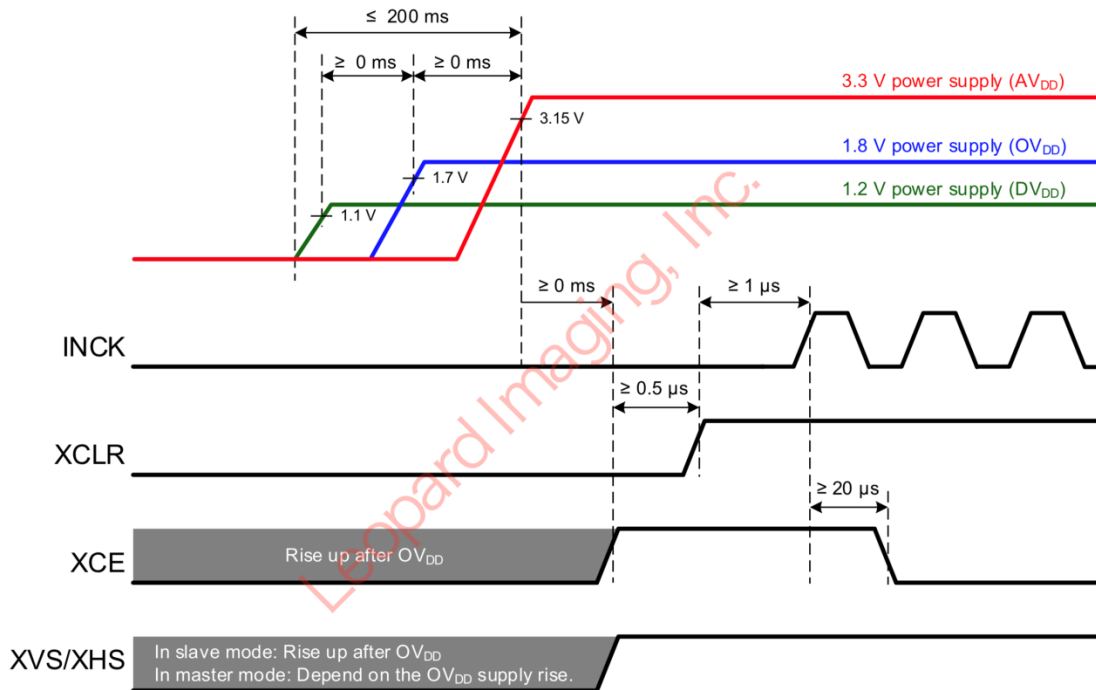
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Power-on Sequence

Follow the sequence below to turn On the power supplies.

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) → 1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
3. Start the input of INCK after turning the level of XCLR into the high.
4. Make the sensor setting by register communication after the system clear. A period of 0 μ s or more should be provided after setting XCLR High before inputting the communication enable signal XCE.

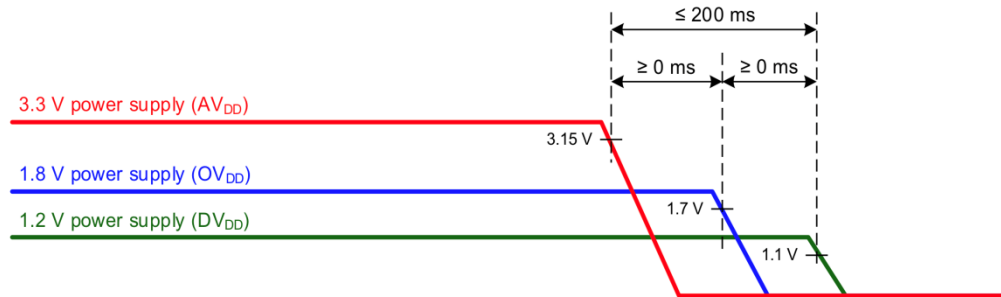


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Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG, SLAMODE, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.



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