



LEOPARD IMAGING INC

LI-XAVIER-KIT-IMX290M12-X

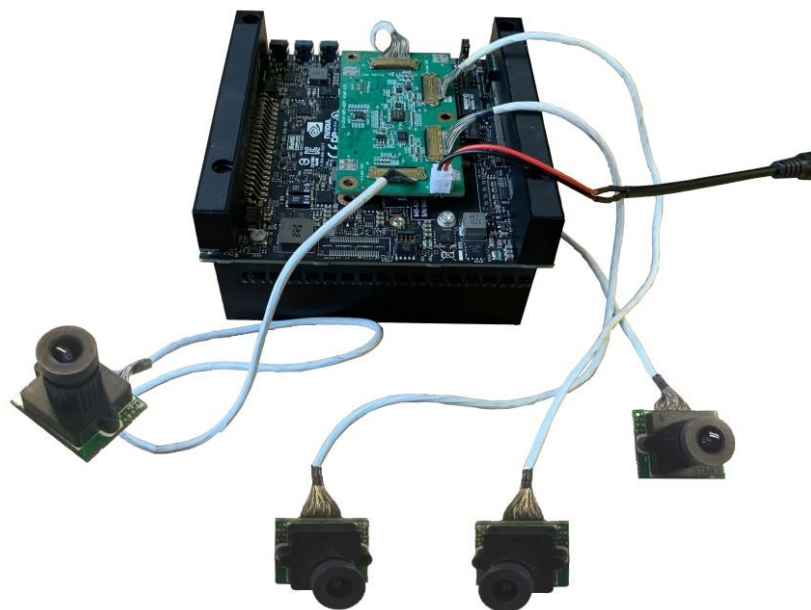
Data Sheet

Key Features

- Compatible with Nvidia® Jetson AGX Xavier™ Developer Kit
- MIPI CSI-2 interface
- Support up to four 4-lane cameras
- Sony Diagonal 6.46 mm (Type 1/2.8) CMOS Image Sensor IMX290
- Active pixels: 1945H x 1109V
- Pixel size: 2.9 um x 2.9 um
- Color camera
- High sensitivity
- Length of the I-PEX cable: 300mm
- Support multiple length cables
- Connector Part#: 20525-030E-02C
- Support M12 x P0.5 lens
- Provide customization services
- Part#:
(1 cam) **LI-XAVIER-KIT-IMX290M12**
(2 cam) **LI-XAVIER-KIT-IMX290M12-D**
(3 cam) **LI-XAVIER-KIT-IMX290M12-T**
(4 cam) **LI-XAVIER-KIT-IMX290M12-Q**

Applications

- Industrial Cameras
- Surveillance cameras



Lens Spec

- Model: LC001E-0530
- Focal length: 3.98 mm +/- 5%
- Aperture, F/#: 2.3 +/- 5%
- Built in 650nm IR cut filter
- FOV (D/H/V): 96 °/ 82.4 °/50 °
- TV Distortion: < 12%
- Mount: M12 x P0.5

BOM

Nvidia AGX Xavier Developer Kit not included

#	Items	QTY
1	LI-JXAV-MIPI-ADPT-4CAM	1
2	LI-IMX290-MIPI-M12	1, 2,3 or 4
3	FAW-1233-03 cable	1, 2,3 or 4



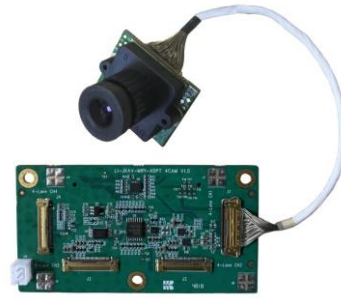
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LI-XAVIER-KIT-IMX290M12

BOM

#	Items	QTY
1	LI-JXAV-MIPI-ADPT-4CAM	1
2	LI-IMX290-MIPI-M12	1
3	FAW-1233-03 cable	1



LI-XAVIER-KIT-IMX290M12-D

BOM

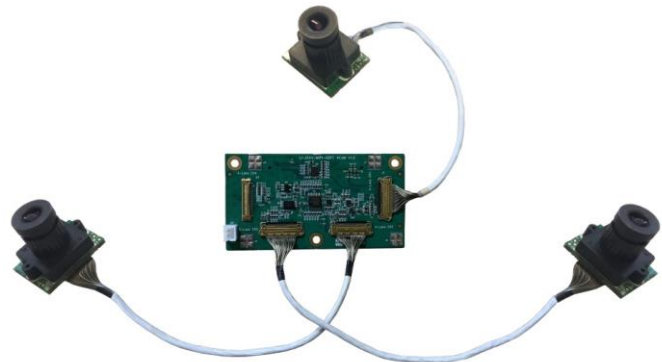
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1	LI-JXAV-MIPI-ADPT-4CAM	1
2	LI-IMX290-MIPI-M12	2
3	FAW-1233-03 cable	2



LI-XAVIER-KIT-IMX290M12-T

BOM

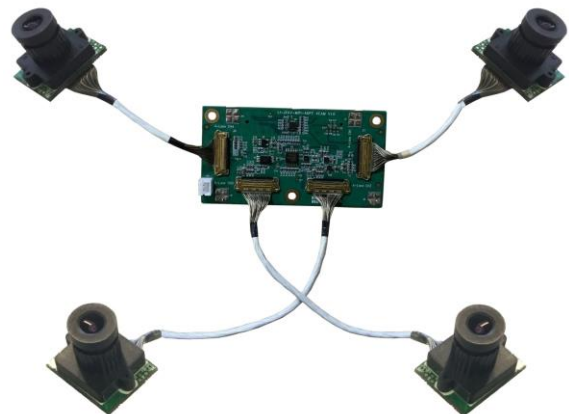
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1	LI-JXAV-MIPI-ADPT-4CAM	1
2	LI-IMX290-MIPI-M12	3
3	FAW-1233-03 cable	3



LI-XAVIER-KIT-IMX290M12-Q

BOM

#	Items	QTY
1	LI-JXAV-MIPI-ADPT-4CAM	1
2	LI-IMX290-MIPI-M12	4
3	FAW-1233-03 cable	4

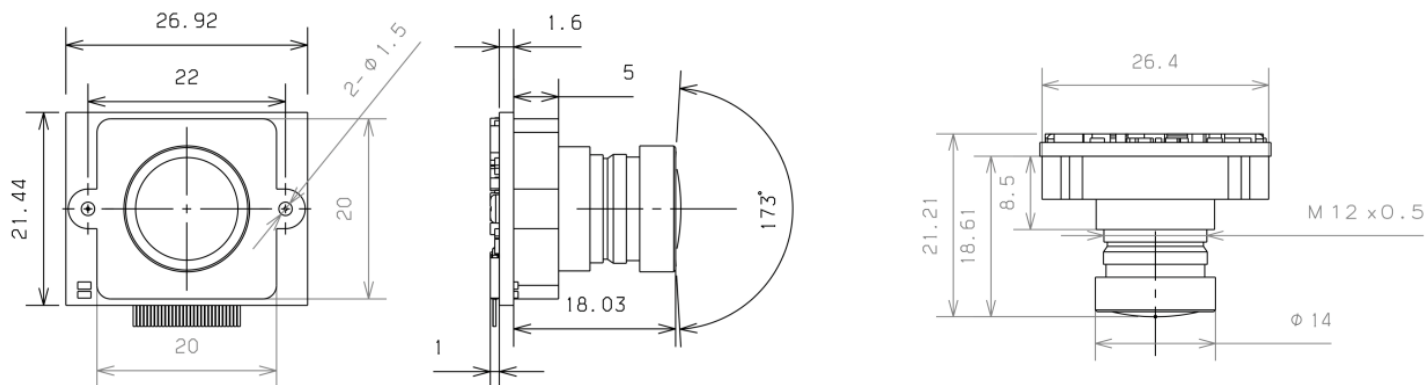


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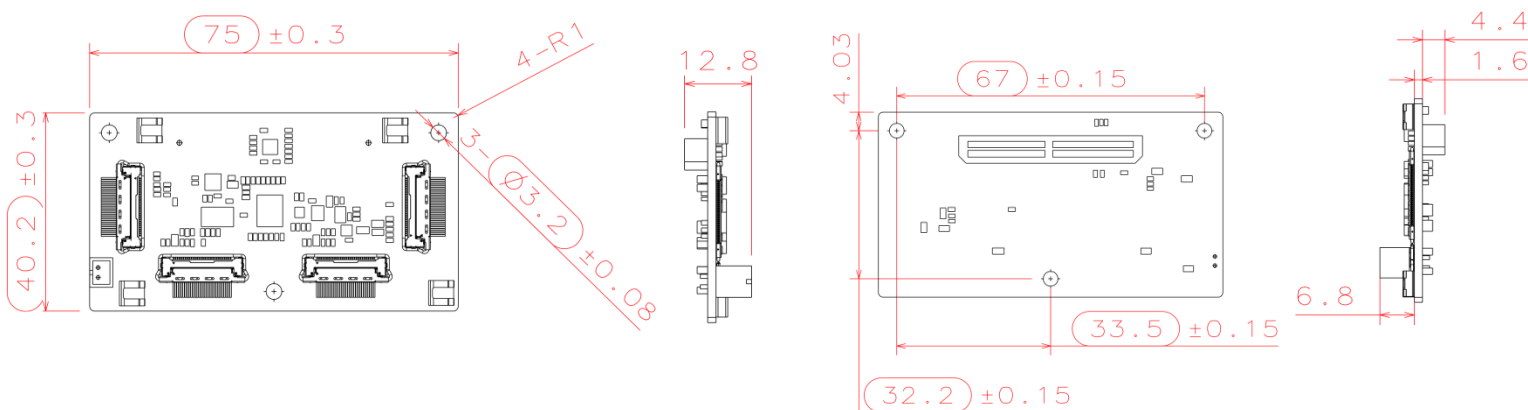
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Dimensions

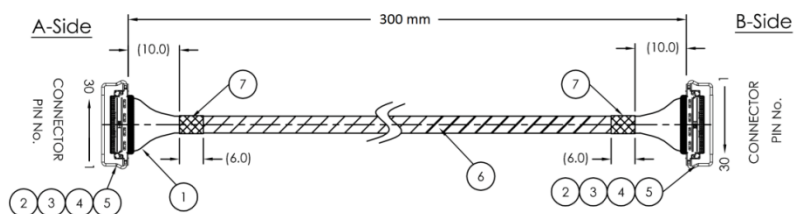
LI-IMX290-MIPI-M12



LI-JXAV-MIPI-ADPT-4CAM



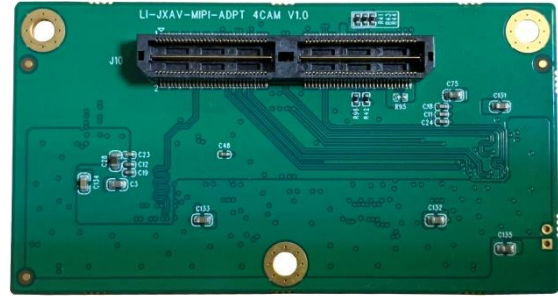
FAW-1233-03



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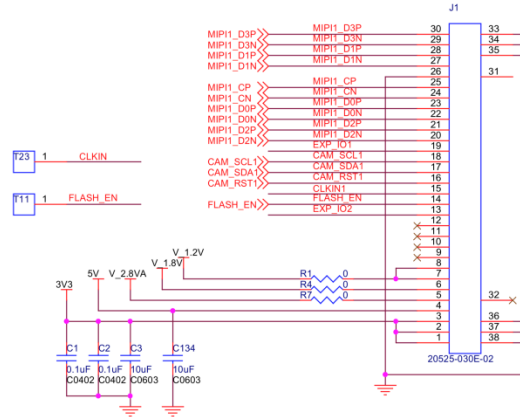
LI-JXAV-MIPI-ADPT-4CAM



Interfaces

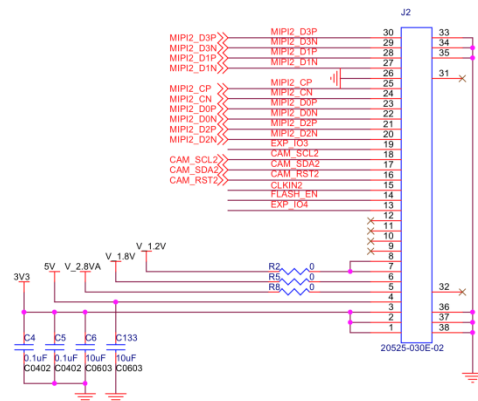
Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



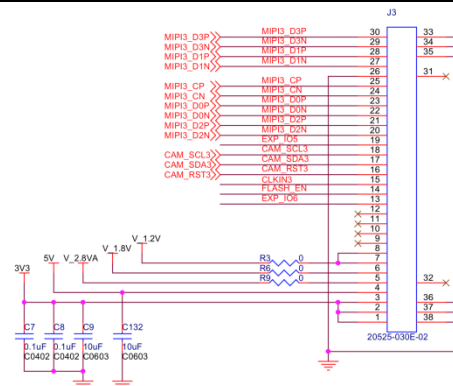
Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)

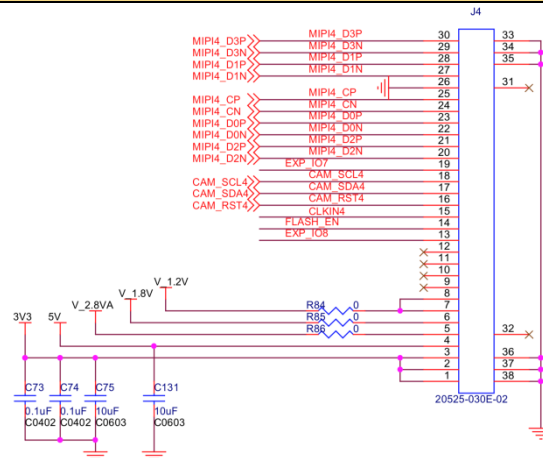


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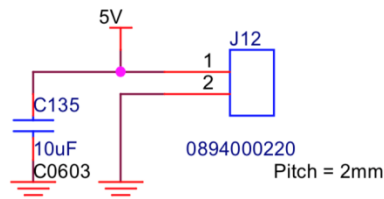
Interface J4

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



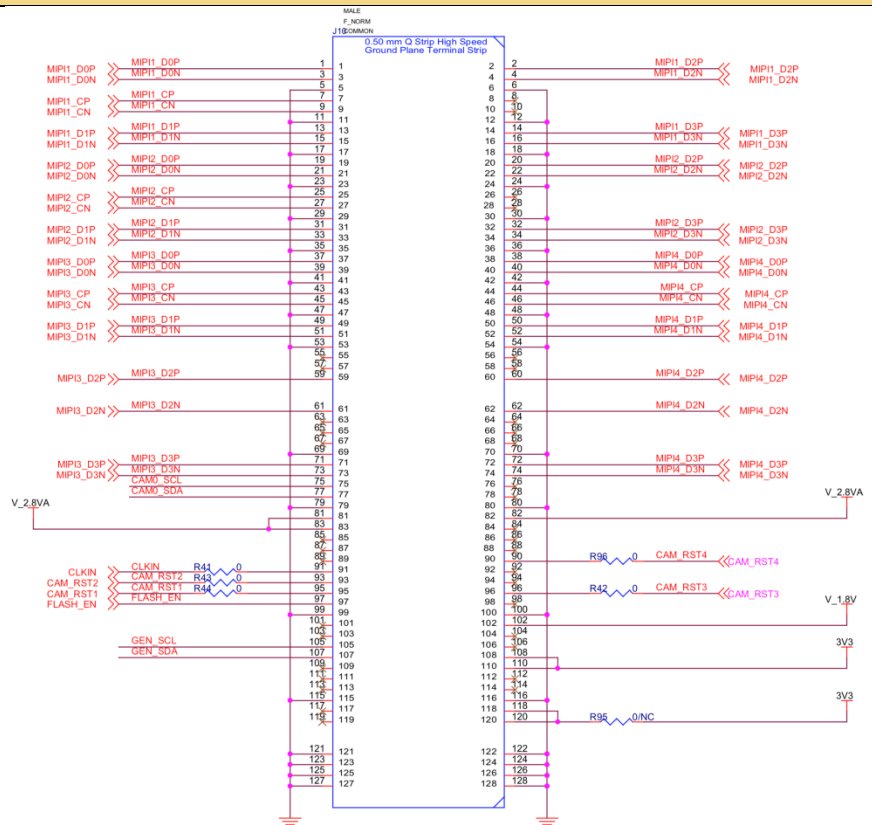
Interface J5

- Part#: 0894000220
- Number of Positions: 2
- Pitch: 2mm



Interface J10

- Part#: QTH-060-01-L-D-A
- Number of Positions: 120
- Number of Rows: 2
- Pitch: 0.5 mm



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LI-IMX290-MIPI-M12



Camera Spec	
Image Sensor	Sony Diagonal 6.46 mm (Type 1/2.8) CMOS Image Sensor IMX290
Optical format	1/2.8"
Number of active pixels	1945 (H) x 1109(V)
Pixel size	2.9um (H) x 2.9um (V)
Color or Mono	Color
Interface	MIPI interface
Lens mount	M12
Weight	14 g
Interfaces	
Interface J2:	- Part#: 20525-030E-02C - Number of Positions: 30 - Pitch: 0.4mm - Mating I-PEX cable: FAW-1233-03 (300mm)



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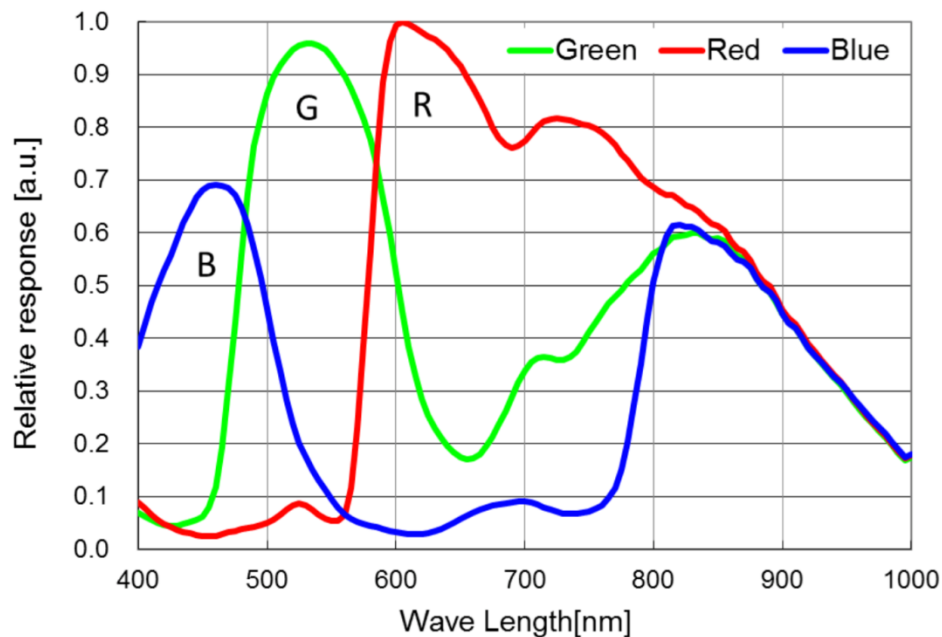
Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 2.9 V)	AV _{DD}	-0.3	3.3	V	
Supply voltage (interface 1.8 V)	OV _{DD}	-0.3	3.3	V	
Supply voltage (digital 1.2 V)	DV _{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV _{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV _{DD} + 0.3	V	Not exceed 3.3 V

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 2.9 V)	AV _{DD}	2.80	2.90	3.00	V
Supply voltage (Interface 1.8 V)	OV _{DD}	1.70	1.80	1.90	V
Supply voltage (digital 1.2 V)	DV _{DD}	1.10	1.20	1.30	V
Performance guarantee temperature	Tspec	-10	—	60	°C
Operating guarantee temperature	Topr	-30	—	85	°C
Storage guarantee temperature	Tstg	-40	—	85	°C

Spectral Sensitivity Characteristics



DC Characteristics

Item	Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	analog	VDDHx	AV _{DD}	2.80	2.90	3.00	V
	Interface	VDDMx	OV _{DD}	1.70	1.80	1.90	V
	digital	VDDLx	DV _{DD}	1.10	1.20	1.30	V
Digital input voltage	XHS XVS XCLR INCK XMASTER OMODE SCK SDI XCE XTRIG	VIH	XVS / XHS Slave Mode	0.8OV _{DD}	—	—	V
		VIL		—	—	0.2OV _{DD}	V
Digital output voltage	DLOP [A:F] DLOM [A:F] DLCKP DLCKM	VOH	IOH = -2 mA	OV _{DD} -0.4	—	—	V
		VOL	IOL = 2 mA	—	—	0.4	V
		VCM	Low voltage LVDS	—	OV _{DD} /2	—	V
		VOD	Low voltage LVDS (Termination resistance: 100 Ω)	100	150	220	mV
	XHS XVS SDO TOUT	VOH	XVS / XHS Master Mode	OV _{DD} -0.4	—	—	V
		VOL		—	—	0.4	V

Current Consumption

Item	pin	Symbol	Typ.		Max.		Unit
			Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current Low voltage LVDS serial 8 ch 12 bit 60 frame / s Full HD 1080p mode	VDDH	IAV _{DD}	54	53	111	108	mA
	VDDM	IOV _{DD}	16	15	29	27	mA
	VDDL	IDV _{DD}	77	95	123	214	mA
Operating current MIPI CSI-2 / 4 Lane 12 bit, 60 frame/s Full HD 1080p mode	VDDH	IAV _{DD}	55	54	111	108	mA
	VDDM	IOV _{DD}	1	1	2	2	mA
	VDDL	IDV _{DD}	94	111	143	252	mA
Operating current CMOS parallel SDR 12 bit, 30 frame/s Full HD 1080p	VDDH	IAV _{DD}	55	54	111	110	mA
	VDDM	IOV _{DD}	17	17	28	28	mA
	VDDL	IDV _{DD}	49	59	90	159	mA
Standby current	VDDH	IAV _{DD_STB}	—		0.1		mA
	VDDM	IOV _{DD_STB}	—		0.1		mA
	VDDL	IDV _{DD_STB}	—		14.0		mA

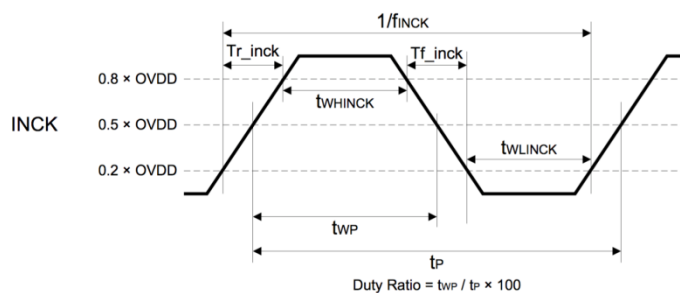


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AC Characteristics

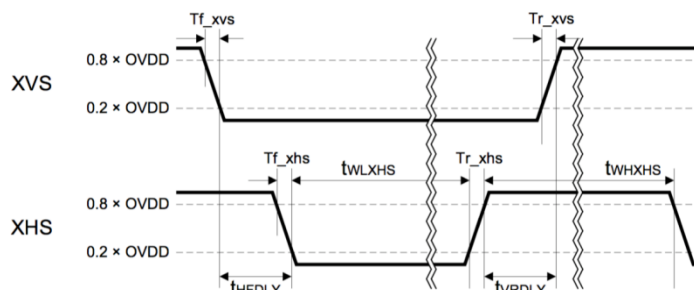
INCK



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	$f_{INCK} \times 0.96$	f_{INCK}	$f_{INCK} \times 1.02$	MHz	$f_{INCK} = 37.125 \text{ MHz}, 74.25 \text{ MHz}$
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	$f_{INCK} = 37.125 \text{ MHz}, 74.25 \text{ MHz}$
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	$f_{INCK} = 37.125 \text{ MHz}, 74.25 \text{ MHz}$
INCK clock duty	—	45.0	50.0	55.0	%	Define with $0.5 \times OV_{DD}$
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

*The INCK fluctuation affects the frame rate.

XHS, XVS Input Characteristics In Slave Mode (XMASTER pin = High)



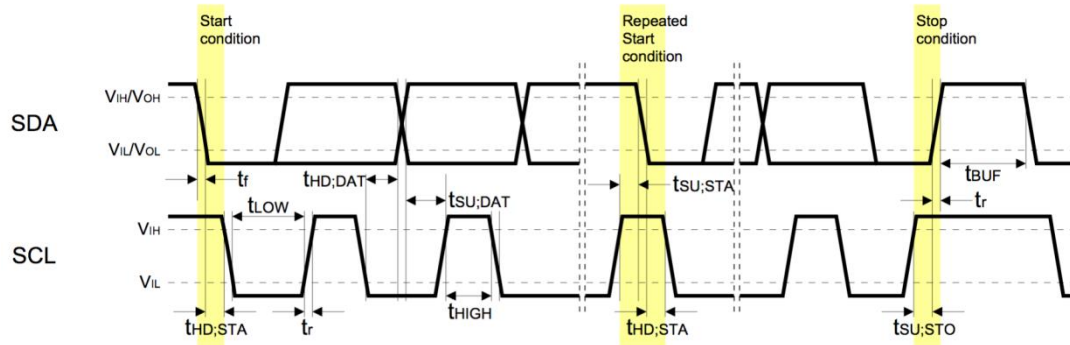
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	$4 / f_{INCK}$	—	—	ns	
XHS High level pulse width	t_{WHXHS}	$4 / f_{INCK}$	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	$1 / f_{INCK}$	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	$1 / f_{INCK}$	—	—	ns	
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %



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I²C Communication



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	条件
Low level input voltage	VIL	-0.3	—	$0.3 \times OV_{DD}$	V	
High level input voltage	VIH	$0.7 \times OV_{DD}$	—	1.9	V	
Low level input voltage	VOL	0	—	$0.2 \times OV_{DD}$	V	$OV_{DD} < 2\text{ V}$, Sink 3 mA
High level input voltage	VOH	$0.8 \times OV_{DD}$	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, $0.7 \times OV_{DD} - 0.3 \times OV_{DD}$
Input current	li	-10	—	10	μA	$0.1 \times OV_{DD} - 0.9 \times OV_{DD}$
Capacitance for SCK (SCL) /SDI (SDA)	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μs
Low period of the SCL clock	t_{LOW}	1.3	—	—	μs
High period of the SCL clock	t_{HIGH}	0.6	—	—	μs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μs

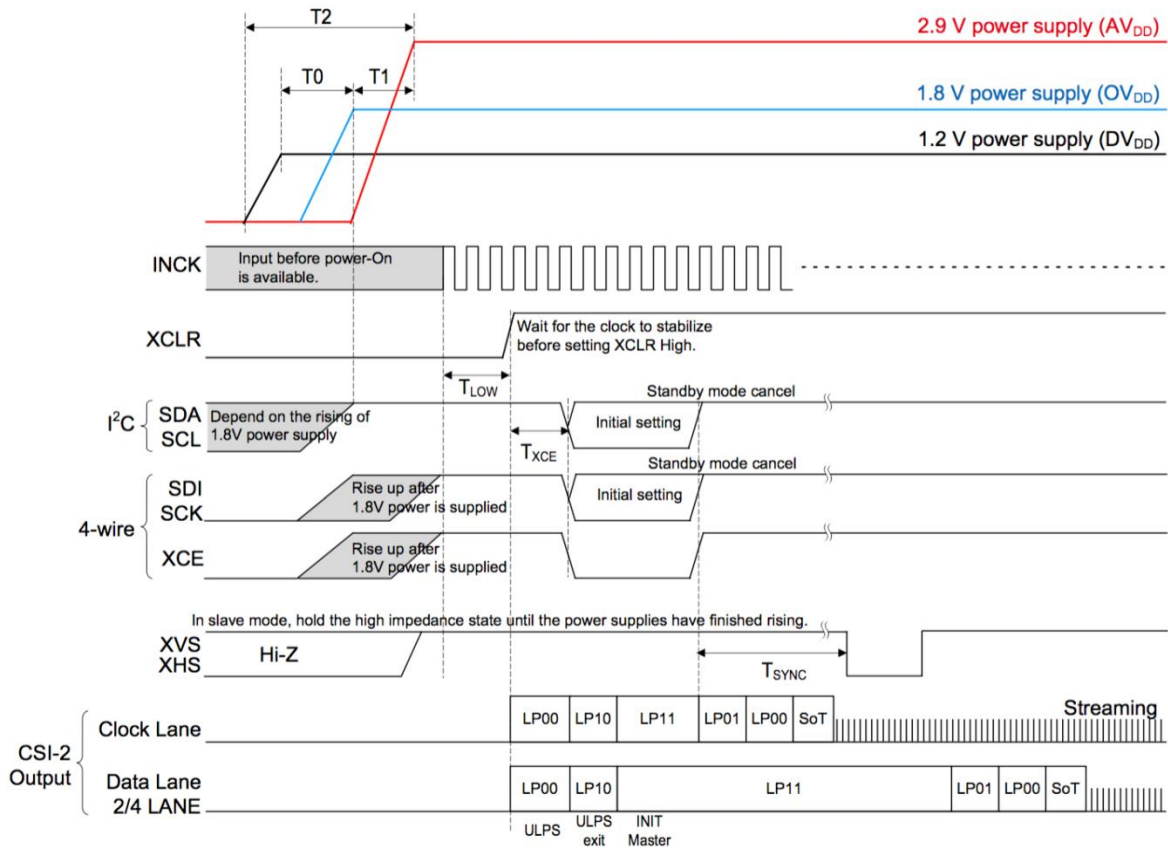


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Power-on Sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) → 1.8 V power supply (OV_{DD}) → 2.9 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. Start master clock (INCK) input after turning On the power supplies.
3. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.) In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}).
4. The system clear is applied by setting XCLR to High level. However, the maser clock needs to stabilize before setting the XCLR pin to High level.
5. Make the sensor setting by register communication after the system clear. A period of 20 μ s or more should be provided after setting XCLR High before inputting the communication enable signal XCE. In I^2C communication, XCE is fixed to High.

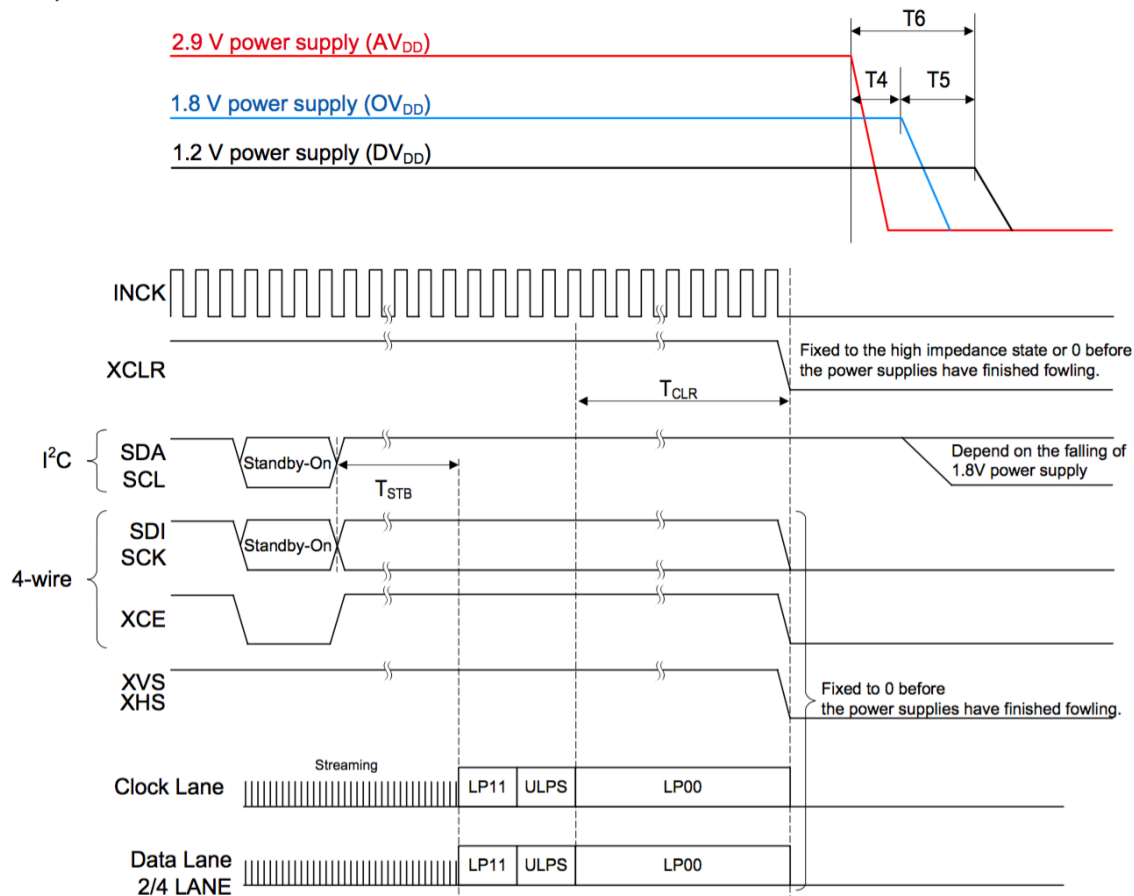


Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T_0	0	—	ns
1.8 V power supply rising → 2.9 V power supply rising	T_1	0	—	ns
Rising time of all power supply	T_2	—	200	ms
INCK active → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → Communication start	T_{XCE}	20	—	μ s
Standby OFF (communication) → External input XHS, XVS (slave mode only)	T_{SYNC}	20	—	ms



Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, OMODE, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



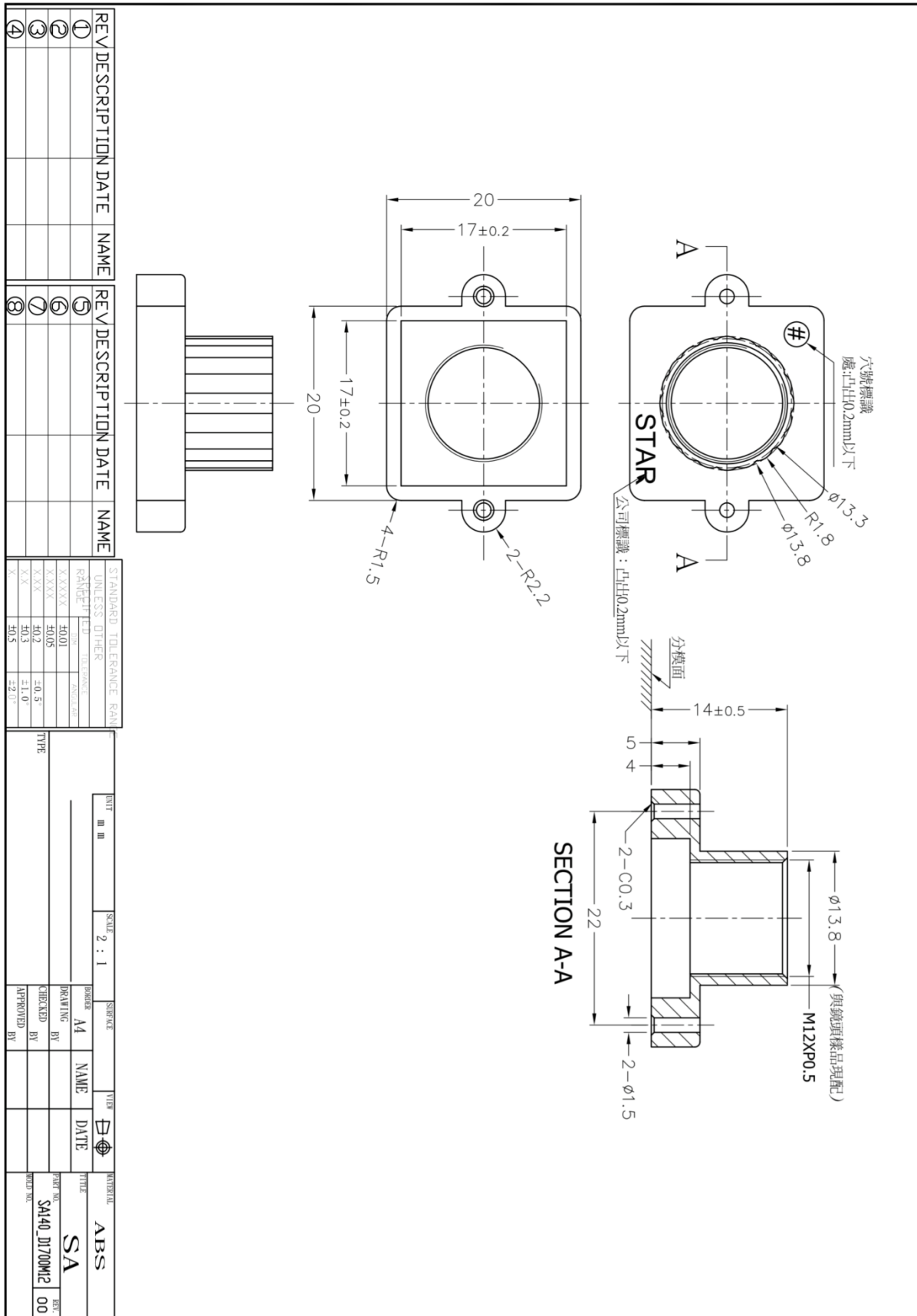
Item	Symbol	Min.	Max.	Unit
Standby ON (communication) → LP11 mode start	T_{STB}	Until FE		—
LP00 → XCLR falling	T_{CLR}	128	—	cycle
2.9 V shut down → 1.8 V shut down	$T4$	0	—	ns
1.8 V shut down → 1.2 V shut down	$T5$	0	—	ns
Shut down time of all power supply	$T6$	—	200	ms



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Revision History

Revision	Description	Release Date
1.0	First Release	11. May. 2019



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