



## **CrossLink Family**

## **Data Sheet**

FPGA-DS-02007-1.8

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## Acronyms in This Document

A list of acronyms used in this document.

| Acronym          | Definition                                          |
|------------------|-----------------------------------------------------|
| AR               | Augmented Reality                                   |
| ASIC             | Application-Specific Integrated Circuit             |
| BGA              | Ball Grid Array                                     |
| CMOS             | Complementary Metal Oxide Semiconductor             |
| CSI              | Camera Serial Interface                             |
| DBI              | Display Bus Interface                               |
| DDR              | Double Data Rate                                    |
| DPI              | Display Pixel Interface                             |
| DSI              | Display Serial Interface                            |
| EBR              | Embedded Block RAM                                  |
| ECLK             | Edge Clock                                          |
| FPGA             | Field-Programmable Gate Array                       |
| FPD              | Flat Panel Display                                  |
| GPIO             | General-Purpose Input/Output                        |
| HFOSC            | High Frequency Oscillator                           |
| HMI              | Human Machine Interface                             |
| I <sup>2</sup> C | Inter-Integrated Circuit                            |
| ISM              | Industrial, Scientific, Medical                     |
| LFOSC            | Low Frequency Oscillator                            |
| LUT              | Look Up Table                                       |
| LVC MOS          | Low-Voltage Complementary Metal Oxide Semiconductor |
| LVDS             | Low-Voltage Differential Signaling                  |
| LVTTTL           | Low Voltage Transistor-Transistor Logic             |
| MIPI             | Mobile Industry Processor Interface                 |
| NVCM             | Non-Volatile Configuration Memory                   |
| OTP              | One Time Programmable                               |
| PCLK             | Primary Clock                                       |
| PFU              | Programmable Functional Unit                        |
| PLL              | Phase Locked Loops                                  |
| PMU              | Power Management Unit                               |
| RAM              | Random Access Memory                                |
| Rx               | Receive                                             |
| SDR              | Single Data Rate                                    |
| SLVS200          | Scalable Low-Voltage Signaling                      |
| SPI              | Serial Peripheral Interface                         |
| TransFR          | Transparent Field Reconfiguration                   |
| Tx               | Transmit                                            |
| UHD              | Ultra-High-Definition                               |
| VR               | Virtual Reality                                     |
| WLCSP            | Wafer Level Chip Scale Packaging                    |

# 1. General Description

CrossLink™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice mobile FPGA 40-nm technology. It combines the extreme flexibility of an FPGA with the low power, low cost and small footprint of an ASIC.

CrossLink supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, subLVDS, HiSPi and more.

Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for CrossLink. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLink. Synthesis library support for CrossLink devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLink device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLink provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at 4 UHD and beyond.

## 1.1. Features

- Ultra-low power
- Sleep Mode Support
- Normal Operation – From 5 mW to 150 mW
- Ultra small footprint packages
  - 36-ball WLCSP (6 mm<sup>2</sup>)
  - 64-ball ucfBGA (12 mm<sup>2</sup>)
  - 80-ball ctfBGA (42 mm<sup>2</sup>)
  - 80-ball ckfBGA (49 mm<sup>2</sup>)
  - 81-ball csfBGA (20 mm<sup>2</sup>)
- Programmable architecture
  - 5936 LUTs
  - 180 Kb block RAM
  - 47 Kb distributed RAM
- Two hardened 4-lane MIPI D-PHY interfaces
  - Transmit and receive
  - 6 Gb/s per D-PHY interface
- Programmable source synchronous I/O
  - MIPI D-PHY Rx, LVDS Rx, LVDS Tx, subLVDS Rx, SLVS200 Rx, HiSPi Rx
  - Up to 1200 Mb/s per I/O
  - Four high-speed clock inputs
- Programmable CMOS I/O
  - LVTTTL and LVCMOS
  - 3.3 V, 2.5 V, 1.8 V and 1.2 V (outputs)
  - LVCMOS differential outputs
- Flexible device configuration
  - One Time Programmable (OTP) non-volatile configuration memory
  - Master SPI boot from external flash
  - Dual image booting supported
  - I<sup>2</sup>C programming
  - SPI programming
  - TransFR™ I/O for simple field updates
- Enhanced system level support
  - Reveal logic analyzer
  - TraceID for system tracking
  - On-chip hardened I<sup>2</sup>C block
- Applications examples
  - Dual MIPI CSI-2 to Single MIPI CSI-2 Aggregation
  - Quad MIPI CSI-2 to Single MIPI CSI-2 Aggregation
  - Single MIPI DSI to Single MIPI DSI Repeater
  - Single MIPI CSI-2 to Single MIPI CSI-2 Repeater
  - Single MIPI DSI to Dual MIPI DSI Splitter
  - Single MIPI CSI-2 to Dual MIPI CSI-2 Splitter
  - MIPI DSI to OpenLDI/FPD-Link/LVDS Translator
  - OpenLDI/FPD-Link/LVDS to MIPI DSI Translator
  - MIPI DSI/CSI-2 to CMOS Translator
  - CMOS to MIPI DSI/CSI-2 Translator
  - subLVDS to MIPI CSI-2 Translator

## 2. Product Feature Summary

Table 2.1 lists CrossLink device information and packages.

**Table 2.1. CrossLink Feature Summary**

| Device                                                         | CrossLink         |
|----------------------------------------------------------------|-------------------|
| LUTs                                                           | 5936              |
| sysMEM Blocks (9 Kb)                                           | 20                |
| Embedded Memory (Kb)                                           | 180               |
| Distributed RAM Bits (Kb)                                      | 47                |
| General Purpose PLL                                            | 1                 |
| NVCM                                                           | Yes               |
| Embedded I <sup>2</sup> C                                      | 2                 |
| Oscillator (10 KHz)                                            | 1                 |
| Oscillator (48 MHz)                                            | 1                 |
| Hardened MIPI D-PHY                                            | 2 <sup>1, 2</sup> |
| <b>Packages (Footprint, Pitch)</b>                             | <b>I/O</b>        |
| 36 WLCSP <sup>2</sup> (2.535 × 2.583 mm <sup>2</sup> , 0.4 mm) | 17                |
| 64 ucfBGA (3.5 × 3.5 mm <sup>2</sup> , 0.4 mm)                 | 29                |
| 80 ctfBGA (6.5 × 6.5 mm <sup>2</sup> , 0.65 mm)                | 37                |
| 80 ckfBGA (7.0 × 7.0 mm <sup>2</sup> , 0.65 mm)                | 37                |
| 81 csfBGA (4.5 × 4.5 mm <sup>2</sup> , 0.5 mm)                 | 37                |

**Notes:**

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

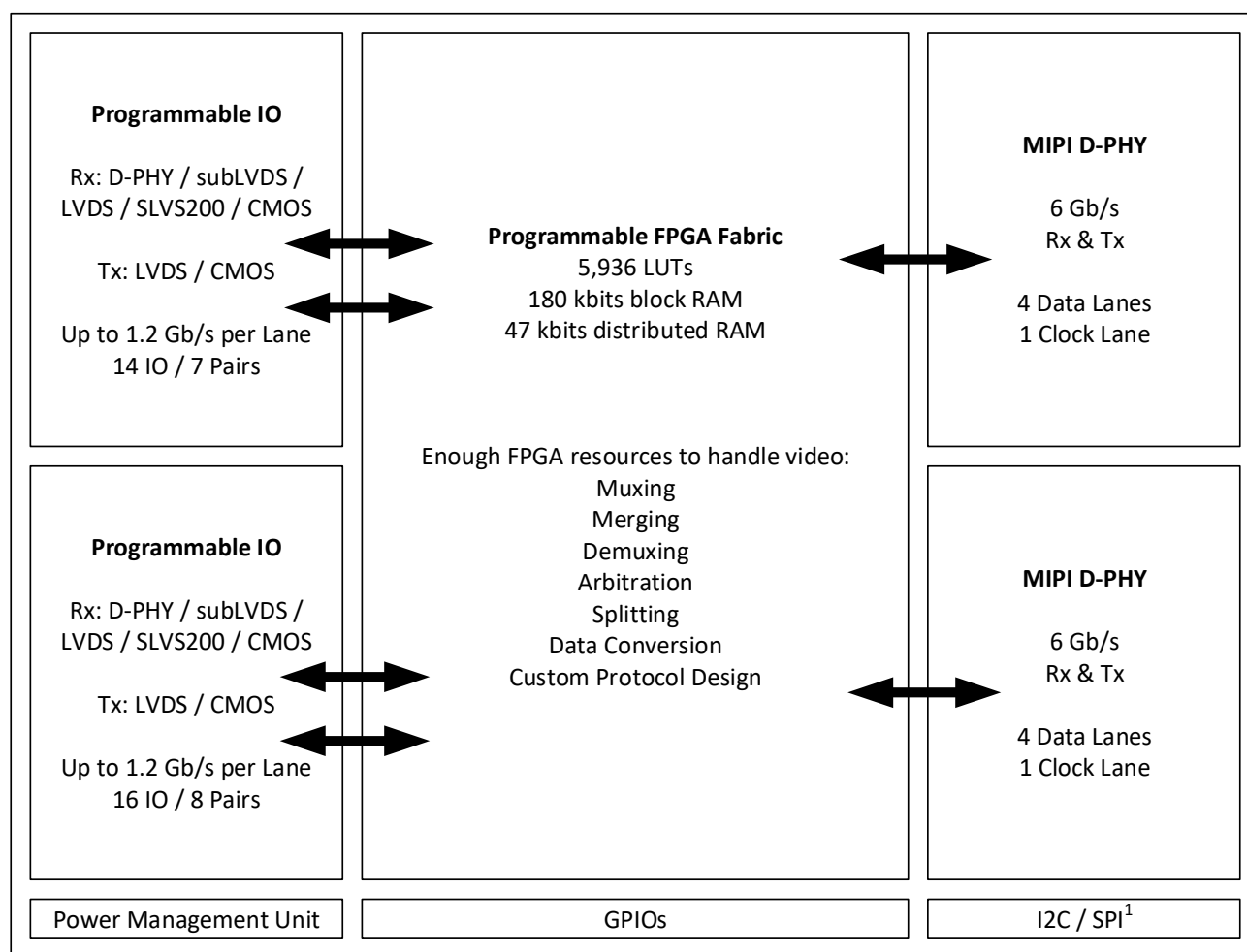
### 3. Architecture Overview

CrossLink is designed as a flexible, chip-to-chip bridging solution which supports a wide variety of applications. The device provides three key building blocks for these bridging applications:

- Up to two embedded Hard D-PHY blocks
- Two banks of flexible programmable I/O supporting a variety of standards including D-PHY Rx, subLVDS, SLVS200, LVDS, and CMOS
- A programmable logic core providing the LUTs, memory, and system resources to implement a wide range of bridging operations

In addition to these blocks, CrossLink also provides key system resources including a Power Management Unit, flexible configuration interface, additional CMOS GPIO, and user I<sup>2</sup>C blocks.

The block diagram for the device is shown in [Figure 3.1](#).



**Figure 3.1. CrossLink Device Block Diagram**

**Note:** I<sup>2</sup>C and SPI configuration modes are supported. User mode hardened I<sup>2</sup>C is also supported.

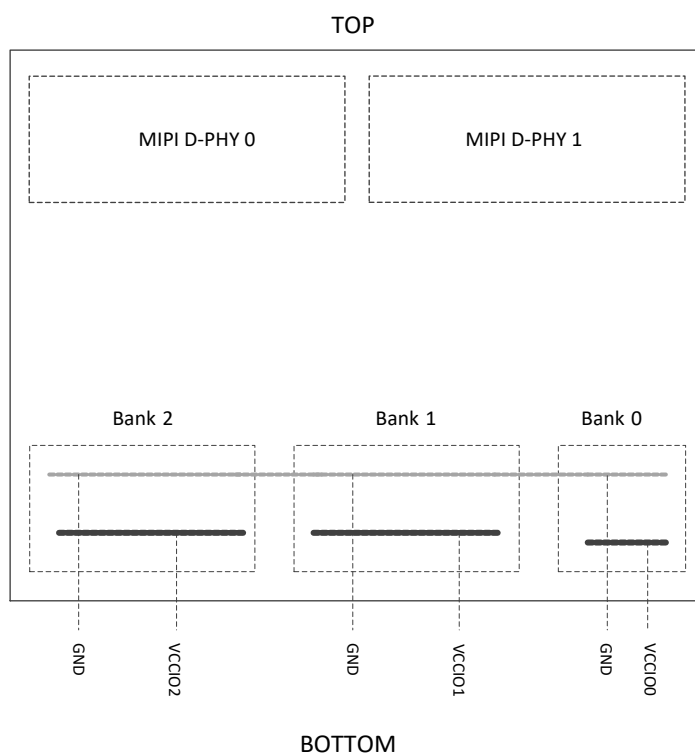
### 3.1. MIPI D-PHY Blocks

The top side of the device ([Figure 3.2](#)) includes two hard MIPI D-PHY quads. The D-PHY can be configured to support both camera interface (CSI-2) and display interface (DSI) applications. Below is a summary of the features supported by the hard D-PHY quads.

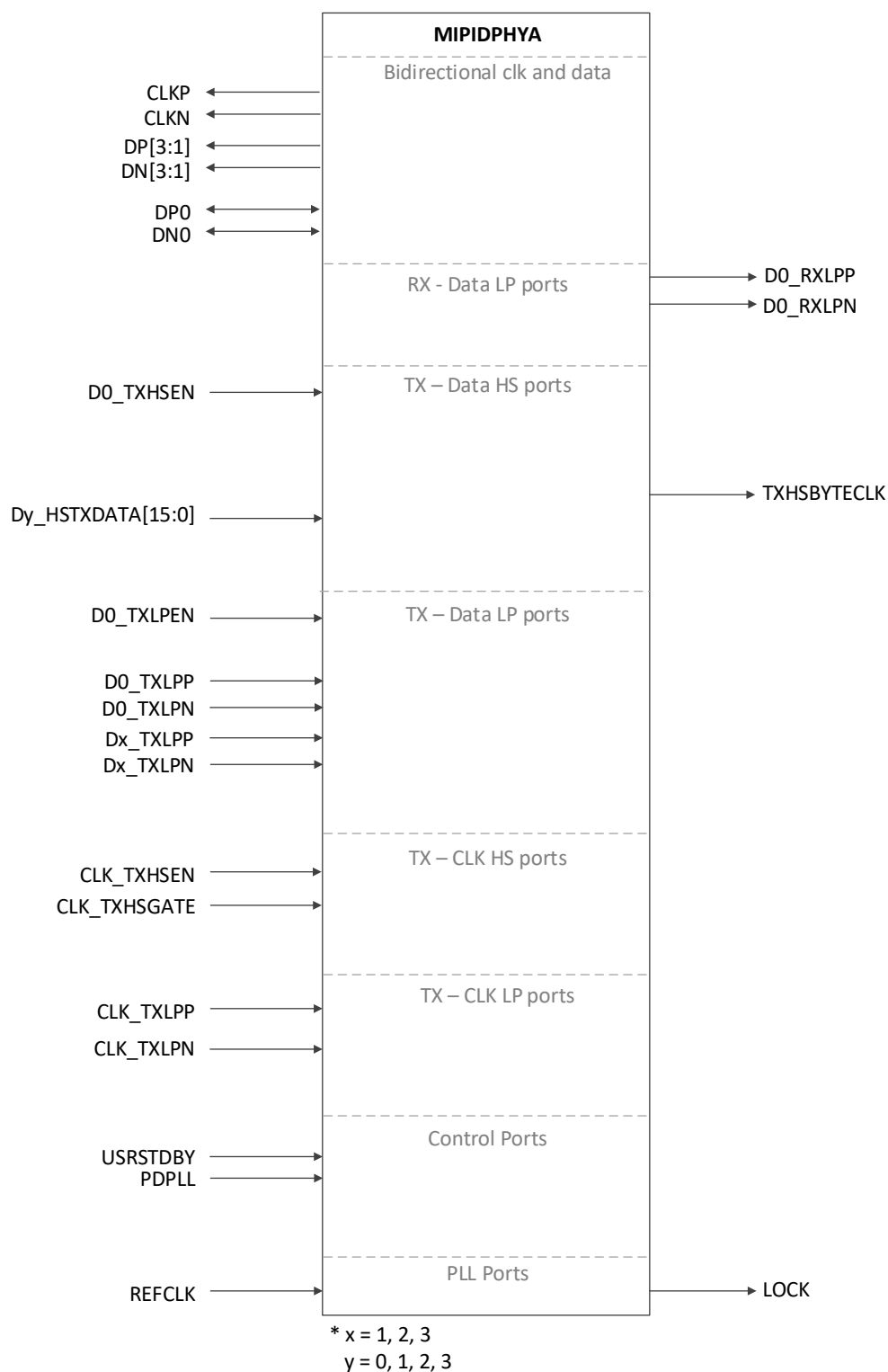
- Transmit and Receive compliant to MIPI Alliance Specification for D-PHY Revision 1.1
- High-Speed (HS) and Low-Power (LP) mode support (including built-in contention detect)
- Supports continuous clock mode or low power clock mode
- Up to 6 Gb/s per quad (1500 Mb/s data rate per lane)
- Dedicated PLL for Transmit Frequency Synthesis

Dedicated Serializer and De-Serializer blocks for fabric interfacing. Lattice Semiconductor provides a set of pre-engineered IP modules which include the full implementation and control of the hard D-PHY blocks to enable designers to focus on unique aspects of their design.

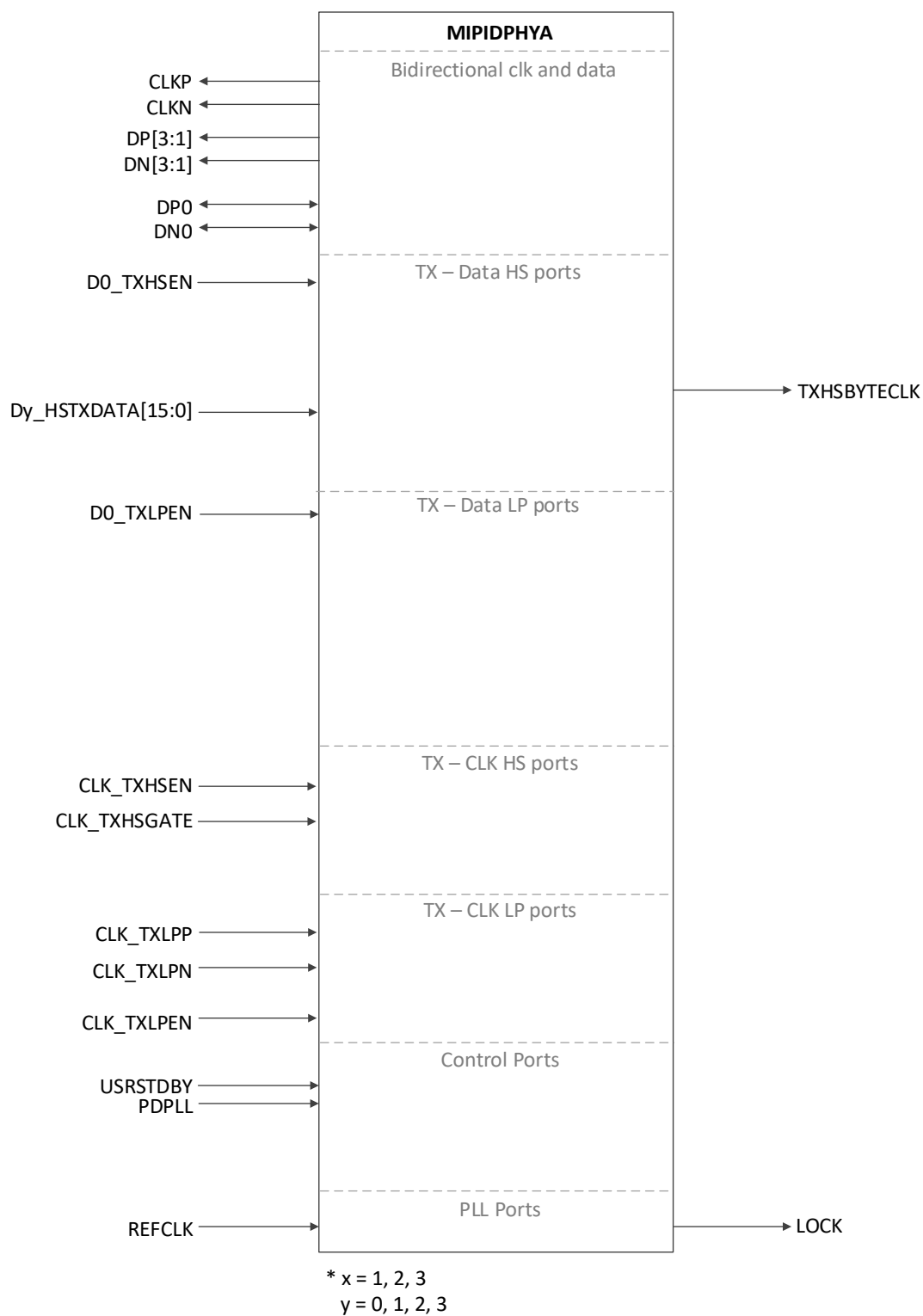
[Figure 3.3](#) to [Figure 3.6](#) show the signals connected to the fabric and the automatic settings when the hardened D-PHY is configured for the DSI/CSI-2 transmit and receive modes. Refer to [CrossLink High-Speed I/O Interface \(FPGA-TN-02012\)](#) for more information on the Hard D-PHY quads.



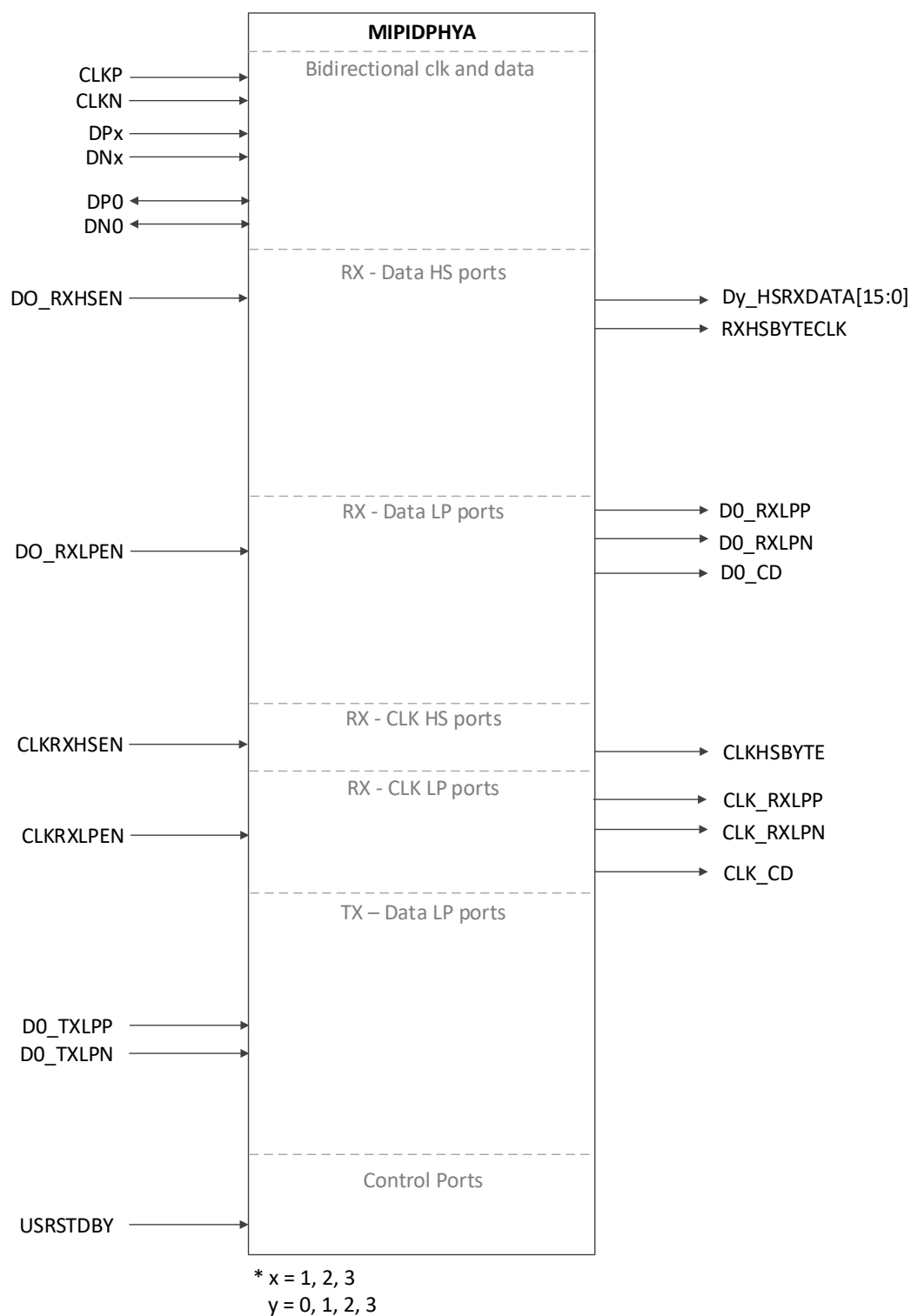
**Figure 3.2. CrossLink sysI/O Banking**



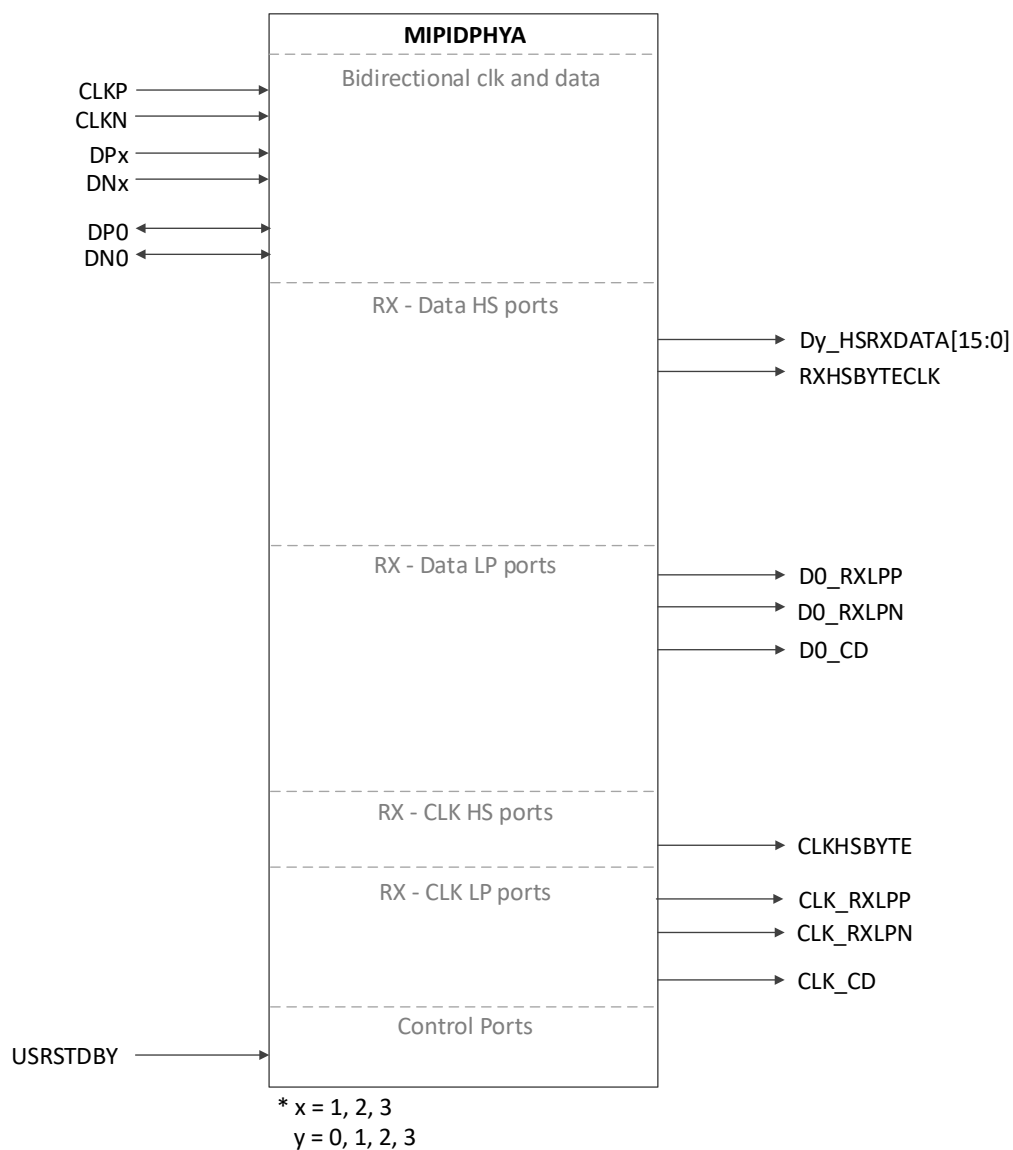
**Figure 3.3. MIPI DSI Transmit Interface with Hard D-PHY Module**



**Figure 3.4. MIPI CSI-2 Transmit Interface with Hard D-PHY Module**



**Figure 3.5. MIPI DSI Receive Interface with Hard D-PHY Module**



**Figure 3.6. MIPI CSI-2 Receive Interface with Hard D-PHY Module**

## 3.2. Programmable I/O Banks

CrossLink devices provide programmable I/O which can be used to interface to a variety of external standards on Banks 1 and 2. CrossLink devices also provide dedicated CMOS GPIOs on Bank 0. Bank 0 GPIOs only support Single Data Rate (SDR) interfaces, while Bank 1 and Bank 2 support both SDR and Double Data Rate (DDR) interfaces. The GPIOs on Bank 0 do not include differential signaling capabilities. The location of the three Banks and their associated supplies are shown in [Figure 3.2](#).

Bank 0 features:

- Support for the following single ended standards
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVTTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 k $\Omega$ , 6.8 k $\Omega$ , and 10 k $\Omega$

Bank 1 and Bank 2 features:

- Built-in support for the following differential standards
  - LVDS – Tx and Rx
  - SLVS200 – Rx
  - subLVDS – Rx
  - MIPI – Rx (both LP and HS receive on a single differential pair)
- Support for the following single ended standards
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs Only)
  - LVTTTL33
- Independent voltage levels per bank based on VCCIO supply
- Input/output gearboxes per LVDS pair supporting several ratios for video interface applications
  - DDRX1, DDRX2, DDRX4, DDRX8 and DDRX71, DDRX141
  - Programmable delay cells to support edge-aligned and center-aligned interfaces
- Programmable differential termination (~ 100  $\Omega$ ) with dynamic enable control
- Tri-state control for output
- Input/output register blocks
- Single-ended standards support open-drain and programmable input hysteresis
- Optional weak pull-up resistors

**Table 3.1. CrossLink Output Support per Bank Basis**

| OUTPUT   | BANK 0 | BANK 1 | BANK 2 |
|----------|--------|--------|--------|
| LVCMOS12 | —      | ✓      | ✓      |
| LVCMOS18 | ✓      | ✓      | ✓      |
| LVCMOS25 | ✓      | ✓      | ✓      |
| LVCMOS33 | ✓      | ✓      | ✓      |
| LVTTTL33 | ✓      | ✓      | ✓      |
| LVDS25   | —      | ✓      | ✓      |

**Table 3.2. CrossLink Input Support per Bank Basis**

| INPUT      | BANK 0 | BANK 1 | BANK 2 |
|------------|--------|--------|--------|
| LVC MOS12  | —      | —      | —      |
| LVC MOS18  | ✓      | ✓      | ✓      |
| LVC MOS25  | ✓      | ✓      | ✓      |
| LVC MOS33  | ✓      | ✓      | ✓      |
| LVTTL33    | ✓      | ✓      | ✓      |
| LVDS25     | —      | ✓      | ✓      |
| MIPI D-PHY | —      | ✓      | ✓      |
| SLVS200    | —      | ✓      | ✓      |
| subLVDS    | —      | ✓      | ✓      |

### 3.3. sysI/O Buffers

The CrossLink sysI/O buffers are distributed across three banks located at the bottom of the CrossLink device as shown in [Figure 3.2](#). The sysI/O buffers support a wide variety of standards to interface to a range of systems including LVDS, subLVDS, LVC MOS, LVTTL, SLVS200 and MIPI. CrossLink supports single-ended buffers on all three banks. Differential I/O is supported on Bank 1 and Bank 2.

#### 3.3.1. Programmable PULLMODE Settings

The CrossLink sysI/O buffers offer multiple programmable value pull-up resistors on the three banks. The pull-up values are programmable on a “per-pin” basis. The default state of the I/O pins prior to configuration is tri-stated with a weak pull-up to  $V_{CCIOx}$ . The I/O pins convert to the software user-defined settings after the configuration bitstream is successfully downloaded to the device. Each sysIO buffer can be programmed with a 100 k $\Omega$  (weak pull-up), 3.3 k $\Omega$ , 6.8 k $\Omega$ , 10 k $\Omega$  or no pull-up. These pull-up options allow an I<sup>2</sup>C interface to be placed on the majority of the pins on the device. These options are not exclusively for I<sup>2</sup>C protocol and may be used for other functions.

#### 3.3.2. Output Drive Strength

Each CrossLink output can have its own individual drive strength setting, but is predefined based on the  $V_{CCIOx}$  setting. [Table 3.3](#) lists the drive settings for the corresponding I/O type.

**Table 3.3. Drive Strength Values**

| VCCIOx (V) | I/O Type  | Drive Strength (mA) |
|------------|-----------|---------------------|
| 3.3        | LVTTL33   | 8                   |
| 3.3        | LVC MOS33 | 8                   |
| 2.5        | LVC MOS25 | 6                   |
| 1.8        | LVC MOS18 | 4                   |
| 1.2        | LVC MOS12 | 2                   |

#### 3.3.3. On-Chip Termination

Bank 1 and bank 2 of CrossLink support LVDS, SLVS200 subLVDS and MIPI D-PHY inputs. These two banks support on-chip 100  $\Omega$  input differential termination between LVDS, SLVS200 and subLVDS pairs. For MIPI D-PHY inputs, the on-chip 100  $\Omega$  termination is dynamically enabled based on the HSSEL (High Speed Select) signal.

See [CrossLink High-Speed I/O Interface \(FPGA-TN-02012\)](#) and [CrossLink sysI/O Usage Guide \(FPGA-TN-02016\)](#) for details.

### 3.4. Programmable FPGA Fabric

CrossLink is built around a programmable logic fabric consisting of 5936 four input lookup tables (LUT4) arranged alongside dedicated registers in Programmable Functional Units (PFU). These PFU blocks are the building blocks for logic, arithmetic, RAM and ROM functions. The PFU blocks are connected via a programmable routing network. The Lattice Diamond design software configures the PFU blocks and the programmable routing for each unique design. Interspersed between rows of PFU are rows of sysMEM™ Embedded Block RAM (EBR), with programmable I/O banks, embedded I<sup>2</sup>C and embedded MIPI D-PHY arranged on the top and bottom of the device as shown in Figure 3.7.

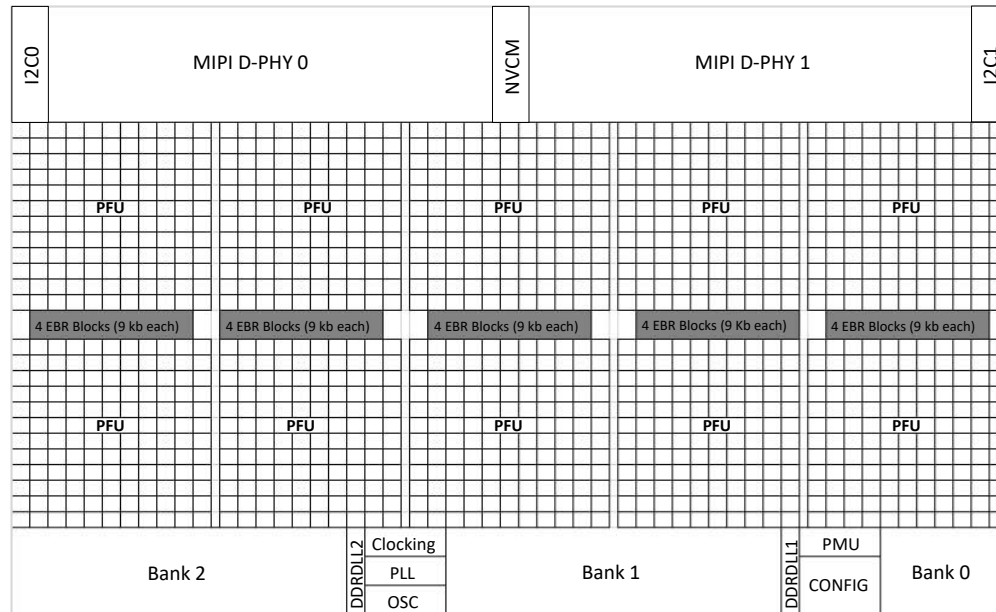


Figure 3.7. CrossLink Device Simplified Block Diagram (Top Level)

#### 3.4.1. PFU Blocks

The core of the CrossLink device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0 – 3 as shown in Figure 3.8. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic or ROM functions.

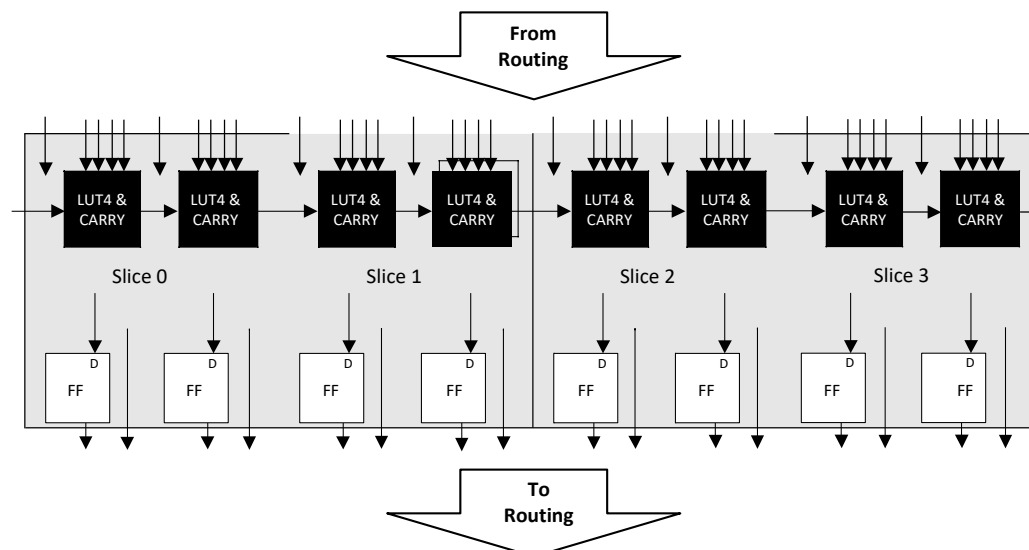
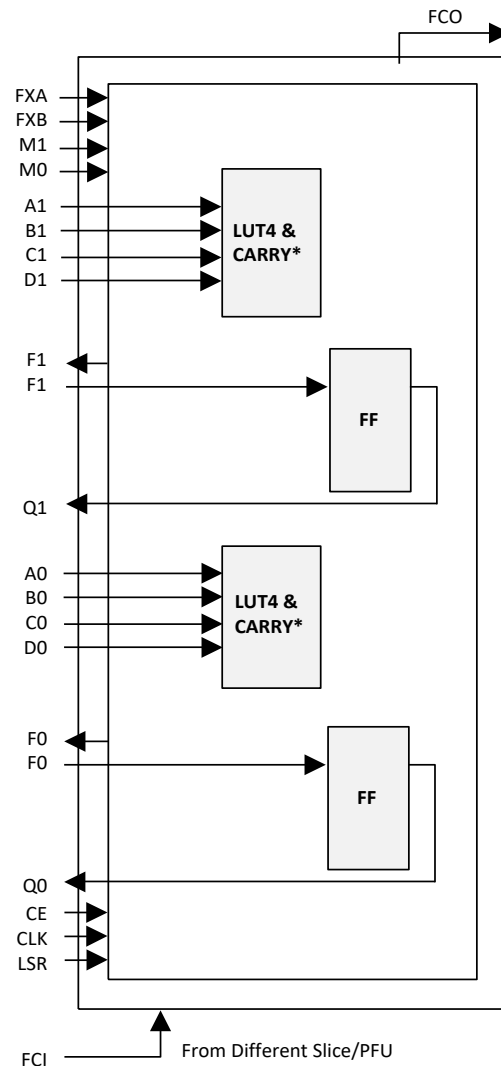


Figure 3.8. CrossLink PFU Diagram

### 3.4.2. Slice

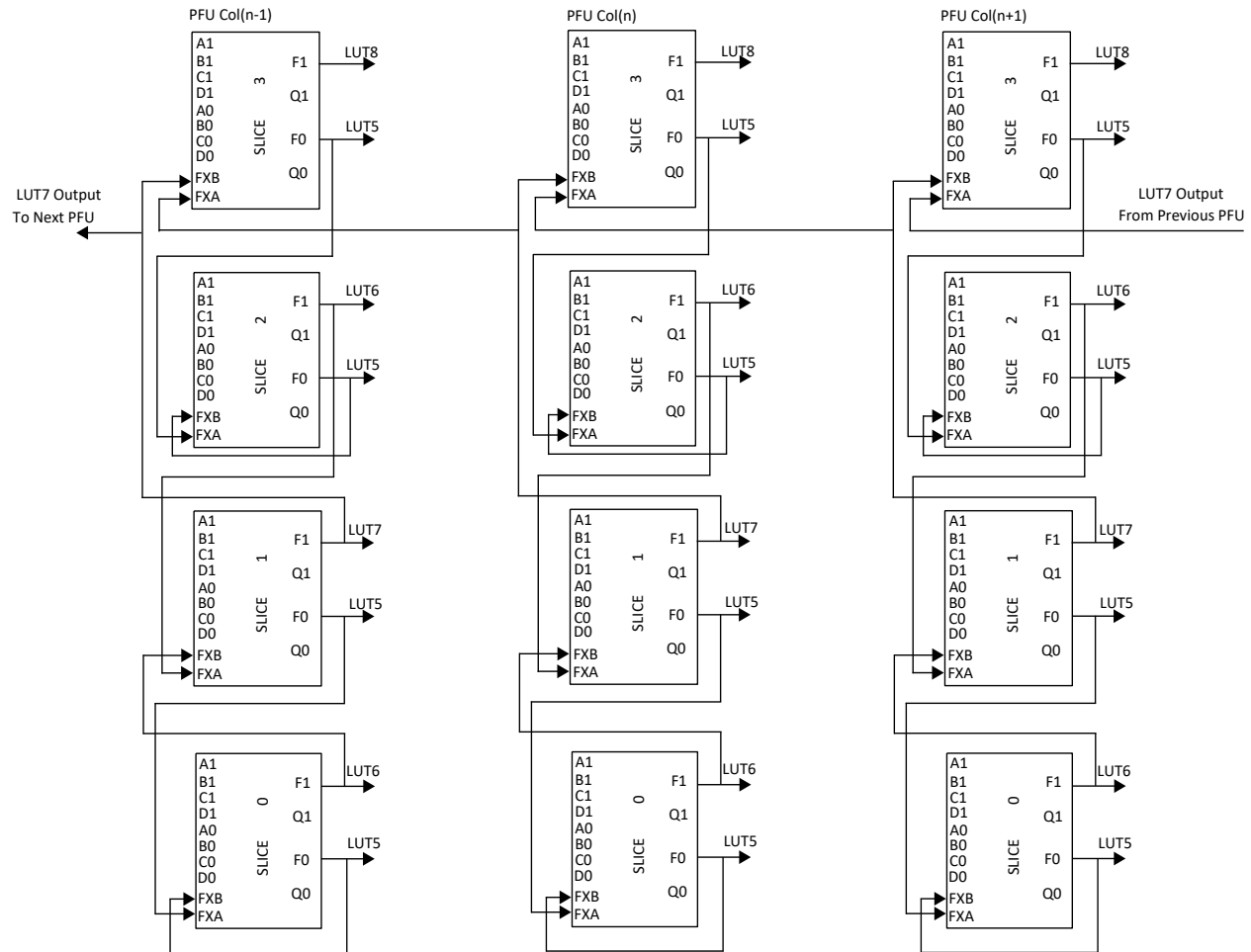
Each slice contains two LUT4s feeding two registers. Each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 3.9 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals: 13 signals from routing and 1 signal from the carry-chain routed from the adjacent slice or PFU. There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7, and LUT8. Table 3.4 and Figure 3.10 list the signals associated with all the slices. Figure 3.8 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7, and LUT8.



**Notes:** For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:  
WCK is CLK  
WRE is from LSR  
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2  
WAD [A:D] is a 4-bit address from slice 2 LUT input

**Figure 3.9. Slice Diagram**



**Figure 3.10. Connectivity Supporting LUT5, LUT6, LUT7 and LUT8**

**Table 3.4. Slice Signal Descriptions**

| Function | Type               | Signal Names   | Description                                                      |
|----------|--------------------|----------------|------------------------------------------------------------------|
| Input    | Data signal        | A0, B0, C0, D0 | Inputs to LUT4                                                   |
| Input    | Data signal        | A1, B1, C1, D1 | Inputs to LUT4                                                   |
| Input    | Multi-purpose      | M0             | Multipurpose Input                                               |
| Input    | Multi-purpose      | M1             | Multipurpose Input                                               |
| Input    | Control signal     | CE             | Clock Enable                                                     |
| Input    | Control signal     | LSR            | Local Set/Reset                                                  |
| Input    | Control signal     | CLK            | System Clock                                                     |
| Input    | Inter-PFU signal   | FCI            | Fast Carry-in <sup>1</sup>                                       |
| Input    | Inter-slice signal | FXA            | Intermediate signal to generate LUT6, LUT7 and LUT8 <sup>2</sup> |
| Input    | Inter-slice signal | FXB            | Intermediate signal to generate LUT6, LUT7 and LUT8 <sup>2</sup> |
| Output   | Data signals       | F0, F1         | LUT4 output register bypass signals                              |
| Output   | Data signals       | Q0, Q1         | Register outputs                                                 |
| Output   | Inter-PFU signal   | FCO            | Fast carry chain output <sup>1</sup>                             |

**Notes:**

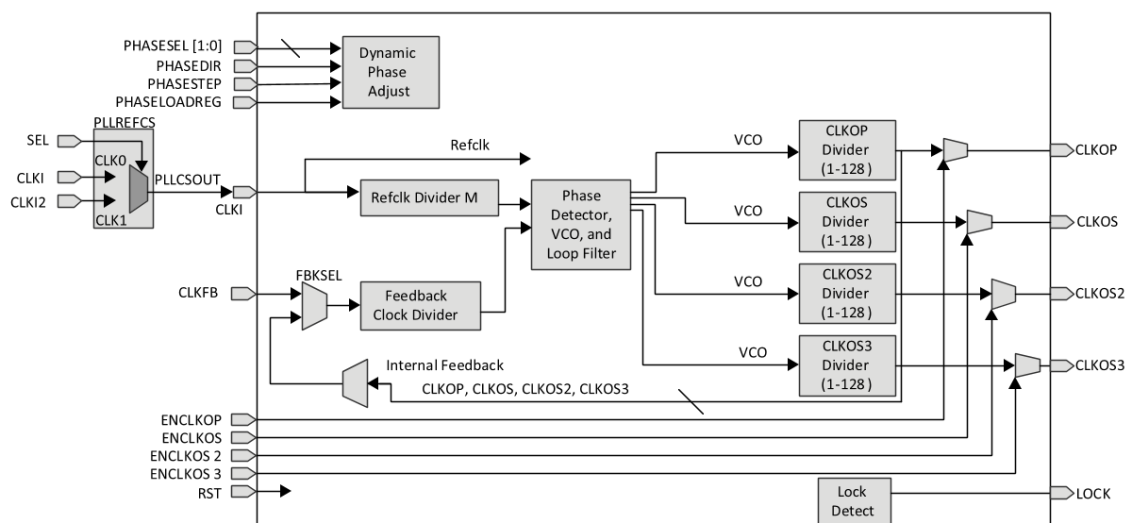
1. See [Figure 3.9](#) for connection details.
2. Requires two adjacent PFUs.

## 3.5. Clocking Structure

The CrossLink device family provides resources to support a wide range of clocking requirements for programmable video bridging. These resources are described below. For details, refer to [CrossLink sysCLOCK PLL/DLL Design and Usage Guide \(FPGA-TN-02015\)](#).

### 3.5.1. sysCLK PLL

The CrossLink sysCLK PLL provides the ability to synthesis clock frequencies (See [Table 4.14](#) for input frequency range). The PLL provides features such as dynamic selectable clock input, clock injection delay removal, independent dynamic output enable control, and programmable output phase adjustment. The architecture of the PLL is shown in [Figure 3.11](#).



**Figure 3.11. CrossLink PLL Block Diagram**

[Table 3.5](#) provides a description of the signals in the PLL block.

**Table 3.5. CrossLink PLL Port Definition**

| Signal        | I/O | Description                                                               |
|---------------|-----|---------------------------------------------------------------------------|
| CLKI          | I   | Input clock to PLL                                                        |
| CLKFB         | I   | Feedback clock                                                            |
| USRSTDBY      | I   | User port to put the PLL to sleep mode                                    |
| PHASESEL[1:0] | I   | Select the output affected by Dynamic Phase adjustment                    |
| PHASEDIR      | I   | Dynamic phase adjustment direction                                        |
| PHASESTEP     | I   | Dynamic phase adjustment step                                             |
| PHASELOADREG  | I   | Load dynamic phase adjustment values into PLL                             |
| RST           | I   | Resets the whole PLL                                                      |
| ENCLKOP       | I   | Enable PLL output CLKOP                                                   |
| ENCLKOS       | I   | Enable PLL output CLKOS                                                   |
| ENCLKOS2      | I   | Enable PLL output CLKOS2                                                  |
| ENCLKOS3      | I   | Enable PLL output CLKOS3                                                  |
| PLLWAKESYNC   | I   | Enable PLL switching from internal to user feedback path when PLL wake up |
| CLKOP         | O   | PLL main output clock                                                     |
| CLKOS         | O   | PLL output clock                                                          |
| CLKOS2        | O   | PLL output clock                                                          |
| CLKOS3        | O   | PLL output clock                                                          |
| LOCK          | O   | PLL LOCK to CLKI, asynchronous signal. Active high indicates PLL lock     |

### 3.5.2. Primary Clocks

The primary clock routing network is made up of low skew clock routing resources with connectivity to every synchronous element of the device. Primary clock sources are selected in the center mux and distributed on the primary clock routing to clock the synchronous elements in the FPGA fabric. CrossLink family of devices provide up to eight unique global primary clocks. Primary clock sources are:

- LVDS PIO pins
- GPIO pins
- PLL outputs
- Clock dividers
- Fabric internally generated clock signal
- Divided down clock from DPHY
- OSCI

The routing clock structure is shown in [Figure 3.12](#).

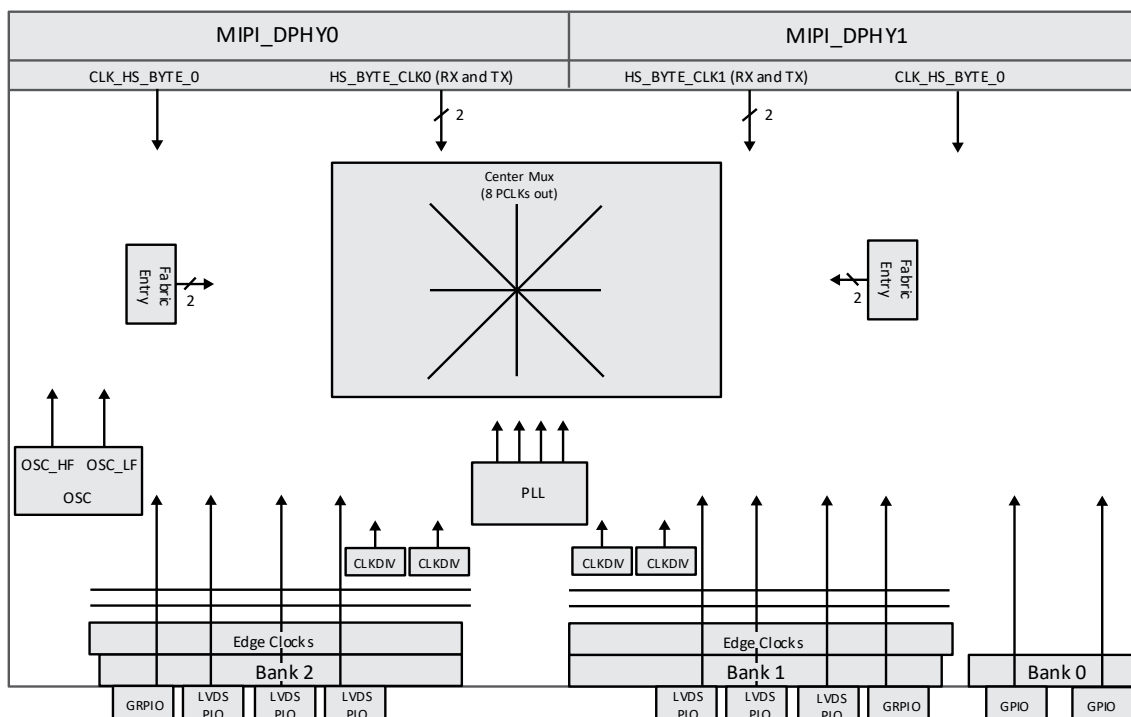


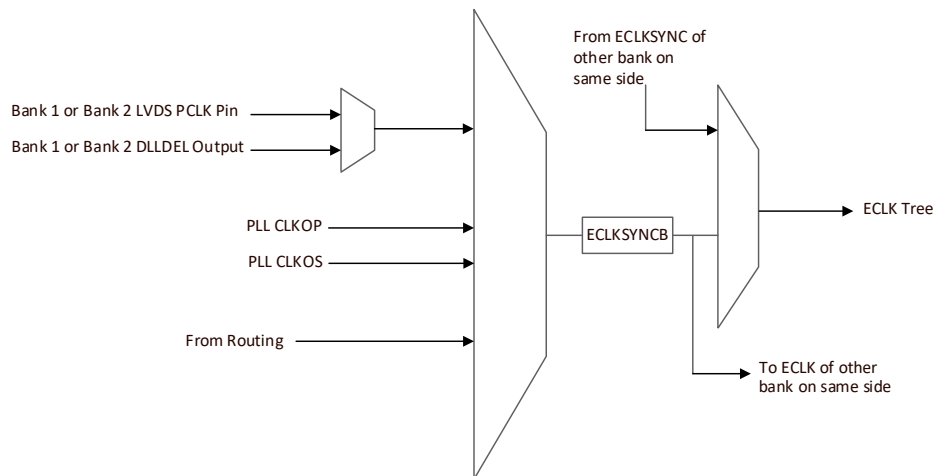
Figure 3.12. CrossLink Clocking Structure

### 3.5.3. Edge Clocks

The CrossLink device has Edge Clock (ECLK) at the bottom two banks (Bank 1 and Bank 2) of the device ([Figure 3.12](#)). The CrossLink device has two edge clocks per Programmable I/O bank. These clocks, which have low injection time and skew, are used to clock I/O registers. Edge clock resources are designed for high speed I/O interfaces with high fan-out capability. The sources of edge clocks are:

- Dedicated Clock (PCLK) pins muxed with the DLLDEL output
- PLL outputs (CLKOP and CLKOS)
- Internal nodes

ECLK input MUX collects all clock sources as shown in [Figure 3.13](#) below. There are two ECLK Input MUXs, one on each bank. It drives the ECLK SYNC modules and the ECLK Clock Divider through a 2 to 1 MUX.



**Figure 3.13. CrossLink Edge Clock Sources per Bank**

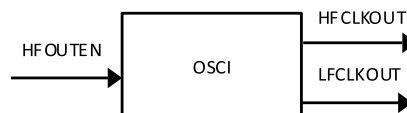
### 3.5.4. Dynamic Clock Enables

Each PLL output has a user input signal to dynamically enable/disable its output to provide a glitch free clock. Then the clock enable signal is set to logic '0', the corresponding output clock is held to logic '0'. This allows the user to save power by stopping the corresponding output clock when not in use.

### 3.5.5. Internal Oscillator (OSCI)

The OSCI element performs multiple functions on the CrossLink device. It is used for configuration and available during user mode. OSCI element has the following features in user mode:

- Always-on low frequency clock output (LFCLKOUT) with nominal frequency of 10 kHz
- High-frequency clock output (HFCLKOUT) with nominal frequency of 48 MHz that can be enabled or disabled using HFOUTEN input
- Programmable output dividers (HFCLKDIV) for 48 MHz, 24 MHz, 12 MHz or 6 MHz HFCLKOUT output
- Both output clocks have a direct connection to primary clock routing
- [Figure 3.14](#), [Table 3.6](#) and [Table 3.7](#) below show the OSCI definitions



**Figure 3.14. CrossLink OSCI Component Symbol**

**Table 3.6. OSCI Component Port Definition**

| Port Name | I/O | Description                        |
|-----------|-----|------------------------------------|
| HFOUTEN   | I   | High frequency clock output enable |
| HFCLKOUT  | O   | High frequency clock output        |
| LFCLKOUT  | O   | Low Frequency clock output         |

**Table 3.7. OSCI Component Attribute Definition**

| Defparam Name | Description                            | Value      | Default |
|---------------|----------------------------------------|------------|---------|
| HFCLKDIV      | Configure HF oscillator output divider | 1, 2, 4, 8 | 1       |

### 3.6. Embedded Block RAM Overview

CrossLink devices contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-KB RAM with memory core, dedicated input registers and output registers with separate clock and clock enable.

Support for different memory configurations:

- Single Port
- True Dual Port
- Pseudo Dual Port
- ROM
- FIFO (logic wrapper added automatically by design tools)

Flexible customization features:

- Initialization of RAM/ROM
- Memory cascading (handled automatically by design tools)
- Optional parity bit support
- Byte-enable
- Multiple block size options
- RAM modes support optional Write Through or Read-Before-Write modes

For details, refer to [CrossLink Memory Usage Guide \(FPGA-TN-02017\)](#).

**Table 3.8. sysMEM Block Configurations**

| Memory Mode      | Memory Size Configurations                                   |
|------------------|--------------------------------------------------------------|
| Single Port      | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| True Dual Port   | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9             |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| ROM              | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |

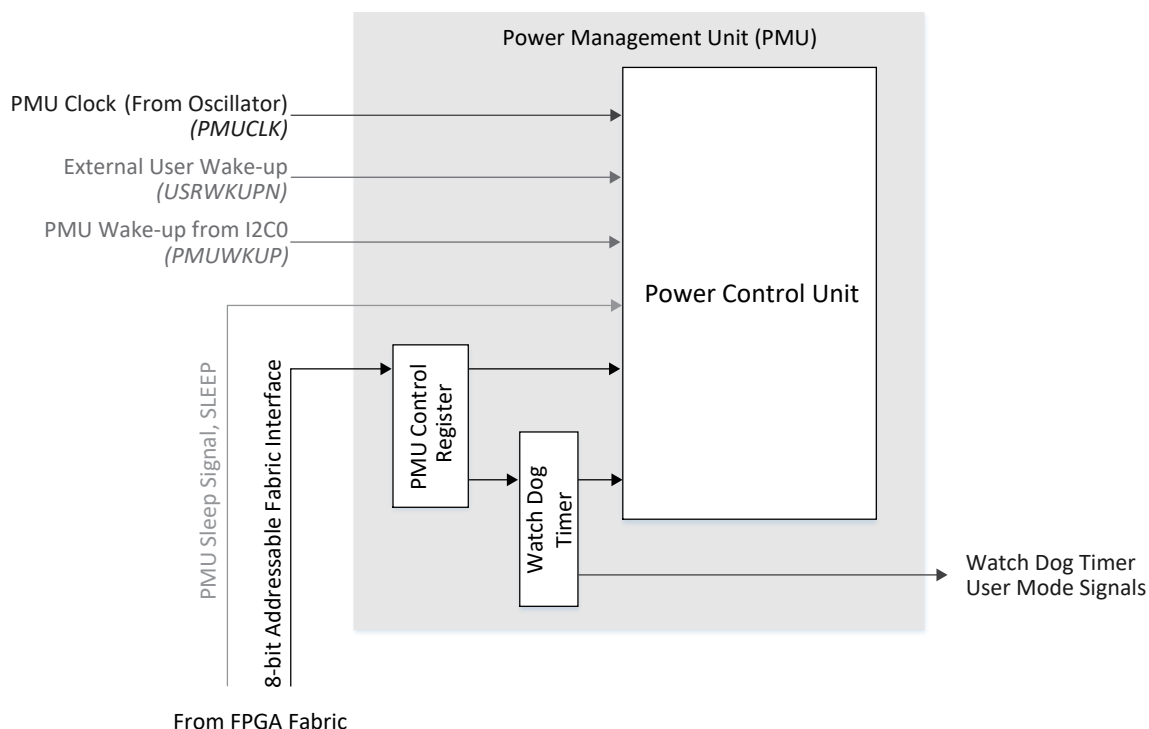
### 3.7. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 3.15 shows the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU's FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I<sup>2</sup>C).

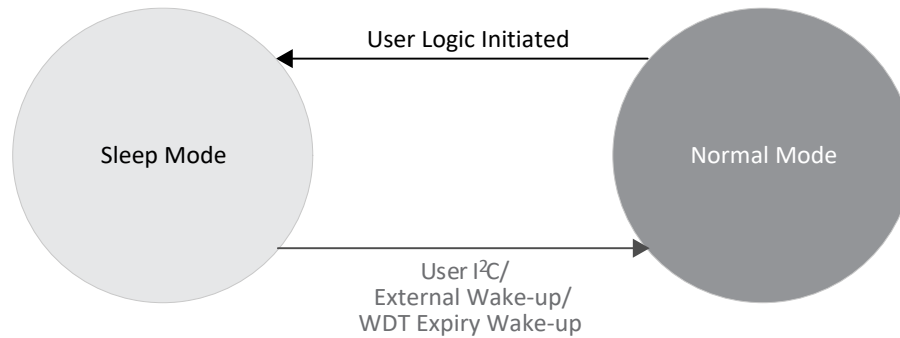


**Figure 3.15. CrossLink MIPI D-PHY Block**

#### 3.7.1. PMU State Machine

PMU can place the device in two mutually exclusive states – Normal State and Sleep State. Figure 3.16 shows the PMU State Machine triggers for transition from one state to the other.

- Normal state – All elements of the device are active to the extent required by the design. In this state, the device is at fully active and performing as required by the application.  
Note that the power consumption of the device is highest in this state.
- Sleep state – The device is power gated such that the device is not operational. The configuration of the device and the EBR contents are retained; thus in Sleep mode, the device does not lose configuration SRAM and EBR contents. When it transitions to Normal state, device operates with these contents preserved.  
The PMU is active along with the associated GPIOs.  
The power consumption of the device is lowest in this state. This helps reduce the overall power consumption for the device.



**Figure 3.16. CrossLink PMU State Machine**

For more details, refer to [Power Management and Calculation for CrossLink Devices \(FPGA-TN-02018\)](#).

### 3.8. User I²C IP

CrossLink devices have two I²C IP cores that can be configured either as an I²C master or as an I²C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I²C. The pins for the I2C1 interface are not pre-assigned – user can use any General Purpose I/O pins.

The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, refer to [CrossLink I2C Hardened IP Usage Guide \(FPGA-TN-02019\)](#).

### 3.9. Programming and Configuration

CrossLink is a SRAM-based programmable logic device that includes an internal Non-Volatile Configuration Memory (NVCM), as well as flexible SPI and I<sup>2</sup>C configuration modes. CrossLink provides four modes for loading the configuration data into the SRAM memory.

- Self-Download (NVCM) mode – CrossLink retrieves bitstream from internal NVCM
- Master SPI mode – CrossLink retrieves bitstream from an external SPI Flash
- Slave SPI mode – System microprocessor writes bitstream to CrossLink through SPI port
- Slave I<sup>2</sup>C mode – System microprocessor writes bitstream to CrossLink through I<sup>2</sup>C port

CrossLink provides a set of sysCONFIG I/O pins to program and configure the FPGA. The sysCONFIG pins are grouped together to create ports (I<sup>2</sup>C, SSPI or MSPI) that are used to interact with the FPGA for programming, configuration, and access of resources inside the FPGA. The sysCONFIG pins (Table 3.9) in a configuration group may be active and used for programming the FPGA or they can be reconfigured to act as general purpose I/Os.

**Table 3.9. CrossLink sysCONFIG Pins**

| Pin Name        | Associated sysCONFIG Port                     |
|-----------------|-----------------------------------------------|
| CRESETB         | Self Download Mode/SSPI/MSPI/I <sup>2</sup> C |
| CDONE           | Self Download Mode/SSPI/MSPI/I <sup>2</sup> C |
| SPI_SCK/MCK/SDA | SSPI/MSPI/I <sup>2</sup> C                    |
| SPI_SS/CSN/SCL  | SSPI/MSPI/I <sup>2</sup> C                    |
| MOSI            | SSPI/MSPI                                     |
| MISO            | SSPI/MSPI                                     |

As external power ramps up, a Power On Reset (POR) circuit inside the FPGA becomes active. When POR conditions are met, the POR circuit releases an internal reset strobe, allowing the device to begin its initialization process. After CrossLink drives CDONE low, CrossLink enters the memory initialization phase where it clears all of the SRAM memory inside the FPGA. CrossLink remains in initialization state until the CRESETB pin is deasserted or after SSPI/I<sup>2</sup>C activation code is received.

- After CRESETB goes from low to high, the Configuration Logic puts the device into master auto booting mode where it boots either from the internal NVRAM or an external SPI boot PROM.
- Holding the CRESETB low postpones the master auto booting event and allows the slave configuration ports (Slave SPI or Slave I<sup>2</sup>C) to detect a ‘Slave Active’ condition where the SPI or I<sup>2</sup>C Master sends an Activation Key code to CrossLink. An external SPI Master or I<sup>2</sup>C Master needs to write the Activation Key to the FPGA while CRESETB is held LOW and within 9.5 ms from V<sub>cc</sub> min during power up to enter into one of the slave configuration modes.
- Sources should not drive output to CrossLink until configuration has been completed to ensure CrossLink is in a known state.

In addition to the flexible configuration modes, the CrossLink configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing users to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent read back
- 64-bit unique TraceID per device

For more information, refer to [CrossLink Programming and Configuration Usage Guide \(FPGA-TN-02014\)](#).

## 4. DC and Switching Characteristics

### 4.1. Absolute Maximum Ratings

**Table 4.1. Absolute Maximum Ratings** <sup>1, 2, 3</sup>

| Symbol                                                                       | Parameter                                                              | Min  | Max  | Unit |
|------------------------------------------------------------------------------|------------------------------------------------------------------------|------|------|------|
| V <sub>CC</sub>                                                              | Core Supply Voltage                                                    | −0.5 | 1.32 | V    |
| V <sub>CCGPLL</sub>                                                          | PLL Supply Voltage                                                     | −0.5 | 1.32 | V    |
| V <sub>CCAUX</sub>                                                           | Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 2.5 V <sup>4</sup> | −0.5 | 2.75 | V    |
|                                                                              | Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 3.3 V <sup>4</sup> | −0.5 | 3.63 | V    |
| V <sub>CCIO</sub>                                                            | I/O Driver Supply Voltage for Banks 0, 1, 2                            | −0.5 | 3.63 | V    |
| —                                                                            | Input or I/O Transient Voltage Applied                                 | −0.5 | 3.63 | V    |
| V <sub>CCA_DPHYx</sub><br>V <sub>CCPLL_DPHY</sub><br>V <sub>CCMU_DPHY1</sub> | MIPI D-PHY Supply Voltages                                             | −0.5 | 1.32 | V    |
| —                                                                            | Voltage Applied on MIPI D-PHY Pins                                     | −0.5 | 1.32 | V    |
| T <sub>A</sub>                                                               | Storage Temperature (Ambient)                                          | −65  | 150  | °C   |
| T <sub>J</sub>                                                               | Junction Temperature (TJ)                                              | —    | +125 | °C   |

**Notes:**

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. V<sub>CCAUX</sub> must be set to 2.5 V when an external I<sup>2</sup>C Master or SPI Master is used to program CrossLink’s NVCM. This restriction is not applicable for read access of the NVCM, such as Self-Download Mode, where the NVCM is already programmed and CrossLink retrieves the bitstream from the NVCM and programs it to the SRAM memory.

### 4.2. Recommended Operating Conditions

**Table 4.2. Recommended Operating Conditions** <sup>1, 2</sup>

| Symbol                             | Parameter                                                                             | Min   | Max   | Unit |
|------------------------------------|---------------------------------------------------------------------------------------|-------|-------|------|
| V <sub>CC</sub>                    | Core Supply Voltage                                                                   | 1.14  | 1.26  | V    |
| V <sub>CCGPLL</sub>                | PLL Supply Voltage                                                                    | 1.14  | 1.26  | V    |
| V <sub>CCAUX</sub>                 | Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 2.5 V <sup>3</sup>                | 2.375 | 2.625 | V    |
|                                    | Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 3.3 V <sup>3</sup>                | 3.135 | 3.465 | V    |
| V <sub>CCIO0</sub>                 | I/O Driver Supply Voltage for Bank 0                                                  | 1.71  | 3.465 | V    |
| V <sub>CCIO1/2</sub>               | I/O Driver Supply Voltage for Bank 1, 2                                               | 1.14  | 3.465 | V    |
| T <sub>JIND</sub>                  | Junction Temperature, Industrial Operation                                            | −40   | 100   | °C   |
| <b>D-PHY External Power Supply</b> |                                                                                       |       |       |      |
| V <sub>CCA_DPHYx</sub>             | Analog Supply Voltage for D-PHY                                                       | 1.14  | 1.26  | V    |
| V <sub>CCPLL_DPHYx</sub>           | PLL Supply voltage for D-PHY                                                          | 1.14  | 1.26  | V    |
| V <sub>CCMU_DPHY1</sub>            | Supply for V <sub>CCA_DPHY1</sub> and V <sub>CCPLL_DPHY1</sub> on the WLCSP36 package | 1.14  | 1.26  | V    |

**Notes:**

1. For Correct Operation, all supplies must be held in their valid operation range.
2. Like power supplies, must be tied together if they are at the same supply voltage. Follow the noise filtering recommendations in [CrossLink Hardware Checklist \(FPGA-TN-02013\)](#).
3. V<sub>CCAUX</sub> must be set to 2.5 V when an external I<sup>2</sup>C Master or SPI Master is used to program CrossLink’s NVCM. This restriction is not applicable for read access of the NVCM, such as Self-Download Mode, where the NVCM is already programmed and CrossLink retrieves the bitstream from the NVCM and programs it to the SRAM memory.

### 4.3. Power Supply Ramp Rates

Over recommended operating conditions.

**Table 4.3. Power Supply Ramp Rates\***

| Symbol            | Parameter                                      | Min | Max | Unit |
|-------------------|------------------------------------------------|-----|-----|------|
| $t_{\text{RAMP}}$ | Power supply ramp rates for all power supplies | 0.6 | 10  | V/ms |

\*Note: Assume monotonic ramp rates.

### 4.4. Power-On-Reset Voltage Levels

Over recommended operating conditions.

**Table 4.4. Power-On-Reset Voltage Levels <sup>1,3</sup>**

| Symbol             | Parameter                                                                                                          |                      | Min  | Max  | Unit |
|--------------------|--------------------------------------------------------------------------------------------------------------------|----------------------|------|------|------|
| $V_{\text{PORUP}}$ | Power-On-Reset ramp up trip point<br>(Monitoring $V_{\text{CC}}$ , $V_{\text{CCIO0}}$ , and $V_{\text{CCAUX}}$ )   | $V_{\text{CC}}$      | 0.62 | 0.93 | V    |
|                    |                                                                                                                    | $V_{\text{CCIO0}}^2$ | 0.87 | 1.50 | V    |
|                    |                                                                                                                    | $V_{\text{CCAUX}}$   | 0.90 | 1.53 | V    |
| $V_{\text{PORDN}}$ | Power-On-Reset ramp down trip point<br>(Monitoring $V_{\text{CC}}$ , $V_{\text{CCIO0}}$ , and $V_{\text{CCAUX}}$ ) | $V_{\text{CC}}$      | —    | 0.79 | V    |
|                    |                                                                                                                    | $V_{\text{CCIO0}}^2$ | —    | 1.50 | V    |
|                    |                                                                                                                    | $V_{\text{CCAUX}}$   | —    | 1.53 | V    |

**Notes:**

- These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only  $V_{\text{CCIO0}}$  (Config Bank) has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
- Configuration starts after  $V_{\text{CC}}$ ,  $V_{\text{CCIO0}}$  and  $V_{\text{CCAUX}}$  reach  $V_{\text{PORUP}}$ . For details, see  $t_{\text{CONFIGURATION}}$  time in [Table 4.21](#) on page 44.

## 4.5. Power Supply Sequence Requirements

CrossLink includes the following supplies:

- $V_{CC}$  – Core supply
- $V_{CCGPLL}$  – PLL supply
- $V_{CCAUX}$  – Auxiliary supply
- $V_{CCIOX}$  (includes  $V_{CCIO0}$ ,  $V_{CCIO1}$  and  $V_{CCIO2}$ ) – Bank I/O driver supply
- $V_{CCA\_DPHYX}$  (includes  $V_{CCA\_DPHY0}$  and  $V_{CCA\_DPHY1}$ ) – D-PHY analog supply
- $V_{CCPLL\_DPHYX}$  (includes  $V_{CCPLL\_DPHY0}$  and  $V_{CCPLL\_DPHY1}$ ) – D-PHY PLL supply
- $V_{CCMU\_DPHY1}$  –  $V_{CCA\_DPHY1}$  and  $V_{CCPLL\_DPHY1}$  supplies for WLCSP36 package

It is recommended to bring up power supplies in the following order. Note that there is no specific timing delay between the power supplies.

### Power Supply Power-Up Sequence

1.  $V_{CCIOX}$  supplies should be powered-up first, before the other supplies.  $V_{CCIOX}$  must reach a level of 0.6 V before any subsequent power supplies are ramped.
2.  $V_{CC}/V_{CCGPLL}/V_{CCA\_DPHYX}/V_{CCPLL\_DPHYX}/V_{CCMU\_DPHY1}$  should be powered-up next, after  $V_{CCIOX}$  has reached a level of 0.6 V or higher.
3.  $V_{CCAUX}$  must be powered up at the same time or after  $V_{CC}$ . If  $V_{CC}$  and  $V_{CCAUX}$  are powered up concurrently, at no point can the  $V_{CCAUX}$  supply be higher than  $V_{CC}$  until the point when  $V_{CC}$  has reached the minimum operating voltage.

### Power Supply Power-Down Sequence

There are no sequencing requirements for the Power-Down of the device. In the event that any supply is powered down below the POR trip point, then all supplies should be powered down before the device can be powered up following the [Power Supply Power-Up Sequence](#).

## 4.6. ESD Performance

Refer to the [LIFMD Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

## 4.7. DC Electrical Characteristics

Over recommended operating conditions.

**Table 4.5. DC Electrical Characteristics**

| Symbol                     | Parameter                                | Condition                                                                                   | Min | Typ | Max  | Unit    |
|----------------------------|------------------------------------------|---------------------------------------------------------------------------------------------|-----|-----|------|---------|
| $I_{IL}, I_{IH}^{1, 4, 5}$ | Input or I/O Leakage                     | $0 \leq V_{IN} \leq V_{CCIO}$                                                               | -10 | —   | +10  | $\mu A$ |
| $I_{PU}^4$                 | Internal Pull-Up Current                 | $V_{CCIO} = 1.8 V$ between $0 \leq V_{IN} \leq 0.65 * V_{CCIO}$                             | -3  | —   | -31  | $\mu A$ |
|                            |                                          | $V_{CCIO} = 2.5 V$ between $0 \leq V_{IN} \leq 0.65 * V_{CCIO}$                             | -8  | —   | -72  | $\mu A$ |
|                            |                                          | $V_{CCIO} = 3.3 V$ between $0 \leq V_{IN} \leq 0.65 * V_{CCIO}$                             | -11 | —   | -128 | $\mu A$ |
| $C_1^2$                    | I/O Capacitance <sup>2</sup>             | $V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V$ ,<br>$V_{CC} = 1.2 V, V_{IO} = 0$ to $V_{IH} (MAX)$ | —   | 6   | —    | pF      |
| $C_2^2$                    | Dedicated Input Capacitance <sup>2</sup> | $V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V$ ,<br>$V_{CC} = 1.2 V, V_{IO} = 0$ to $V_{IH} (MAX)$ | —   | 6   | —    | pF      |
| $C_3^2$                    | MIPI D-PHY High Speed I/O Capacitance    | $V_{CCIO} = 2.5V, V_{CC} = 1.2V, V_{CC*\_DPHY} = 1.2V, V_{IO} = 0$ to $V_{IH} (MAX)$        | —   | 5   | —    | pF      |
| $V_{HYST}^3$               | Hysteresis for Single-Ended Inputs       | $V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$<br>$V_{CC} = 1.2 V, V_{IO} = 0$ to $V_{IH} (MAX)$          | —   | 200 | —    | mV      |

**Notes:**

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2.  $T_A = 25^\circ C$ ,  $f = 1.0 MHz$ .
3. Hysteresis is not available for  $V_{CCIO} = 1.2 V$ .
4. Weak pull-up setting. Programmable pull-up resistors on Bank 0 will see higher current. Refer to [CrossLink sys/I/O Usage Guide \(FPGA-TN-02016\)](#) for details on programmable pull-up resistors.
5. Input pins are clamped to  $V_{CCIO}$  and GND by a diode. When input is higher than  $V_{CCIO}$ , or lower than GND, the Input Leakage current will be higher than the  $I_{IL}$  and  $I_{IH}$ .

## 4.8. CrossLink Supply Current

Over recommended operating conditions.

**Table 4.6. CrossLink Supply Current**

| Symbol                                           | Parameter                                                                                            | Typ | Unit |
|--------------------------------------------------|------------------------------------------------------------------------------------------------------|-----|------|
| <b>Normal Operation<sup>1</sup></b>              |                                                                                                      |     |      |
| I <sub>CC</sub>                                  | V <sub>CC</sub> Power Supply Current                                                                 | 7   | mA   |
| I <sub>CCPLL</sub>                               | PLL Power Supply Current                                                                             | 50  | μA   |
| I <sub>CCAUX</sub>                               | Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current                     | 3   | mA   |
| I <sub>CCIOx</sub>                               | Bank x Power Supply Current (per Bank)                                                               | 60  | μA   |
| I <sub>CCA_DPHYx</sub>                           | V <sub>CCA_DPHYx</sub> Power Supply Current                                                          | 8.5 | mA   |
| I <sub>CCPLL_DPHYx</sub>                         | V <sub>CCPLL_DPHYx</sub> Power Supply Current                                                        | 1.5 | mA   |
| I <sub>CCMLL_DPHYx</sub>                         | V <sub>CCA_DPHY1</sub> & V <sub>CCPLL_DPHY1</sub> Power Supply Operation Current for WLCSP36 Package | 10  | mA   |
| <b>Standby Current<sup>2</sup></b>               |                                                                                                      |     |      |
| I <sub>CC_STDBY</sub>                            | V <sub>CC</sub> Power Supply Standby Current                                                         | 4   | mA   |
| I <sub>CCPLL_STDBY</sub>                         | PLL Power Supply Standby Current                                                                     | 10  | μA   |
| I <sub>CCAUX_STDBY</sub>                         | Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Standby Current             | 0.2 | mA   |
| I <sub>CCIOx_STDBY</sub>                         | Bank Power Supply Standby Current (per Bank)                                                         | 6   | μA   |
| I <sub>CCA_DPHYx_STDBY</sub>                     | V <sub>CCA_DPHYx</sub> Power Supply Standby Current                                                  | 6   | μA   |
| I <sub>CCPLL_DPHYx_STDBY</sub>                   | V <sub>CCPLL_DPHYx</sub> Power Supply Standby Current                                                | 4   | μA   |
| I <sub>CCMLL_DPHYx_STDBY</sub>                   | V <sub>CCA_DPHY1</sub> & V <sub>CCPLL_DPHY1</sub> Power Supply Static Current for WLCSP36 Package    | 10  | μA   |
| <b>Sleep/Power Down Mode Current<sup>3</sup></b> |                                                                                                      |     |      |
| I <sub>CC_SLEEP</sub>                            | V <sub>CC</sub> Power Supply Sleep Current                                                           | 0.2 | mA   |
| I <sub>CCPLL_SLEEP</sub>                         | PLL Power Supply Current                                                                             | 10  | μA   |
| I <sub>CCAUX_SLEEP</sub>                         | Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current                     | 20  | μA   |
| I <sub>CCIOx_SLEEP</sub>                         | Bank Power Supply Current (per Bank)                                                                 | 6   | μA   |
| I <sub>CCA_DPHY_SLEEP</sub>                      | V <sub>CCA_DPHYx</sub> Power Supply Sleep Current                                                    | 6   | μA   |
| I <sub>CCPLL_DPHY_SLEEP</sub>                    | V <sub>CCPLL_DPHYx</sub> Power Supply Sleep Current                                                  | 4   | μA   |
| I <sub>CCAMLL_DPHYx_SLEEP</sub>                  | V <sub>CCA_DPHY1</sub> & V <sub>CCPLL_DPHY1</sub> Power Supply Static Current for WLCSP36 Package    | 10  | μA   |

### Notes:

- Normal Operation
  - 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge design under the following conditions:
    - T<sub>J</sub> = 25 °C, all power supplies at nominal voltages.
    - Typical processed device in csfBGA81 package.
    - To determine power for all other applications and operating conditions, use Power Calculator in Lattice Diamond design software
- Standby Operation
 

A typically processed device in csfBGA81 package with “blank” pattern programmed. A “blank” pattern configures the part to the following conditions:

  - All outputs are tri-stated, all inputs are held at either V<sub>CCIO</sub>, or GND.
  - All clock inputs are at 0 MHz.
  - T<sub>J</sub> = 25 °C, all power supplies at nominal voltages.
  - No pull-ups on I/O.
- Sleep/Power Down Mode
 

2:1 MIPI CSI-2 Image Sensor Aggregator Bridge design under the following conditions:

  - Design is put into Sleep/Power Down Mode with user logic powers down D-PHY, and enters into Sleep Mode in PMU.
  - T<sub>J</sub> = 25 °C, all power supplies at nominal voltages.
  - Typical processed device in csfBGA81 package.
- For ucfBGA64 package
  - V<sub>CCA\_DPHY0</sub> and V<sub>CCA\_DPHY1</sub> are tied together as V<sub>CCA\_DPHYx</sub>.
  - V<sub>CCPLL\_DPHY0</sub> and V<sub>CCPLL\_DPHY1</sub> are tied together as V<sub>CCPLL\_DPHYx</sub>.

5. For WLCS36 package
  - a.  $V_{CCGP_{LL}}$  and  $V_{CCIO1}$  (Bank 1) are tied together to  $V_{CC}$ .
  - b.  $V_{CCPLL\_DPHY1}$  and  $V_{CCA\_DPHY1}$  are tied together as  $V_{CCMU\_DPHY1}$ .
6. To determine the CrossLink start-up peak current, use the Power Calculator tool in the Lattice Diamond design software.

## 4.9. Power Management Unit (PMU) Timing

Over recommended operating conditions.

**Table 4.7. PMU Timing\***

| Symbol        | Parameter                            | Device      | Max | Unit |
|---------------|--------------------------------------|-------------|-----|------|
| $t_{PMUWAKE}$ | Time for PMU to wake from Sleep mode | All Devices | 0.5 | ms   |

\*Note: For details on PMU usage, refer to [Power Management and Calculation for CrossLink Devices \(FPGA-TN-02018\)](#).

## 4.10. sysI/O Recommended Operating Conditions

Over recommended operating conditions.

**Table 4.8. sysI/O Recommended Operating Conditions<sup>1</sup>**

| Standard                             | $V_{CCIO}$ |      |       |
|--------------------------------------|------------|------|-------|
|                                      | Min        | Typ  | Max   |
| LVC MOS33/LVTTL33                    | 3.135      | 3.30 | 3.465 |
| LVC MOS25                            | 2.375      | 2.50 | 2.625 |
| LVC MOS18                            | 1.710      | 1.80 | 1.890 |
| LVC MOS12 (Output only) <sup>2</sup> | 1.140      | 1.20 | 1.260 |
| subLVDS (Input only)                 | 1.710      | 1.80 | 1.890 |
|                                      | 2.375      | 2.50 | 2.625 |
|                                      | 3.135      | 3.30 | 3.465 |
| SLVS200 (Input only) <sup>3</sup>    | 1.140      | 1.20 | 1.260 |
|                                      | 1.710      | 1.80 | 1.890 |
|                                      | 2.375      | 2.50 | 2.625 |
|                                      | 3.135      | 3.30 | 3.465 |
| LVDS (Input only)                    | 1.710      | 1.80 | 1.890 |
|                                      | 2.375      | 2.50 | 2.625 |
|                                      | 3.135      | 3.30 | 3.465 |
| LVDS (Output only)                   | 2.375      | 2.50 | 2.625 |
| MIPI (Input only)                    | 1.140      | 1.20 | 1.260 |

**Notes:**

1. For input voltage compatibility, refer to [CrossLink sysI/O Usage Guide \(FPGA-TN-02016\)](#).
2. For VCCIO1 and VCCIO2 only.
3. For SLVS200/MIPI interface I/O placement, see the [Programmable I/O Banks](#) section.

## 4.11. sysI/O Single-Ended DC Electrical Characteristics

Table 4.9. sysI/O Single-Ended DC Electrical Characteristics<sup>1</sup>

| Input/Output Standard                  | $V_{IL}$ |                 | $V_{IH}$        |                | $V_{OL} \text{ Max (V)}$ | $V_{OH} \text{ Min (V)}$ | $I_{OL} \text{ (mA)}$ | $I_{OH} \text{ (mA)}$ |
|----------------------------------------|----------|-----------------|-----------------|----------------|--------------------------|--------------------------|-----------------------|-----------------------|
|                                        | Min (V)  | Max (V)         | Min (V)         | Max (V)        |                          |                          |                       |                       |
| LVCMOS33/<br>LVTTL33                   | -0.3     | 0.8             | 2.0             | $V_{CCIO}+0.2$ | 0.40                     | $V_{CCIO} - 0.4$         | 8                     | -8                    |
|                                        |          |                 |                 |                | 0.20                     | $V_{CCIO} - 0.2$         | 0.1                   | -0.1                  |
| LVCMOS25                               | -0.3     | 0.7             | 1.7             | $V_{CCIO}+0.2$ | 0.40                     | $V_{CCIO} - 0.4$         | 6                     | -6                    |
|                                        |          |                 |                 |                | 0.20                     | $V_{CCIO} - 0.2$         | 0.1                   | -0.1                  |
| LVCMOS18                               | -0.3     | $0.35 V_{CCIO}$ | $0.67 V_{CCIO}$ | $V_{CCIO}+0.2$ | 0.40                     | $V_{CCIO} - 0.4$         | 4                     | -4                    |
|                                        |          |                 |                 |                | 0.20                     | $V_{CCIO} - 0.2$         | 0.1                   | -0.1                  |
| LVCMOS12 <sup>2</sup><br>(Output only) | —        | —               | —               | —              | 0.40                     | $V_{CCIO} - 0.4$         | 2                     | -2                    |
|                                        |          |                 |                 |                | 0.20                     | $V_{CCIO} - 0.2$         | 0.1                   | -0.1                  |

**Notes:**

- $V_{CCIO}$  in the table follows the  $V_{CCIO}$  power rail setting of the respective bank.
- For  $V_{CCIO1}$  and  $V_{CCIO2}$  only.

## 4.12. sysI/O Differential Electrical Characteristics

### 4.12.1. LVDS/subLVDS/SLVS200

Over recommended operating conditions.

Table 4.10. LVDS/subLVDS1/SLVS200<sup>1, 2</sup>

| Parameter          | Description                                  | Test Conditions                                     | Min   | Typ   | Max   | Unit    |
|--------------------|----------------------------------------------|-----------------------------------------------------|-------|-------|-------|---------|
| $V_{INP}, V_{INN}$ | Input Voltage                                | —                                                   | 0.00  | —     | 2.40  | V       |
| $V_{CM}$           | Input Common Mode Voltage                    | Half the sum of the two inputs                      | 0.05  | —     | 2.35  | V       |
| $V_{THD(LVDS)}$    | Differential Input Threshold                 | $ V_{INP} - V_{INN} $                               | 100   | —     | —     | mV      |
| $V_{THD(subLVDS)}$ | Differential Input Threshold                 | $ V_{INP} - V_{INN} $                               | 90    | —     | —     | mV      |
| $V_{THD(SLVS200)}$ | Differential Input Threshold                 | $ V_{INP} - V_{INN} $                               | 70    | —     | —     | mV      |
| $I_{IN}$           | Input Current                                | Normal Mode                                         | -10   | —     | 10    | $\mu A$ |
|                    |                                              | Standby Mode                                        | -10   | —     | 10    | $\mu A$ |
| $V_{OH}$           | Output High Voltage for $V_{OP}$ or $V_{OM}$ | $RT = 100 \Omega$                                   | —     | 1.43  | 1.60  | V       |
| $V_{OL}$           | Output Low Voltage for $V_{OP}$ or $V_{OM}$  | $RT = 100 \Omega$                                   | 0.90  | 1.08  | —     | V       |
| $V_{OD}$           | Output Voltage Differential                  | $ V_{OP} - V_{OM} , RT = 100 \Omega$                | 250   | 350   | 450   | mV      |
| $\Delta V_{OD}$    | Change in $V_{OD}$ between High and Low      | —                                                   | —     | —     | 50    | mV      |
| $V_{OS}$           | Output Voltage Offset (Common Mode Voltage)  | $(V_{OP} + V_{OM})/2, RT = 100 \Omega$              | 1.125 | 1.250 | 1.375 | V       |
| $\Delta V_{OS}$    | Change in $V_{OS}$ between H and L           | —                                                   | —     | —     | 50    | mV      |
| $I_{SAB}$          | Output Short Circuit Current                 | $V_{OD} = 0 V$ driver outputs shorted to each other | —     | —     | 12    | mA      |

**Notes:**

- Inputs only for subLVDS and SLVS200.
- For SLVS200/MIPI interface I/O placement, see the [Programmable I/O Banks](#) section.

#### 4.12.2. Hardened MIPI D-PHY I/Os

Over recommended operating conditions.

**Table 4.11. MIPI D-PHY**

| Symbol               | Description                                      | Min | Typ | Max  | Unit |
|----------------------|--------------------------------------------------|-----|-----|------|------|
| <b>Receiver</b>      |                                                  |     |     |      |      |
| <b>High Speed</b>    |                                                  |     |     |      |      |
| V <sub>CMRX</sub>    | Common-Mode Voltage HS Receive Mode              | 70  | —   | 330  | mV   |
| V <sub>IDTH</sub>    | Differential Input High Threshold                | —   | —   | 70   | mV   |
| V <sub>IDTL</sub>    | Differential Input Low Threshold                 | –70 | —   | —    | mV   |
| V <sub>IHHS</sub>    | Single-ended input High Voltage                  | —   | —   | 460  | mV   |
| V <sub>ILHS</sub>    | Single-ended Input Low Voltage                   | –40 | —   | —    | mV   |
| V <sub>TERM-EN</sub> | Single-ended Threshold for HS Termination Enable | —   | —   | 450  | mV   |
| Z <sub>ID</sub>      | Differential Input Impedance                     | 80  | 100 | 125  | Ω    |
| <b>Low Power</b>     |                                                  |     |     |      |      |
| V <sub>IH</sub>      | Logic 1 Input Voltage                            | 880 | —   | —    | mV   |
| V <sub>IL</sub>      | Logic 0 Input Voltage, not in ULP State          | —   | —   | 550  | mV   |
| V <sub>IL-ULPS</sub> | Logic 0 Input Voltage, in ULP State              | —   | —   | 300  | mV   |
| V <sub>HYST</sub>    | Input Hysteresis                                 | 25  | —   | —    | mV   |
| <b>Transmitter</b>   |                                                  |     |     |      |      |
| <b>High Speed</b>    |                                                  |     |     |      |      |
| V <sub>CMTX</sub>    | HS Transmit Static Common Mode Voltage           | 150 | 200 | 250  | mV   |
| V <sub>OD</sub>      | HS Transmit Differential Voltage                 | 140 | 200 | 270  | mV   |
| V <sub>OHHS</sub>    | HS Single-ended Output High Voltage              | —   | —   | 360  | mV   |
| Z <sub>OS</sub>      | Single-ended Output Impedance                    | 40  | 50  | 62.5 | Ω    |
| ΔZ <sub>OS</sub>     | Single-ended Output Impedance Mismatch           | —   | —   | 10   | %    |
| <b>Low Power</b>     |                                                  |     |     |      |      |
| V <sub>OH</sub>      | Output High Voltage                              | 1.1 | 1.2 | 1.3  | V    |
| V <sub>OL</sub>      | Output Low Voltage                               | –50 | —   | 50   | mV   |
| Z <sub>OLP</sub>     | Output Impedance in LP Mode                      | 110 | —   | —    | Ω    |

## 4.13. CrossLink Maximum General Purpose I/O Buffer Speed

Over recommended operating conditions.

**Table 4.12. CrossLink Maximum I/O Buffer Speed**

| Buffer                          | Description                                                                          | Max | Unit |
|---------------------------------|--------------------------------------------------------------------------------------|-----|------|
| <b>Maximum Input Frequency</b>  |                                                                                      |     |      |
| LVDS25                          | LVDS, $V_{CCIO} = 2.5\text{ V}$ , csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages    | 600 | MHz  |
|                                 | LVDS, $V_{CCIO} = 2.5\text{ V}$ , WLCSP36 package                                    | 500 | MHz  |
| subLVDS                         | subLVDS, $V_{CCIO} = 2.5\text{ V}$ , csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages | 600 | MHz  |
|                                 | subLVDS, $V_{CCIO} = 2.5\text{ V}$ , WLCSP36 package                                 | 500 | MHz  |
| MIPI D-PHY (HS) <sup>6, 7</sup> | MIPI D-PHY, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages                          | 600 | MHz  |
|                                 | MIPI D-PHY, WLCSP36 package                                                          | 500 | MHz  |
| MIPI D-PHY (LP) <sup>7</sup>    | MIPI D-PHY, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages                          | 5   | MHz  |
|                                 | MIPI D-PHY, WLCSP36 package                                                          | 5   | MHz  |
| SLVS200 <sup>7</sup>            | SLVS200, $V_{CCIO} = 2.5\text{ V}$ , csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages | 600 | MHz  |
|                                 | SLVS200, $V_{CCIO} = 2.5\text{ V}$ , WLCSP36 package                                 | 500 | MHz  |
| LVCMS33/LVTTL33                 | LVCMS/LVTTL, $V_{CCIO} = 3.3\text{ V}$                                               | 300 | MHz  |
| LVCMS25D                        | Differential LVCMS, $V_{CCIO} = 2.5\text{ V}$                                        | 300 | MHz  |
| LVCMS25                         | LVCMS, $V_{CCIO} = 2.5\text{ V}$                                                     | 300 | MHz  |
| LVCMS18                         | LVCMS, $V_{CCIO} = 1.8\text{ V}$                                                     | 155 | MHz  |
| <b>Maximum Output Frequency</b> |                                                                                      |     |      |
| LVDS25                          | LVDS, $V_{CCIO} = 2.5\text{ V}$ , csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages    | 600 | MHz  |
|                                 | LVDS, $V_{CCIO} = 2.5\text{ V}$ , WLCSP36 package                                    | 500 | MHz  |
| LVCMS33/LVTTL33                 | LVCMS/LVTTL, $V_{CCIO} = 3.3\text{ V}$                                               | 300 | MHz  |
| LVTTL33D                        | Differential LVTTL, $V_{CCIO} = 3.3\text{ V}$                                        | 300 | MHz  |
| LVCMS33D                        | Differential LVCMS, $3.3\text{ V}$                                                   | 300 | MHz  |
| LVCMS25                         | LVCMS, $2.5\text{ V}$                                                                | 300 | MHz  |
| LVCMS25D                        | Differential LVCMS, $2.5\text{ V}$                                                   | 300 | MHz  |
| LVCMS18                         | LVCMS, $1.8\text{ V}$                                                                | 155 | MHz  |
| LVCMS12                         | LVCMS, $V_{CCIO/2} = 1.2\text{ V}$                                                   | 70  | MHz  |

### Notes:

- These maximum speeds are characterized but not tested on every device.
- Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
- LVCMS timing is measured with the load specified in [Table 4.22](#).
- Actual system operation may vary depending on user logic implementation.
- Maximum data rate equals two times the clock rate when utilizing DDR.
- This is the maximum MIPI D-PHY input rate on the programmable I/O banks 1 and 2. The hardened MIPI D-PHY input and output rates are described in [Hardened MIPI D-PHY Performance](#) section. For SLVS200/MIPI interface I/O placement, see the [Programmable I/O Banks](#) section.
- Implement the following guidelines for I/O placement when MIPI Rx inputs are present on the programmable I/O banks to ensure optimal performance:

|                                      | Bank 1           | Bank 2           |
|--------------------------------------|------------------|------------------|
| SLVS200/MIPI Rx on Bank 1            | No LVCMS Outputs | No LVCMS Outputs |
| SLVS200/MIPI Rx on Bank 2            | No LVCMS Outputs | No LVCMS Outputs |
| SLVS200/MIPI Rx on Bank 1 and Bank 2 | No LVCMS Outputs | No LVCMS Outputs |

- The Diamond Software PAR Design Strategy setting of LVCMOS12\_18\_ONLY (default) allows outputs as long as they are LVCMOS12 or LVCMOS18.
- The Diamond Software PAR Design Strategy setting of LVCMOS\_NOT\_PERMITTED will cause an error in PAR regarding IO placement if there are any outputs in Bank 1 or Bank 2 when a MIPI Receiver interface is present.

## 4.14. CrossLink External Switching Characteristics

Over recommended operating conditions.

**Table 4.13. CrossLink External Switching Characteristics<sup>3, 4</sup>**

| Parameter                                                                                                                                                                                                                | Description                                                  | Conditions                                                                         | -6     |     | Unit     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------------------------------------|--------|-----|----------|
|                                                                                                                                                                                                                          |                                                              |                                                                                    | Min    | Max |          |
| Clocks                                                                                                                                                                                                                   |                                                              |                                                                                    |        |     |          |
| Primary Clock                                                                                                                                                                                                            |                                                              |                                                                                    |        |     |          |
| f <sub>MAX_PRI</sub>                                                                                                                                                                                                     | Frequency for Primary Clock Tree                             | —                                                                                  | —      | 150 | MHz      |
| t <sub>W_PRI</sub>                                                                                                                                                                                                       | Clock Pulse Width for Primary Clock                          | —                                                                                  | 0.8    | —   | ns       |
| t <sub>SKEW_PRI</sub>                                                                                                                                                                                                    | Primary Clock Skew Within a Clock                            | —                                                                                  | —      | 450 | ps       |
| Edge Clock                                                                                                                                                                                                               |                                                              |                                                                                    |        |     |          |
| f <sub>MAX_EDGE</sub>                                                                                                                                                                                                    | Frequency for Edge Clock Tree                                | —                                                                                  | —      | 600 | MHz      |
| t <sub>W_EDGE</sub>                                                                                                                                                                                                      | Clock Pulse Width for Edge Clock                             | —                                                                                  | 0.783  | —   | ns       |
| t <sub>SKEW_EDGE</sub>                                                                                                                                                                                                   | Edge Clock Skew Within a Bank                                | —                                                                                  | —      | 120 | ps       |
| Generic DDR Interfaces <sup>1</sup>                                                                                                                                                                                      |                                                              |                                                                                    |        |     |          |
| Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Centered at General Purpose Pins (GDDR <sub>X</sub> 8_RX/TX.ECLK.Centered or GDDR <sub>X</sub> 4_RX/TX.ECLK.Centered or GDDR <sub>X</sub> 2_RX/TX.ECLK.Centered) |                                                              |                                                                                    |        |     |          |
| t <sub>SU_GDDR<sub>X</sub>2_4_8_CENTERED</sub>                                                                                                                                                                           | Input Data Set-Up Before CLK Rising and Falling edges        | —                                                                                  | 0.167  | —   | ns       |
| t <sub>HD_GDDR<sub>X</sub>2_4_8_CENTERED</sub>                                                                                                                                                                           | Input Data Hold After CLK Rising and Falling edges           | —                                                                                  | 0.167  | —   | ns       |
| t <sub>DVB_GDDR<sub>X</sub>2_4_8_CENTERED</sub>                                                                                                                                                                          | Output Data Valid Before CLK Output Rising and Falling edges | Data Rate = 1.2 Gb/s <sup>5</sup>                                                  | 0.297  | —   | ns       |
|                                                                                                                                                                                                                          |                                                              | Other Data Rates <sup>5</sup>                                                      | -0.120 | —   | ns+1/2UI |
| t <sub>DVA_GDDR<sub>X</sub>2_4_8_CENTERED</sub>                                                                                                                                                                          | Output Data Valid After CLK Output Rising and Falling edges  | Data Rate = 1.2 Gb/s <sup>5</sup>                                                  | 0.297  | —   | ns       |
|                                                                                                                                                                                                                          |                                                              | Other Data Rates <sup>5</sup>                                                      | -0.120 | —   | ns+1/2UI |
| f <sub>MAX_GDDR<sub>X</sub>2_4_8_CENTERED</sub>                                                                                                                                                                          | Frequency for ECLK <sup>2</sup>                              | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 GDDR <sub>X</sub> 2                         | —      | 300 | MHz      |
|                                                                                                                                                                                                                          |                                                              | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 GDDR <sub>X</sub> 4 and GDDR <sub>X</sub> 8 | —      | 600 | MHz      |
|                                                                                                                                                                                                                          |                                                              | WLCSP36 GDDR <sub>X</sub> 2                                                        | —      | 250 | MHz      |

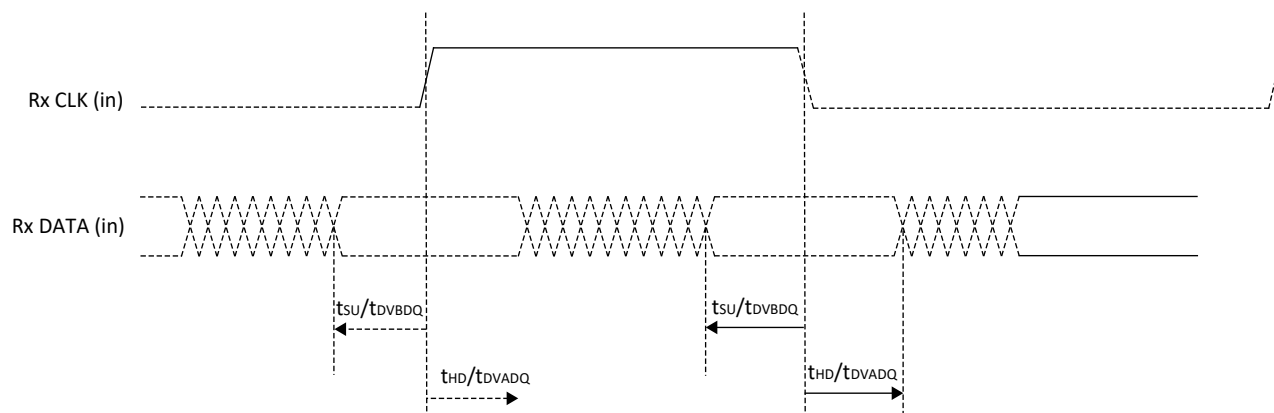
| Parameter                                                                                                                                                                      | Description                                                    | Conditions                                                | −6     |        | Unit     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------|--------|--------|----------|
|                                                                                                                                                                                |                                                                |                                                           | Min    | Max    |          |
| Generic DDR Interfaces <sup>1</sup>                                                                                                                                            |                                                                |                                                           |        |        |          |
| Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Centered at General Purpose Pins (GDDR8_RX/TX.ECLK.Centered or GDDR4_RX/TX.ECLK.Centered or GDDR2_RX/TX.ECLK.Centered) |                                                                |                                                           |        |        |          |
| —                                                                                                                                                                              | —                                                              | WLCSP36<br>GDDR4 and GDDR8                                | —      | 500    | MHz      |
| Generic DDRX1 I/O with Clock and Data Centered at General Purpose Pins (GDDR1_RX/TX.SCLK.Centered)                                                                             |                                                                |                                                           |        |        |          |
| t <sub>SU_GDDR1_CENTERED</sub>                                                                                                                                                 | Input Data Set-Up Before CLK Rising and Falling edges          | —                                                         | 0.917  | —      | ns       |
| t <sub>HD_GDDR1_CENTERED</sub>                                                                                                                                                 | Input Data Hold After CLK Rising and Falling edges             | —                                                         | 0.917  | —      | ns       |
| —                                                                                                                                                                              | —                                                              | Data Rate = 300 Mb/s                                      | 1.217  | —      | ns       |
|                                                                                                                                                                                |                                                                | Other Data Rates                                          | −0.450 | —      | ns+1/2UI |
| —                                                                                                                                                                              | —                                                              | Data Rate = 300 Mb/s                                      | 1.217  | —      | ns       |
|                                                                                                                                                                                |                                                                | Other Data Rates                                          | −0.450 | —      | ns+1/2UI |
| f <sub>MAX_GDDR1_CENTERED</sub>                                                                                                                                                | Frequency for PCLK <sup>2</sup>                                | —                                                         | —      | 150    | MHz      |
| Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Aligned at General Purpose Pins (GDDR8_RX/TX.ECLK.Aligned or GDDR4_RX/TX.ECLK.Aligned or GDDR2_RX/TX.ECLK.Aligned)     |                                                                |                                                           |        |        |          |
| t <sub>SU_GDDR2_4_8_ALIGNED</sub>                                                                                                                                              | Input Data Valid After CLK Rising and Falling edges            | Data Rate = 1.2 Gb/s <sup>5</sup>                         | —      | 0.188  | ns       |
|                                                                                                                                                                                |                                                                | Other Data Rates <sup>5</sup>                             | —      | −0.229 | ns+1/2UI |
| t <sub>HD_GDDR2_4_8_ALIGNED</sub>                                                                                                                                              | Input Data Hold After CLK Rising and Falling edges             | Data Rate = 1.2 Gb/s <sup>5</sup>                         | 0.646  | —      | ns       |
|                                                                                                                                                                                |                                                                | Other Data Rates <sup>5</sup>                             | 0.229  | —      | ns+1/2UI |
| t <sub>DIA_GDDR2_4_8_ALIGNED</sub>                                                                                                                                             | Output Data Invalid After CLK Rising and Falling edges Output  | —                                                         | —      | 0.120  | ns       |
| t <sub>DIB_GDDR2_4_8_ALIGNED</sub>                                                                                                                                             | Output Data Invalid Before CLK Output Rising and Falling edges | —                                                         | —      | 0.120  | ns       |
| f <sub>MAX_GDDR2_4_8_ALIGNED</sub>                                                                                                                                             | Frequency for ECLK <sup>2</sup>                                | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64<br>GDDR2           | —      | 300    | MHz      |
|                                                                                                                                                                                |                                                                | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64<br>GDDR4 and GDDR8 | —      | 600    | MHz      |
|                                                                                                                                                                                |                                                                | WLCSP36 GDDR2                                             | —      | 250    | MHz      |
|                                                                                                                                                                                |                                                                | WLCSP36 GDDR4 and GDDR8                                   | —      | 500    | MHz      |

| Parameter                                                                                         | Description                                                    | Conditions                                                                                       | -6    |        | Unit     |
|---------------------------------------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-------|--------|----------|
|                                                                                                   |                                                                |                                                                                                  | Min   | Max    |          |
| Generic DDR Interfaces <sup>2</sup>                                                               |                                                                |                                                                                                  |       |        |          |
| Generic DDRX1 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX1_RX/TX.SCLK.Aligned) |                                                                |                                                                                                  |       |        |          |
| t <sub>SU_GDDR1_ALIGNED</sub>                                                                     | Input Data Valid After CLK Rising and Falling edges            | Data Rate = 300 Mb/s                                                                             | —     | 0.750  | ns       |
|                                                                                                   |                                                                | Other Data Rates                                                                                 | —     | -0.917 | ns+1/2UI |
| t <sub>HD_GDDR1_ALIGNED</sub>                                                                     | Input Data Hold After CLK Rising and Falling edges             | Data Rate = 300 Mb/s                                                                             | 2.583 | —      | ns       |
|                                                                                                   |                                                                | Other Data Rates                                                                                 | 0.916 | —      | ns+1/2UI |
| t <sub>DIA_GDDR1_ALIGNED</sub>                                                                    | Output Data Invalid After CLK Rising and Falling edges Output  | —                                                                                                | —     | 0.450  | ns       |
| t <sub>DIB_GDDR1_ALIGNED</sub>                                                                    | Output Data Invalid Before CLK Output Rising and Falling edges | —                                                                                                | —     | 0.450  | ns       |
| f <sub>MAX_GDDR1_ALIGNED</sub>                                                                    | Frequency for ECLK <sup>2</sup>                                | —                                                                                                | —     | 150    | MHz      |
| General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing                                        |                                                                |                                                                                                  |       |        |          |
| t <sub>SU_GDDR1_MP</sub>                                                                          | Input Data Set-Up Before CLK                                   | 842 Mb/s < Data Rate ≤ 1.2 Gb/s and<br>V <sub>IDTH</sub> = 140 mV<br>V <sub>IDTL</sub> = -140 mV | 0.200 | —      | UI       |
|                                                                                                   |                                                                | 473 Mb/s < Data Rate ≤ 842 Mb/s and<br>V <sub>IDTH</sub> = 140 mV<br>V <sub>IDTL</sub> = -140 mV | 0.150 | —      | UI       |
|                                                                                                   |                                                                | Data Rate ≤ 473 Mb/s and<br>V <sub>IDTH</sub> = 70 mV<br>V <sub>IDTL</sub> = -70 mV              | 0.150 | —      | UI       |
| t <sub>HD_GDDR1_MP</sub>                                                                          | Input Data Hold After CLK                                      | 842 Mb/s < Data Rate ≤ 1.2 Gb/s and<br>V <sub>IDTH</sub> = 140 mV<br>V <sub>IDTL</sub> = -140 mV | 0.200 | —      | UI       |
|                                                                                                   |                                                                | 473 Mb/s < Data Rate ≤ 842 Mb/s &<br>V <sub>IDTH</sub> = 140 mV<br>V <sub>IDTL</sub> = -140 mV   | 0.150 | —      | UI       |
|                                                                                                   |                                                                | Data Rate ≤ 473 Mb/s and<br>V <sub>IDTH</sub> = 70 mV<br>V <sub>IDTL</sub> = -70 mV              | 0.150 | —      | UI       |
| f <sub>MAX_GDDR1_MP</sub>                                                                         | Frequency for ECLK <sup>2</sup>                                | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64                                                           | —     | 600    | MHz      |
|                                                                                                   |                                                                | WLCSP36                                                                                          | —     | 500    | MHz      |

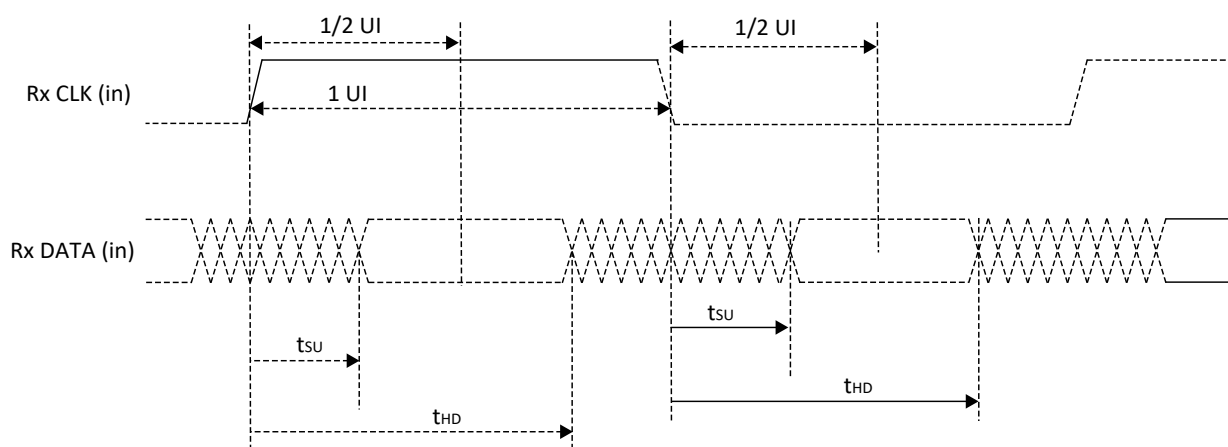
| Parameter                                                                    | Description                                                                                  | Conditions                                      | -6     |        | Unit            |
|------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|-------------------------------------------------|--------|--------|-----------------|
|                                                                              |                                                                                              |                                                 | Min    | Max    |                 |
| Generic DDRX71 or DDRX141 Inputs (GDDR71_RX.ECLK or GDDRX141_RX.ECLK)        |                                                                                              |                                                 |        |        |                 |
| t <sub>RPBi_DVA</sub>                                                        | Input Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)         | —                                               | —      | 0.3    | UI              |
|                                                                              |                                                                                              | —                                               | —      | -0.222 | ns+ (i+ 1/2)*UI |
| t <sub>RPBi_DVE</sub>                                                        | Input Hold Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)          | —                                               | 0.7    | —      | UI              |
|                                                                              |                                                                                              | —                                               | 0.222  | —      | ns+ (i+ 1/2)*UI |
| f <sub>MAX_RX71_141</sub>                                                    | DDR71/DDR141 ECLK Frequency <sup>2</sup>                                                     | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64, WLCSP36 | —      | 450    | MHz             |
| Generic DDR Interfaces <sup>1</sup>                                          |                                                                                              |                                                 |        |        |                 |
| Generic DDRX71 Outputs with Clock and Data Aligned at Pin (GDDR71_TX.ECLK)   |                                                                                              |                                                 |        |        |                 |
| t <sub>TPBi_DOV</sub>                                                        | Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)   | —                                               | —      | 0.143  | ns+i*UI         |
| t <sub>TPBi_DOI</sub>                                                        | Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK) | —                                               | -0.143 | —      | ns+i*UI         |
| t <sub>TPBi_skew_UI</sub>                                                    | Tx skew in UI                                                                                | —                                               | —      | 0.15   | UI              |
| f <sub>MAX_TX71</sub>                                                        | DDR71 ECLK Frequency <sup>2</sup>                                                            | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64          | —      | 525    | MHz             |
|                                                                              |                                                                                              | WLCSP36                                         | —      | 500    | MHz             |
| Generic DDRX141 Outputs with Clock and Data Aligned at Pin (GDDR141_TX.ECLK) |                                                                                              |                                                 |        |        |                 |
| t <sub>TPBi_DOV</sub>                                                        | Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)   | All Devices                                     | —      | 0.125  | ns+i*UI         |
| t <sub>TPBi_DOI</sub>                                                        | Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK) | All Devices                                     | -0.125 | —      | ns+i*UI         |
| t <sub>TPBi_skew_UI</sub>                                                    | TX skew in UI                                                                                | All Devices                                     | —      | 0.15   | UI              |
| f <sub>MAX_TX141</sub>                                                       | DDR141 ECLK Frequency <sup>2</sup>                                                           | csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64          | —      | 600    | MHz             |
|                                                                              |                                                                                              | WLCSP36                                         | —      | 500    | MHz             |

**Notes:**

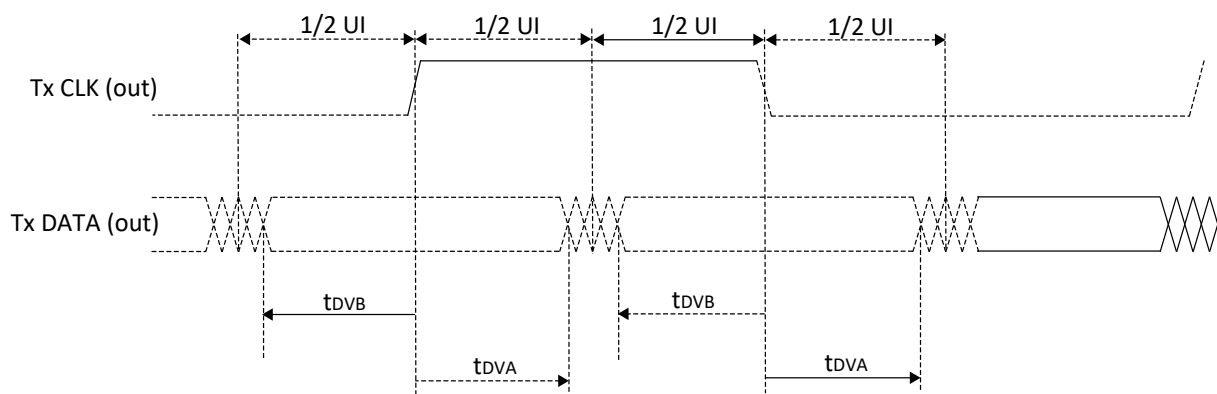
- Generic DDRX8, DDRX71 and DDRX141 timing numbers based on LVDS I/O.
- Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- These numbers are generated using best case PLL location.
- All numbers are generated with the Lattice Diamond design software.
- Maximum data rate for GDDR2 mode is 500 Mbps for WLCSP36 package and 600 Mbps for all other packages.



**Figure 4.1. Receiver RX.CLK.Centered Waveforms**



**Figure 4.2. Receiver RX.CLK.Aligned Input Waveforms**



**Figure 4.3. Transmit TX.CLK.Centered Output Waveforms**

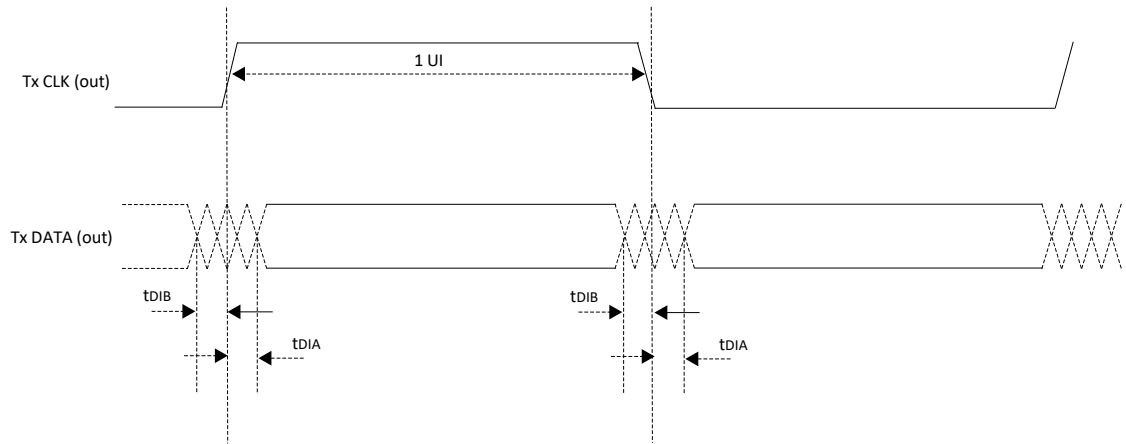


Figure 4.4. Transmit TX.CLK.Aligned Waveforms

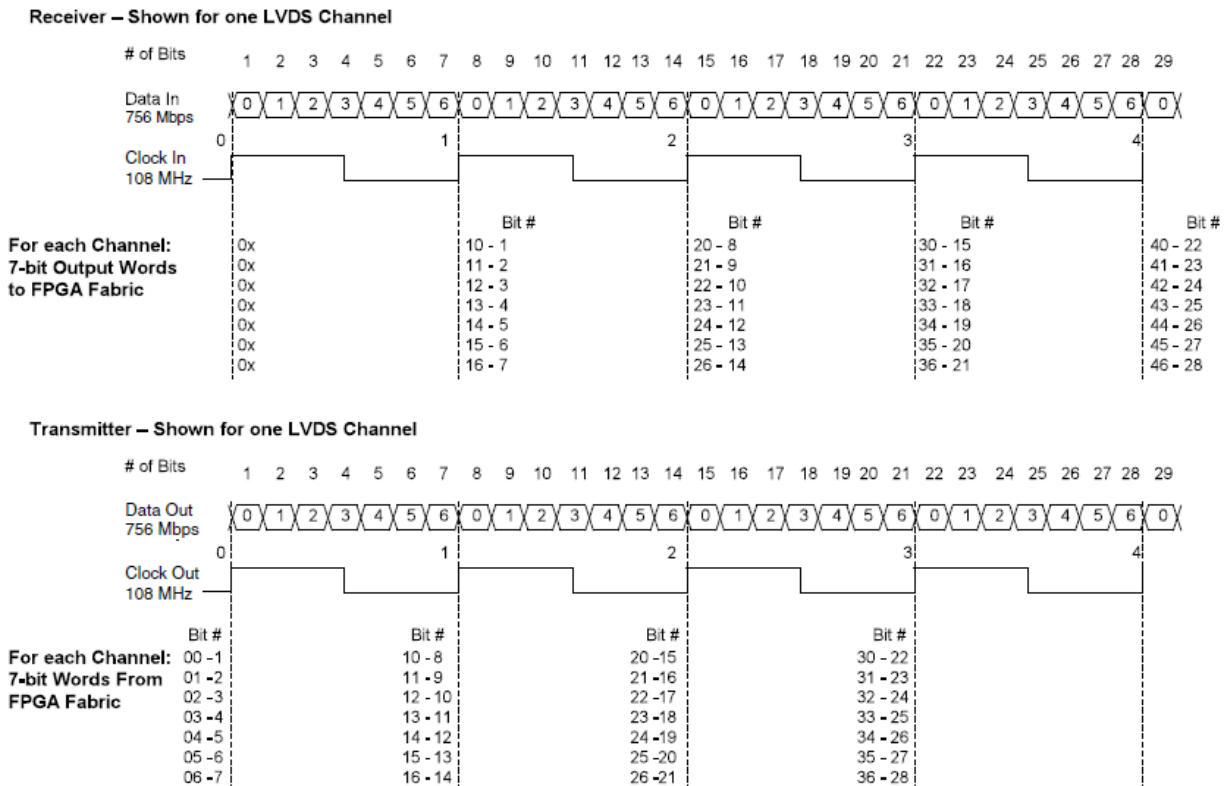


Figure 4.5. DDRX71, DDRX141 Video Timing Waveforms

## 4.15. sysCLOCK PLL Timing

Over recommended operating conditions.

**Table 4.14. sysCLOCK PLL Timing**

| Parameter                 | Descriptions                                    | Conditions              | Min    | Max   | Unit   |
|---------------------------|-------------------------------------------------|-------------------------|--------|-------|--------|
| $f_{IN}$                  | Input Clock Frequency (CLKI, CLKFB)             | —                       | 10     | 400   | MHz    |
| $f_{PD}$                  | Phase Detector Input Clock Frequency            | —                       | 10     | 400   | MHz    |
| $f_{OUT}$                 | Output Clock Frequency (CLKOP, CLKOS)           | —                       | 4.6875 | 600   | MHz    |
| $f_{VCO}$                 | PLL VCO Frequency                               | —                       | 600    | 1200  | MHz    |
| <b>AC Characteristics</b> |                                                 |                         |        |       |        |
| $t_{DT}$                  | Output Clock Duty Cycle                         | —                       | 45     | 55    | %      |
| $t_{PH}$                  | Output Phase Accuracy                           | —                       | –5     | 5     | %      |
| $t_{OPIJT}^1$             | Output Clock Period Jitter <sup>3</sup>         | $f_{OUT} \geq 100$ MHz  | —      | 100   | ps p-p |
|                           |                                                 | $f_{OUT} < 100$ MHz     | —      | 0.025 | UIPP   |
|                           | Output Clock Cycle-to-Cycle Jitter <sup>3</sup> | $f_{OUT} \geq 100$ MHz  | —      | 200   | ps p-p |
|                           |                                                 | $f_{OUT} < 100$ MHz     | —      | 0.05  | UIPP   |
|                           | Output Clock Phase Jitter                       | $f_{PD} > 100$ MHz      | —      | 200   | ps p-p |
|                           |                                                 | $f_{PD} < 100$ MHz      | —      | 0.05  | UIPP   |
| $t_{SPO}$                 | Static Phase Offset                             | Divider ratio = integer | —      | 400   | ps p-p |
| $t_{LOCK}^2$              | PLL Lock-in Time                                | —                       | —      | 15    | ms     |
| $t_{UNLOCK}$              | PLL Unlock Time                                 | —                       | —      | 50    | ns     |
| $t_{IPJIT}$               | Input Clock Period Jitter                       | $f_{PD} \geq 20$ MHz    | —      | 500   | ps p-p |
|                           |                                                 | $f_{PD} < 20$ MHz       | —      | 0.02  | UIPP   |
| $t_{HI}$                  | Input Clock High Time                           | 90% to 90%              | 0.5    | —     | ns     |
| $t_{LO}$                  | Input Clock Low Time                            | 10% to 10%              | 0.5    | —     | ns     |

**Notes:**

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PD} \geq 10$  MHz. For  $f_{PD} < 10$  MHz, the jitter numbers may not be met in certain conditions.

## 4.16. Hardened MIPI D-PHY Performance

Over recommended operating conditions.

**Table 4.15. 1500 Mb/s MIPI\_DPHY\_X8\_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)\***

| Parameter         | Description                         | Min   | Max | Unit |
|-------------------|-------------------------------------|-------|-----|------|
| $t_{SU\_MIPIX8}$  | Input Data Setup before CLK         | 0.227 | —   | UI   |
| $t_{HD\_MIPIX8}$  | Input Data Hold after CLK           | 0.305 | —   | UI   |
| $t_{DVB\_MIPIX8}$ | Output Data Valid before CLK Output | 0.200 | —   | UI   |
| $t_{DVA\_MIPIX8}$ | Output Data Valid after CLK Output  | 0.200 | —   | UI   |

\*Note: For WLCSP36 package, the MIPI D-PHY  $f_{max}$  is 1200 Mb/s, for other packages,  $f_{max}$  is 1500 Mb/s.

**Table 4.16. 1200 Mb/s MIPI\_DPHY\_X4\_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)**

| Parameter         | Description                         | Min   | Max | Unit |
|-------------------|-------------------------------------|-------|-----|------|
| $t_{SU\_MIPIX4}$  | Input Data Setup before CLK         | 0.200 | —   | UI   |
| $t_{HD\_MIPIX4}$  | Input Data Hold after CLK           | 0.200 | —   | UI   |
| $t_{DVB\_MIPIX4}$ | Output Data Valid before CLK Output | 0.200 | —   | UI   |
| $t_{DVA\_MIPIX4}$ | Output Data Valid after CLK Output  | 0.200 | —   | UI   |

**Table 4.17. 1000 Mb/s MIPI\_DPHY\_X4\_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)**

| Parameter         | Description                         | Min   | Max | Unit |
|-------------------|-------------------------------------|-------|-----|------|
| $t_{SU\_MIPIX4}$  | Input Data Setup before CLK         | 0.150 | —   | UI   |
| $t_{HD\_MIPIX4}$  | Input Data Hold after CLK           | 0.150 | —   | UI   |
| $t_{DVB\_MIPIX4}$ | Output Data Valid before CLK Output | 0.150 | —   | UI   |
| $t_{DVA\_MIPIX4}$ | Output Data Valid after CLK Output  | 0.150 | —   | UI   |

## 4.17. Internal Oscillators (HFOSC, LFOSC)

Over recommended operating conditions.

**Table 4.18. Internal Oscillators**

| Parameter     | Parameter Description                | Min  | Typ | Max  | Unit |
|---------------|--------------------------------------|------|-----|------|------|
| $f_{CLKHF}$   | HFOSC CLKK Clock Frequency           | 43.2 | 48  | 52.8 | MHz  |
| $f_{CLKLF}$   | LFOSC CLKK Clock Frequency           | 9    | 10  | 11   | kHz  |
| $DCH_{CLKHF}$ | HFOSC Duty Cycle (Clock High Period) | 45   | 50  | 55   | %    |
| $DCH_{CLKLF}$ | LFOSC Duty Cycle (Clock High Period) | 45   | 50  | 55   | %    |

## 4.18. User I<sup>2</sup>C

Over recommended operating conditions.

**Table 4.19. User I<sup>2</sup>C<sup>1</sup>**

| Symbol             | Parameter                          | STD Mode |     |     | FAST Mode |     |     | FAST Mode Plus <sup>2</sup> |     |                   | Units |
|--------------------|------------------------------------|----------|-----|-----|-----------|-----|-----|-----------------------------|-----|-------------------|-------|
|                    |                                    | Min      | Typ | Max | Min       | Typ | Max | Min                         | Typ | Max               |       |
| f <sub>SCL</sub>   | SCL Clock Frequency                | —        | —   | 100 | —         | —   | 400 | —                           | —   | 1000 <sup>2</sup> | kHz   |
| T <sub>DELAY</sub> | Optional delay through delay block | —        | 62  | —   | —         | 62  | —   | —                           | 62  | —                 | ns    |

**Notes:**

1. Refer to the I<sup>2</sup>C Specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I<sup>2</sup>C bus. Internal pull up may not be sufficient to support the maximum speed.

## 4.19. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

**Table 4.20. CrossLink sysCONFIG Port Timing Specifications**

| Symbol                            | Parameter                                                                                            | Min | Max  | Unit |
|-----------------------------------|------------------------------------------------------------------------------------------------------|-----|------|------|
| <b>All Configuration Mode</b>     |                                                                                                      |     |      |      |
| t <sub>PRGM</sub> <sup>3</sup>    | Minimum CRESETB LOW pulse width required to restart configuration (from falling edge to rising edge) | 290 | —    | ns   |
| <b>Slave SPI<sup>1</sup></b>      |                                                                                                      |     |      |      |
| f <sub>CCLK</sub>                 | SPI_SCK Input Clock Frequency                                                                        | —   | 110  | MHz  |
| t <sub>STSU</sub>                 | MOSI Setup Time                                                                                      | 0.5 | —    | ns   |
| t <sub>STH</sub>                  | MOSI Hold Time                                                                                       | 2.0 | —    | ns   |
| t <sub>STCO</sub>                 | SPI_SCK Falling Edge to Valid MISO Output                                                            | —   | 13.3 | ns   |
| t <sub>SCS</sub>                  | Chip Select HIGH Time                                                                                | 25  | —    | ns   |
| t <sub>SCSS</sub>                 | Chip Select Setup Time                                                                               | 0.5 | —    | ns   |
| t <sub>SCSH</sub>                 | Chip Select Hold Time                                                                                | 0.5 | —    | ns   |
| <b>Master SPI</b>                 |                                                                                                      |     |      |      |
| f <sub>CCLK</sub>                 | MCK Output Clock Frequency                                                                           | —   | 52.8 | MHz  |
| <b>I<sup>2</sup>C<sup>2</sup></b> |                                                                                                      |     |      |      |
| f <sub>MAX</sub>                  | Maximum SCL Clock Frequency (Fast-Mode Plus)                                                         | —   | 1    | MHz  |

**Notes:**

1. Refer to [CrossLink Programming and Configuration Usage Guide \(FPGA-TN-02014\)](#), for timing requirements to enable CrossLink SSPI Mode.
2. Refer to the I<sup>2</sup>C specification for timing requirements when configuring with I<sup>2</sup>C port.
3. t<sub>PRGM</sub> minimum time does not apply when SLAVE\_SPI\_PORT, MASTER\_SPI\_PORT and I2C\_PORT are disabled through Diamond Software. Contact your Lattice Sales Representatives for details.

## 4.20. SRAM Configuration Time from NVCM

Over recommended operating conditions.

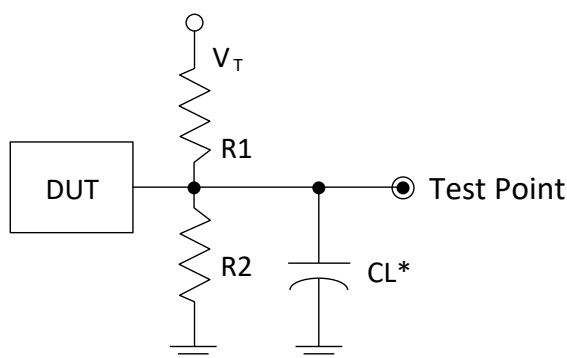
**Table 4.21. SRAM Configuration Time from NVCM**

| Symbol                     | Parameter                          | Typ | Unit |
|----------------------------|------------------------------------|-----|------|
| T <sub>CONFIGURATION</sub> | POR/CRESET_B to Device I/O Active* | 83  | ms   |

**\*Note:** Before and during configuration, the I/O are held in tristate with weak internal pullups enabled. I/O are released to user functionality when the device has finished configuration.

## 4.21. Switching Test Conditions

Figure 4.6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.22.



\*CL Includes Test Fixture and Probe Capacitance

**Figure 4.6. Output Test Load, LVTTTL and LVCMOS Standards**

**Table 4.22. Test Fixture Required Components, Non-Terminated Interfaces\***

| Test Condition                                  | R <sub>1</sub> | R <sub>2</sub> | C <sub>L</sub> | Timing Ref.                       | V <sub>T</sub>    |
|-------------------------------------------------|----------------|----------------|----------------|-----------------------------------|-------------------|
| LVTTTL and other LVCMOS settings (L ≥ H, H ≥ L) | ∞              | ∞              | 0 pF           | LVCMOS 3.3 = 1.5 V                | —                 |
|                                                 |                |                |                | LVCMOS 2.5 = V <sub>CCIO</sub> /2 | —                 |
|                                                 |                |                |                | LVCMOS 1.8 = V <sub>CCIO</sub> /2 | —                 |
|                                                 |                |                |                | LVCMOS 1.2 = V <sub>CCIO</sub> /2 | —                 |
| LVCMOS 2.5 I/O (Z ≥ H)                          | ∞              | 1 MΩ           | 0 pF           | V <sub>CCIO</sub> /2              | —                 |
| LVCMOS 2.5 I/O (Z ≥ L)                          | 1 MΩ           | ∞              | 0 pF           | V <sub>CCIO</sub> /2              | V <sub>CCIO</sub> |
| LVCMOS 2.5 I/O (H ≥ Z)                          | ∞              | 100            | 0 pF           | V <sub>OH</sub> - 0.10            | —                 |
| LVCMOS 2.5 I/O (L ≥ Z)                          | 100            | ∞              | 0 pF           | V <sub>OL</sub> + 0.10            | V <sub>CCIO</sub> |

**\*Note:** Output test conditions for all other interfaces are determined by the respective standards.

## 5. Pinout Information

The pinout tables below correspond to CrossLink LIF-MD6000 Pinout Version 1.4.

GND pins are referenced as V<sub>SS</sub> in Lattice Diamond Software.

### 5.1. WLCSP36 Pinout

Table 5.1. WLCSP36 Pinout

| Pin Number | Pin Function | Bank   | Dual Function     | Differential      |
|------------|--------------|--------|-------------------|-------------------|
| A1         | GNDMU_DPHY1  | GND    | —                 | —                 |
| A2         | VCCMU_DPHY1  | DPHY1  | —                 | —                 |
| A3         | DPHY1_DP2    | DPHY1  | —                 | True_OF_DPHY1_DN2 |
| A4         | DPHY1_DN2    | DPHY1  | —                 | Comp_OF_DPHY1_DP2 |
| A5         | VCCAUX       | VCCAUX | —                 | —                 |
| A6         | PB2C         | 2      | MIPI_CLKT2_0      | True_OF_PB2D      |
| B1         | DPHY1_DP0    | DPHY1  | —                 | True_OF_DPHY1_DN0 |
| B2         | DPHY1_DP1    | DPHY1  | —                 | True_OF_DPHY1_DN1 |
| B3         | DPHY1_DP3    | DPHY1  | —                 | True_OF_DPHY1_DN3 |
| B4         | DPHY1_DN3    | DPHY1  | —                 | Comp_OF_DPHY1_DP3 |
| B5         | PB16D        | 2      | PCLKC2_1          | Comp_OF_PB16C     |
| B6         | PB2D         | 2      | MIPI_CLKC2_0      | Comp_OF_PB2C      |
| C1         | DPHY1_DN0    | DPHY1  | —                 | Comp_OF_DPHY1_DP0 |
| C2         | DPHY1_DN1    | DPHY1  | —                 | Comp_OF_DPHY1_DP1 |
| C3         | PB52         | 0      | SPI_SS/CSN/SCL    | —                 |
| C4         | VCC          | VCC    | —                 | —                 |
| C5         | PB16C        | 2      | PCLKT2_1          | True_OF_PB16D     |
| C6         | GND          | GND    | —                 | —                 |
| D1         | DPHY1_CKP    | DPHY1  | —                 | True_OF_DPHY1_CKN |
| D2         | PB48         | 0      | PCLKT0_1/USER_SCL | —                 |
| D3         | PB47         | 0      | PCLKT0_0/USER_SDA | —                 |
| D4         | CRESET_B     | 0      | —                 | —                 |
| D5         | PB16B        | 2      | PCLKC2_0          | Comp_OF_PB16A     |
| D6         | PB6B         | 2      | —                 | Comp_OF_PB6A      |
| E1         | DPHY1_CKN    | DPHY1  | —                 | Comp_OF_DPHY1_CKP |
| E2         | VCCIO0       | 0      | —                 | —                 |
| E3         | GND          | GND    | —                 | —                 |
| E4         | PB50         | 0      | MOSI              | —                 |
| E5         | PB16A        | 2      | PCLKT2_0          | True_OF_PB16B     |
| E6         | PB6A         | 2      | GR_PCLK2_0        | True_OF_PB6B      |
| F1         | PB51         | 0      | MISO              | —                 |
| F2         | PB49         | 0      | PMU_WKUPN/CDONE   | —                 |
| F3         | PB53         | 0      | SPI_SCK/MCK/SDA   | —                 |
| F4         | PB12A        | 2      | GPLLT2_0          | True_OF_PB12B     |
| F5         | PB12B        | 2      | GPLLC2_0          | Comp_OF_PB12A     |
| F6         | VCCIO2       | 2      | —                 | —                 |

## 5.2. ucfBGA64 Pinout

Table 5.2. ucfBGA64 Pinout

| Pin Number | Pin Function | Bank   | Dual Function     | Differential      |
|------------|--------------|--------|-------------------|-------------------|
| A1         | DPHY1_CKP    | DPHY1  | —                 | True_OF_DPHY1_CKN |
| A2         | DPHY1_CKN    | DPHY1  | —                 | Comp_OF_DPHY1_CKP |
| A3         | DPHY1_DP3    | DPHY1  | —                 | True_OF_DPHY1_DN3 |
| A4         | DPHY1_DN3    | DPHY1  | —                 | Comp_OF_DPHY1_DP3 |
| A5         | DPHY0_DN2    | DPHY0  | —                 | Comp_OF_DPHY0_DP2 |
| A6         | DPHY0_DP0    | DPHY0  | —                 | True_OF_DPHY0_DN0 |
| A7         | DPHY0_CKP    | DPHY0  | —                 | True_OF_DPHY0_CKN |
| A8         | DPHY0_CKN    | DPHY0  | —                 | Comp_OF_DPHY0_CKP |
| B1         | DPHY1_DP2    | DPHY1  | —                 | True_OF_DPHY1_DN2 |
| B2         | DPHY1_DN2    | DPHY1  | —                 | Comp_OF_DPHY1_DP2 |
| B3         | DPHY1_DP1    | DPHY1  | —                 | True_OF_DPHY1_DN1 |
| B4         | DPHY1_DN1    | DPHY1  | —                 | Comp_OF_DPHY1_DP1 |
| B5         | DPHY0_DP2    | DPHY0  | —                 | True_OF_DPHY0_DN2 |
| B6         | DPHY0_DN0    | DPHY0  | —                 | Comp_OF_DPHY0_DP0 |
| B7         | DPHY0_DP3    | DPHY0  | —                 | True_OF_DPHY0_DN3 |
| B8         | DPHY0_DN3    | DPHY0  | —                 | Comp_OF_DPHY0_DP3 |
| C1         | DPHY1_DP0    | DPHY1  | —                 | True_OF_DPHY1_DN0 |
| C2         | DPHY1_DN0    | DPHY1  | —                 | Comp_OF_DPHY1_DP0 |
| C3         | PB47         | 0      | PCLKT0_0/USER_SDA | —                 |
| C4         | VCCPLL_DPHYx | DPHY   | —                 | —                 |
| C5         | VCCA_DPHYx   | DPHY   | —                 | —                 |
| C6         | GND_A_DPHYx  | GND    | —                 | —                 |
| C7         | DPHY0_DP1    | DPHY0  | —                 | True_OF_DPHY0_DN1 |
| C8         | DPHY0_DN1    | DPHY0  | —                 | Comp_OF_DPHY0_DP1 |
| D1         | PB34B        | 1      | —                 | Comp_OF_PB34A     |
| D2         | PB34A        | 1      | GR_PCLK1_0        | True_OF_PB34B     |
| D3         | PB52         | 0      | SPI_SS/CSN/SCL    | —                 |
| D4         | GND          | GND    | —                 | —                 |
| D5         | VCC          | VCC    | —                 | —                 |
| D6         | VCCAUX       | VCCAUX | —                 | —                 |
| D7         | PB16A        | 2      | PCLKT2_0          | True_OF_PB16B     |
| D8         | PB12A        | 2      | GPLL2_0           | True_OF_PB12B     |
| E1         | PB51         | 0      | MISO              | —                 |
| E2         | CRESET_B     | 0      | —                 | —                 |
| E3         | PB48         | 0      | PCLKT0_1/USER_SCL | —                 |
| E4         | VCC          | VCC    | —                 | —                 |
| E5         | GND          | GND    | —                 | —                 |
| E6         | VCCIO2       | 2      | —                 | —                 |
| E7         | PB16B        | 2      | PCLKC2_0          | Comp_OF_PB16A     |
| E8         | PB12B        | 2      | GPLL2_0           | Comp_OF_PB12A     |
| F1         | PB53         | 0      | SPI_SCK/MCK/SDA   | —                 |
| F2         | PB50         | 0      | MOSI              | —                 |

**Table 5.2. ucfBGA64 Pinout (Continued)**

| Pin Number | Pin Function | Bank    | Dual Function   | Differential  |
|------------|--------------|---------|-----------------|---------------|
| F3         | VCCIO0       | 0       | —               | —             |
| F4         | VCCIO1       | 1       | —               | —             |
| F5         | GND          | GND     | —               | —             |
| F6         | VCCIO2       | 2       | —               | —             |
| F7         | PB6A         | 2       | GR_PCLK2_0      | True_OF_PB6B  |
| F8         | PB6B         | 2       | —               | Comp_OF_PB6A  |
| G1         | PB38D        | 1       | —               | Comp_OF_PB38C |
| G2         | PB38C        | 1       | —               | True_OF_PB38D |
| G3         | PB49         | 0       | PMU_WKUPN/CDONE | —             |
| G4         | VCCGPLL      | VCCGPLL | —               | —             |
| G5         | PB29B        | 1       | PCLKC1_0        | Comp_OF_PB29A |
| G6         | PB29A        | 1       | PCLKT1_0        | True_OF_PB29B |
| G7         | PB2D         | 2       | MIPI_CLKC2_0    | Comp_OF_PB2C  |
| G8         | PB2C         | 2       | MIPI_CLKT2_0    | True_OF_PB2D  |
| H1         | PB34D        | 1       | MIPI_CLKC1_0    | Comp_OF_PB34C |
| H2         | PB34C        | 1       | MIPI_CLKT1_0    | True_OF_PB34D |
| H3         | PB29C        | 1       | PCLKT1_1        | True_OF_PB29D |
| H4         | PB29D        | 1       | PCLKC1_1        | Comp_OF_PB29C |
| H5         | PB16D        | 2       | PCLKC2_1        | Comp_OF_PB16C |
| H6         | PB16C        | 2       | PCLKT2_1        | True_OF_PB16D |
| H7         | PB12D        | 2       | —               | Comp_OF_PB12C |
| H8         | PB12C        | 2       | —               | True_OF_PB12D |

### 5.3. ctfBGA80/ckfBGA80 Pinout

Table 5.3. ctfBGA80/ckfBGA80 Pinout

| Pin Number | Pin Function | Bank   | Dual Function     | Differential      |
|------------|--------------|--------|-------------------|-------------------|
| A1         | DPHY1_DN2    | DPHY1  | —                 | Comp_OF_DPHY1_DP2 |
| A2         | DPHY1_DN0    | DPHY1  | —                 | Comp_OF_DPHY1_DP0 |
| A3         | DPHY1_CKN    | DPHY1  | —                 | Comp_OF_DPHY1_CKP |
| A4         | DPHY1_DN1    | DPHY1  | —                 | Comp_OF_DPHY1_DP1 |
| A5         | DPHY1_DN3    | DPHY1  | —                 | Comp_OF_DPHY1_DP3 |
| A6         | DPHY0_DN2    | DPHY0  | —                 | Comp_OF_DPHY0_DP2 |
| A7         | DPHY0_DN0    | DPHY0  | —                 | Comp_OF_DPHY0_DP0 |
| A8         | DPHY0_CKN    | DPHY0  | —                 | Comp_OF_DPHY0_CKP |
| A9         | DPHY0_DN1    | DPHY0  | —                 | Comp_OF_DPHY0_DP1 |
| A10        | DPHY0_DN3    | DPHY0  | —                 | Comp_OF_DPHY0_DP3 |
| B1         | DPHY1_DP2    | DPHY1  | —                 | True_OF_DPHY1_DN2 |
| B2         | DPHY1_DP0    | DPHY1  | —                 | True_OF_DPHY1_DN0 |
| B3         | DPHY1_CKP    | DPHY1  | —                 | True_OF_DPHY1_CKN |
| B4         | DPHY1_DP1    | DPHY1  | —                 | True_OF_DPHY1_DN1 |
| B5         | DPHY1_DP3    | DPHY1  | —                 | True_OF_DPHY1_DN3 |
| B6         | DPHY0_DP2    | DPHY0  | —                 | True_OF_DPHY0_DN2 |
| B7         | DPHY0_DP0    | DPHY0  | —                 | True_OF_DPHY0_DN0 |
| B8         | DPHY0_CKP    | DPHY0  | —                 | True_OF_DPHY0_CKN |
| B9         | DPHY0_DP1    | DPHY0  | —                 | True_OF_DPHY0_DN1 |
| B10        | DPHY0_DP3    | DPHY0  | —                 | True_OF_DPHY0_DN3 |
| C1         | GND          | GND    | —                 | —                 |
| C2         | GND_A_DPHY1  | DPHY1  | —                 | —                 |
| C9         | GND_A_DPHY0  | DPHY0  | —                 | —                 |
| C10        | GND          | GND    | —                 | —                 |
| D1         | PB48         | 0      | PCLKT0_1/USER_SCL | —                 |
| D2         | VCCPLL_DPHY1 | DPHY1  | —                 | —                 |
| D4         | VCCA_DPHY1   | DPHY1  | —                 | —                 |
| D5         | VCCAUX       | VCCAUX | —                 | —                 |
| D6         | GNDPLL_DPHYx | GND    | —                 | —                 |
| D7         | VCCPLL_DPHY0 | DPHY0  | —                 | —                 |
| D9         | PB16A        | 2      | PCLKT2_0          | True_OF_PB16B     |
| D10        | PB16B        | 2      | PCLKC2_0          | Comp_OF_PB16A     |
| E1         | PB34A        | 1      | GR_PCLK1_0        | True_OF_PB34B     |
| E2         | PB34B        | 1      | —                 | Comp_OF_PB34A     |
| E4         | VCC          | VCC    | —                 | —                 |
| E5         | GND          | GND    | —                 | —                 |
| E6         | VCC          | VCC    | —                 | —                 |
| E7         | VCCA_DPHY0   | DPHY0  | —                 | —                 |
| E9         | PB12A        | 2      | GPLL2_0           | True_OF_PB12B     |
| E10        | PB12B        | 2      | GPLL2_0           | Comp_OF_PB12A     |
| F1         | PB38A        | 1      | —                 | True_OF_PB38B     |
| F2         | PB38B        | 1      | —                 | Comp_OF_PB38A     |

**Table 5.3. ctfBGA80/ckfBGA80 Pinout (Continued)**

| Pin Number | Pin Function | Bank    | Dual Function     | Differential  |
|------------|--------------|---------|-------------------|---------------|
| F4         | VCCIO0       | 0       | —                 | —             |
| F5         | VCCIO1       | 1       | —                 | —             |
| F6         | VCCIO2       | 2       | —                 | —             |
| F7         | VCCIO2       | 2       | —                 | —             |
| F9         | PB6A         | 2       | GR_PCLK2_0        | True_OF_PB6B  |
| F10        | PB6B         | 2       | —                 | Comp_OF_PB6A  |
| G1         | PB50         | 0       | MOSI              | —             |
| G2         | GND          | GND     | —                 | —             |
| G4         | VCCIO1       | 1       | —                 | —             |
| G5         | GND          | GND     | —                 | —             |
| G6         | VCCGPLL      | VCCGPLL | —                 | —             |
| G7         | GNDGPLL      | GND     | —                 | —             |
| G9         | PB2A         | 2       | —                 | True_OF_PB2B  |
| G10        | PB2B         | 2       | —                 | Comp_OF_PB2A  |
| H1         | PB52         | 0       | SPI_SS/CSN/SCL    | —             |
| H2         | CRESET_B     | 0       | —                 | —             |
| H9         | PB2D         | 2       | MIPI_CLKC2_0      | Comp_OF_PB2C  |
| H10        | PB2C         | 2       | MIPI_CLKT2_0      | True_OF_PB2D  |
| J1         | PB53         | 0       | SPI_SCK/MCK/SDA   | —             |
| J2         | PB49         | 0       | PMU_WKUPN/CDONE   | —             |
| J3         | PB43D        | 1       | —                 | Comp_OF_PB43C |
| J4         | PB38D        | 1       | —                 | Comp_OF_PB38C |
| J5         | PB34D        | 1       | MIPI_CLKC1_0      | Comp_OF_PB34C |
| J6         | PB29D        | 1       | PCLKC1_1          | Comp_OF_PB29C |
| J7         | PB29A        | 1       | PCLKT1_0          | True_OF_PB29B |
| J8         | PB16D        | 2       | PCLKC2_1          | Comp_OF_PB16C |
| J9         | PB6D         | 2       | —                 | Comp_OF_PB6C  |
| J10        | PB6C         | 2       | —                 | True_OF_PB6D  |
| K1         | PB51         | 0       | MISO              | —             |
| K2         | PB47         | 0       | PCLKT0_0/USER_SDA | —             |
| K3         | PB43C        | 1       | —                 | True_OF_PB43D |
| K4         | PB38C        | 1       | —                 | True_OF_PB38D |
| K5         | PB34C        | 1       | MIPI_CLKT1_0      | True_OF_PB34D |
| K6         | PB29C        | 1       | PCLKT1_1          | True_OF_PB29D |
| K7         | PB29B        | 1       | PCLKC1_0          | Comp_OF_PB29A |
| K8         | PB16C        | 2       | PCLKT2_1          | True_OF_PB16D |
| K9         | PB12D        | 2       | —                 | Comp_OF_PB12C |
| K10        | PB12C        | 2       | —                 | True_OF_PB12D |

## 5.4. csfBGA81 Pinout

Table 5.4. csfBGA81 Pinout

| Pin Number | Pin Function | Bank   | Dual Function | Differential      |
|------------|--------------|--------|---------------|-------------------|
| A1         | DPHY1_CKP    | DPHY1  | —             | True_OF_DPHY1_CKN |
| A2         | DPHY1_CKN    | DPHY1  | —             | Comp_OF_DPHY1_CKP |
| A3         | DPHY1_DP1    | DPHY1  | —             | True_OF_DPHY1_DN1 |
| A4         | DPHY1_DP3    | DPHY1  | —             | True_OF_DPHY1_DN3 |
| A5         | VCCA_DPHY1   | DPHY1  | —             | —                 |
| A6         | DPHY0_DN2    | DPHY0  | —             | Comp_OF_DPHY0_DP2 |
| A7         | DPHY0_DN0    | DPHY0  | —             | Comp_OF_DPHY0_DP0 |
| A8         | DPHY0_CKP    | DPHY0  | —             | True_OF_DPHY0_CKN |
| A9         | DPHY0_CKN    | DPHY0  | —             | Comp_OF_DPHY0_CKP |
| B1         | DPHY1_DP0    | DPHY1  | —             | True_OF_DPHY1_DN0 |
| B2         | DPHY1_DN0    | DPHY1  | —             | Comp_OF_DPHY1_DP0 |
| B3         | DPHY1_DN1    | DPHY1  | —             | Comp_OF_DPHY1_DP1 |
| B4         | DPHY1_DN3    | DPHY1  | —             | Comp_OF_DPHY1_DP3 |
| B5         | GNDPLL_DPHYx | GND    | —             | —                 |
| B6         | DPHY0_DP2    | DPHY0  | —             | True_OF_DPHY0_DN2 |
| B7         | DPHY0_DP0    | DPHY0  | —             | True_OF_DPHY0_DN0 |
| B8         | DPHY0_DP1    | DPHY0  | —             | True_OF_DPHY0_DN1 |
| B9         | DPHY0_DN1    | DPHY0  | —             | Comp_OF_DPHY0_DP1 |
| C1         | DPHY1_DP2    | DPHY1  | —             | True_OF_DPHY1_DN2 |
| C2         | DPHY1_DN2    | DPHY1  | —             | Comp_OF_DPHY1_DP2 |
| C3         | GNDPLL_DPHY1 | DPHY1  | —             | —                 |
| C4         | VCCPLL_DPHY1 | DPHY1  | —             | —                 |
| C5         | GND          | GND    | —             | —                 |
| C6         | VCCPLL_DPHY0 | DPHY0  | —             | —                 |
| C7         | GNDPLL_DPHY0 | DPHY0  | —             | —                 |
| C8         | DPHY0_DP3    | DPHY0  | —             | True_OF_DPHY0_DN3 |
| C9         | DPHY0_DN3    | DPHY0  | —             | Comp_OF_DPHY0_DP3 |
| D1         | PB34A        | 1      | GR_PCLK1_0    | True_OF_PB34B     |
| D2         | PB34B        | 1      | —             | Comp_OF_PB34A     |
| D3         | VCCA_DPHY1   | DPHY1  | —             | —                 |
| D4         | GND          | GND    | —             | —                 |
| D5         | VCCAUX       | VCCAUX | —             | —                 |
| D6         | GND          | GND    | —             | —                 |
| D7         | VCCA_DPHY0   | DPHY0  | —             | —                 |
| D8         | PB16B        | 2      | PCLKC2_0      | Comp_OF_PB16A     |
| D9         | PB16A        | 2      | PCLKT2_0      | True_OF_PB16B     |
| E1         | PB38A        | 1      | —             | True_OF_PB38B     |
| E2         | PB38B        | 1      | —             | Comp_OF_PB38A     |
| E3         | VCC          | VCC    | —             | —                 |
| E4         | VCC          | VCC    | —             | —                 |
| E5         | GND          | GND    | —             | —                 |
| E6         | VCCIO2       | 2      | —             | —                 |

**Table 5.4 csfBGA81 Pinout (Continued)**

| Pin Number | Pin Function | Bank    | Dual Function     | Differential  |
|------------|--------------|---------|-------------------|---------------|
| E7         | PB12B        | 2       | GPLL2_0           | Comp_OF_PB12A |
| E8         | PB6B         | 2       | —                 | Comp_OF_PB6A  |
| E9         | PB6A         | 2       | GR_PCLK2_0        | True_OF_PB6B  |
| F1         | PB50         | 0       | MOSI              | —             |
| F2         | PB48         | 0       | PCLKT0_1/USER_SCL | —             |
| F3         | VCCIO1       | 1       | —                 | —             |
| F4         | GND          | GND     | —                 | —             |
| F5         | GNDGPLL      | GND     | —                 | —             |
| F6         | VCCIO2       | 2       | —                 | —             |
| F7         | PB12A        | 2       | GPLL2_0           | True_OF_PB12B |
| F8         | PB2B         | 2       | —                 | Comp_OF_PB2A  |
| F9         | PB2A         | 2       | —                 | True_OF_PB2B  |
| G1         | PB52         | 0       | SPI_SS/CSN/SCL    | —             |
| G2         | CRESET_B     | 0       | —                 | —             |
| G3         | VCCIO0       | 0       | —                 | —             |
| G4         | VCCIO1       | 1       | —                 | —             |
| G5         | VCCGPLL      | VCCGPLL | —                 | —             |
| G6         | PB29B        | 1       | PCLKC1_0          | Comp_OF_PB29A |
| G7         | PB29A        | 1       | PCLKT1_0          | True_OF_PB29B |
| G8         | PB2D         | 2       | MIPI_CLKC2_0      | Comp_OF_PB2C  |
| G9         | PB2C         | 2       | MIPI_CLKT2_0      | True_OF_PB2D  |
| H1         | PB53         | 0       | SPI_SCK/MCK/SDA   | —             |
| H2         | PB49         | 0       | PMU_WKUPN/CDONE   | —             |
| H3         | PB43D        | 1       | —                 | Comp_OF_PB43C |
| H4         | PB38D        | 1       | —                 | Comp_OF_PB38C |
| H5         | PB34D        | 1       | MIPI_CLKC1_0      | Comp_OF_PB34C |
| H6         | PB29D        | 1       | PCLKC1_1          | Comp_OF_PB29C |
| H7         | PB16D        | 2       | PCLKC2_1          | Comp_OF_PB16C |
| H8         | PB6D         | 2       | —                 | Comp_OF_PB6C  |
| H9         | PB6C         | 2       | —                 | True_OF_PB6D  |
| J1         | PB51         | 0       | MISO              | —             |
| J2         | PB47         | 0       | PCLKT0_0/USER_SDA | —             |
| J3         | PB43C        | 1       | —                 | True_OF_PB43D |
| J4         | PB38C        | 1       | —                 | True_OF_PB38D |
| J5         | PB34C        | 1       | MIPI_CLKT1_0      | True_OF_PB34D |
| J6         | PB29C        | 1       | PCLKT1_1          | True_OF_PB29D |
| J7         | PB16C        | 2       | PCLKT2_1          | True_OF_PB16D |
| J8         | PB12D        | 2       | —                 | Comp_OF_PB12C |
| J9         | PB12C        | 2       | —                 | True_OF_PB12D |

## 5.5. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLink device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

**Table 5.5. Dual Function Pin Descriptions**

| Signal Name            | I/O | Description                                                                                                                                                                                                                                                                                                                                      |
|------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>General Purpose</b> |     |                                                                                                                                                                                                                                                                                                                                                  |
| USER_SCL               | I/O | User Slave I2C0 clock input and Master I <sup>2</sup> C0 clock output. Enables PMU wake-up via I2C0.                                                                                                                                                                                                                                             |
| USER_SDA               | I/O | User Slave I2C0 data input and Master I <sup>2</sup> C0 data output. Enables PMU wakeup via I2C0.                                                                                                                                                                                                                                                |
| PMU_WKUPN              | —   | This pin wakes the PMU from sleep mode when toggled low.                                                                                                                                                                                                                                                                                         |
| <b>Clock Functions</b> |     |                                                                                                                                                                                                                                                                                                                                                  |
| GPLL2_0[T, C]_IN       | I   | General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network.                                                                                                                 |
| GR_PCLK[Bank]0         | I   | These pins provide a short General Routing path to the primary clock network, but should only be used when the design has used up all the PCLK pins. These pins should only be used for low speed clocks that are not sensitive to skew. Refer to <a href="#">CrossLink sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02015)</a> for details. |
| PCLK[T/C][Bank]_num    | I/O | General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.                                                                                                                                                                                       |
| MIPI_CLK[T/C][Bank]_0  | I/O | MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network.                                                                                                               |
| <b>Configuration</b>   |     |                                                                                                                                                                                                                                                                                                                                                  |
| CDONE                  | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.                                                                                                                                                                                              |
| SPI_SCK                | I   | Input Configuration Clock for configuring CrossLink in Slave SPI mode (SSPI).                                                                                                                                                                                                                                                                    |
| MCK                    | O   | Output Configuration Clock for configuring CrossLink in Master SPI mode (MSPI).                                                                                                                                                                                                                                                                  |
| SPI_SS                 | I   | Input Chip Select for configuring CrossLink in Slave SPI mode (SSPI).                                                                                                                                                                                                                                                                            |
| CSN                    | O   | Output Chip Select for configuring CrossLink in Master SPI mode (MSPI).                                                                                                                                                                                                                                                                          |
| MOSI                   | I/O | Data Output when configuring CrossLink in Master SPI mode (MSPI), data input when configuring CrossLink in Slave SPI mode (SSPI).                                                                                                                                                                                                                |
| MISO                   | I/O | Data Input when configuring CrossLink in Master SPI mode (MSPI), data output when configuring CrossLink in Slave SPI mode (SSPI).                                                                                                                                                                                                                |
| SCL                    | I/O | Slave I <sup>2</sup> C clock I/O when configuring CrossLink in I <sup>2</sup> C mode.                                                                                                                                                                                                                                                            |
| SDA                    | I/O | Slave I <sup>2</sup> C data I/O when configuring CrossLink in I <sup>2</sup> C mode.                                                                                                                                                                                                                                                             |

## 5.6. Dedicated Function Pin Descriptions

**Table 5.6. Dedicated Function Pin Descriptions**

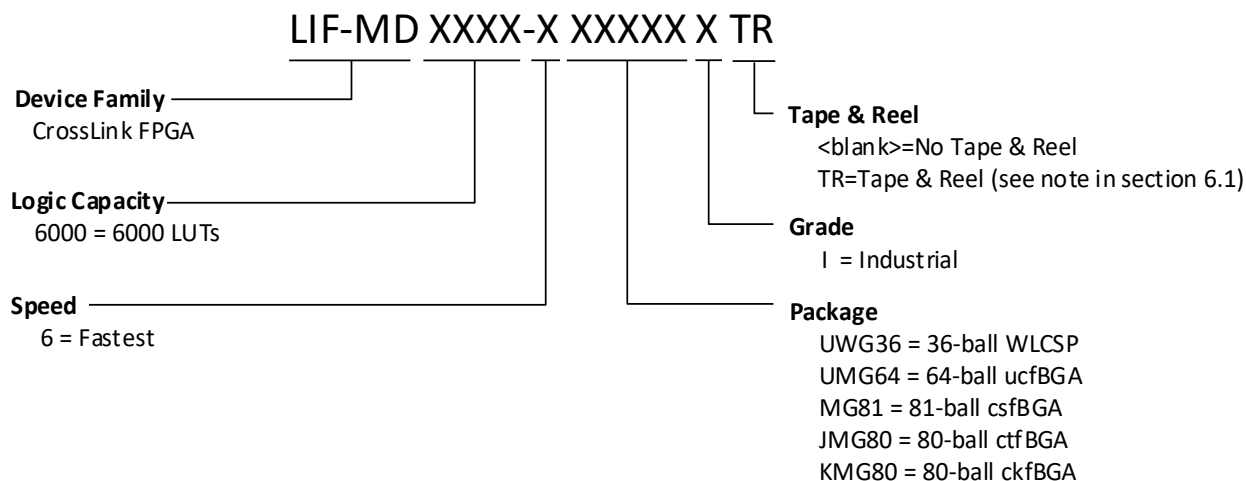
| Signal Name            | I/O | Description                                                                                                            |
|------------------------|-----|------------------------------------------------------------------------------------------------------------------------|
| <b>Configuration</b>   |     |                                                                                                                        |
| CRESET_B               | I   | Configuration Reset, active LOW.                                                                                       |
| <b>MIPI D-PHY</b>      |     |                                                                                                                        |
| DPHY[num]_CK[P/N]      | I/O | MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.                                                     |
| DPHY[num]_D[P/N][lane] | I/O | MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative,<br>Lane = data lane in the D-PHY block 0, 1, 2 or 3. |

## 5.7. Pin Information Summary

Table 5.7. Pin Information Summary

| Pin Type                                            | CrossLink |           |           |           |           |
|-----------------------------------------------------|-----------|-----------|-----------|-----------|-----------|
|                                                     | WLCSP36   | ucfBGA64  | ctfBGA80  | ckfBGA80  | csfBGA81  |
| Total General Purpose I/O                           | 17        | 29        | 37        | 37        | 37        |
| VCC/VCCIOx/VCCAUX/VCCGPLL                           | 4         | 8         | 9         | 9         | 10        |
| GND                                                 | 2         | 3         | 6         | 6         | 6         |
| D-PHY Clock/Data                                    | 10        | 20        | 20        | 20        | 20        |
| D-PHY VCC                                           | 1         | 2         | 4         | 4         | 4         |
| D-PHY GND                                           | 1         | 1         | 3         | 3         | 3         |
| CRESETB                                             | 1         | 1         | 1         | 1         | 1         |
| <b>Total Balls</b>                                  | <b>36</b> | <b>64</b> | <b>80</b> | <b>80</b> | <b>81</b> |
| <b>General Purpose I/O per Bank</b>                 |           |           |           |           |           |
| Bank 0                                              | 7         | 7         | 7         | 7         | 7         |
| Bank 1                                              | 0         | 10        | 14        | 14        | 14        |
| Bank 2                                              | 10        | 12        | 16        | 16        | 16        |
| <b>Total General Purpose Single Ended I/O</b>       | <b>17</b> | <b>29</b> | <b>37</b> | <b>37</b> | <b>37</b> |
| <b>Differential I/O Pairs per Bank</b>              |           |           |           |           |           |
| Bank 0                                              | 0         | 0         | 0         | 0         | 0         |
| Bank 1                                              | 0         | 5         | 7         | 7         | 7         |
| Bank 2                                              | 5         | 6         | 8         | 8         | 8         |
| <b>Total General Purpose Differential I/O Pairs</b> | <b>5</b>  | <b>11</b> | <b>15</b> | <b>15</b> | <b>15</b> |

## 6. CrossLink Part Number Description



### 6.1. Ordering Part Numbers

#### Industrial\*

| Part Number          | Grade | Package          | Pins | Temp.      | LUTs (K) |
|----------------------|-------|------------------|------|------------|----------|
| LIF-MD6000-6UWG36ITR | –6    | Lead free WLCSP  | 36   | Industrial | 5.9      |
| LIF-MD6000-6UMG64I   | –6    | Lead free ucfBGA | 64   | Industrial | 5.9      |
| LIF-MD6000-6MG81I    | –6    | Lead free csfBGA | 81   | Industrial | 5.9      |
| LIF-MD6000-6JMG80I   | –6    | Lead free ctfBGA | 80   | Industrial | 5.9      |
| LIF-MD6000-6KMG80I   | –6    | Lead free ckfBGA | 80   | Industrial | 5.9      |

**\*Note:** UWG36 package is available in shipments of 5000 pieces/reel (TR), 1000 pieces/reel (TR1K), and 50 pieces/reel (TR50 – for samples only).

## References

For more information, refer to the following technical notes:

- [CrossLink High-Speed I/O Interface \(FPGA-TN-02012\)](#)
- [CrossLink Hardware Checklist \(FPGA-TN-02013\)](#)
- [CrossLink Programming and Configuration Usage Guide \(FPGA-TN-02014\)](#)
- [CrossLink sysCLOCK PLL/DLL Design and Usage Guide \(FPGA-TN-02015\)](#)
- [CrossLink sysI/O Usage Guide \(FPGA-TN-02016\)](#)
- [CrossLink Memory Usage Guide \(FPGA-TN-02017\)](#)
- [Power Management and Calculation for CrossLink Devices \(FPGA-TN-02018\)](#)
- [CrossLink I2C Hardened IP Usage Guide \(FPGA-TN-02019\)](#)
- [Advanced CrossLink I2C Hardened IP Reference Guide \(FPGA-TN-02020\)](#)

For package information, refer to the following technical notes:

- [PCB Layout Recommendations for BGA Packages \(TN1074\)](#)
- [Solder Reflow Guide for Surface Mount Devices \(FPGA-TN-12041, previously TN1076\)](#)
- [Wafer-Level Chip-Scale Package Guide \(TN1242\)](#)
- [Thermal Management \(FPGA-TN-02044\)](#)
- [Package Diagrams \(FPGA-DS-02053\)](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS): [www.jedec.org](http://www.jedec.org)
- MIPI Standards (D-PHY): [www.mipi.org](http://www.mipi.org)

## Technical Support

For assistance, submit a technical support case at [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

## Revision History

### Revision 1.8, January 2021

| Section                          | Change Summary                                                                                                                               |
|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| DC and Switching Characteristics | Corrected table formatting error. Removed duplicated section from <a href="#">Table 4.13. CrossLink External Switching Characteristics</a> . |

### Revision 1.7, December 2020

| Section                          | Change Summary                                                                                                                                                                                                                                                 |
|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DC and Switching Characteristics | <ul style="list-style-type: none"> <li>Updated footnotes in Table 4.4. Power-On-Reset Voltage Levels.</li> <li>Added the Power Supply Sequence Requirements section.</li> <li>Updated footnote 7 in Table 4.12. CrossLink Maximum I/O Buffer Speed.</li> </ul> |
| —                                | Adjusted table formatting.                                                                                                                                                                                                                                     |

### Revision 1.6, November 2019

| Section                          | Change Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| —                                | Added Disclaimers section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Architecture Overview            | Revised referenced diagram to Figure 3.12 in Edge Clocks section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| DC and Switching Characteristics | <ul style="list-style-type: none"> <li>Added Over recommended operating conditions to the following sections: <ul style="list-style-type: none"> <li>Power Supply Ramp Rates</li> <li>Power-On-Reset Voltage Levels</li> <li>Power Management Unit (PMU) Timing</li> <li>sysI/O Recommended Operating Conditions</li> <li>LVDS/subLVDS/SLVS200</li> <li>CrossLink External Switching Characteristics</li> <li>Hardened MIPI D-PHY Performance</li> <li>User I2C</li> </ul> </li> <li>Added footnote to Table 4.9. sysI/O Single-Ended DC Electrical Characteristics<sup>1</sup>.</li> <li>Revised footnote 7 in Table 4.12. CrossLink Maximum I/O Buffer Speed.</li> <li>Updated footnotes in Table 4.13. CrossLink External Switching Characteristics 3,4.</li> <li>Updated Table 4.20. CrossLink sysCONFIG Port Timing Specifications. <ul style="list-style-type: none"> <li>Changed tPGRM Min value.</li> <li>Added footnote 3.</li> </ul> </li> </ul> |
| Pinout Information               | In the Table 5.5. Dual Function Pin Descriptions table, added information to GR_PCLK[Bank]0 description.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| References                       | <ul style="list-style-type: none"> <li>Updated document number of PCB Layout Recommendations for BGA Packages.</li> <li>Fixed link to the Thermal Management document and updated document number.</li> <li>Provided document number of Package Diagrams.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Revision History                 | Updated format.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Back Cover                       | Updated template.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

### Revision 1.5, July 2018

| Section                          | Change Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DC and Switching Characteristics | <ul style="list-style-type: none"> <li>Updated Table 4.1. Absolute Maximum Ratings. Added footnote 4 to V<sub>CCAUX</sub> parameters.</li> <li>Updated Table 4.2. Recommended Operating Conditions. Added footnote 3 to V<sub>CCAUX</sub> parameters.</li> <li>Updated Table 4.13. CrossLink External Switching Characteristics. Revised t<sub>SU_GDDR_X_MP</sub> and t<sub>HD_GDDR_X_MP</sub> conditions under I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing.</li> </ul> |

**Revision 1.4, February 2018**

| Section                          | Change Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| All                              | Removed Application Examples section and its associated references throughout the document                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Architecture Overview            | <ul style="list-style-type: none"> <li>General update applied to this section.</li> <li>Reordered the list of features supported by the hard D-PHY quads.</li> <li>Added Figure 3.3 to Figure 3.6 to the MIPI D-PHY Blocks section.</li> <li>Updated the Programmable I/O Banks section. <ul style="list-style-type: none"> <li>Added Bank 0 list of features.</li> <li>Added Table 3.1, Table 3.2, Table 3.3, and Table 3.4.</li> </ul> </li> <li>Updated Programmable FPGA Fabric section. <ul style="list-style-type: none"> <li>Removed FPGA Fabric Overview header.</li> <li>Added PFU Blocks section.</li> <li>Added Slice section.</li> </ul> </li> <li>Moved Clocking Overview as a new Clocking Structure (heading 2) section and added contents.</li> <li>Moved Embedded Block RAM Overview as a new (heading 2) section and added contents.</li> <li>Removed System Resources section.</li> <li>Moved Power Management Unit section under Embedded Block RAM Overview.</li> <li>Removed Device Configuration section.</li> <li>Moved User I2C IP as a new (heading 2) section.</li> <li>Added Programming and Configuration section.</li> </ul> |
| DC and Switching Characteristics | <ul style="list-style-type: none"> <li>Updated CrossLink Maximum General Purpose I/O Buffer Speed section. Changed LVTTTL33/LVCMOS33 to LVCMOS33/LVTTTL33.</li> <li>Updated CrossLink External Switching Characteristics section (general update).</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Pinout Information               | Placed captions to pinout tables.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Revision 1.3, November 2017**

| Section                   | Change Summary                                                                                                                                                                                                                                                                                                                                           |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Acronyms in This Document | Added entries to the section.                                                                                                                                                                                                                                                                                                                            |
| Features                  | <ul style="list-style-type: none"> <li>Changed footprint to 80-ball ctfBGA (42 mm<sup>2</sup>).</li> <li>Removed Application Examples section and its associated references throughout the document.</li> </ul>                                                                                                                                          |
| Product Feature Summary   | <ul style="list-style-type: none"> <li>Added 80-ball ckfBGA (49 mm<sup>2</sup>) package in Features section.</li> <li>Updated note in Table 2.1, Table 2.2, Table 2.3, Table 2.4, Table 2.5, Table 2.6, Table 2.7, Table 2.8, and Table 2.9 Added 80 ckfBGA (7.0 x 7.0 mm<sup>2</sup>, 1 mm) package to Table 2.1. CrossLink Feature Summary.</li> </ul> |
| Architecture Overview     | <ul style="list-style-type: none"> <li>Updated System Resources section.</li> <li>Removed LVCMOS12 (Outputs Only) from CMOS GPIO (Bank 0) section.</li> <li>Added information in Device Configuration section.</li> </ul>                                                                                                                                |

| Section                          | Change Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DC and Switching Characteristics | <ul style="list-style-type: none"> <li>Updated Table 4.1. Absolute Maximum Ratings. <ul style="list-style-type: none"> <li>Changed symbol from VCCPLL to VCCGPLL.</li> <li>Removed VCC_DPHY symbol.</li> </ul> </li> <li>Updated Table 4.2. Recommended Operating Conditions. <ul style="list-style-type: none"> <li>Revised symbols to VCCGPLL and VCCIO0.</li> <li>Added row of VCCIO1/2 symbol.</li> <li>Removed row of VCC_DPHYx symbol.</li> <li>Removed VCC_DPHY1 from V<sub>CCMU_DPHY1</sub> parameter description.</li> </ul> </li> <li>Added notes to Table 4.8. sysI/O Recommended Operating Conditions1 and Table 4.20. CrossLink sysCONFIG Port Timing Specifications.</li> <li>Updated link to the LIFMD Product Family Qualification Summary reference in the ESD Performance section.</li> <li>Removed V<sub>CCIO</sub> = 1.2 V between <math>0 \leq V_{IN} \leq 0.65 * V_{CCIO}</math> condition from Table 4.5. DC Electrical Characteristics.</li> <li>Updated Table 4.6. CrossLink Supply Current. <ul style="list-style-type: none"> <li>Updated ICCMLL_DPHYx, ICCMLL_DPHYx_STDBY, and ICCPLL_DPHY_SLEEP parameters.</li> <li>Moved ICCA_DPHY_SLEEP and updated parameter.</li> <li>Updated ICCAMLL_DPHYx_SLEEP parameter and unit.</li> <li>Updated footnote 4-a, 4-b, and 5-b.</li> </ul> </li> <li>Updated Table 4.12. CrossLink Maximum I/O Buffer Speed. <ul style="list-style-type: none"> <li>Added ckfBGA80 package in descriptions.</li> <li>Changed LVTTTL33/LVCMOS to LVTTTL33/LVCMOS33.</li> <li>Changed V<sub>CCIO</sub> to V<sub>CCIO1/2</sub> in LVCMOS12 description.</li> </ul> </li> <li>Updated the CrossLink External Switching Characteristics section and Table 4.13. CrossLink External Switching Characteristics.</li> <li>Removed “Over recommended commercial operating conditions.” <ul style="list-style-type: none"> <li>General update of information under Generic DDR Interfaces2 including the addition of “Generic DDRX1 I/O with Clock and Data Centered at General Purpose Pins (GDDR1_RX/TX.ECLK.Centered)” and “Generic DDRX1 I/O with Clock and Data Aligned at General Purpose Pins (GDDR1_RX/TX.ECLK.Aligned)” rows</li> <li>Added ckfBGA80 package in specific conditions.</li> </ul> </li> <li>Changed T<sub>REFRESH</sub> to T<sub>CONFIGURATION</sub> in Table 4.21. SRAM Configuration Time from NVCM.</li> </ul> |
| Pinout Information               | <ul style="list-style-type: none"> <li>Updated section introduction.</li> <li>Updated WLCSP36 Pinout. Changed C4 bank to VCC.</li> <li>Updated section to ctfBGA80/ckfBGA80 Pinout and revised pin function of C1, C2, C9, C10, D6, E5, G2, G5, and G7.</li> <li>Updated pin function of B5 in csfBGA81 Pinout.</li> <li>Updated Pin Information Summary section.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Ordering Part Number             | <ul style="list-style-type: none"> <li>Updated CrossLink Part Number Description section.</li> <li>Added LIF-MD6000-6KMG80I part number to Ordering Part Numbers section.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| References                       | Update reference to the Solder Reflow Guide for Surface Mount Devices document.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Revision 1.2, June 2017**

| Section                          | Change Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Feature Summary          | Updated Fabric Resources Used in Table 2.1, Table 2.2, Table 2.3, Table 2.4, Table 2.5, Table 2.6, and Table 2.9.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Architecture Overview            | <ul style="list-style-type: none"> <li>Updated Figure 3.1. CrossLink Device Block Diagram.</li> <li>Added row of <math>V_{CCAUX}</math> for 3.3 V in Table 4.1. Absolute Maximum Ratings and Table 4.2. Recommended Operating Conditions.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| DC and Switching Characteristics | <ul style="list-style-type: none"> <li>Added row of <math>C_3</math> to Table 4.5. DC Electrical Characteristics.</li> <li>Added rows of <math>I_{CCAMLL\_DPHYX}</math>, <math>I_{CCAMLL\_DPHYX\_STDBY}</math>, and <math>I_{CCAMLL\_DPHYX\_SLEEP}</math> to Table 4.6. CrossLink Supply Current.</li> <li>Updated Max value in Table 4.7. PMU Timing.</li> <li>Updated values of subLVDS (Input only) and SLVS200 (Input only), and added row of LVDS (Input only) to Table 4.8. sysI/O Recommended Operating Conditions.</li> <li>Updated Table 5.10. LVDS/subLVDS1/SLVS200.</li> <li>Updated parameter descriptions in Table 4.11. MIPI D-PHY.</li> <li>Added row of MIPI D-PHY (LP Mode), and updated Max values of subLVDS and SLVS200 in Table 4.12. CrossLink Maximum I/O Buffer Speed.</li> <li>Updated conditions in Table 4.13. CrossLink External Switching Characteristics.</li> <li>Added rows of <math>f_{PD}</math> and <math>f_{VCO}</math> to Table 4.14. sysCLOCK PLL Timing.</li> <li>Updated values in Table 4.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s &gt; MIPI D-PHY Data Rate &gt; 1200 Mb/s), Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s &gt; MIPI D-PHY Data Rate &gt; 1000 Mb/s) and Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s &gt; MIPI D-PHY Data Rate &gt; 10 Mb/s).</li> <li>Updated Typ values of <math>DCH_{CLKHF}</math> and <math>DCH_{CLKLF}</math> in Table 4.18. Internal Oscillators.</li> <li>Added row of TDELAY to Table 4.19. User I2C.</li> <li>Updated Min value of <math>t_{SCS}</math> in Table 4.20. CrossLink sysCONFIG Port Timing Specifications.</li> <li>Updated symbol and parameter in Table 4.21. SRAM Configuration Time from NVCM.</li> <li>Included version number in Pinout Information.</li> </ul> |

**Revision 1.1, March 2017**

| Section                          | Change Summary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Architecture Overview            | Updated I/O placements on banks containing MIPI interface in Programmable I/O Banks section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| DC and Switching Characteristics | <ul style="list-style-type: none"> <li>Updated Table 4.4. Power-On-Reset Voltage Levels, added row of <math>V_{PORDN}</math></li> <li>Added Note 5 to Table 4.5. DC Electrical Characteristics.</li> <li>Updated Table 4.6. CrossLink Supply Current, added notes.</li> <li>Updated max values of <math>V_{THD}</math> and <math>V_{THD(subLVDS)}</math> in Table 4.10. LVDS/subLVDS1/SLVS200.</li> <li>Maximum input frequency values of subLVDS and SLVS200 are TBD in Table 4.12. CrossLink Maximum I/O Buffer Speed.</li> <li>Updated Table 4.13. CrossLink External Switching Characteristics.</li> <li>Updated min values of <math>t_{SU\_MIPIX4}</math> and <math>t_{HO\_MIPIX4}</math> in Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s &gt; MIPI D-PHY Data Rate &gt; 1000 Mb/s) and Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s &gt; MIPI D-PHY Data Rate &gt; 10 Mb/s).</li> <li>Updated Table 4.20. CrossLink sysCONFIG Port Timing Specifications.</li> <li>Updated Table 4.21. SRAM Configuration Time from NVCM.</li> </ul> |
| Pinout Information               | Updated this section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Ordering Part Numbers            | Updated CrossLink Part Number Description.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Revision 1.0, July 2016**

| Section | Change Summary           |
|---------|--------------------------|
| All     | Updated document number. |

**Revision 1.0, May 2016**

| Section | Change Summary             |
|---------|----------------------------|
| All     | First preliminary release. |



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