All Devices Discontinued!

Product Change Notification (PCN) #09-10 has been issued to discontinue all devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

<table>
<thead>
<tr>
<th>Product Line</th>
<th>Ordering Part Number</th>
<th>Product Status</th>
<th>Reference PCN</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAL20RA10</td>
<td></td>
<td>Discontinued</td>
<td>PCN#09-10</td>
</tr>
<tr>
<td>GAL20RA10B-10LP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-15LP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-20LP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-30LP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-20LPI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-7LJ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-10LJ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-15LJ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-20LJ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-30LJ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAL20RA10B-20LJI</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
GAL20RA10
High-Speed Asynchronous E2CMOS PLD
Generic Array Logic™

Features

- **HIGH PERFORMANCE E2CMOS® TECHNOLOGY**
  - 7.5 ns Maximum Propagation Delay
  - Fmax = 83.3 MHz
  - 9 ns Maximum from Clock Input to Data Output
  - TTL Compatible 8 mA Outputs
  - UltraMOS® Advanced CMOS Technology

- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - 75mA Typical Icc

- **ACTIVE PULL-UPS ON ALL PINS**

- **E2 CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100 ms)
  - 20 Year Data Retention

- **TEN OUTPUT LOGIC MACROCELLS**
  - Independent Programmable Clocks
  - Independent Asynchronous Reset and Preset
  - Registered or Combinatorial with Polarity
  - Full Function and Parametric Compatibility with PAL20RA10

- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability

- **APPLICATIONS INCLUDE**:
  - State Machine Control
  - Standard Logic Consolidation
  - Multiple Clock Logic Designs

- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

Description

The GAL20RA10 combines a high performance CMOS process with electrically erasable (E2) floating gate technology to provide the highest speed performance available in the PLD market. Lattice Semiconductor’s E2CMOS circuitry achieves power levels as low as 75mA typical Icc which represents a substantial savings in power when compared to bipolar counterparts. E2 technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. Therefore, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

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LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

July 1997

20ra10_02
GAL20RA10 Ordering Information

### Commercial Grade Specifications

<table>
<thead>
<tr>
<th>Tpd (ns)</th>
<th>Tsu (ns)</th>
<th>Tco (ns)</th>
<th>Icc (mA)</th>
<th>Ordering #</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.5</td>
<td>3</td>
<td>9</td>
<td>100</td>
<td>GAL20RA10B-7LJ</td>
<td>28-Lead PLCC</td>
</tr>
<tr>
<td>10</td>
<td>4</td>
<td>11</td>
<td>100</td>
<td>GAL20RA10B-10LP</td>
<td>24-Pin Plastic DIP</td>
</tr>
<tr>
<td>15</td>
<td>7</td>
<td>15</td>
<td>100</td>
<td>GAL20RA10B-15LP</td>
<td>24-Pin Plastic DIP</td>
</tr>
<tr>
<td>20</td>
<td>10</td>
<td>20</td>
<td>100</td>
<td>GAL20RA10B-20LP</td>
<td>24-Pin Plastic DIP</td>
</tr>
<tr>
<td>30</td>
<td>20</td>
<td>30</td>
<td>100</td>
<td>GAL20RA10B-30LP</td>
<td>24-Pin Plastic DIP</td>
</tr>
</tbody>
</table>

### Industrial Grade Specifications

<table>
<thead>
<tr>
<th>Tpd (ns)</th>
<th>Tsu (ns)</th>
<th>Tco (ns)</th>
<th>Icc (mA)</th>
<th>Ordering #</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>10</td>
<td>20</td>
<td>120</td>
<td>GAL20RA10B-20LP</td>
<td>24-Pin Plastic DIP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>28-Lead PLCC</td>
</tr>
</tbody>
</table>

### Part Number Description

- **Device Name**: GAL20RA10B
- **Speed (ns)**: 20
- **Power**: Low Power
- **Grade**: Blank = Commercial, I = Industrial
- **Package**: P = Plastic DIP, J = PLCC

*ALL DEVICES DISCONTINUED*
Output Logic Macrocell (OLMC)

The GAL20RA10 OLMC consists of 10 D flip-flops with individual asynchronous programmable reset, preset and clock product terms. The sum of four product terms and an Exclusive-OR provides a programmable polarity D-input to each flip-flop. An output enable term combined with the dedicated output enable pin provides tri-state control of each output. Each OLMC has a flip-flop bypass, allowing any combination of registered or combinatorial outputs.

The GAL20RA10 has 10 dedicated input pins and 10 programmable I/O pins, which can be either inputs, outputs, or dynamic I/O. Each pin has a unique path to the logic array. All macrocells have the same type and number of data and control product terms, allowing the user to exchange I/O pin assignments without restriction.

Independent Programmable Clocks

An independent clock control product term is provided for each GAL20RA10 macrocell. Data is clocked into the flip-flop on the active edge of the clock product term. The use of individual clock control product terms allows up to ten separate clocks. These clocks can be derived from any pin or combination of pins and/or feedback from other flip-flops. Multiple clock sources allow a number of asynchronous register functions to be combined into a single GAL20RA10. This allows the designer to combine discrete logic functions into a single device.

Programmable Polarity

The polarity of the D-input to each macrocell flip-flop is individually programmable to be active high or low. This is accomplished with a programmable Exclusive-OR gate on the D-input of each flip-flop. The polarity of the pin is active low when XOR bit is programmed (or zero) and is active high when XOR bit is erased (or one). Because of the inverted output buffer, the XOR gate output node is opposite polarity from the pin. It should be noted that the programmable polarity only affects the data latched into the flip-flop on the active edge of the clock product term. The reset, preset and preload will alter the state of the flip-flop independently of the state of programmable polarity bit. The ability to program the active polarity of the D-inputs can be used to reduce the total number of product terms used, by allowing the DeMorganization of the logic functions. This logic reduction is accomplished by the logic compiler, and does not require the designer to define the polarity.

Output Enable

The output of each GAL20RA10 macrocell is controlled by the “AND’ing” of an independent output enable product term and a common active low output enable pin (pin 13 on DIP package / pin 16 on PLCC package). The output is enabled while the output enable product term is active and the output enable pin is low. This output control structure allows several output enable alternatives.

Asynchronous Reset and Preset

Each GAL20RA10 macrocell has an independent asynchronous reset and preset control product term. The reset and preset product terms are level sensitive, and will hold the flip-flop in the reset or preset state while the product term is active independent of the clock or D-inputs. It should be noted that the reset and preset term alter the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low.

<table>
<thead>
<tr>
<th>RESET</th>
<th>PRESET</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Registered function of data product term</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Reset register to “0” (device pin = “1”)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Preset register to “1” (device pin = “0”)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Register-bypass (combinatorial output)</td>
</tr>
</tbody>
</table>

Combinatorial Control

The register in each GAL20RA10 macrocell may be bypassed by asserting both the reset and preset product terms. While both product terms are active the flip-flop is bypassed and the D-input is presented directly to the inverting output buffer. This provides the designer the ability to dynamically configure any macrocell as a combinatorial output, or to fix the macrocell as combinatorial only by forcing both reset and preset product terms active. Some logic compilers will configure macrocells as registered or combinatorial based on the logic equations, others require the designer to force the reset and preset product terms active for combinatorial macrocells.

Parallel Flip-Flop Preload

The flip-flops of a GAL20RA10 can be reset or preset from the I/O pins by applying a logic low to the preload pin (pin 1 on DIP package / pin 2 on PLCC package) and applying the desired logic level to each I/O pin. The I/O pins must remain valid for the preload setup and hold time. All 10 flip-flops are reset or preset during preload, independent of all other OLMC inputs.

A logic low on an I/O pin during preload will preset the flip-flop, a logic high will reset the flip-flop. The output of any flip-flop to be preloaded must be disabled. Enabling the output during preload will maintain the current logic state. It should be noted that the preload alters the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low. Note that the common output enable pin will disable all 10 outputs of the GAL20RA10 when held high.
Specifications GAL20RA10B

Absolute Maximum Ratings(1)

Supply voltage $V_{CC}$ ........................................ -0.5 to +7V
Input voltage applied ........................................ -2.5 to $V_{CC} +1.0V$
Off-state output voltage applied .......................... -2.5 to $V_{CC} +1.0V$
Storage Temperature ........................................ -65 to 150°C

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature ($T_A$) ............................. 0 to +75°C
Supply voltage ($V_{CC}$) with Respect to Ground .......... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature ($T_A$) .......................... -40 to +85°C
Supply voltage ($V_{CC}$) with Respect to Ground .......... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN.</th>
<th>TYP. 3</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>$V_{SS} - 0.5$</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>$2.0$</td>
<td>—</td>
<td>$V_{CC} +1$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input or I/O Low Leakage Current</td>
<td>$0V \leq V_{IN} \leq V_{IL} (MAX.)$</td>
<td>—</td>
<td>—</td>
<td>-100</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>IIH</td>
<td>Input or I/O High Leakage Current</td>
<td>$3.5V \leq V_{IN} \leq V_{CC}$</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>$I_{OL} = MAX., V_{IN} = V_{IL} or V_{IH}$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>$I_{OH} = MAX., V_{IN} = V_{IL} or V_{IH}$</td>
<td>2.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Output Current</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IOH</td>
<td>High Level Output Current</td>
<td>—</td>
<td>—</td>
<td>-3.2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short Circuit Current</td>
<td>$V_{CC} = 5V, V_{OUT} = 0.5V, T_A = 25°C$</td>
<td>-50</td>
<td>—</td>
<td>-135</td>
<td>mA</td>
</tr>
</tbody>
</table>

COMMERCIAL

| ICC    | Operating Power Supply Current | $V_{IL} = 0.5V, V_{IH} = 3.0V, f_{pulse} = 15MHz$ | 75   | 100   | mA    |

INDUSTRIAL

| ICC    | Operating Power Supply Current | $V_{IL} = 0.5V, V_{IH} = 3.0V, f_{pulse} = 15MHz$ | 75   | 120   | mA    |

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at $V_{CC} = 5V$ and $T_A = 25°C$
## Specifications GAL20RA10B

### AC Switching Characteristics

**Over Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>PARAM</th>
<th>TEST COND</th>
<th>DESCRIPTION</th>
<th>COM</th>
<th>COM</th>
<th>COM</th>
<th>COM / IND</th>
<th>COM</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>-7</td>
<td>-10</td>
<td>-15</td>
<td>-20</td>
<td>-30</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>tpd</td>
<td>A</td>
<td>Input or I/O to Combinatorial Output</td>
<td>2</td>
<td>7.5</td>
<td>2</td>
<td>10</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>tco</td>
<td>A</td>
<td>Clock to Output Delay</td>
<td>2</td>
<td>9</td>
<td>2</td>
<td>11</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>tsu</td>
<td>—</td>
<td>Setup Time, Input or Fdbk before Clk↑</td>
<td>3</td>
<td>—</td>
<td>4</td>
<td>—</td>
<td>7</td>
<td>—</td>
</tr>
<tr>
<td>th</td>
<td>—</td>
<td>Hold Time, Input or Fdbk after Clk↑</td>
<td>2</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>9</td>
<td>—</td>
</tr>
<tr>
<td>fmax³</td>
<td>A</td>
<td>Maximum Clock Frequency with External Feedback, 1/(tsu + tco)</td>
<td>83.3</td>
<td>—</td>
<td>66.7</td>
<td>—</td>
<td>45.0</td>
<td>33.3</td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>Maximum Clock Frequency with No Feedback</td>
<td>83.3</td>
<td>—</td>
<td>71.4</td>
<td>—</td>
<td>50.0</td>
<td>41.7</td>
</tr>
<tr>
<td>twh</td>
<td>—</td>
<td>Clock Pulse Duration, High</td>
<td>6</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>twl</td>
<td>—</td>
<td>Clock Pulse Duration, Low</td>
<td>6</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>ten/tdis</td>
<td>B,C</td>
<td>I or I/O to Output Enabled / Disabled</td>
<td>—</td>
<td>7.5</td>
<td>—</td>
<td>10</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>ten/tdis</td>
<td>B,C</td>
<td>OE to Output Enabled / Disabled</td>
<td>5</td>
<td>—</td>
<td>9</td>
<td>—</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tar/tap</td>
<td>A</td>
<td>Input or I/O to Async. Reset / Preset</td>
<td>9</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>tar/tapw</td>
<td></td>
<td>Async. Reset / Preset Pulse Duration</td>
<td>6</td>
<td>10</td>
<td>—</td>
<td>15</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td>tar/tapr</td>
<td></td>
<td>Async. Reset / Preset Recovery Time</td>
<td>7</td>
<td>10</td>
<td>—</td>
<td>12</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td>twp</td>
<td>—</td>
<td>Preload Pulse Duration</td>
<td>8</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>tsp</td>
<td>—</td>
<td>Preload Setup Time</td>
<td>5</td>
<td>10</td>
<td>—</td>
<td>15</td>
<td>25</td>
<td>—</td>
</tr>
<tr>
<td>thp</td>
<td>—</td>
<td>Preload Hold Time</td>
<td>5</td>
<td>10</td>
<td>—</td>
<td>15</td>
<td>25</td>
<td>—</td>
</tr>
</tbody>
</table>

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Descriptions** section.

### Capacitance (T_A = 25°C, f = 1.0 MHz)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MAXIMUM*</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_i</td>
<td>Input Capacitance</td>
<td>8</td>
<td>pF</td>
<td>V_{cc} = 5.0V, V_i = 2.0V</td>
</tr>
<tr>
<td>C_io</td>
<td>I/O Capacitance</td>
<td>10</td>
<td>pF</td>
<td>V_{cc} = 5.0V, V_{io} = 2.0V</td>
</tr>
</tbody>
</table>

*Characterized but not 100% tested.
Specifications **GAL20RA10**

### Switching Waveforms

#### Combinatorial Output

- **INPUT or I/O FEEDBACK**
  - **VALID INPUT**
  - **twp**

#### Registered Output

- **INPUT or I/O FEEDBACK**
  - **CLK**
  - **tsu**
  - **ths**

#### Input or I/O to Output Enable/Disable

- **INPUT or I/O FEEDBACK**
  - **OUTPUT**
  - **tdis**
  - **ten**

#### Clock Width

- **CLK**
  - **twh**
  - **twl**

#### Parallel Preload

- **PL**
  - **twp**
  - **tsp**
  - **thp**

#### Asynchronous Reset and Preset

- **OE**
  - **Q-OUTPUT OF REGISTER**
  - **tsw/ars**
  - **tsa/ars**

#### Asynchronous Reset and Preset Recovery

- **INPUT or I/O FEEDBACK**
  - **DRIVING AP or AR**
  - **CLK**
  - **taw/ars**
  - **tapw/arw**

---

ALL DEVICES DISCONTINUED

---

8
Specifications GAL20RA10

f\text{max} Descriptions

\[ f_{\text{max}} \text{ with External Feedback} = \frac{1}{(t_{su} + t_{co})} \]

\textit{Note: }f_{\text{max}} \text{ with external feedback is calculated from measured } t_{su} \text{ and } t_{co}.\]

Switching Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>-7/-10 2ns 10% - 90%  -15/-20/-30 3ns 10% - 90%</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load Conditions (see figure)</td>
<td>See Figure</td>
</tr>
</tbody>
</table>

3-state levels are measured 0.5V from steady-state active level.

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>R1</th>
<th>R2</th>
<th>CL</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>470Ω</td>
<td>390Ω</td>
<td>50pF</td>
</tr>
<tr>
<td>B</td>
<td>Infinity</td>
<td>390Ω</td>
<td>50pF</td>
</tr>
<tr>
<td></td>
<td>470Ω</td>
<td>390Ω</td>
<td>50pF</td>
</tr>
<tr>
<td>C</td>
<td>Infinity</td>
<td>390Ω</td>
<td>5pF</td>
</tr>
<tr>
<td></td>
<td>470Ω</td>
<td>390Ω</td>
<td>5pF</td>
</tr>
</tbody>
</table>

Note: f\text{max} \text{ with no feedback may be less than } 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.
Specifications **GAL20RA10**

### Electronic Signature

An electronic signature word is provided in every GAL20RA10 device. It contains 64 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

**NOTE:** The electronic signature bits if programmed to any value other than zero(0) will alter the checksum of the device.

### Security Cell

A security cell is provided in every GAL20RA10 device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

### Latch-Up Protection

GAL20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

### Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

### Input Buffers

GAL20RA10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance and present a much lighter load to the driving logic than traditional bipolar devices.

GAL20RA10 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/Os will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.
Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their \( Q \) outputs set low after a specified time (\( t_{\text{pr}} \), 1\( \mu \)s MAX). As a result, the state on the registered output pins (if they are enabled) will be high on power-up, because of the inverting buffer on the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown to the right. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20RA10. First, the Vcc rise must be monotonic. Second, the clock input must be at a static TTL level as shown in the diagram during power up. The registers will reset within a maximum of 1\( \mu \)s. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

**Input/Output Equivalent Schematics**

**Typical Input**

**Typical Output**

(Vref Typical = 3.2V)
GAL20RA10B-7/-10: Typical AC and DC Characteristic Diagrams

Normalized Tpd vs Vcc

Normalized Tco vs Vcc

Normalized Tsu vs Vcc

Normalized Tpd vs Temp

Normalized Tco vs Temp

Normalized Tsu vs Temp

Delta Tpd vs # of Outputs Switching

Delta Tco vs # of Outputs Switching

Delta Tpd vs Output Loading

Delta Tco vs Output Loading
GAL20RA10B-7/-10: Typical AC and DC Characteristic Diagrams

Vol vs Iol

Voh vs Ioh

Voh vs Ioh

Normalized Icc vs Vcc

Normalized Icc vs Temp

Normalized Icc vs Freq.

Delta Icc vs Vin (1 input)

Input Clamp (Vik)

Specifications GAL20RA10
GAL20RA10B-15/-20/-30: Typical AC and DC Characteristic Diagrams

Normalized Tpd vs Vcc

Normalized Tco vs Vcc

Normalized Tsu vs Vcc

Normalized Tpd vs Temp

Normalized Tco vs Temp

Normalized Tsu vs Temp

Delta Tpd vs # of Outputs Switching

Delta Tco vs # of Outputs Switching

Delta Tpd vs Output Loading

Delta Tco vs Output Loading
GAL20RA10B-15/-20/-30: Typical AC and DC Characteristic Diagrams

Vol vs Iol

Voh vs Ioh

Normalized Icc vs Vcc

Normalized Icc vs Temp

Normalized Icc vs Freq.

Delta Icc vs Vin (1 Input)

Input Clamp (Vik)

Specifications GAL20RA10