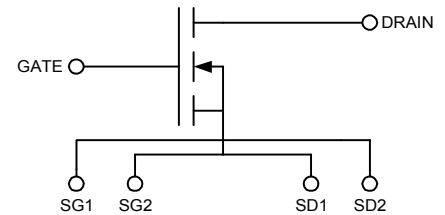
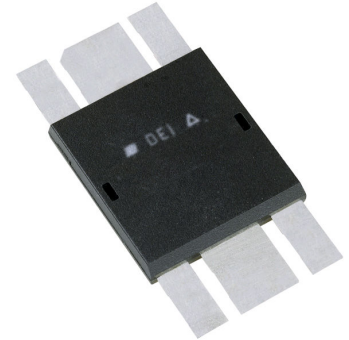


N-Channel Enhancement Mode
Low Q_g and R_g
High dv/dt
Nanosecond Switching
50MHz Maximum Frequency

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	1000	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	1000	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_c = 25^\circ\text{C}$	15	A
I_{DM}	$T_c = 25^\circ\text{C}$, pulse width limited by T_{JM}	90	A
I_{AR}	$T_c = 25^\circ\text{C}$	15	A
E_{AR}	$T_c = 25^\circ\text{C}$	1	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 0.2\Omega$	5	V/ns
	$I_S = 0$	>200	V/ns
P_{DC}		940	W
P_{DHS}	$T_c = 25^\circ\text{C}$ Derate $3.7\text{W}/^\circ\text{C}$ above 25°C	425	W
P_{DAMB}	$T_c = 25^\circ\text{C}$	4.5	W

Symbol	Test Conditions	Characteristic Values		
T _J = 25°C unless otherwise specified		min.	typ.	max.
V _{DSS}	V _{GS} = 0 V, I _D = 3 ma	1000		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 ma	4.0	5.4	6.0 V
I _{GSS}	V _{GS} = ±20 V _{DC} , V _{DS} = 0			±100 nA
I _{DSS}	V _{DS} = 0.8 V _{DSS} T _J = 25°C V _{GS} = 0 T _J = 125°C			50 μA 1 mA
R _{DS(on)}	V _{GS} = 15 V, I _D = 0.5I _{D25} Pulse test, t ≤ 300μS, duty cycle d ≤ 2%			1.00 Ω
R _{thJC} R _{thJHS}			0.3	0.13 °C/W °C/W
g _{fs}	V _{DS} = 15 V, I _D = 0.5I _{D25} , pulse test		11.3	13.0 S
T _J		-55		+150 °C
T _{JM}			150	°C
T _{stg}		-55		+150 °C
T _L	1.6mm (0.063 in) from case for 10 s		300	°C
Weight			3	g

$$\begin{aligned} V_{DSS} &= 1000\text{ V} \\ I_{D25} &= 15\text{ A} \\ R_{DS(on)} &\leq 1.0\ \Omega \\ P_{DC} &= 940\text{ W} \end{aligned}$$



Features

- Isolated Substrate
-High isolation voltage (>2500V)
- Excellent thermal transfer
- Increased temperature and power cycling capability
- IXYS advanced low Q_g process
- Low gate charge and capacitances
-Easier to drive
- Faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed switching at frequencies to 50MHz
- Easy to mount—no insulators needed
- High power density

Symbol	Test Conditions	Characteristic Values		
		min.	typ.	max.
(T _J = 25°C unless otherwise specified)				
R _G			0.2	Ω
C _{iss}			3000	pF
C _{oss}	V _{GS} = 0 V, V _{DS} = 0.8 V _{DSS(max)} , f = 1 MHz		93	pF
C _{rss}			9	pF
C _{stray}	Back Metal to any Pin		33	pF
T _{d(on)}			5	ns
T _{on}	V _{GS} = 15 V, V _{DS} = 0.8 V _{DSS} I _D = 0.5 I _{DM}		3	ns
T _{d(off)}	R _G = 0.2 Ω (External)		5	ns
T _{off}			8	ns
Q _{g(on)}			57	nC
Q _{gs}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} I _D = 0.5 I _{D25}		24	nC
Q _{gd}			22	nC

Source-Drain Diode
Characteristic Values

(T_J = 25°C unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.
I_S	V _{GS} = 0 V			15 A
I_{SM}	Repetitive; pulse width limited by T _{JM}			72 A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle ≤ 2%			1.4 V
T_{rr}				250 ns
Q_{RM}	I _F = I _S , -di/dt = 100A/μs, V _R = 100V		0.66	μC
I_{RM}			7.6	A

CAUTION: Operation at or above the Maximum Ratings values may impact device reliability or cause permanent damage to the device.

Information in this document is believed to be accurate and reliable. IXYS RF reserves the right to make changes to information published in this document at any time and without notice.

For detailed device mounting and installation instructions, see the “*Device Installation & Mounting Instructions*” technical note on the IXYS RF web site at;

http://www.ixysrf.com/pdf/switch_mode/appnotes/7de_series_mosfet_installation_instructions.pdf

IXYS RF reserves the right to change limits, test conditions and dimensions.

IXYS RF MOSFETS are covered by one or more of the following U.S. patents:

4,835,592	4,860,072	4,881,106	4,891,686	4,931,844	5,017,508
5,034,796	5,049,961	5,063,307	5,187,117	5,237,481	5,486,715
5,381,025	5,640,045				

Fig. 1

Typical Transfer Characteristics

$V_{DS} = 50V$

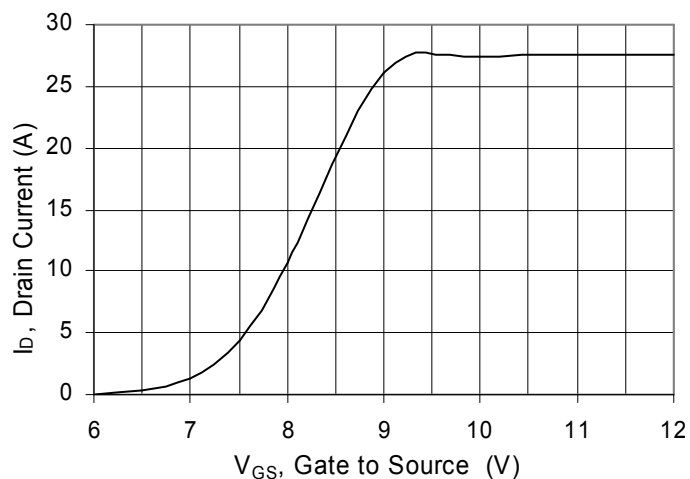


Fig. 2

Typical Output Characteristics

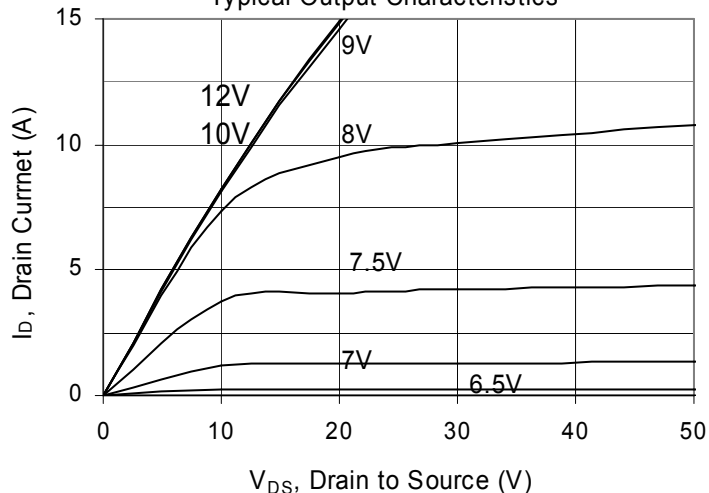


Fig. 3

Gate Charge vs. Gate to Source Voltage

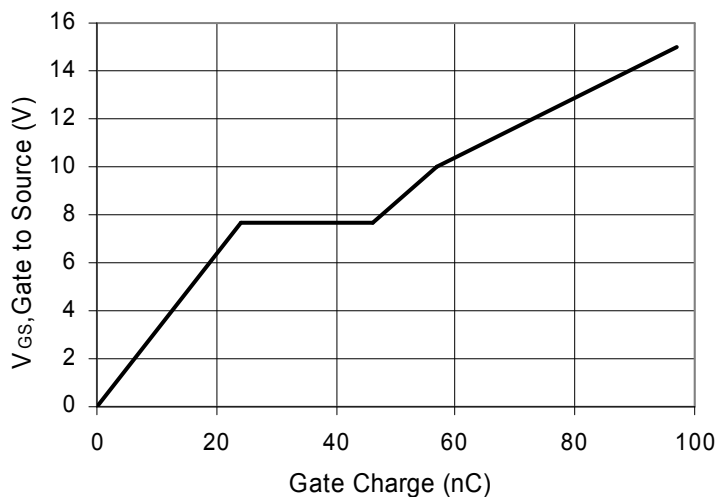


Fig. 4

Extended Typical Output Characteristics

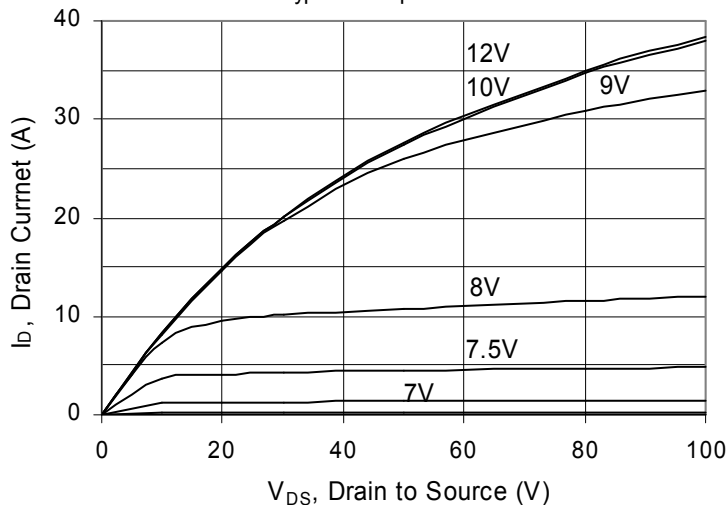


Fig. 5

Capacitance vs. V_{DS}

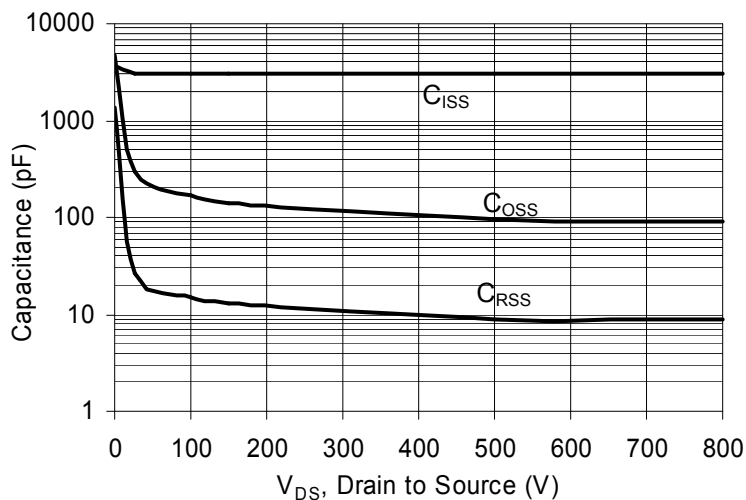


Fig. 6

Maximum Transient Thermal Impedance

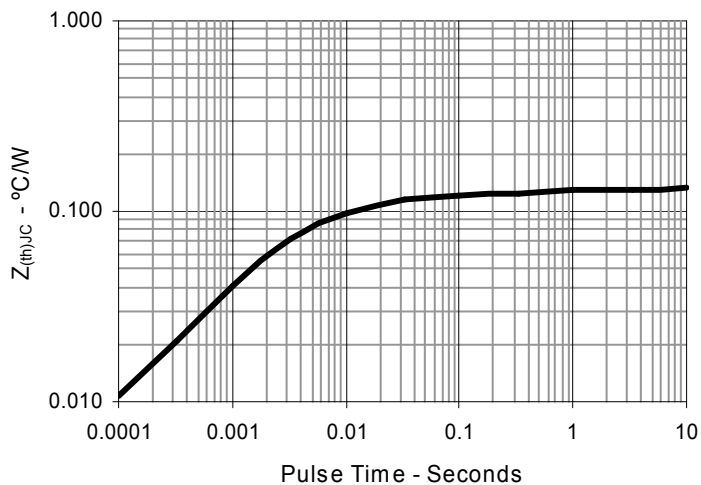


Fig. 7

Transfer Curve vs. Temperature
 $V_{DS} = 50V$

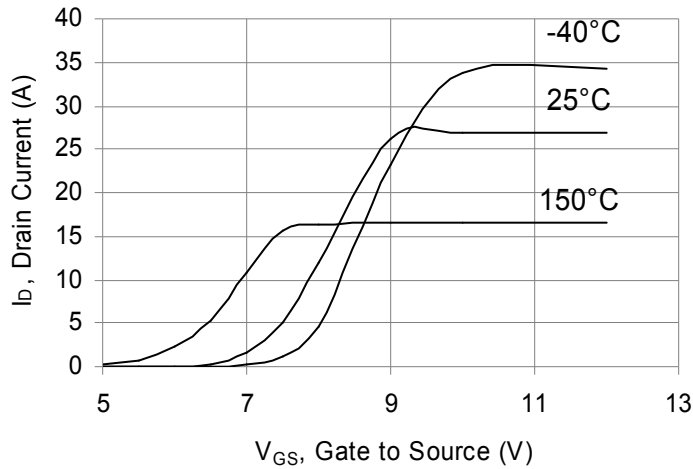


Fig. 8

Normalized $V_{GS(TH)}$ vs. Temperature
 $I_D = 1mA$

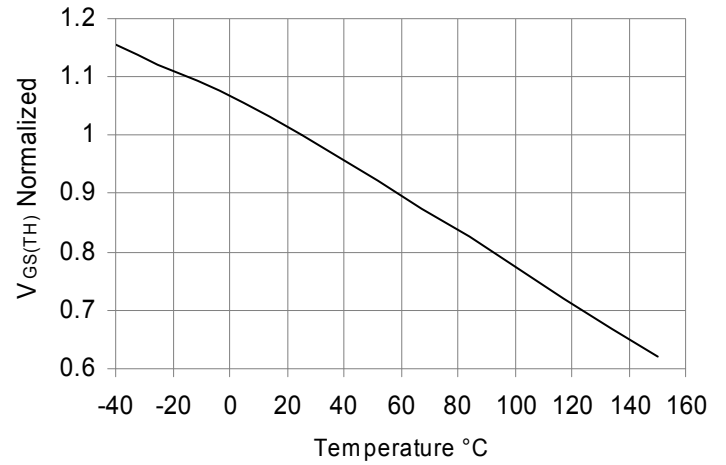


Fig. 9

Normalized G_{FS} vs. Temperature
 $I_D = 7.5A$ $V_{DS} = 50V$

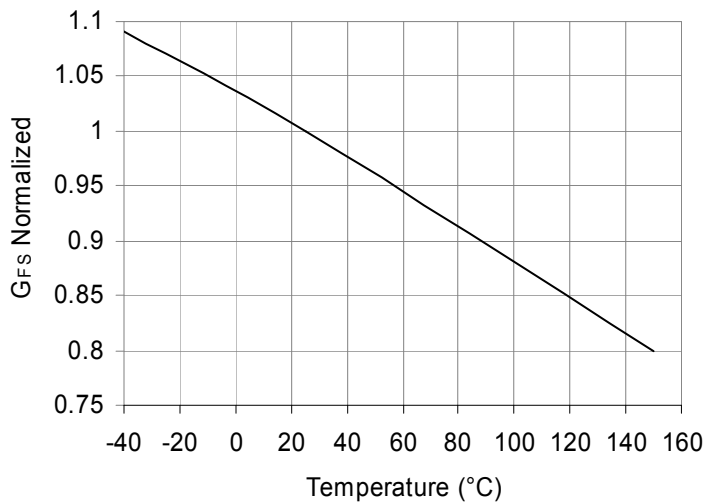


Fig. 10

Normalized $R_{DS(ON)}$ vs. Temperature
 $I_D = 7.5A$ $V_{GS} = 10V$

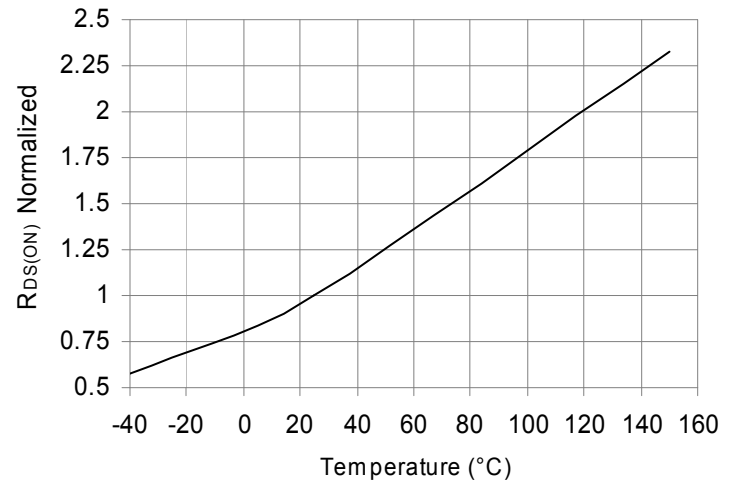
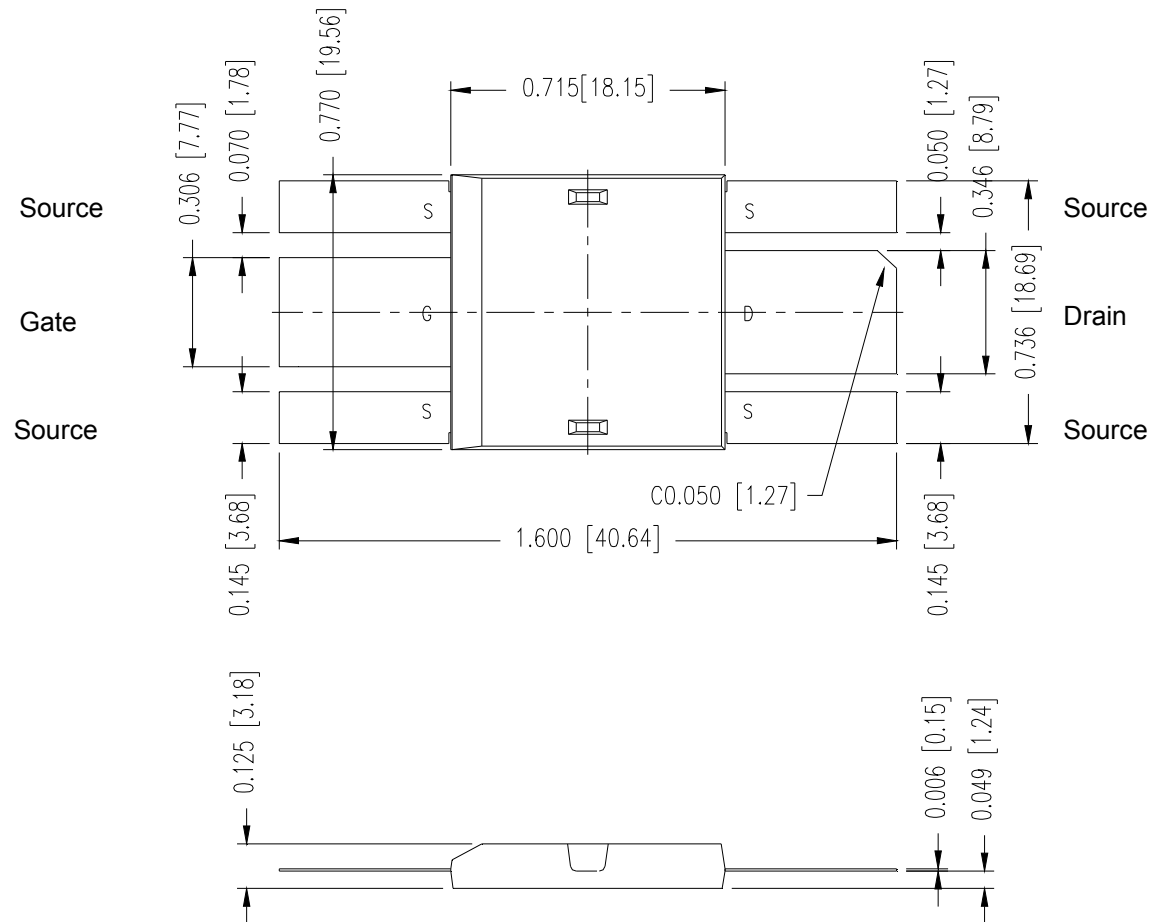


Fig. 11 Package Drawing



102N15A DE-SERIES SPICE Model

The DE-SERIES SPICE Model is illustrated in Figure 12. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms L_G , L_S and L_D . R_d is the $R_{DS(ON)}$ of the device, R_{ds} is the resistive leakage term. The output capacitance, C_{OSS} , and reverse transfer capacitance, C_{RSS} are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via R_{on} and R_{off} .

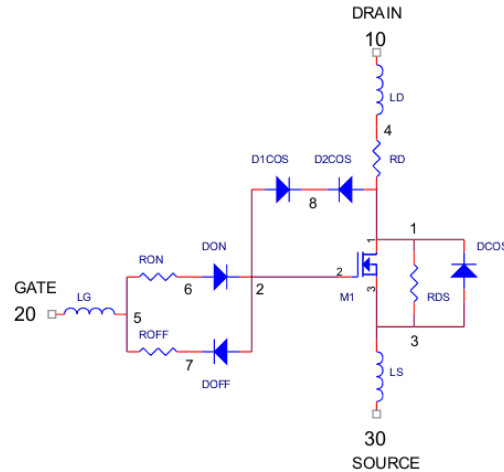


Figure 12 DE-SERIES SPICE Model

Net List:

```
.SUBCKT 102N15A 10 20 30
* TERMINALS: D G S
* 1000 Volt 15 Amp 1 ohm N-Channel Power MOSFET
* REV.A 02-10-12
M1 1 2 3 3 DMOS L=1U W=1U
RON 5 6 0.2
DON 6 2 D1
ROFF 5 7 .1
DOF 2 7 D1
D1CRS 2 8 D2
D2CRS 1 8 D2
CGS 2 3 3.0N
RD 4 1 1.0
DCOS 3 1 D3
RDS 1 3 5.0MEG
LS 3 30 .5N
LD 10 4 1N
LG 20 5 1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=3.8)
.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)
.MODEL D2 D (IS=.5F CJO=400P BV=1000 M=.4 VJ=.6 TT=400N RS=10M)
.MODEL D3 D (IS=.5F CJO=900P BV=1000 M=.3 VJ=.4 TT=400N RS=10M)
.ENDS
```

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