15-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

July 2019

GENERAL DESCRIPTION

The IS31SE5111 is an ultra-low power, fully integrated 15-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric such as glass or plastic. On-chip calibration logic continuously monitors the environment and automatically adjusts on-and-off threshold levels to prevent false sensor activation.

The IS31SE5111 supports the 400kHz I²C serial bus data protocol and includes a field programmable slave address. An INTB is generated when a button event (touched or released) occurs, triggered and cleared condition could be configured by setting the interrupt register.

Many peripheral functions are also embedded in the chip such as UART, EUART with LIN capability, one I2C master/slave and two I2C pure slave controllers, one SPI master/slave controller, PWMs, GPIOs, etc. Unused touch key pins can be programmed for selected I/O function. User can refer to the Technical Reference Manual, TRM-5111_R1 for detail.

IS31SE5111 is available in TSSOP-16 and TSSOP-24 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +105°C.

FEATURES

- Fifteen sensors capacitive touch controller with readable key value through shared GPIO
- Individual sensitivity threshold setting for each key
- Optional multiple-key function
- Press and hold function
- Automatic calibration
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- 400kHz fast-mode I²C interface
- One SPI master/slave controllers
- One 8051 UART
- One full-duplex LIN-capable EUART2
- Operating temperature is -40°C ~ +105°C
- TSSOP-16 and TSSOP-24 package

APPLICATIONS

- Home appliance control keys
- Industrial touch keys

TYPICAL APPLICATION CIRCUIT (TSSOP-24)

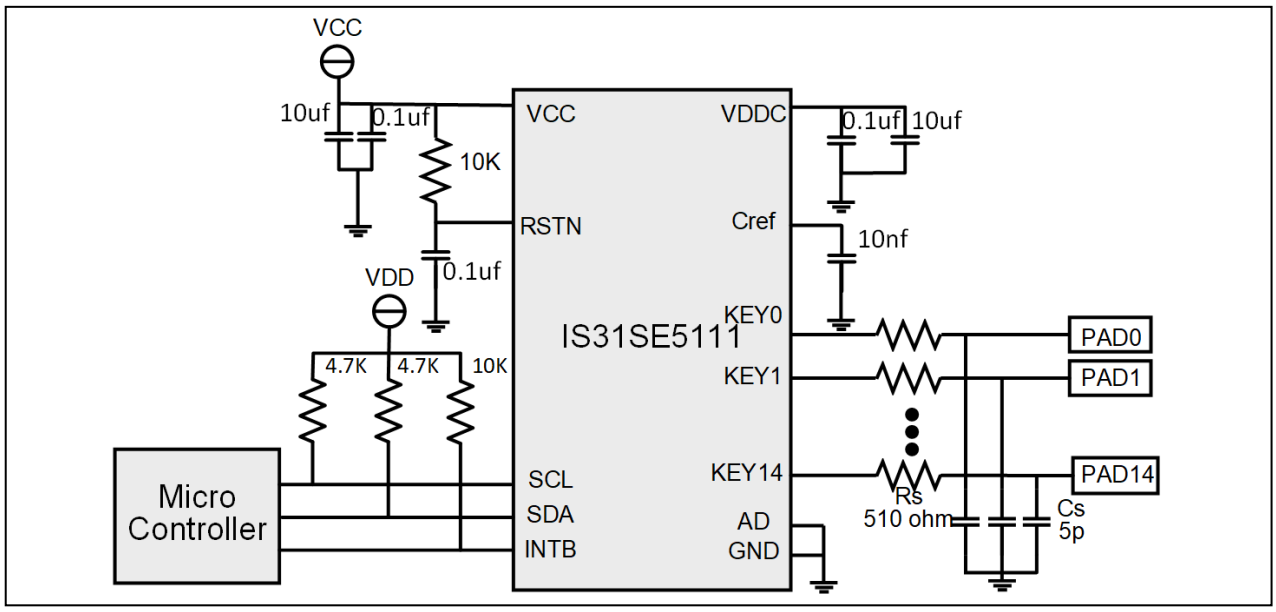
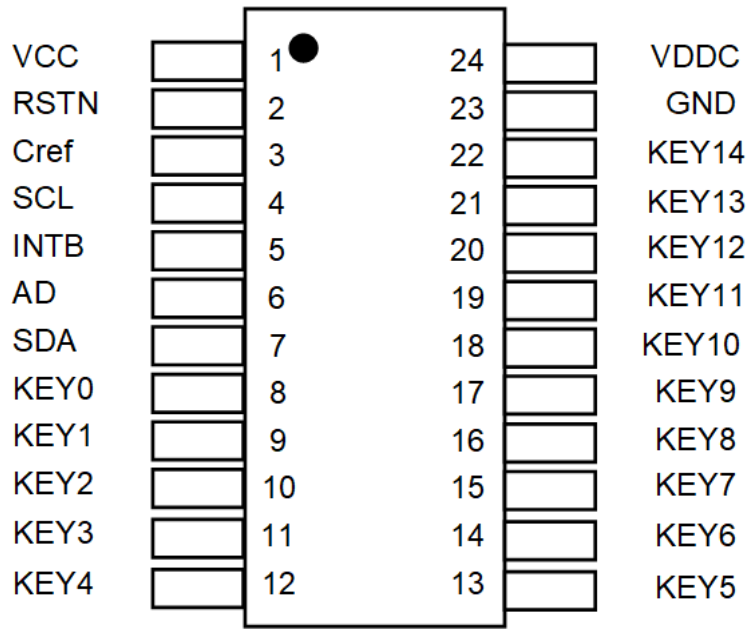


Figure 1 Typical Application Circuit (TSSOP-24)

Note 1: The IC should be placed far away from the noise points in order to prevent the EMI.

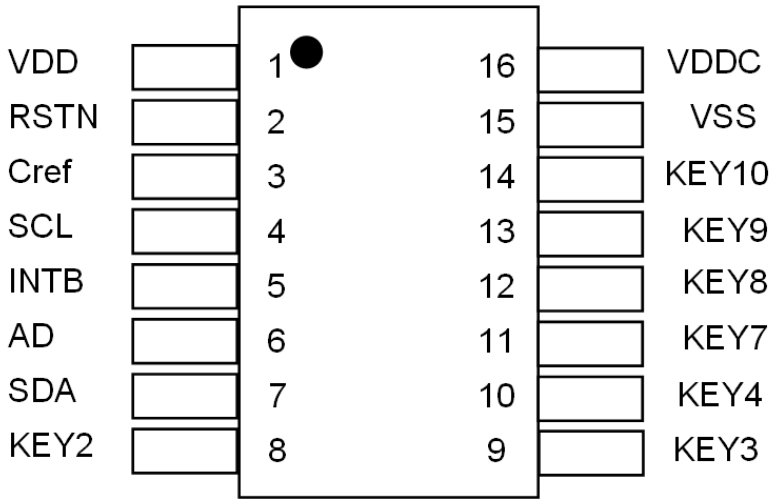
Note 2: The R_S and C_S should place as close to IC as possible to reduce EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
TSSOP-24	

PIN DESCRIPTION

No.	Pin	Description
1	VCC	Power supply.
2	RSTN	Reset Low Active.
3	Cref	External Capacitor.
4	SCL	I2C serial clock.
5	INTB	Interrupt output, active low.
6	AD	I2C address setting.
7	SDA	I2C serial data
8 – 22	KEY0 – KEY14	Input sense channel 0 - 14
23	GND	Ground.
24	VDDC	Typical decoupling capacitors of 0.1μF and 10μF should be connected between VDDC and GND.

Package	Pin Configuration (Top View)
TSSOP-16	

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1	VCC	Power supply.
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3	Cref	External Capacitor.
4	SCL	I2C serial clock.
5	INTB	Interrupt output, active low.
6	AD	I2C address setting.
7	SDA	I2C serial data
8-10	KEY2 – KEY4	Input sense channel 2 - 4
11-14	KEY7 – KEY10	Input sense channel 7 - 10
15	GND	Ground.
16	VDDC	Typical decoupling capacitors of 0.1μF and 10μF should be connected between VDDC and GND.

ORDERING INFORMATION

Industrial Range: -40°C to +105°C

Order Part No.	Package	QTY
IS31SE5111A-ZNLS3-TR IS31SE5111A-ZNLS3	TSSOP-24, Lead-free	2500/Reel 60/Tube
IS31SE5111C-ZNLS3-TR IS31SE5111C-ZNLS3	TSSOP-16, Lead-free	2500/Reel 96/Tube

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +105°C
Junction Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}(TSSOP-24) θ_{JA}(TSSOP-16)	 73.3°C/W 50.2°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.7V ~ 5.5V, unless otherwise noted. Typical value are T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC} = 5.5V		100		μA
I_{SD}	Shutdown current	V_{CC} = 5.5V		15		μA
ΔC_S	Minimum detectable capacitance	C_S = 5pF (Note 4)		0.2		pF
Logic Electrical Characteristics						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V (Note 4)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC} (Note 4)		5		nA

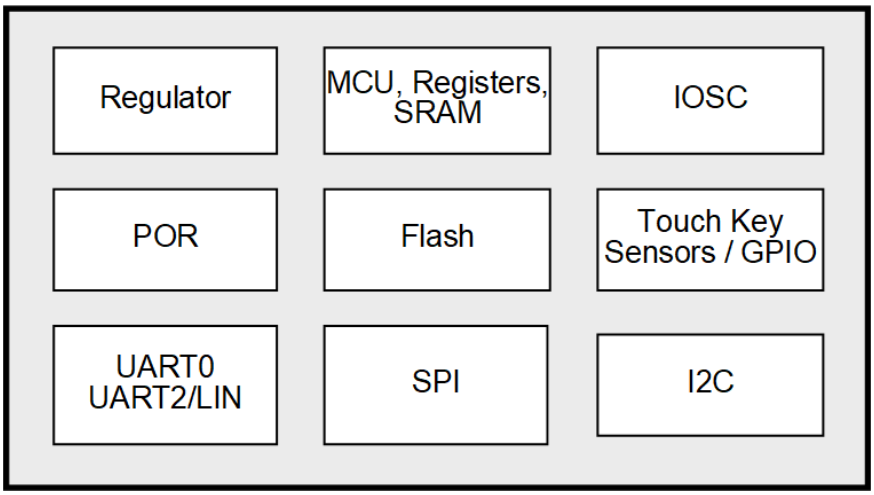
DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 5)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 5)		20+0.1C_b	300	ns

Note 4: Guaranteed by design.

Note 5: C_b = total capacitance of one bus line in pF. $I_{SINK} \le 6mA$. t_R and t_F measured between 0.3 × V_{CC} and 0.7 × V_{CC}.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31SE5111 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31SE5111 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address

Bit	A7:A3	A2:A1	A0
Value	01111	AD	1/0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31SE5111.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31SE5111's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31SE5111 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5111, the register address byte is sent, most significant bit first. IS31SE5111 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31SE5111 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31SE5111 address with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31SE5111 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31SE5111 to the master (Figure 5).

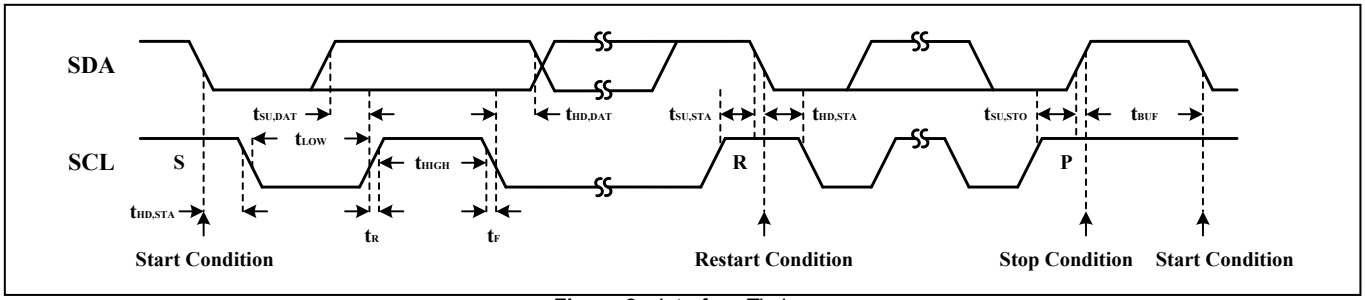


Figure 2 Interface Timing

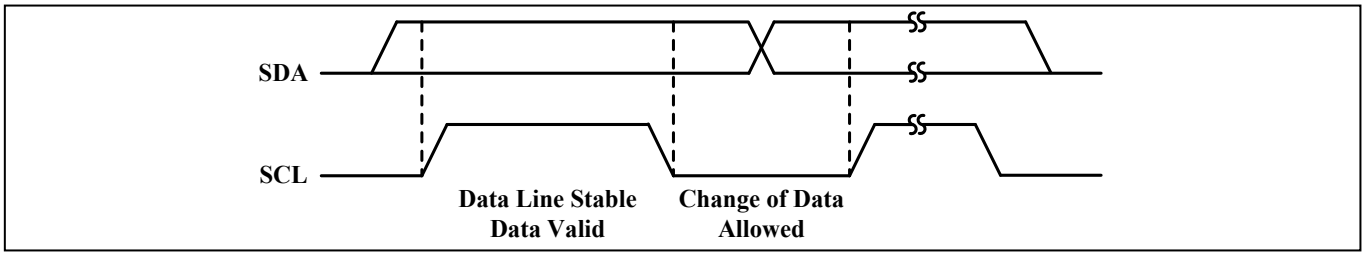


Figure 3 Bit Transfer

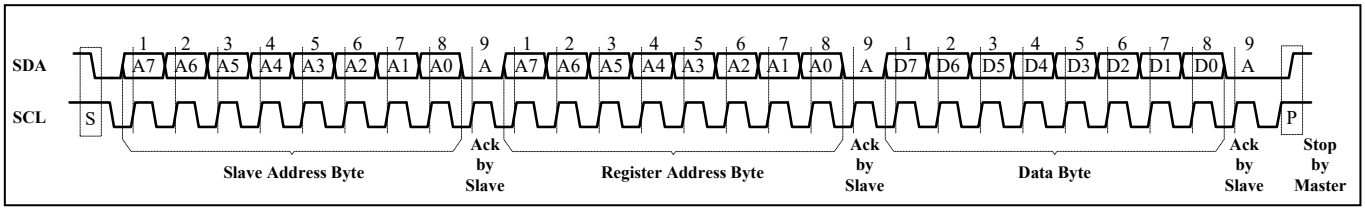


Figure 4 Writing to IS31SE5111

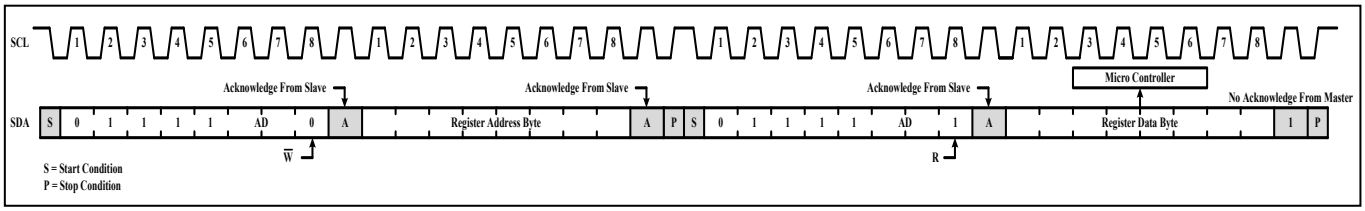
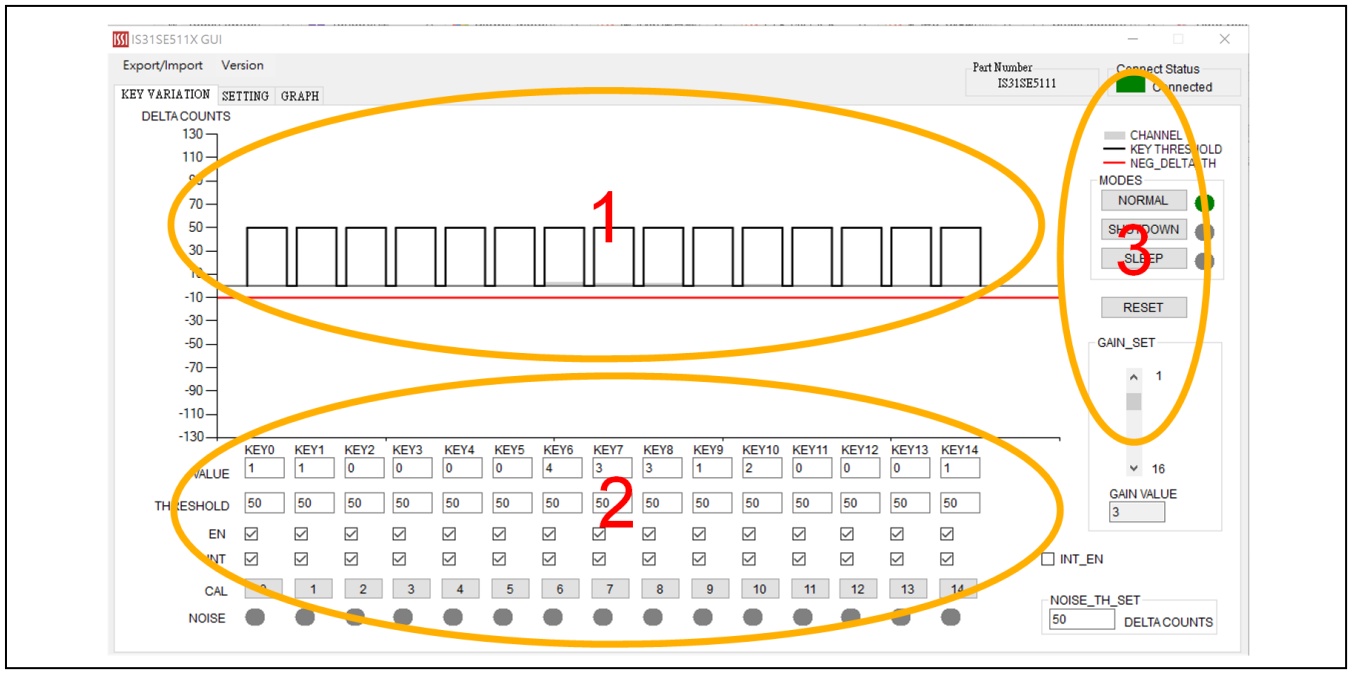


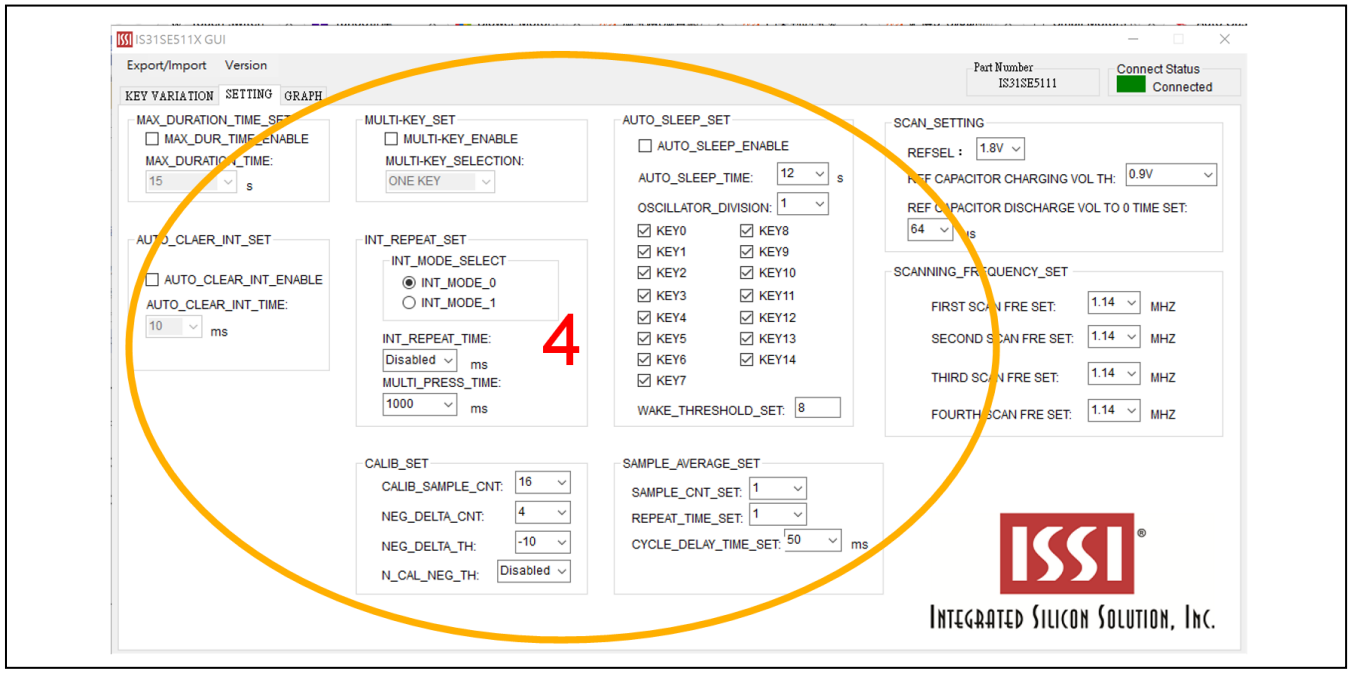
Figure 5 Reading from IS31SE5111

IS31SE5111 GUI

IS31SE5111 GUI is a windows-based Integrated Design Environment (IDE). User can use it to develop touch key applications without firmware coding. With the GUI user can design the touch key system easily. With the GUI you can:

1. Monitor the Key value
2. Set touch threshold and enable keys
3. Switch the operating modes
4. Tune System parameters





FUNCTIONAL DEFINITOIN of KEY PERIPHRALS

The IS31SE5111 is a capacitive touch-sensing controller with MCU. The MCU is based on 1-T 8051 core. Embedded in the MCU core are also a full-duplex UART port, an enhanced EUART port with LIN capability, one I2C master/slave and two I2C pure slave controllers, one SPI marter/slave controller, up to 20 GPIO pins

GPIO

Each GPIO is controlled by two registers. One is IOCFGPx.y (I/O Configuration) and the other is MFCFGPx.y (Multifunction Configuration).

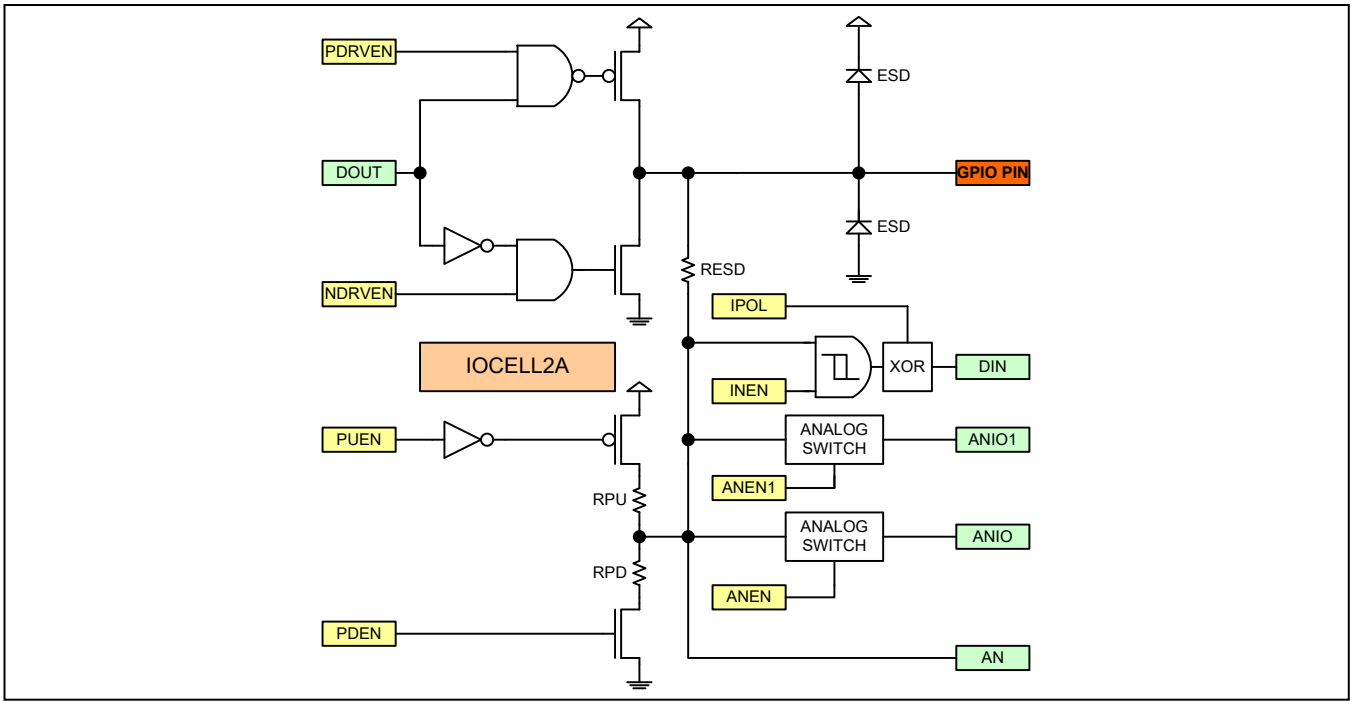


Figure 6 I/O Configuration

Figure 6 shows that there are 7 control bits for the IOCFGPx.y register, and these registers are located at XFR 0xA040 – 0xA047 for P0.0 to P0.7, 0xA048 – 0xA04F for P1.0 to P1.7, 0xA060 – 0xA063 for P2.0 to P2.3.

GPIO Port Multi-Function

Each signal pin is multi-functional and the pin configuration is specified by MFCFGP register. There are 7 control bits for the MFCFGPx.y register, and these registers are located at XFR 0xA050 – 0xA057 for P0.0 to P0.7, 0xA058 – 0xA05F for P1.0 to P1.7, and 0xA070 – 0xA073 for P2.0 to P2.3

The touch keys and GPIO mapping table are as follows:

Touch KEY No.	GPIO Port
KEY0	P0.5
KEY1	P0.6
KEY2	P0.7
KEY3	P1.0
KEY4	P1.1
KEY5	P1.2
KEY6	P1.3
KEY7	P1.4

KEY8	P1.5
KEY9	P1.6
KEY10	P1.7
KEY11	P2.0
KEY12	P2.1
KEY13	P2.2
KEY14	P2.3

Serial Port – UART0

UART0 is full duplex and fully compatible with the standard 8052 UART. The receive path of UART0 is double-buffered that can commence reception of second byte before previously received byte is read from the receive register. Writing to SBUF0 loads the transmit register while reading SBUF0, reads a physically separate receive register. The UART0 can operate in four modes.

The touch keys related function and UART0 pins mapping table are as follows:

Touch KEY No.	GPIO Port
KEY3	P1.0/RX0
KEY4	P1.1/TX0

To use UART0 function, IOCFGP1.0, IOCFGP1.1, MFCFGP1.0, and MFCFGP1.1 should be defined in advance to enable UART0.

MFCFGP1.0 (0xA058h) GPIO P1.0 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	RXD0EN	-	-	-	-	GPIOEN
WR	-	-	RXD0EN	-	-	-	-	GPIOEN

RXD0EN RXD0EN=1 uses this pin as RXD input for UART0

GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

MFCFGP1.1 (0xA059h) GPIO P1.1 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	TXD0EN	-	-	-	-	GPIOEN
WR	-	-	TXD0EN	-	-	-	-	GPIOEN

TXD0EN TXD0EN=1 uses this pin as TXD output for UART0

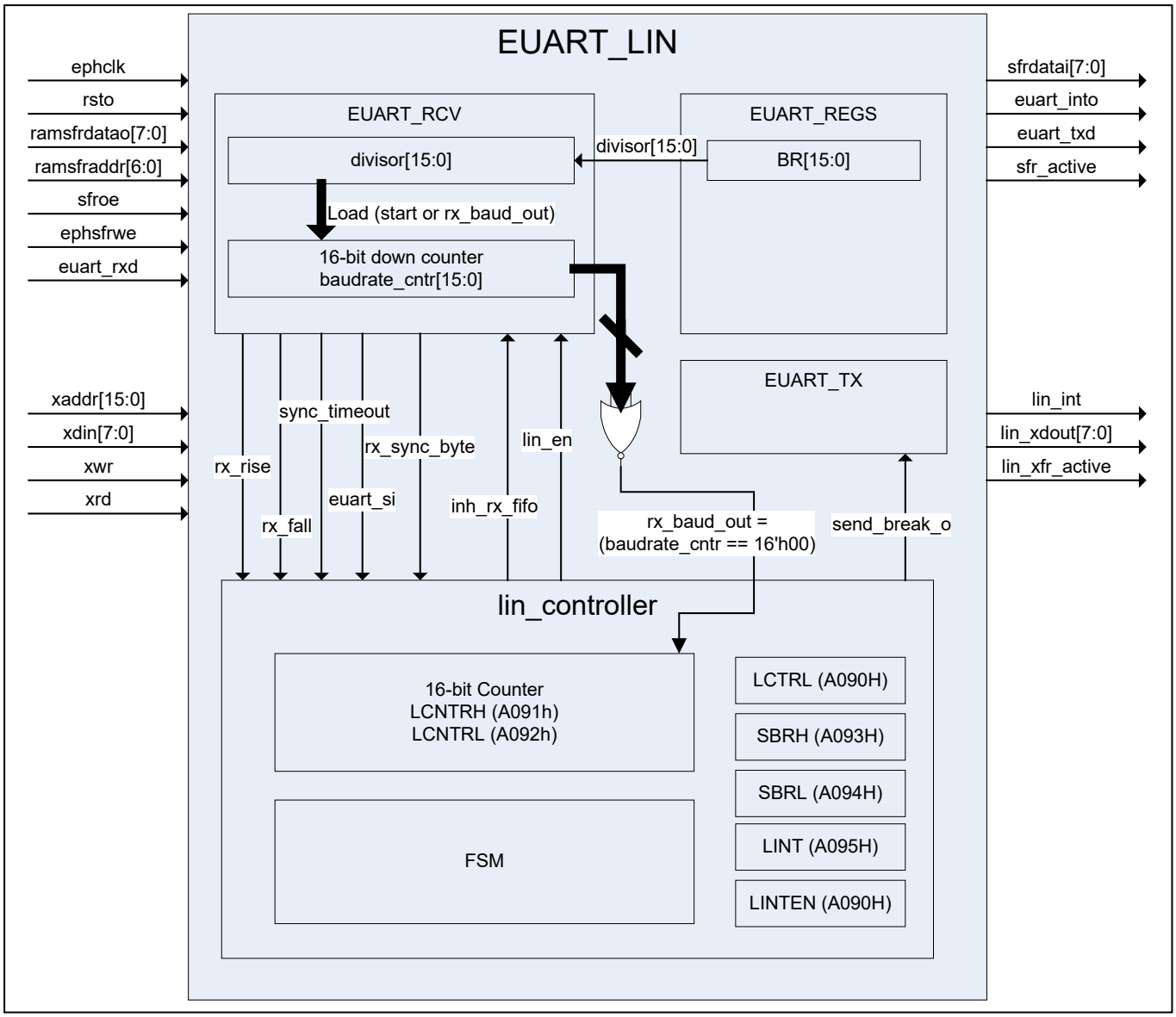
GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

To enable UART0, four GPIO related configuration registers, the setting is as follows:

Register Name	Value
IOCFGP1.0	0xA0
IOCFGP1.1	0x06
MFCFGP1.0	0x20 (input only)
MFCFGP1.1	0x20 (output pin)

EUART2 with LIN Controller (EUART2)

LIN-capable 16550-like EUART2 is an enhanced UART controller (EUART) with separate transmit and receive FIFO. Both transmit and receive FIFO are 15-byte deep and can be parameterized for interrupt triggering. The addition of FIFO significantly reduces the CPU load to handle high-speed serial interface. Transmit FIFO and receive FIFO have respective interrupt trigger levels that can be set based on optimal CPU performance adjustment. EUART2 also has dedicated 16-bit Baud Rate generator and thus provides accurate baud rate under wide range of system clock frequency. EUART2 also provides LIN extensions that incorporate message handling and baud-rate synchronization. The block diagram of EUART2 is shown in the following.



EUART2 can be configured to add LIN capability. The major enhancement of LIN includes master/slave configurations, auto baud-rate synchronization, and frame-based protocol with header. Under LIN extension mode, all EUART2 registers and functions are still effective and operational. LIN is a single-wire bus and it requires external components to combine RX and TX signals externally. LIN is frame based and consists of message protocols with master/slave configurations.

The touch keys related function and UART2/LIN pins mapping table are as follows:

Touch KEY No.	GPIO Port
KEY3	P1.0/RX2
KEY4	P1.1/TX2

To use UART0 function, IOCFGP1.0, IOCFGP1.1, MFCFGP1.0, and MFCFGP1.1 should be defined in advance to enable UART0.

MFCFGP1.0 (0xA058h) GPIO P1.0 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	RXD2EN	-	-	-	-	-	GPIOEN
WR	-	RXD2EN	-	-	-	-	-	GPIOEN

RXD2EN RXD2EN=1 use this pin as RXD input for EUART2

GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

MFCFGP1.1 (0xA059h) GPIO P1.1 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	TXD2EN	-	-	-	-	-	GPIOEN
WR	-	TXD2EN	-	-	-	-	-	GPIOEN

TXD2EN TXD2EN=1 uses this pin as TXD output for EUART2

GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

To enable EUART2/LIN, four GPIO related configuration registers, the setting is as follows:

Register Name	Value
IOCFGP1.0	0xA0
IOCFGP1.1	0x06
MFCFGP1.0	0x40 (input only)
MFCFGP1.1	0x40 (output pin)

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an enhanced synchronous serial hardware which is compatible with Motorola's SPI specifications. The SPI Controller includes 4-byte FIFO for both transmit and receive. SPI Interface uses Master-Out-Slave-In (MOSI), Master-In-Slave-Out (MISO), Serial Clock (SCK) and Slave Select (SSN) for interface. SSN is low active and only meaningful in slave mode.

The touch keys related function and SPI pins mapping table are as follows:

Touch KEY No.	GPIO Port
SDA, KEY1, KEY7	P0.4, P0.6, P1.4 (MISO)
INTB, KEY3, KEY9	P0.2, P1.0, P1.6 (MOSI)
SCL, KEY0, KEY2, KEY8	P0.1, P0.5, P0.7, P1.5 (SCK)
AD, KEY4	P0.3, P1.1 (SSN)

PWM0/PWM1 Controller

PWM0/1 controller provides an 8-bit programmable duty cycle output. The counting clock of PWM0/1 is programmable and the base frequency of the PWM0/1 is just the counting clock divided by 256. The duty cycle setting is always double buffered. PWM0 output is connected to only one of the pins: P04, P06, P12, P17 or P23. PWM1 output is connected to only one of the pins: P05, P13, P15, P16 or P22.

The frequency of the counting clock is SYSCLK/CS[7-5]/(CS[4-0]+1). The frequency of the PWM clock is counting clock divided by 256. Assuming SYSCLK is 16MHz, and we want the PWM base frequency of 120Hz. First, we get 16MHz/120Hz/256 = 520.8. Where 520.8 needs to be separated as two multiplicands of CS[7-5] and CS[4-0]. Then by trial and error we can select CS[7-5] = 100, and CS[4-0] = 0x0F. This gives 16MHz/256/32/(15+1) = 122Hz.

PWM0DTY registers define the PWM0 duty cycle. The maximum duty cycle is 254/255. PWM0DTY is always double buffered and is loaded to duty cycle comparator when the current counting cycle is completed.

The touch keys related function and PWM0/PWM1 pins mapping table are as follows:

Touch KEY No.	GPIO Port
SDA, KEY1, KEY5, KEY10, KEY14	P0.4, P0.6, P1.2, P1.7, P2.3 (PWM0)
KEY0, KEY6, KEY8, KEY9, KEY13	P0.5, P1.3, P1.5, P1.6, P2.2 (PWM1)

Table 2 Register Function

Address	Name	Function	R/W	Table	Default
00h	Main Control Register	Controls general power states and power dissipation	W	3	0000 0000
01h	INT Configuration Register	Interrupt configuration	R/W	4	
02h	Key Status Register 1	Key0~Key7 status bits	R	5-1	
03h	Key Status Register 2	Key8~Key14 status bits		5-2	
04h	Interrupt Enable Register 1	Key0~key7 Enables Interrupts associated with capacitive touch sensor inputs	R/W	6-1	1111 1111
05h	Interrupt Enable Register 2	Key8~key14 Enables Interrupts associated with capacitive touch sensor inputs		6-2	
06h	Key Enable Register 1	Key0~key7 sets the channels enable		7-1	
07h	Key Enable Register 2	Key8~key14 sets the channels enable		7-2	
08h	Multiple Touch Key Configure Register	Multiple touch key function setting		8	0000 0000
09h	Auto-Clean Interrupt Register	Set auto-clean interrupt time and enable		9	
0Ah	Interrupt Repeat Time Register	Set repeat cycle for pressing key interrupt		10	0000 1111
0Bh	Auto-SLEEP Mode Register	Set auto enter SLEEP Mode time		11	
0Ch	Exit SLEEP Mode Register 1	Set press Key0~Key7 to exit SLEEP Mode		12-1	1111 1111
0Dh	Exit SLEEP Mode Register 2	Set press Key8~Key14 to exit SLEEP Mode		12-2	
0Eh	Gain and Press Time Setting Register	Set gain and pressing trigger time		13	0010 1111
0Fh	Key Touch Sampling Configure Register	Set sampling times and cycle time		14	0
10h	Calibration Configure Register	Set auto-calibration cycle and negative value trigger setting		15	0011 0000
11h	Key Calibration Register 1	Key0~Key7 compel calibrate enable set		16-1	0

12h	Key Calibration Register 2	Key8~Key14 compel calibrate enable set		16-2	
13h	Noise Threshold Register	Set noise threshold value		17	0011 0010
14h	Noise Indication Register 1	Key0~Key7 noise indication		18-1	0
15h	Noise Indication Register 2	Key8~key14 noise indication		18-2	
17h	Negative Threshold Register	Set negative threshold and compel calibration threshold		20	0000 1000
18h	Wake Up Threshold Register	Set wake up threshold		21	0000 1000
19h	Scan Voltage Register	Set scanning voltage		19	0
20h~2Fh	Variation Value Register	Keys value setting	R/W	22	0
30h~3Fh	Threshold Set Register	Keys threshold setting		23	0011 0010
40h,42h … 5Ah,5Ch	Calibration Low Bit Register	Internal calibration low 8-bit for KEY0~KEY14	R	24-1	0000 0000
41h,43h … 5Bh,5Dh	Calibration High Bit Register	Internal calibration high 8-bit for KEY0~KEY14		24-2	

Table 3 00h Main Control Register (Write Only)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	SR	-	SDM	SP	-	-
Default	0	0	0	0	0	000

SR System Reset

0 Normal Mode

1 System Reset

SDM Shutdown Mode

0 Normal Mode

1 Shutdown Mode

SP Sleep Mode

0 Normal Mode

1 SLEEP Mode

Table 4 01h Interrupt Configuration Register

Bit	D7:D4	D3	D2	D1	D0
Name	-	MDEN	INM	INE	-
Default	0000	0	0	0	0

MDEN Maximum Duration Time Enable

0 Disable

1 Enable

Maximum press function is used to prevent key pressing all the time by accident. When maximum press function is enabled, once key keep pressing at programmed time the key calibration value will be updated.

INM Interrupt Mode

0 Interrupt Mode 0(Touch key trigger once interrupt)

1 Interrupt Mode 1(Touch key trigger repeated interrupt)

INM bit sets interrupt time for once or multiple. Multiple interrupt is used for key pressing detection.

INE Interrupt Function Enable

0 Enable

1 Disable

Table 5-1 02h Key Status Register 1 (Read only)

Bit	D7:D0
Name	KS[7:1]
Default	0000 0000

Table 5-2 03h Key Status Register 2 (Read only)

Bit	D6:D0
Name	KS[14:8]
Default	000 0000

KSx	Key0~Key14 Status
0	No action
1	Press or release keys

If the value of KSx is detected over programmed threshold, the corresponding bit will be set to "1".

Table 6-1 04h Interrupt Enable Register 1

Bit	D7:D0
Name	KINT[7:1]
Default	1111 1111

Table 6-2 05h Interrupt Enable Register 2

Bit	D6:D0
Name	KINT[14:8]
Default	111 1111

The Interrupt Enable Register determines whether a sensor pad touch or release (if enabled) causes the interrupt pin to be asserted.

KINTx	Key Interrupt Enable
0	Disable
1	Enable

The default value for Interrupt Enable Registers is interrupt enable. Only set INE bit of Interrupt Configuration Register (01h) to "0", INTB pin will generate interrupt signal.

Table 7-1 06h Key Enable Register 1

Bit	D7:D0
Name	KEN[7:1]
Default	1111 1111

Table 7-2 07h Key Enable Register 2

Bit	D6:D0
Name	KEN[15:8]
Default	111 1111

KENx	Touch Key Enable Setting
0	Disable
1	Enable

Table 8 08h Multiple Touch Key Configure Register

Bit	D7:D3	D2	D1:D0
Name	-	MKEN	MTK
Default	0000 0	0	00

MKEN	Multi- Key Enable
0	Disable
1	Enable

MTK	Multi -Key Selection
01	Allow one key triggered at same time
10	Allow two keys triggered at same time
11	Allow three keys triggered at same time

Table 9 09h Auto-Clear Interrupt Register

Bit	D7:D4	D3	D2:D0
Name	-	ACEN	ACT
Default	0000	0	000

ACEN	Auto-Clear Interrupt Enable
0	Disable
1	Enable

ACT	Auto-Clear Interrupt Time
000	10ms
001	20ms
010	30ms
011	40ms
100	50ms
101	100ms
110	150ms
111	200ms

When ACEN=0, the INTB will keep low until MCU read 02h and 03h registers. When ACEN=1, if MCU don't read 02h and 03h registers within programmed time (ACT=10ms~200ms), INTB pin will be release automatically.

Table 10 0Ah Interrupt Repeat Time Register

Bit	D7:D4	D3:D0
Name	INTRT	MPT
Default	0000	0000

INTRT	Interrupt Repeat Time
0000	Close
0001	50ms
0010	100ms
0011	150ms
0100	200ms
0101	250ms
0110	300ms
0111	350ms
1000	400ms
1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

MPT	Multi-key Press Time
0000	Close
0001	50ms
0010	100ms
0011	150ms
0100	200ms
0101	250ms
0110	300ms
0111	350ms
1000	400ms
1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

When set the INM as 1 and several keys are pressed, it will generate the second interrupt until M_PRESS_TIME after the first interrupt. Then wait for INT_RPT_TIME to trigger the third interrupt. After all of these if the keys are still pressing, wait for INT_RPT_TIME to trigger others interrupt until keys release.

Table 11 0Bh Auto-SLEEP Mode Register

Bit	D7	D6:D4	D3:D0
Name	ASEN	OSCD	AST
Default	0	000	0000

ASEN	Auto-SLEEP Enable
0	Disable
1	Enable

OSCD	Auto-Sleep Oscillator Division
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

AST	Auto-SLEEP Time
0000	0.5s
0001	1s
0010	1.5s
0011	2s
0100	2.5s
0101	3s
0110	3.5s
0111	4s
1000	4.5s
1001	5s
1010	6s
1011	7s
1100	8s
1101	9s
1110	10s

When ASEN=1 and no actions on touch key and I2C interface, the IC will enter into SLEEP Mode after programmed time (AST).

Table 12-1 0Ch Exit SLEEP Mode Register 1

Bit	D7:D1
Name	ESMEN[7:1]
Default	0000 000

Table 12-2 0Dh Exit SLEEP Mode Register 2

Bit	D7:D0
Name	ESMEN[15:8]
Default	0000 0000

ESMENx	Exit Sleep Mode Enable
0	Touch key can't trigger exiting SLEEP Mode
1	Touch key trigger exiting SLEEP Mode

When IC is in Normal Mode and ASEN=1, set ESMENx=1 will exit from SLEEP Mode by pressing the corresponding key.

Table 13 0Eh Gain and Press Time Setting Register

Bit	D7:D4	D3:D0
Name	GAIN	MDT
Default	00000	0000

GAIN	Gain Control
0000	1X
0001	2X
0010	3X
0011	4X
0100	5X
0101	6X
0110	7X
0111	8X
1000	9X
1001	10X
1010	11X
1011	12X
1100	13X
1101	14X
1110	15X
1111	16X

The GAIN bits are used to set the gain factor. Internal count will count the final value and put it into KEYx_ΔCOUNT.

MDT	Max Duration Time
0000	0.5s
0001	1s
0010	2s
0011	3s
0100	4s
0101	5s
0110	6s
0111	7s
1000	8s
1001	9s
1010	10s
1011	11s
1100	12s
1101	13s
1110	14s
1111	15s

MPT bits set the pressing time. When key pressed continue over the programmed time (MDT), system will force to calibrate the pressed key. Set MDEN to "1" will enable this function.

Table 14 0Fh Key Touch Sampling Configure Register

Bit	D7:D4	D3:D2	D1:D0
Name	SC	ST	CDS
Default	0000	00	00

SC	Touch Key Sampling Count Setting
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14

1110	15
1111	16

SC is used to set average sampling times for each channel. Higher SC value will increase stability and anti-interference ability, but decrease reaction speed.

ST	Sampling Time (Single Channel)
00	0.5ms
01	1ms
10	2ms
11	3ms

CDS	Cycle Delay Time
00	50ms
01	100ms
10	200ms
11	300ms

Sampling 16 channels is for one cycle.

Table 15 10h Calibration Configure Register

Bit	D7	D6:D4	D3:D2	D1:D0
Name	-	CSC	-	NDC
Default	0	000	00	00

CSC	Calibrate Sample Count
000	2
001	4
010	8
011	16
100	32
101	64
110	128
111	256

If there is no action on keys, environmental capacitance will be calibrated after CSC times.

NDC	Negative Delta Count
00	4
01	8
10	16
11	32

If channel detects the value over negative threshold (NDTH) for NDC times, it will be calibrated forcibly.

Table 16-1 11h Individual Force Calibration Register 1

Bit	D7:D1
Name	FCK7:FCK1
Default	0000 0000

Table 16-2 12h Individual Force Calibration Register 2

Bit	D6:D0
Name	FCK14:FCK8
Default	000 0000

FCKx	Individual Force Calibrate Key
0	Close
1	Enable

When enable FCKx, the corresponding bit will be set to “0”.

Table 17 13h Noise Threshold Register

Bit	D7:D0
Name	NTH
Default	0000 0000

The noise threshold is from 0~127. It is invalid if NTH>127.

If difference value between samplings is over the programmed threshold, the corresponding noise bit will be set to “1”.

Table 18-1 14h Noise Indication Register 1

Bit	D7:D1
Name	NK7:NK1
Default	0000 0000

Table 18-2 15h Noise Indication Register 2

Bit	D6:D0
Name	NK14:NK8
Default	000 0000

NKx	Noise Indication
0	No noise
1	Noise

Table 19 19h Scan Voltage Register

Bit	D7	D6:D4	D3
Name	VTH	ZERO_Time [2:0]	REFSEL
Default	0	000	0

VTH Scan Voltage

If REFSEL = 0

0 Cref charges to 0.9V

1 Cref charges to 1.35V

If REFSEL = 1

0 Cref charges to VDDH/2

1 Cref charges to VDDH*3/4

ZERO_Time [2:0] Discharge time of Cref

000 8 us

001 16 us

010 24 us

011 32 us

100 40 us

101 48 us

110 56 us

111 64 us

REFSEL Cref charges source selection

0 The Cref charging source is 1.8V

1 The Cref charging source is VDDH

Table 20 17h Negative Threshold Register

Bit	D7:D4	D3:D0
Name	NCTH	NDTH
Default	0000	0000

NCTH Negative Calibrate Threshold Setting

0000 Disabled

0001 -10

0010 -20

0011 -30

0100 -40

0101 -50

0110 -60

0111 -70

1000 -80

1001 -90

1010 -100

1011 -110

1100 -120

1101 Not available

1110 Not available

1111 Not available

NDTH Negative Delta Threshold Setting

0000 -1

0001 -2

0010 -3

0011 -4

0100 -5

0101 -6

0110 -7

0111 -8

1000 -9

1001 -10

1010 -11

1011 -12

1100 -13

1101 -14

1110 -15

1111 -16

When negative value is over the programmed threshold (NCTH), the channel will be calibrated forcibly.

If negative value is detected over threshold for NDTH times continually, the channel will be calibrated forcibly.

Table 21 18h Wake Up Threshold Register

Bit	D7	D6:D0
Name	-	WTH[6:0]
Default	0	111 1111

Table 22 21h~2Fh KEY0~KEY14 Variation Value Register

Bit	D7	D6:D0
Name	SIGN	KEYx_ΔCOUNT
Default	0	000 0000

SIGB Sign bit

0 Positive

1 Negative

KEYx_ΔCOUNT Key Value Count

Table 23 30h~3Eh KEY0~KEY14 Threshold Set Register

Bit	D7	D6:D0
Name		KEYx_TH
Default	1	111 1111

KEYx_TH Key Threshold
0~127

Table 24-1 40h, 42h … 5Ah, 5Ch KEY0~KEY14 Calibration Low Byte Register (Read Only)

Bit	D7:D0
Name	KEY0_CAL_L
Default	0000 0000

Table 24-2 41h, 43h … 5Bh, 5Dh KEY0~KEY14 Calibration High Byte Register (Read only)

Bit	D7:D0
Name	KEY0_CAL_H
Default	0000 0000

TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

The IS31SE5111 is an ultra low power, fully integrated 15-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric such as glass or plastic.

SENSITIVITY ADJUSTING

Sensitivity can be adjusted by the external capacitor

or internal register.

The value of capacitor is higher the sensitivity is lower; value of capacitor is lower the sensitivity is higher.

INTERRUPTION

The changing of action can be signed by the INTB pin. The INTB pin will be pulled low when sensitivity channel is pressed or released.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SDM bit of the Configuration Register (00h) to “1”, the IS31SE5111 will operate in software shutdown mode.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

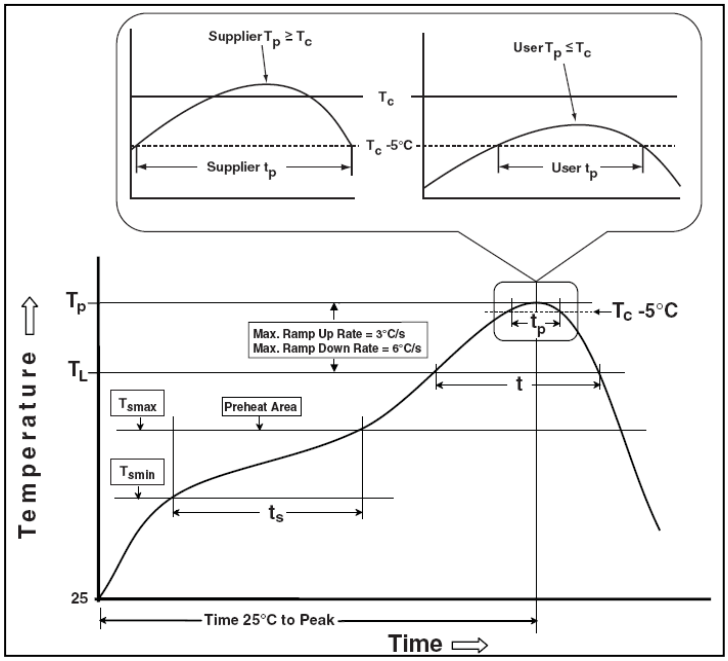
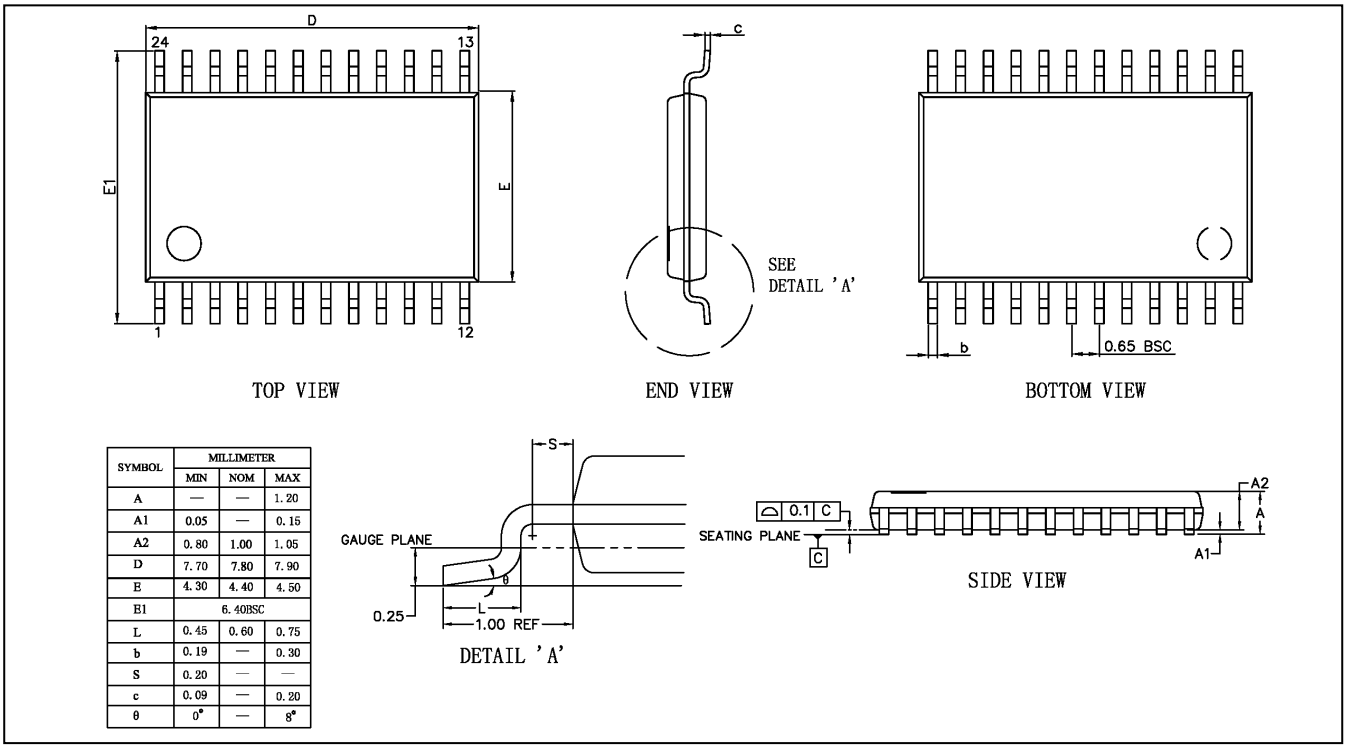


Figure 6 Classification Profile

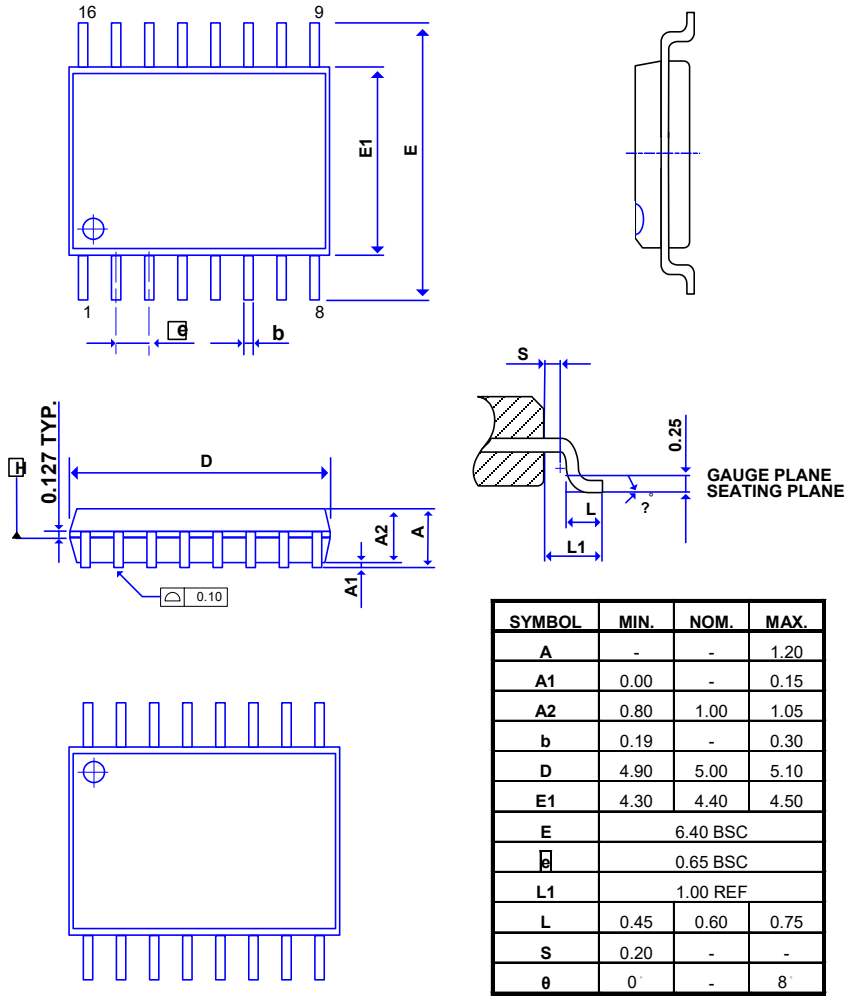
PACKAGE INFORMATION

TSSOP-24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.40BSC		
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

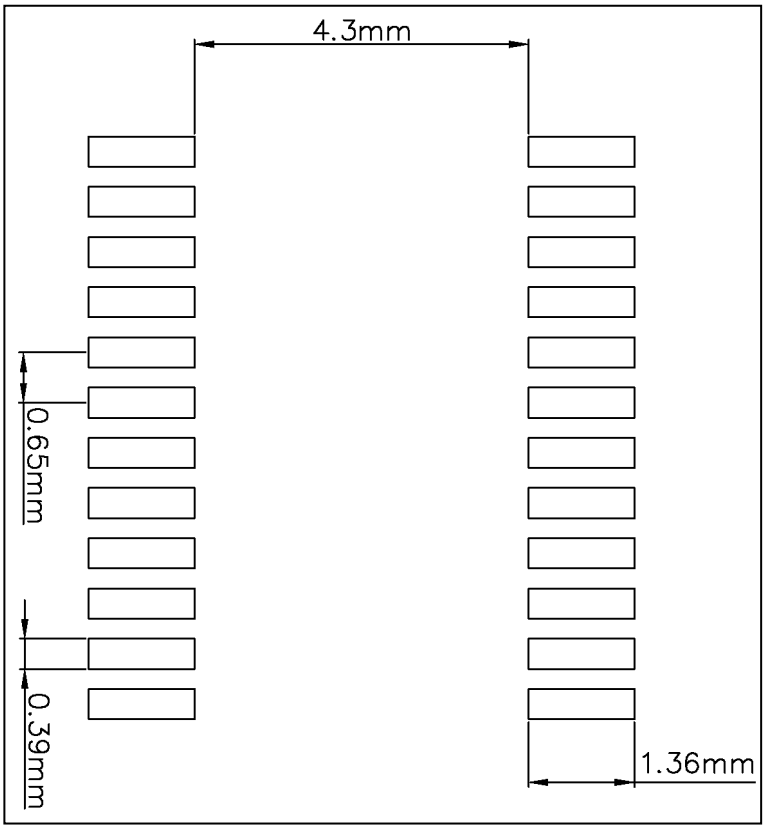
TSSOP-16



SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.00	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	-	-
θ	0°	-	8°

RECOMMENDED LAND PATTERN

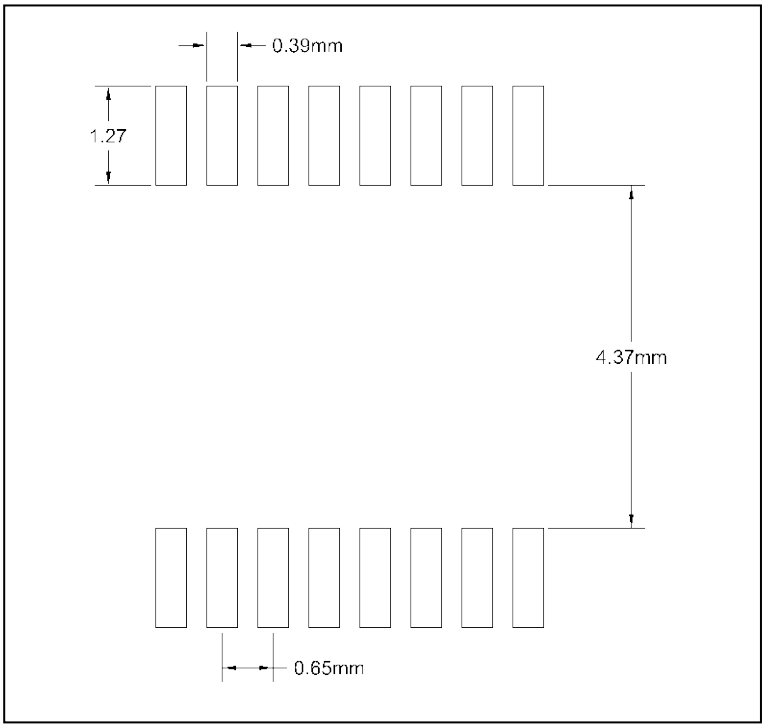
TSSOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

TSSOP-16



Note:

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REVISION HISTORY

Revision	Detail Information	Date
A	Initial release.	2019.07.03

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ISSI:

IS31SE5111A-ZNLS3 IS31SE5111A-ZNLS3-TR IS31SE5111C-ZNLS3 IS31SE5111C-ZNLS3-TR