IS31FL3730

AUDIO MODULATED MATRIX LED DRIVER

May 2018

GENERAL DESCRIPTION

IS31FL3730 is a LED matrix driver which features an audio modulation display mode and a general LED dot matrix display mode. The default configuration of IS31FL3730 is to drive a single 8×8 LED matrix. However, IS31FL3730 may be configured to drive either one or two 8×8, 7×9, 6×10, or 5×11 dot matrix display(s). The intensity of any matrix picture can be modulated by an audio signal.

In matrix display mode, the rows and columns of the matrix are internally scanned, requiring only one time programming of the individual LED on or off state, thus eliminating the need for real time system resource utilization to perform the row and column scanning function.

In the general purpose mode, the ON or OFF condition of each individual LED in the display matrix is programmed via an I2C interface.

IS31FL3730 is available in QFN-24 (4mm × 4mm). It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- 2.7V to 5.5V supply
- I2C interface, automatic address increment function
- Rising edge of SDB reset I2C module
- Internal reset register
- Programmable single or dual 8×8, 7×9, 6×10, or 5×11 LED matrix display mode
- One-time programming, internal scan
- Audio modulated display intensity with digitally programmable input gain
- Internal registers to digitally adjust display intensity
- Modulate LED brightness with 128 different items in PWM
- One address pin with 4 options to allow four I2C slave addresses
- Over-temperature protection
- QFN-24 (4mm × 4mm) package

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

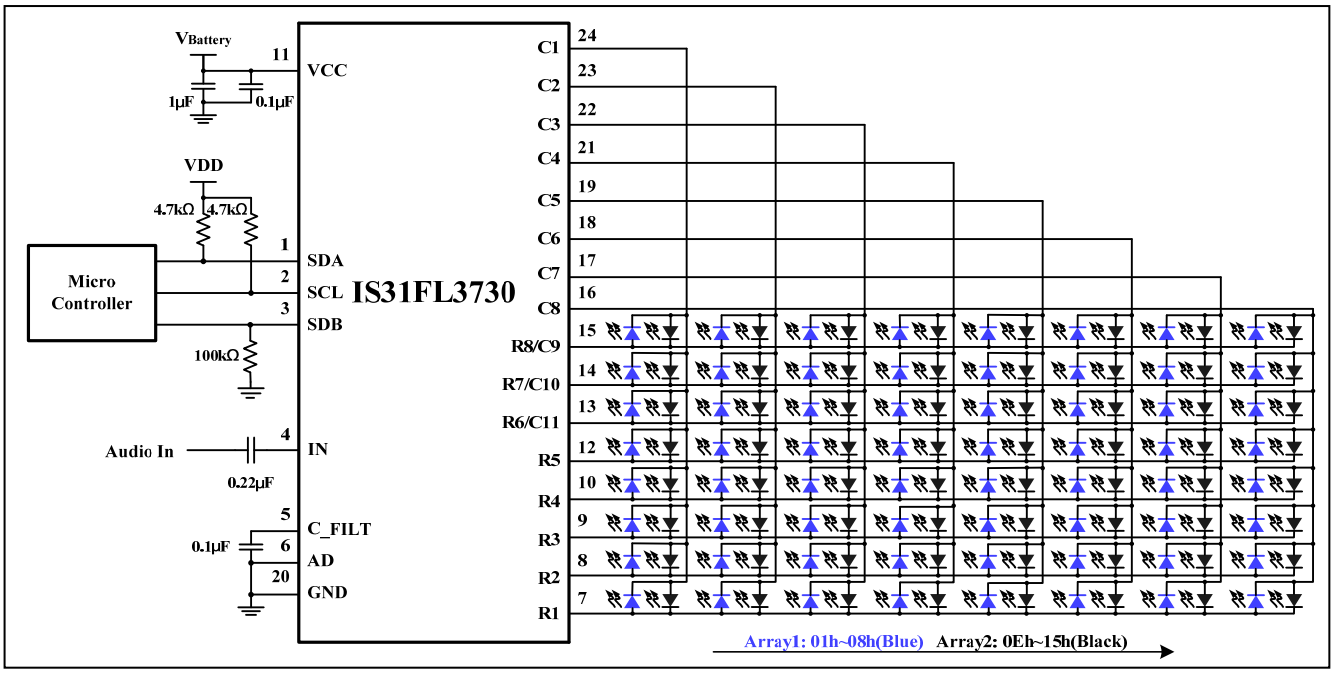


Figure 1 Typical Application Circuit Dual 8×8

Note 1: The IC should be placed far away from the mobile antenna in order to prevent the EMI.

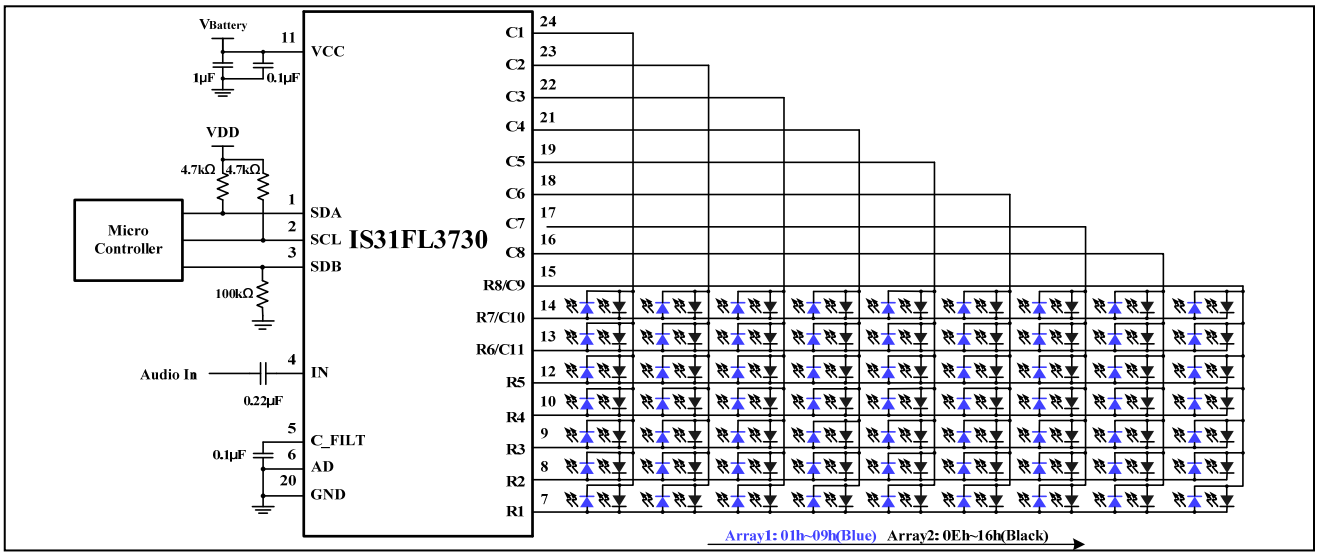


Figure 2 Typical Application Circuit Dual 7×9

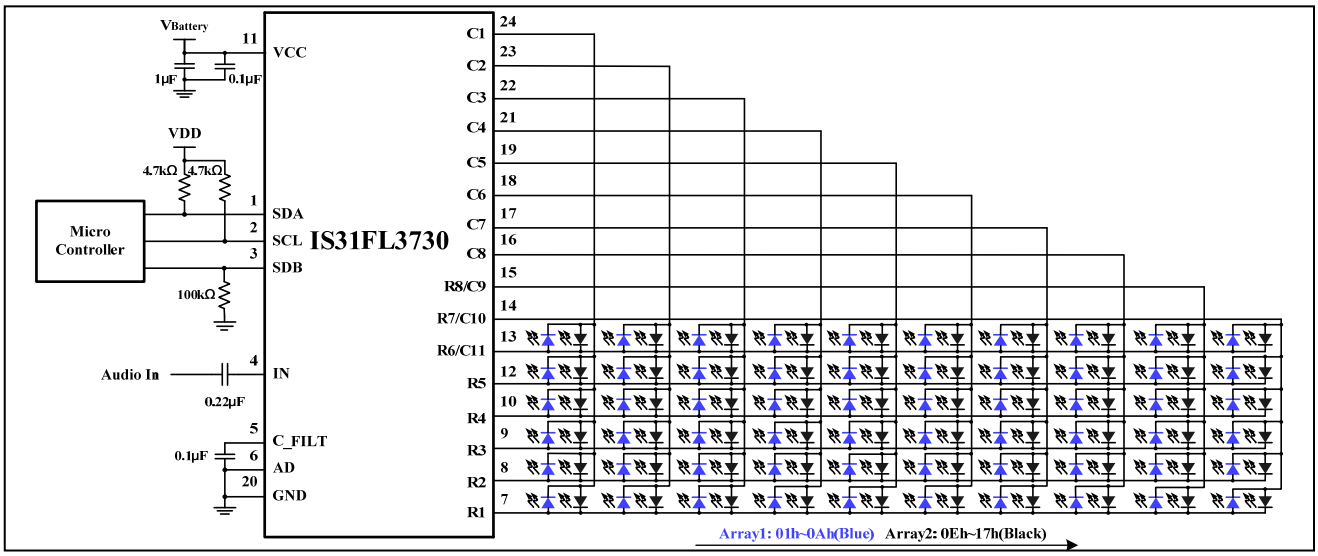


Figure 3 Typical Application Circuit Dual 6×10

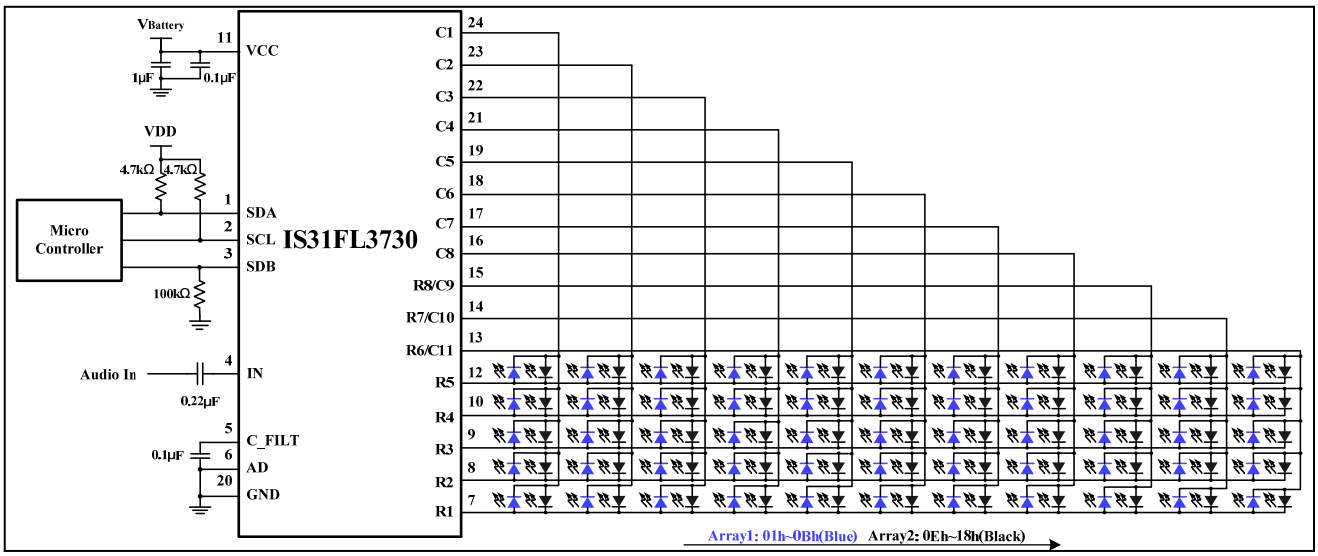
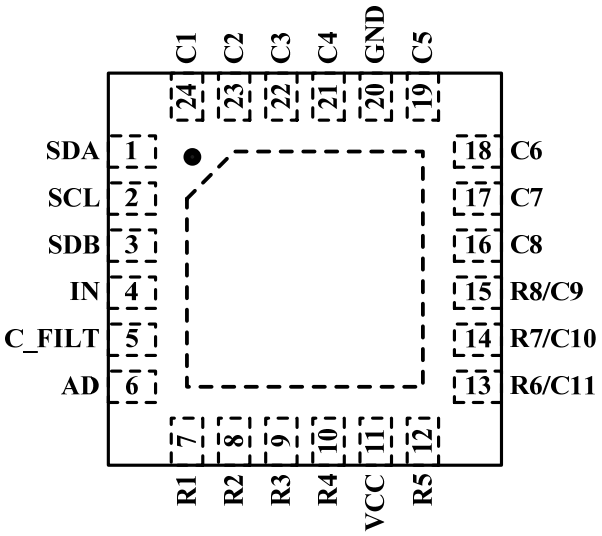


Figure 4 Typical Application Circuit Dual 5×11

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	

PIN DESCRIPTION

No.	Pin	Description
1	SDA	I2C serial data.
2	SCL	I2C serial clock.
3	SDB	Shutdown the chip when pull to low.
4	IN	Audio input.
5	C_FILT	Filter cap for audio control.
6	AD	I2C address setting.
7~10, 12	R1~R5	Row control.
11	VCC	Power supply.
13~15	R6/C11, R7/C10, R8/C9	Row/column control.
16~19, 21~24	C8~C5, C4~C1	Column control.
20	GND	Ground.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3730-QFLS2-TR	QFN-24, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +85°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard), θ_{JA}	29.5°C/W
ESD (HBM) ESD (CDM)	±1kV ±1kV

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A= -40°C ~ +85°C, V_{CC}= 2.7V ~ 5.5V, unless otherwise noted. Typical value are T_A= 25°C, V_{CC}= 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{IN}= 0V, without audio input, all LEDs off		7.0		mA
I_{SD}	Shutdown current	V_{SDB}= 0V		1.7	3.0	μA
		V_{SDB}= V_{CC}, software shutdown		1.7	3.0	
I_{OUT}	Output current of R1~R8, C1~C8	Matrix display mode without audio modulation, Lighting Effect Register(0Dh) = 0xxx 0000 (Note 3)		40		mA
		Matrix display mode with audio modulation, V_{IN}= 2.5V_{P-P}, 1kHz square wave Audio Gain= 0dB (Note 3)		40		
V_{HR}	Current sink headroom voltage R1~R8,C1~C8	I_{SINK}= 320mA		300		mV
	Current source headroom voltage R1~R8,C1~C8	I_{SOURCE}= 40mA		200		
t_{SCAN}	Period of row and column scanning (Figure 10)			32		μs
t_{SCANOL}	Non-overlap blanking time during row and column scan (Figure 10)	(Note 4)		1		μs
Logic Electrical Characteristics (SDA, SCL, AD)						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V~5.5V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 2.7V~5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{IN} = 0V (Note 4)		5		nA
I_{IH}	Logic "1" input current	V_{IN} = V_{CC} (Note 4)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time	(Note 5)	0		0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 6)		$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 6)		$20+0.1C_b$	300	ns

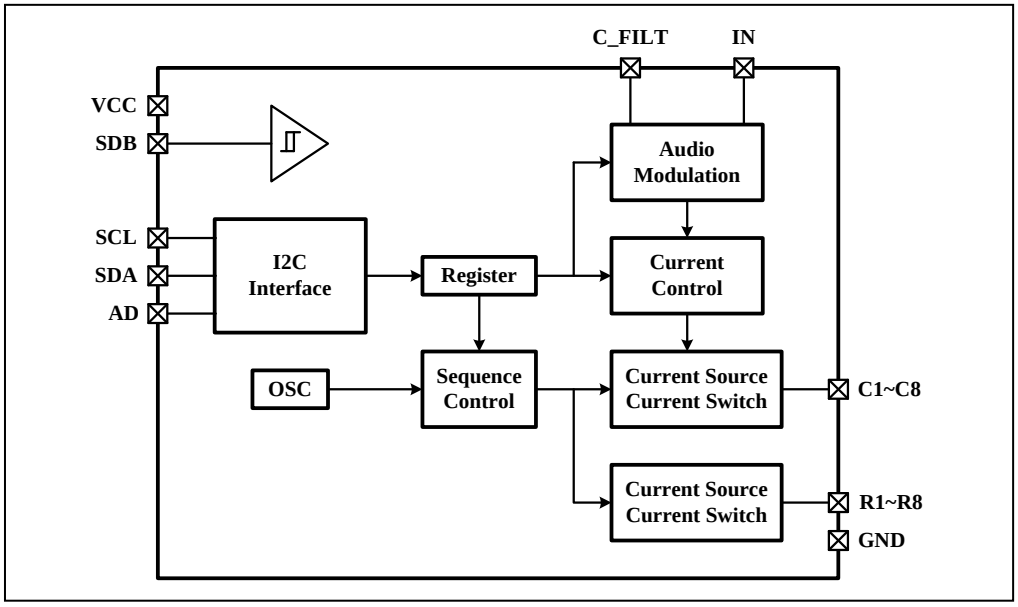
Note 3: Due to the row and column scanning sequence, the average current of an individual LED in the display is $I_{OUT}/8$ when configured to drive a single matrix. When configured to drive two matrices, the average current of an individual LED in the display is $I_{OUT}/16$.

Note 4: Guaranteed by design.

Note 5: The minimum $t_{HD, DAT}$ measured start from V_{IL}(max) of SCL signal. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. V_{IL}(max)

Note 6: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3730 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3730 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Since IS31FL3730 only supports write operations, A0 must always be 0. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write Only):

Bit	A7:A3	A2:A1	A0
Value	11000	AD	0

AD connected to GND, AD=00;
AD connected to VCC, AD=11;
AD connected to SCL, AD=01;
AD connected to SDA, AD=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3730.

The timing diagram for the I2C is shown in Figure 5. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3730's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3730 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3730, the register address byte is sent, most significant bit first. IS31FL3730 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3730 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

Address Auto Increment

To write multiple bytes of data into IS31FL3730, load the address of the data register that the first data byte is intended for. During the IS31FL3730 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3730 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3730. This feature is useful for loading the LED on/off condition for each of the display matrices as a burst of data. Pay careful attention when loading data for dual LED matrix displays since the register addressing is not continuous.

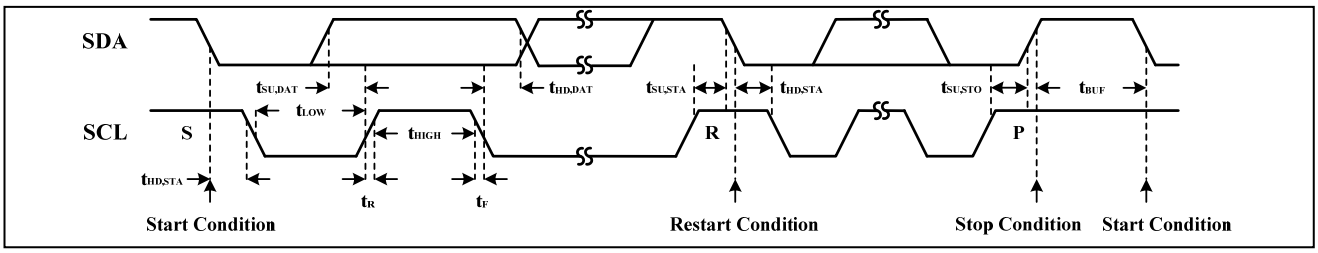


Figure 5 Interface Timing

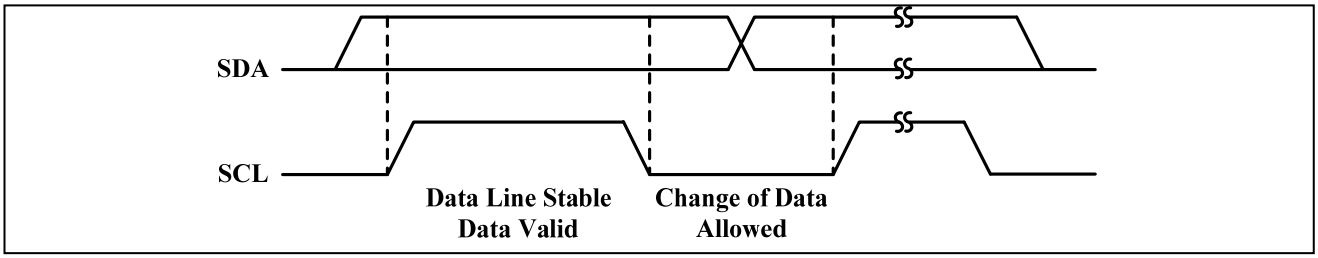


Figure 6 Bit Transfer

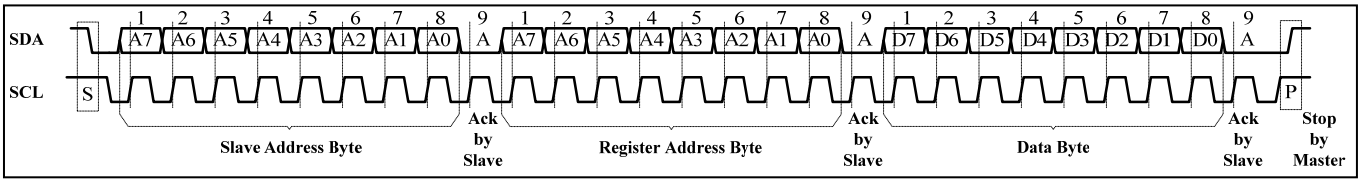


Figure 7 Writing to IS31FL3730(Typical)

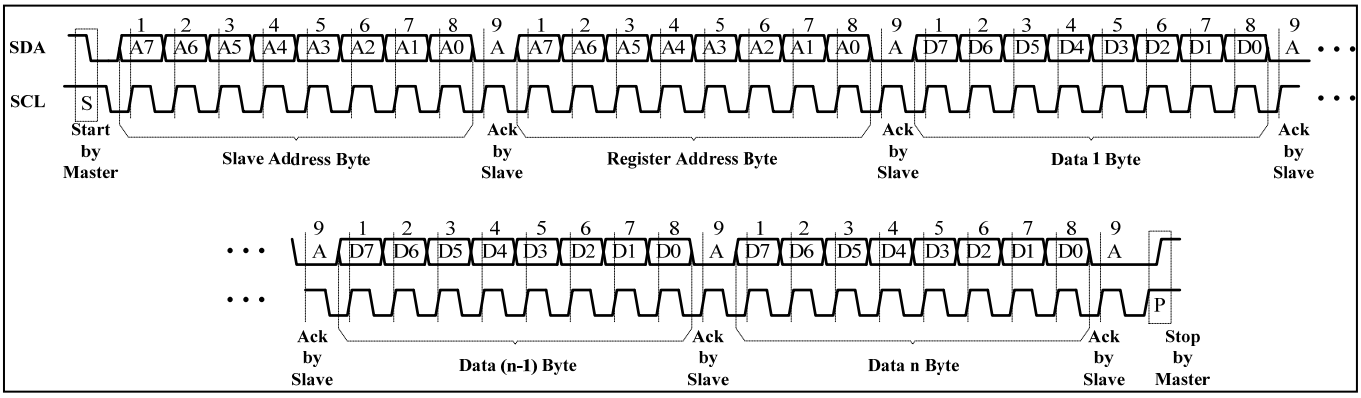


Figure 8 Writing to IS31FL3730(Automatic Address Increment)

REGISTER DEFINITION

Table 2 Register Function

Address	Name	Function	Table	Default
00h	Configuration Register	Set operation mode of IS31FL3730	3	0000 0000
01h~0Bh	Matrix 1 Data Register	Store the on or off state of each LED	4	0000 0000
0Eh~18h	Matrix 2 Data Register	Store the on or off state of each LED	5	
0Ch	Update Column Register	Make the Data Register update the data	-	xxxx xxxx
0Dh	Lighting Effect Register	Store the intensity control settings	6	0000 0000
19h	PWM Register	Modulate LED light with 128 different items	7	1000 0000
FFh	Reset Register	Reset all registers to default value	-	xxxx xxxx

Table 3 00h Configuration Register

Bit	D7	D6:D5	D4:D3	D2	D1:D0
Name	SSD	-	DM	A_EN	ADM
Default	0	00	00	0	00

The Configuration Register sets operation mode of IS31FL3730.

SSD Software Shutdown Enable
0 Normal operation
1 Software shutdown mode

DM Display Mode
00 Matrix 1 only
01 Matrix 2 only
11 Matrix 1 and Matrix 2

A_EN Audio Input Enable
0 Matrix intensity is controlled by the current setting in the Lighting Effect Register (0Dh)
1 Enable audio signal to modulate the intensity of the matrix

ADM Matrix Mode Selection
00 8×8 dot matrix display mode
01 7×9 dot matrix display mode
10 6×10 dot matrix display mode
11 5×11 dot matrix display mode

Table 4 01h~0Bh Matrix 1 Data Register(C1~C11)

Bit	D7:D0
Name	R8:R1
Default	00000000

Table 5 0Eh~18h Matrix 2 Data Register(C1~C11)

Bit	D7:D0
Name	R8:R1
Default	00000000

The Data Registers (Matrix 1/Matrix 2) store the on or off state of each LED in the Matrix.

Rx	LED State
0	LED off
1	LED on

11×2 registers are assigned to C1~C11 columns respectively; the LED at a particular (row, column) location will be turned on when the respective data is set to “1”. When configured for more than 8 column operation, only the required numbers of LSBs are used in each data register. For example, in 5×11 dot matrix mode, only bits R1 thru R5 are used, and bits R6 thru R8 are ignored.

0Ch Update Column Register

The data sent to the Data Registers will be stored in temporary registers. A write operation of “0000 0000” value to the Update Column Register is required to update the Data Registers (01h~0Bh, 0Eh~18h).

Table 6 0Dh Lighting Effect Register

Bit	D7	D6:D4	D3:D0
Name	-	AGS	CS
Default	0	000	0000

The Lighting Effect Register stores the intensity control settings for all of the LEDs in the Matrix.

AGS	Audio Input Gain Selection
000	Gain= 0dB
001	Gain= +3dB
010	Gain= +6dB
011	Gain= +9dB
100	Gain= +12dB
101	Gain= +15dB
110	Gain= +18dB
111	Gain= -6dB

CS	Full Current Setting for Each Row Output
0000	40mA
0001	45mA
...	...
0111	75mA
1000	5mA
1001	10mA
...	...
1110	35mA
Others	Not Available

Table 7 19h PWM Register

Bit	D7	D6:D0
Default	1	0000000

The PWM Register can modulate LED light with 128 different items.

When the D7 set to “1”, the PWM is the 128 item.

When the D7 set to “0”, D6:D0 set the PWM from the 0 item to the 127 item.

For example, if the data in PWM Register is 0000 0100, then the PWM is the 4 item.

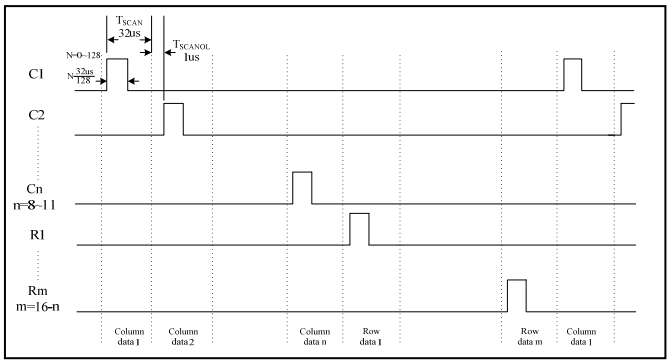


Figure 9 PWM Timing Diagram

Software shutdown and hardware shutdown operation will reset the PWM Register. When restart the IC, the register value will reset to 0x80 and if previous setting is not this value, need to rewrite the PWM Register.

FFh Reset Register

Once user writes “0000 0000” to the Reset Register, IS31FL3730 will reset all registers to default value. On initial power-up, the IS31FL3730 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

GENERAL PURPOSE DOT MATRIX DISPLAY MODE

The general purpose dot matrix display timing diagram is shown in Figure 10. IS31FL3730 may be configured to drive displays of different dimensions from 8×8 to 5×11. Furthermore, IS31FL3730 may be configured to drive one or two LED matrices of the same dimension. Therefore, the overall row and column scan time can vary based on the final LED matrix configuration.

In any LED matrix configuration, a single line (column or row) of LEDs is illuminated for 32μs before IS31FL3730 moves on to the next line of LEDs (Figure 10).

Example 1: When the IS31FL3730 is configured in the general purpose dual 8×8 dot matrix display mode, column controls C8:C1 scans the eight columns of Matrix 1 then row controls R8:R1 scans the eight rows of Matrix 2 at a rate of 1.89kHz, or 528μs per frame. Each line is active for 32μs. The non-overlap interval between adjacent lines is 1μs.

Example 2: When configured to drive a single 7×9 dot matrix display (Matrix 1), the column controls C9:C1 scan the nine columns every 297μs. Also note that in this case, the Data Registers' MSB will be ignored.

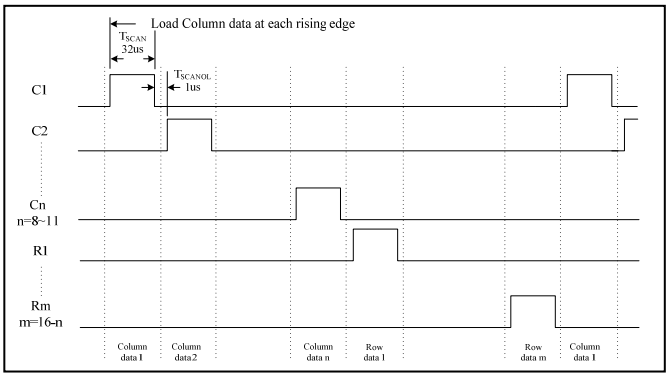


Figure 10 Dot Matrix Display Timing Diagram

DUAL 8×8 DOT MATRIX DISPLAY MODE

The application example in Figure 1 shows the IS31FL3730 in the dual 8×8 LED dot matrix display mode.

The Matrix 1 LED columns have common cathodes and are connected to the C1:C8 outputs. The rows are connected to the row drivers. The Matrix 2 LED rows have common cathodes and connected to the R1:R8. The columns are connected to the C1:C8. Each of the 128 LEDs can be addressed separately.

DUAL 5×11 DOT MATRIX DISPLAY MODE

By setting the ADM bits of the Configuration Register (00h) to "11" and the DM bits to "11", the IS31FL3730 will operate in the dual 5×11 LED dot matrix display mode.

The Matrix 1 LED columns have common cathodes and are connected to the C1:C11 outputs. The rows are connected to the row drivers. The Matrix 2 LED rows have common cathodes and are connected to the R1:R5 outputs. The columns are connected to the column drivers. Each of the 110 LEDs can be addressed separately. The three MSBs (D7:D5) of each Data Register (01h~0Bh, 0Eh~18h) are ignored.

DOT MATRIX DISPLAY MODE WITH AUDIO MODULATION

When the IS31FL3730 operates in any of the dot matrix modes, if the bit A_EN in Configuration Register (00h) is set to "1", the brightness of LED image can be modulated by audio signal not controlled by the CS bit in Lighting Effect Register (0Dh).

An external capacitor, C_FILT is required to control the rate at which the display intensity will change. The rate of change is computed using the formula: ΔT = C×500kΩ. A value of 0.1μF provides a good effect by allowing the display to fade from full intensity to off in approximately 50ms. Smaller capacitance will cause the intensity to change more quickly, and, conversely, a larger capacitance will cause the display intensity to change at a slower rate.

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (00h) to "1", the IS31FL3730 will operate in software shutdown mode, wherein they consume only 1.7μA (Typ.) current. When the IS31FL3730 is in software shutdown mode, all current sources and digital drivers are switched off, so that the matrix is blanked.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

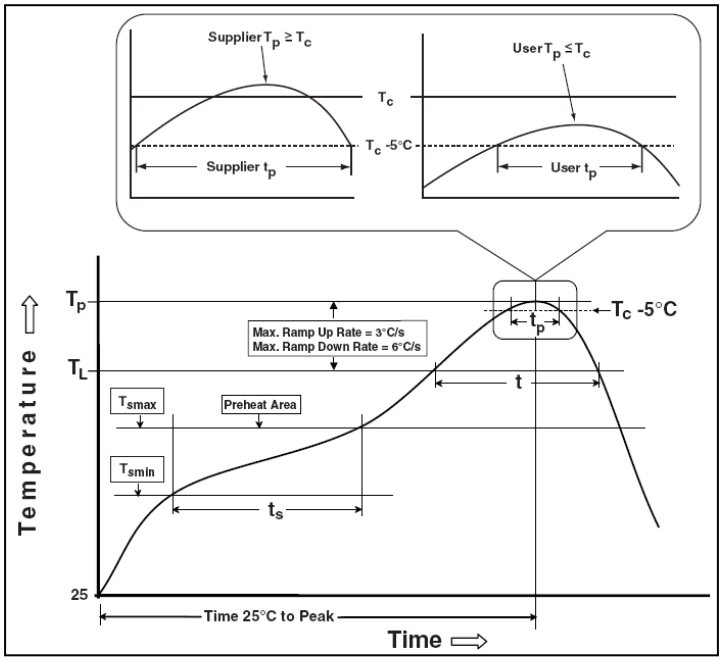
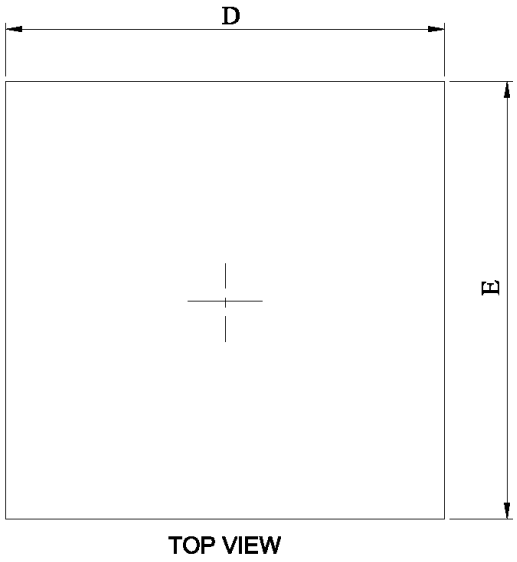


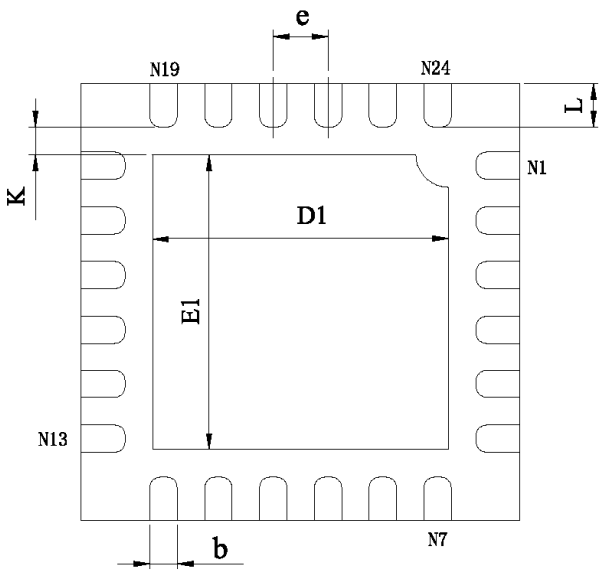
Figure 11 Classification Profile

PACKAGE INFORMATION

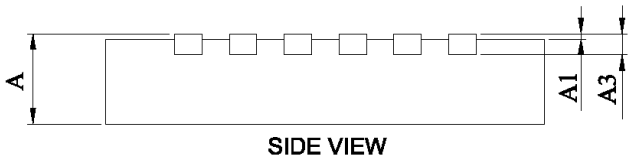
QFN-24



TOP VIEW



BOTTOM VIEW



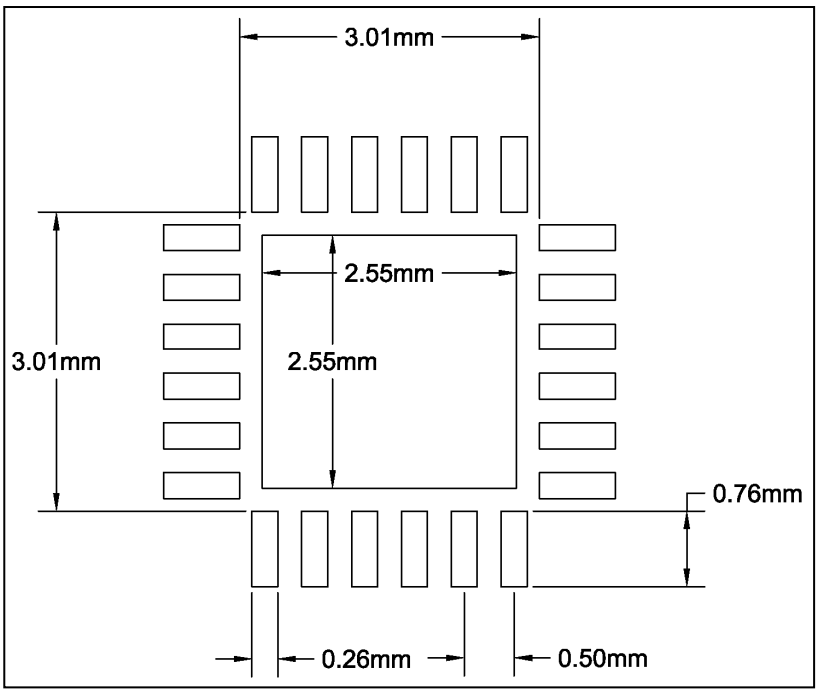
SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.30	—	2.80
e	0.50BSC		
E1	2.30	—	2.80
L	0.30	0.40	0.50
b	0.18	0.25	0.30
K	0.20MIN		

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

QFN-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.12.19
B	1. Add land pattern 2. Add ESD and θ_{JA} value 3. Update POD 4. Add functional block 5. Add description for 19h register 6. EC table V_{IH} and V_{IL} test condition has been changed to 2.7V~5.5V	2017.12.13
C	1. Update ISD hardware shutdown value 2. Add Note 4 for t_{SCANOL} 3. Add SDB rise edge reset I2C function 4. Update function block 5. Update note number	2018.04.02

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