IS31FL3246

36-CHANNEL LED DRIVER

October 2021

GENERAL DESCRIPTION

IS31FL3246 is comprised of 36 constant current channels, each channel can be pulse width modulated (PWM) by total 8 bits+10 bits (261890 steps) for smooth LED brightness control or color mixing control, 8 bits PWM (LFP) operate at 127Hz (can be disabled), 10 bits (HFP) operate at 32kHz, to minimize the audible noise. The output current of each channel can be set at up to 25mA (Max.), all channels are grouped as G group(OUT1, OUT4, OUT7...), R group (OUT2, OUT5, OUT8...) , B group (OUT3, OUT6, OUT9...) and each group has a 8 bits output current control register which allows fine tuning the current for rich global RGB color mixing.

Proprietary programmable technology is used to minimize audible noise caused by MLCC decoupling capacitors. All registers can be programmed via a high speed I2C bus interface (1MHz).

The chip can be turned off by pulling the SDB pin low or by using the software shutdown feature to reduce power consumption. The rising edge of the SDB pin will reset the I2C bus module.

IS31FL3246 is available in QFN-44 (5mm×5mm) and eTQFP-48. It operates from 2.7V to 5.5V over the temperature range -40°C to +125°C.

FEATURES

- 2.7V to 5.5V supply
- Pin to Pin with IS31FL3236A/IS31FL3237 (QFN-44, 5mm×5mm)
- I2C with register address automatic increment
- Four selectable I2C addresses
- SDB rising edge reset I2C module
- Resistor sets operating current of 25mA (Max.)
- Accurate color rendition
  - Three 8-bit global DC current adjust
    - 8-bit DC current adjust for all green channels
    - 8-bit DC current adjust for all red channels
    - 8-bit DC current adjust for all blue channels
  - Each channel total 8-bit+10-bit PWM (261890 steps)
    - 8-bit PWM at 127Hz/254Hz/508Hz (LFP)
    - 10-bit/8-bit PWM at 32kHz (8-bit mode can be at 64kHz or 128kHz, HFP)
- Group dimming to reduce RGB coding
- EMI reduction technology
  - Selectable 6 phase delay
  - Selectable 180 degree clock phase
- -40°C to +125°C extended industrial temperature range

APPLICATIONS

- Hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

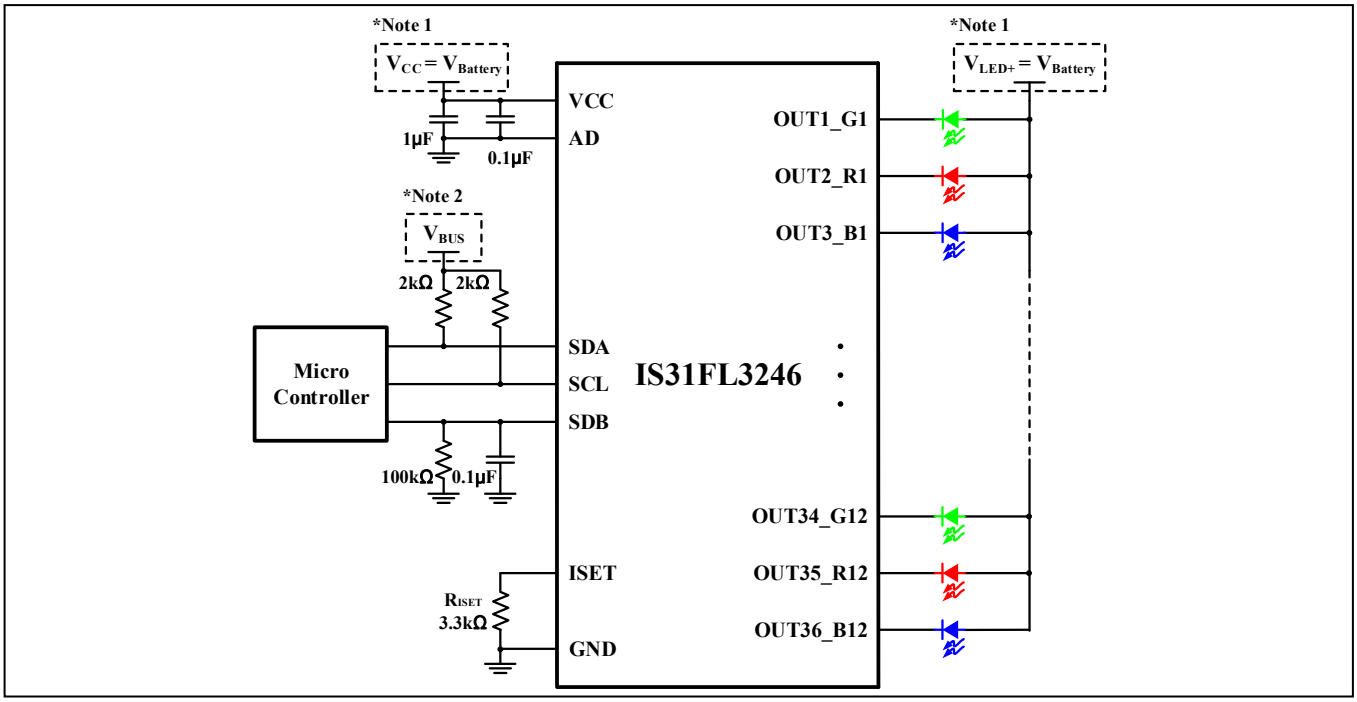


Figure 1 Typical Application Circuit (V_{CC}=$V_{Battery}$)

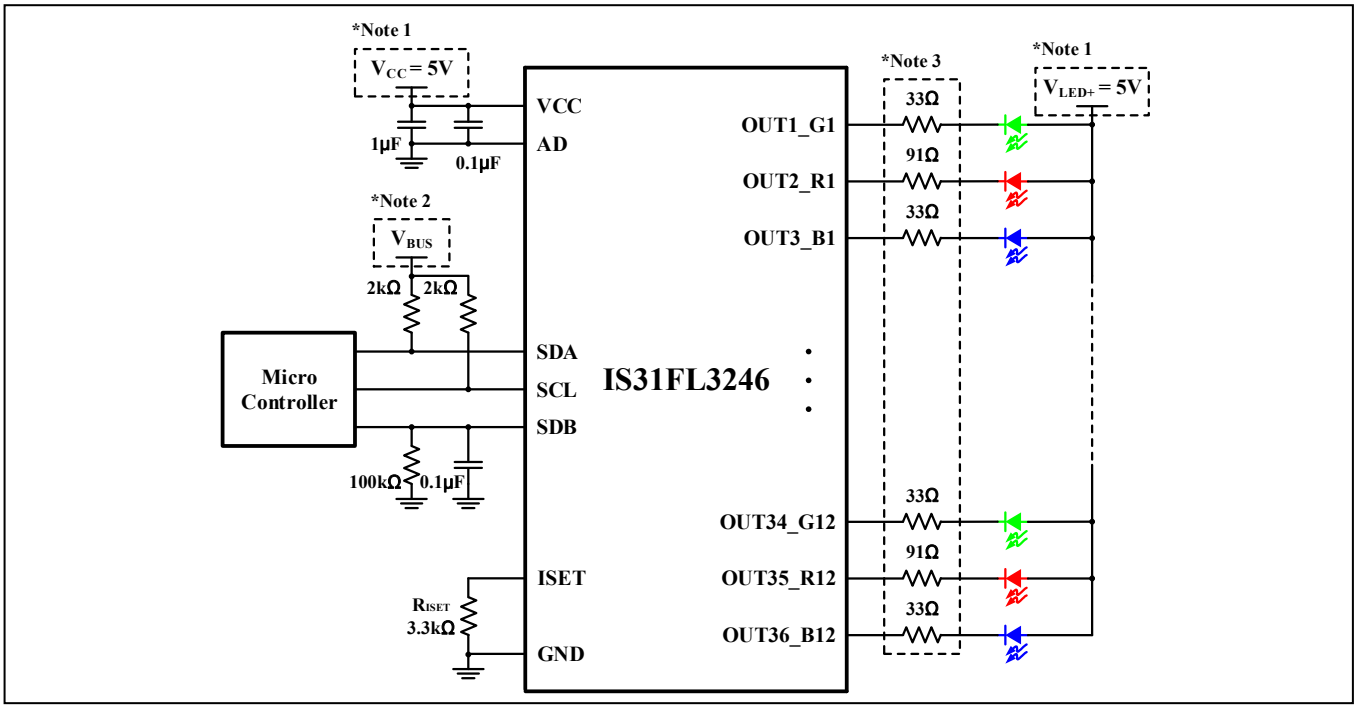


Figure 2 Typical Application Circuit (V_{CC}=5V)

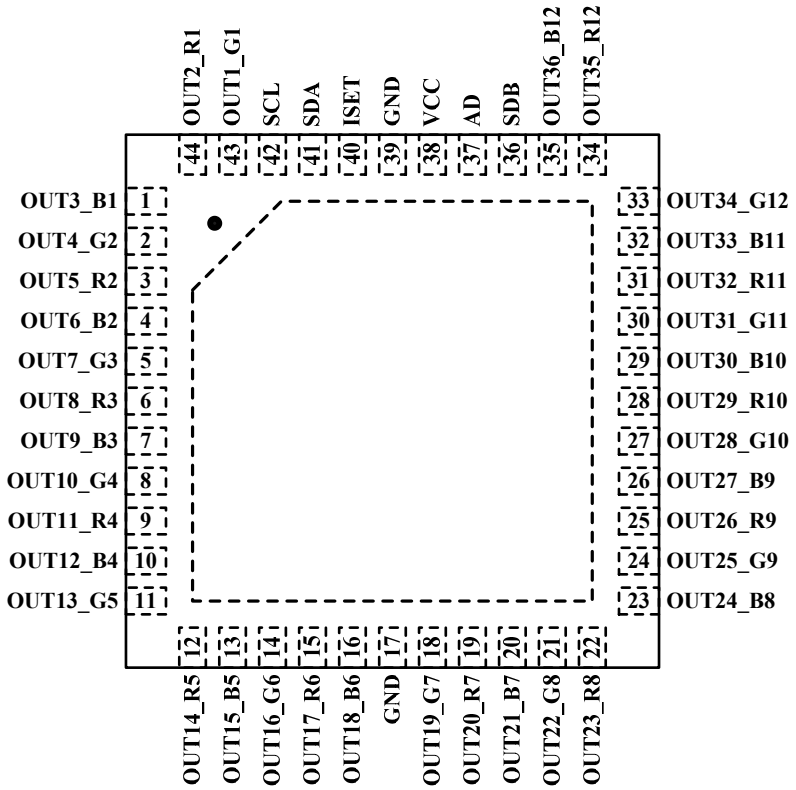
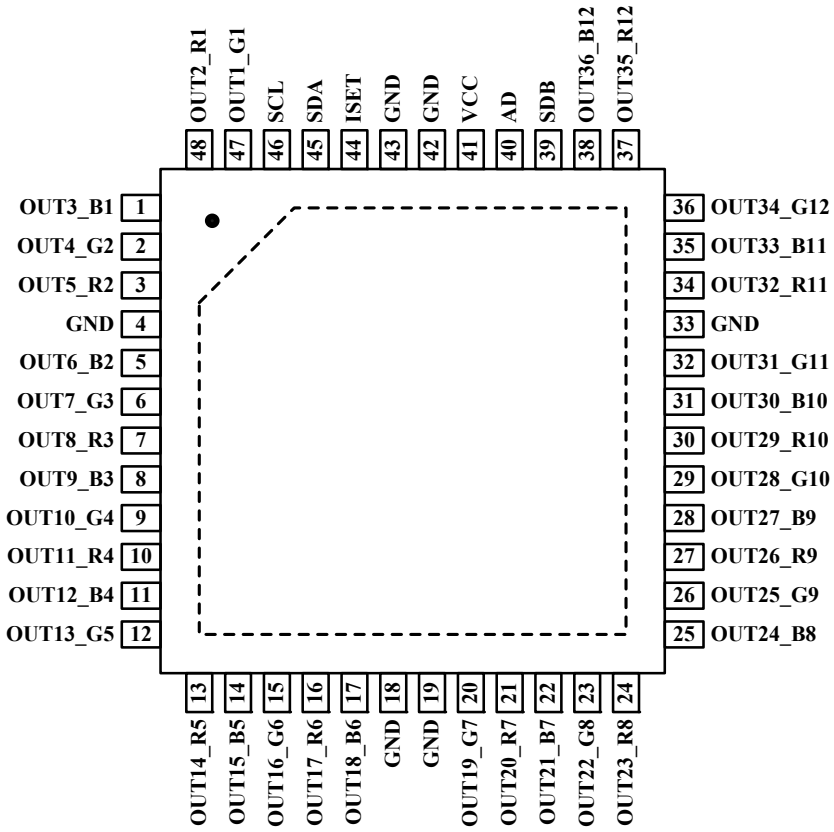
Note 1: V_{LED+} can be the same or less than VCC voltage.

Note 2: V_{BUS} is the pull up voltage for the IS31FL3246 I2C interface, which is usually the same as the micro controller's V_{CC}. If the IS31FL3246 V_{CC}= 5V and V_{BUS} is lower than 2.8V, recommend using an I2C level shift circuit to avoid a high shut down current (I_{SD}). For example with V_{BUS}= 1.8V, if the IS31FL3246 V_{CC}= 4V the I_{SD}= 43μA (Typ.) or if V_{CC}= 5V the I_{SD}=111μA (Typ.).

Note 3: These optional resistors are for offloading the thermal dissipation (P= I^2R) away from the IS31FL3246(values are for V_{LED+}= 5V).

Note 4: The output current is set up to 23mA when R_{ISET}= 3.3kΩ. The maximum global output current can be set by external resistor, R_{ISET}. Please refer to the detail application information in R_{ISET} section.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-44	
eTQFP-48	

PIN DESCRIPTION

No.		Pin	Description
QFN	eTQFP		
1~16	1~3,5~17	OUT3 ~ OUT18	Output channel 3~18 for LEDs.
17,39	4,18,19, 33,42,43	GND	Ground.
18~35	20~32, 34~38	OUT19 ~ OUT36	Output channel 19~36 for LEDs.
36	39	SDB	Shutdown the chip when pulled low.
37	40	AD	I2C address setting.
38	41	VCC	Power supply.
40	44	ISET	Input terminal used to connect an external resistor. This regulates the global output current.
41	45	SDA	I2C serial data.
42	46	SCL	I2C serial clock.
43,44	47,48	OUT1, OUT2	Output channel 1, 2 for LEDs.
		Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
IS31FL3246-QFLS4-TR	QFN-44, Lead-free	2500/Reel
IS31FL3246-TQLS4-TR	eTQFP-48, Lead-free	2500/Reel
IS31FL3246-TQLS4	eTQFP-48, Lead-free	250/Tray

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at SCL, SDA, SDB, OUT1 to OUT36	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	33.1°C/W (QFN) 38.8°C/W (eTQFP)
ESD (HBM) ESD (CDM)	± 8kV ± 750V

Note 5: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Typical values are T_A = 25°C, V_{CC} = 5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{OUT}	Maximum output current	V_{OUT}= 0.8V, R_{ISET}= 3kΩ, GCCX= 0xFF, FMS= "10" (Note 6)		25.3		mA
	Output current	V_{OUT}= 0.8V, R_{ISET}= 3.3kΩ, GCCX= 0xFF, FMS= "10"	21.16	23	24.84	mA
ΔI_{MAT}	Output current error between bits (Note 7)	R_{ISET}= 3.3kΩ, GCCx= 0xFF, FMS= "10", HFP_L= 0x00, V_{CC}=5V, I_{OUT}= 23mA	-7		7	%
ΔI_{ACC}	Output current error between devices (Note 8)	R_{ISET}= 3.3kΩ, GCCx= 0xFF, FMS= "10", HFP_L= 0x00, V_{CC}=5V, I_{OUT}= 23mA	-3		3	%
V_{HR}	Headroom voltage	R_{ISET}= 3.3kΩ, GCCx= 0xFF, FMS= "10", HFP_L= 0x00, V_{CC}=5V, I_{OUT}= 23mA		0.3	0.5	V
I_{CC}	Quiescent power supply current	R_{ISET}= 3.3kΩ, GCCx= 0xFF, FMS= "11", V_{CC}=3.6V,PMS= "0", HFP=32kHz		2.8	4	mA
		R_{ISET}= 3.3kΩ, GCCx= 0xFF, FMS= "11", V_{CC}=5V,PMS= "0", HFP=32kHz		3.3	4.5	mA
I_{SD}	Shutdown current	R_{ISET}= 3.3kΩ, V_{SDB}= 0V or software shutdown, V_{CC}= 3.6V		0.9	1.6	μA
		R_{ISET}= 3.3kΩ, V_{SDB}= 0V or software shutdown, V_{CC}= 5V		2	3	μA
f_{OUT_H}	PWM high frequency	PMS= "1"	30.5	32.5	34.5	kHz
f_{OUT_L}	PWM low frequency	PMS= "1"	119.2	126.9	134.7	Hz
T_{SD}	Thermal shutdown	(Note 9)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 9)		20		°C
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT}= 0V (Note 9)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= V_{CC} (Note 9)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 9)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 6: The recommended minimum value of R_{ISET} is 3kΩ.

Note 7: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n=1\sim 36)}{\left(\frac{I_{OUT1}+I_{OUT2}+...+I_{OUT36}}{36} \right)} - 1 \right) \times 100\%$$

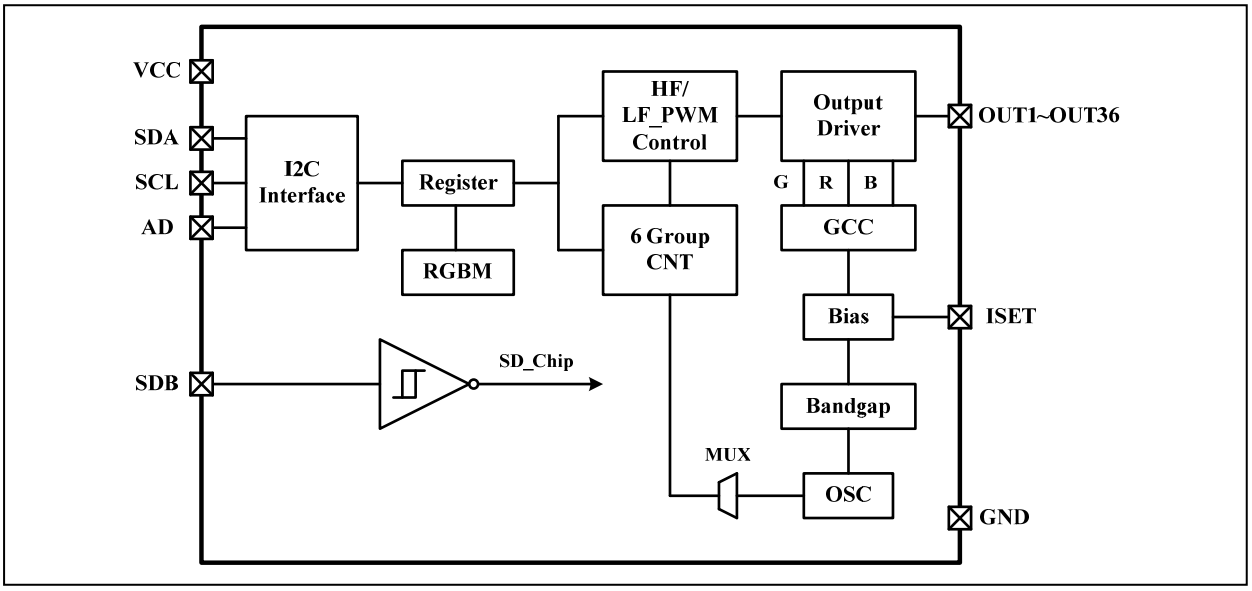
Note 8: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \left(\frac{\left(\frac{I_{OUT1}+I_{OUT3}+...+I_{OUT36}}{36} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 23mA when R_{ISET}= 3.3kΩ.

Note 9: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3246 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3246 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin. The complete slave address is:

Table 1 Slave Address (Write Only):

Bit	A7:A3	A2:A1	A0
Value	0110 0	AD	0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3246.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3246's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3246 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3246, the register address byte is sent, most significant bit first. IS31FL3246 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3246 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3246, load the address of the data register that the first data byte is intended for. During the IS31FL3246 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3246 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3246 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3246 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3246 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3246 to the master (Figure 7).

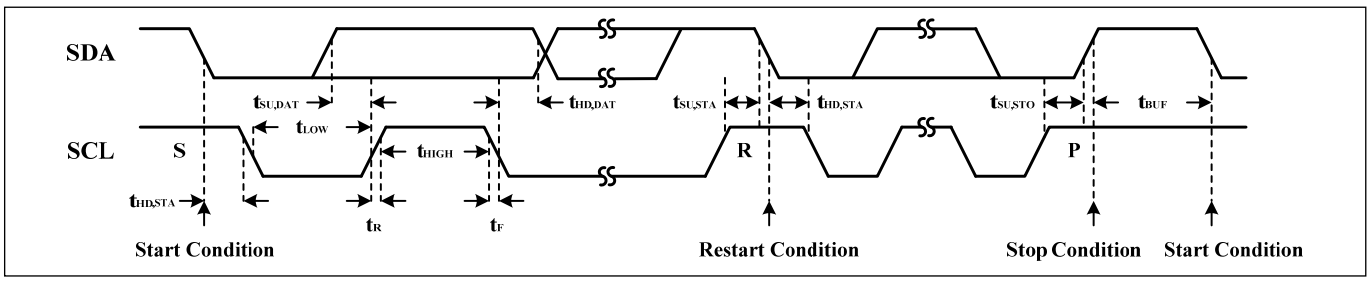


Figure 3 Interface Timing

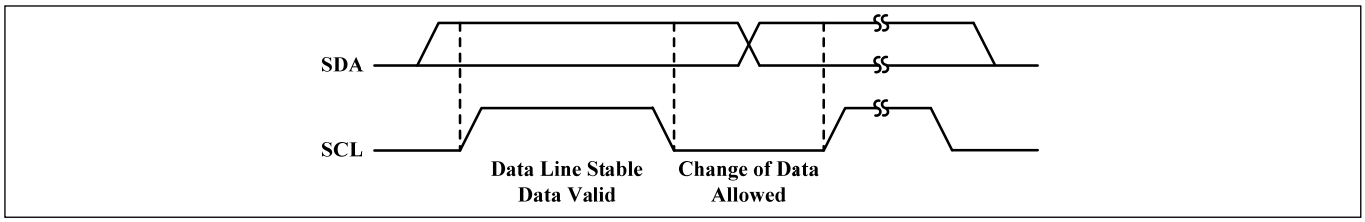


Figure 4 Bit Transfer

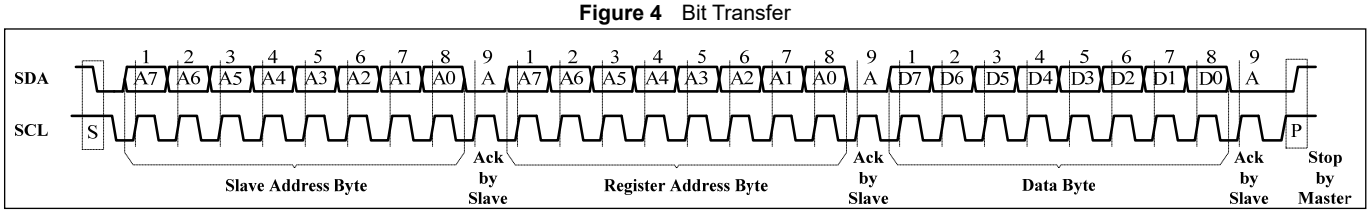


Figure 5 Writing to IS31FL3246 (Typical)

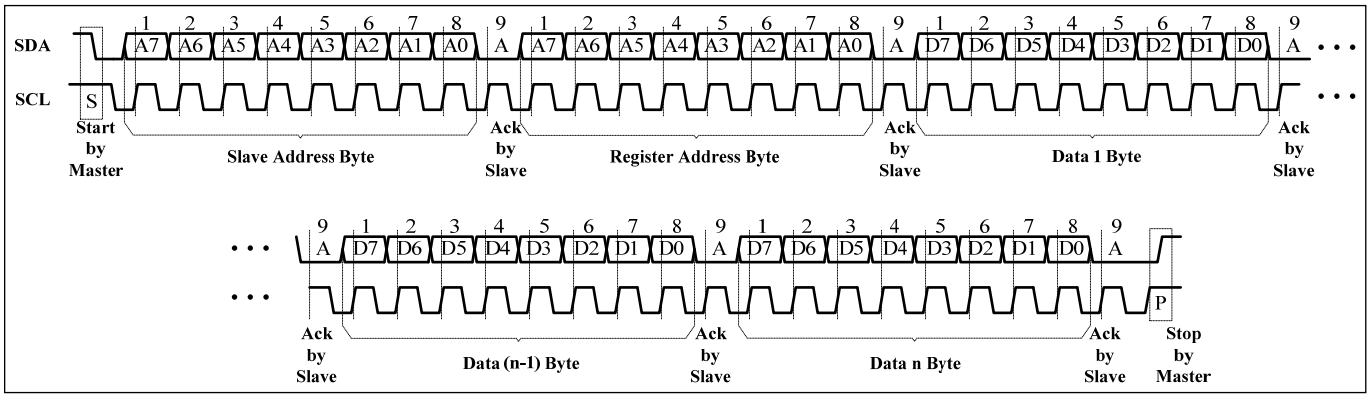


Figure 6 Writing to IS31FL3246 (Automatic Address Increment)

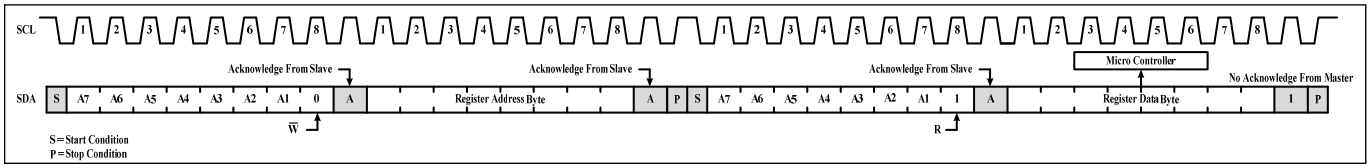


Figure 7 Reading from IS31FL3246

REGISTER DEFINITIONS

Table 2 Register Function

Address	Name	Function	R/W	Table	Default
00h	Control Register	Power control register	R/W	3	0000 0000
01h~48h	High Frequency PWM(HFP) Duty Register	OUT [36:1] high frequency PWM register bytes	R/W	5	
49h~6Ch	Low Frequency PWM(LFP) Duty Register	OUT [36:1] low frequency PWM register byte	R/W	6	
6Dh	Update Register	Update the HFP & LFP data	W	-	
6Eh	Global Current Control Register_G	Global current of all green channels	R/W	9	
6Fh	Global Current Control Register_R	Global current of all red channels	R/W	10	
70h	Global Current Control Register_B	Global current of all blue channels	R/W	11	
71h	Phase Delay and Clock Phase Register	Phase Delay and Clock Phase	R/W	12	
7Fh	Reset Register	Reset all registers	W	-	

Table 3 00h Control Register

Bit	D7	D6	D5:D4	D3:D2	D1	D0
Name	-	RGBM	HFPS	-	PMS	SSD
Default	0	0	00	00	0	0

The Control Register sets software shutdown mode, pulse width modulated (PWM) high/low frequency and PWM resolution.

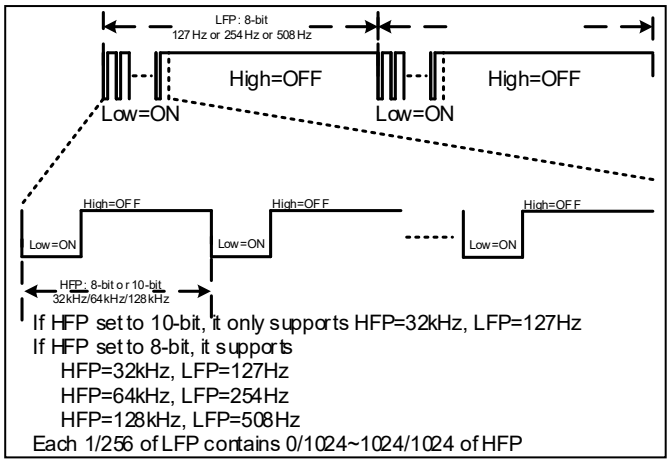


Figure 8 PWM Timing Diagram

Each channel can be (PWM) by total 8bits+10bits (261890 steps) for smooth LED brightness control or color mixing control, 8 bits PWM(LFP) operate at 127Hz(can be disabled), 10 bits(HFP) operate at 32kHz.

When RGBM = “0”, each of the 36 channels are controlled by it’s own PWM register. PWM map in 36 channels as show in Table 7. When RGBM = “1”, 36 channels compose into 12 RGB combinations, all 3 channels in one RGB combinations (OUT1~3, OUT4~6...OUT34~36) control by same PWM register. PWM map in 12 RGB as show in Table 8.

When PMS = “1”, no matter how HFPS is set, HFP (high frequency PWM) is 32kHz, LFP(low frequency PWM) is 127Hz.

When PMS = “0” (8-bit mode), HFPS will decide the internal oscillator clock frequency and the PWM output PWM frequency. Table 4 lists the options of PWM frequency.

SSD Software Shutdown Enable
0 Software shutdown mode
1 Normal operation

PMS High PWM freqyency Resolution
0 8bit mode
1 10bit mode

HFPS High Frequency PWM Select
00 32kHz
01 64kHz
1x 128kHz

RGBM RGB Register Mode Select
0 36 Channel Mode (registers are controlled as table 7)
1 12 RGB Mode (registers are controlled as table 8)

Table 4 PWM Frequency

PMS	HFPS	OSC (MHz)	LFP (Hz)	HFP (kHz)
(“1”) 10-bit	xx	32	127	32
(“0”) 8-bit	00	8	127	32
	01	16	254	64
	1x	32	508	128

Table 5 01h~48h High Frequency PWM Duty Register

Reg	02h (04h, 06h…)			01h (03h, 05h…)
Bit	D7:D4	D3:D2	D1:D0	D7:D0
Name	-	FMS	HFP_H (only enable in 10-bit mode)	HFP_L
Default	0000	00	00	0000 0000

FMS PWM Frequency Mode Select

00 HFP + LFP

01 Only HFP, LFP=256

10 DC Mode, no PWM, output always on

11 Channel Shutdown mode

HFP_H High Frequency PWM High Byte Duty Value (0x00~0x03)

HFP_L High Frequency PWM Low Byte Duty Value (0x00~0xFF)

Each output has 8 bits (N=256)/10 bits (N=1024) to modulate the PWM duty in 256/1024 steps. If using 8 bit PWM resolution, PMS= “0” and only HFP_L bits need to be set.

I_{OUT} and the value of the HFP and LFP Registers decide the average current of each LED noted I_{LED}.

I_{OUT} is computed by Formula (1):

$$I_{OUTx} = I_{OUT\,(MAX)} \times \frac{GCCx}{256} \qquad (1)$$

Where x = R, G or B, $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information), GCCx if the GCCG (6Eh), RCCR (6Fh) and GCCB (70h)(6Eh is for G-group channels (OUT1, OUT4…OUT34). 6Fh is for R-group channels (OUT2, OUT5…OUT35). 70h is for B-group channels (OUT3, OUT6…OUT36)). Please refer to the detail information in Table 7.

$$GCCG\ (6Eh) = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (2)$$

$$GCCR\ (6Fh) = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (3)$$

$$GCCB\ (70h) = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (4)$$

I_{LED} computed by Formula (5):

$$I_{LED} = \frac{HFP}{N} \times \frac{LFP}{256} \times I_{OUT} \qquad (5)$$

$$HFP = \sum_{n=0}^{9} D[n] \cdot 2^n \qquad (6)$$

$$LFP = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (7)$$

Where HFP is the high frequency PWM Duty of each output (01h~48h), and LFP is the low frequency PWM Duty of each output (4Ah~6Ch), N=256/1024 (8/10 bit PWM resolution), If using 8 bit PWM resolution (PMS= “0”), only HFP_L bits need to be set and HFP_H need to be set to ‘00’.

For example: R_{ISET}=3.3kΩ, GCCG=0xFF, GCCR=0x80, GCCB=0x40, LFP=0xFF, PMS= “1” (10-bit PWM resolution), HFP_H=0x03, HFP_L=0xFF, $I_{OUT(MAX)}$= 23.18mA

$$I_{OUTG} = I_{OUT\,(MAX)} \times \frac{255}{256} = 23\,mA \qquad (1)$$

$$I_{OUTR} = I_{OUT\,(MAX)} \times \frac{128}{256} = 11.5\,mA \qquad (1)$$

$$I_{OUTB} = I_{OUT\,(MAX)} \times \frac{64}{256} = 5.76\,mA \qquad (1)$$

$$HFP = \sum_{n=0}^{9} D[n] \cdot 2^n = 1023 \qquad (6)$$

$$LFP = \sum_{n=0}^{7} D[n] \cdot 2^n = 255 \qquad (7)$$

N= 1024

$$I_{LEDG} = \frac{1023}{1024} \times \frac{255}{256} \times 23\,mA = 23\,mA$$

$$I_{LEDR} = \frac{1023}{1024} \times \frac{255}{256} \times 11.5\,mA = 11.5\,mA$$

$$I_{LEDB} = \frac{1023}{1024} \times \frac{255}{256} \times 5.76\,mA = 5.76\,mA \qquad (5)$$

If R_{ISET}=3.3kΩ, GCCG=0xFF, GCCR=0x80, GCCB=0x40, LFP=0xFF, PMS= “0” (8-bit PWM resolution), HFP_H=0x03, HFP_L=0xFF, $I_{OUT(MAX)}$= 23.18mA

$$I_{OUTG} = I_{OUT\,(MAX)} \times \frac{255}{256} = 23\,mA \quad (1)$$

$$I_{OUTR} = I_{OUT\,(MAX)} \times \frac{128}{256} = 11.5\,mA \quad (1)$$

$$I_{OUTB} = I_{OUT\,(MAX)} \times \frac{64}{256} = 5.76\,mA \quad (1)$$

$$HFP = \sum_{n=0}^{7} D[n] \cdot 2^n = 255 \quad (6)$$

$$LFP = \sum_{n=0}^{7} D[n] \cdot 2^n = 255 \quad (7)$$

N= 256

$$I_{LEDG} = \frac{255}{256} \times \frac{255}{256} \times 23\,mA = 23\,mA$$

$$I_{LEDR} = \frac{255}{256} \times \frac{255}{256} \times 11.5\,mA = 11.5\,mA$$

$$I_{LEDB} = \frac{255}{256} \times \frac{255}{256} \times 5.76\,mA = 5.76\,mA \quad (5)$$

Table 6 49h~6Ch Low Frequency PWM Duty Register

Bit	D7:D0
Name	LFP
Default	0000 0000

Each output modulated by the 8bits low frequency PWM duty in 256 steps.

I_{OUT} is computed by Formula (1):

$$I_{OUTx} = I_{OUT\,(MAX)} \times \frac{GCCx}{256} \quad (1)$$

$$I_{LED} = \frac{HFP}{N} \times \frac{LFP}{256} \times I_{OUTx} \quad (5)$$

Where x = R, G or B, $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information), GCCx if the GCCG (6Eh), RCCR (6Fh) and GCCB (70h) (6Eh is for G-group channels (OUT1, OUT4…OUT34). 6Fh is for R-group channels (OUT2, OUT5…OUT35). 70h is for B-group channels (OUT3, OUT6…OUT36)).

Table 7 PWM & GCCx Register Map - 36 Channel Mode (RGBM = "0")

OUT	HFP_H	HFP_L	LFP	GCCx
1	02h	01h	49h	6Eh
2	04h	03h	4Ah	6Fh
3	06h	05h	4Bh	70h
4	08h	07h	4Ch	6Eh
5	0Ah	09h	4Dh	6Fh
6	0Ch	0Bh	4Eh	70h
7	0Eh	0Dh	4Fh	6Eh
8	10h	0Fh	50h	6Fh
9	12h	11h	51h	70h
10	14h	13h	52h	6Eh
11	16h	15h	53h	6Fh
12	18h	17h	54h	70h
13	1Ah	19h	55h	6Eh
14	1Ch	1Bh	56h	6Fh
15	1Eh	1Dh	57h	70h
16	20h	1Fh	58h	6Eh
17	22h	21h	59h	6Fh
18	24h	23h	5Ah	70h
19	26h	25h	5Bh	6Eh
20	28h	27h	5Ch	6Fh
21	2Ah	29h	5Dh	70h
22	2Ch	2Bh	5Eh	6Eh
23	2Eh	2Dh	5Fh	6Fh
24	30h	2Fh	60h	70h
25	32h	31h	61h	6Eh
26	34h	33h	62h	6Fh
27	36h	35h	63h	70h
28	38h	37h	64h	6Eh
29	3Ah	39h	65h	6Fh
30	3Ch	3Bh	66h	70h
31	3Eh	3Dh	67h	6Eh
32	40h	3Fh	68h	6Fh
33	42h	41h	69h	70h
34	44h	43h	6Ah	6Eh
35	46h	45h	6Bh	6Fh
36	48h	47h	6Ch	70h

Table 8 PWM & GCCx Register Map - 12 RGB Mode (RGBM = "1")

RBG Group	OUT	HFP_H	HFP_L	LFP	GCCx
RGB Group 1	1	02h	01h	49h	6Eh
	2			4Ah	6Fh
	3			4Bh	70h
RGB Group 2	4	04h	03h	4Ch	6Eh
	5			4Dh	6Fh
	6			4Eh	70h
RGB Group 3	7	06h	05h	4Fh	6Eh
	8			50h	6Fh
	9			51h	70h
RGB Group 4	10	08h	07h	52h	6Eh
	11			53h	6Fh
	12			54h	70h
RGB Group 5	13	0Ah	09h	55h	6Eh
	14			56h	6Fh
	15			57h	70h
RGB Group 6	16	0Ch	0Bh	58h	6Eh
	17			59h	6Fh
	18			5Ah	70h
RGB Group 7	19	0Eh	0Dh	5Bh	6Eh
	20			5Ch	6Fh
	21			5Dh	70h
RGB Group 8	22	10h	0Fh	5Eh	6Eh
	23			5Fh	6Fh
	24			60h	70h
RGB Group 9	25	12h	11h	61h	6Eh
	26			62h	6Fh
	27			63h	70h
RGB Group 10	28	14h	13h	64h	6Eh
	29			65h	6Fh
	30			66h	70h
RGB Group 11	31	16h	15h	67h	6Eh
	32			68h	6Fh
	33			69h	70h
RGB Group 12	34	18h	17h	6Ah	6Eh
	35			6Bh	6Fh
	36			6Ch	70h

6Dh Update Register

When SDB= “H” and SSD= “1”, a write of “0000 0000” to 6Dh is to update the PWM Register (01h~6Ch) values.

Table 9 6Eh Global Current Control Register-G

Bit	D7:D0
Name	GCCG
Default	0000 0000

Table 10 6Fh Global Current Control Register-R

Bit	D7:D0
Name	GCCR
Default	0000 0000

Table 11 70h Global Current Control Register-B

Bit	D7:D0
Name	GCCB
Default	0000 0000

The Global Current Control Register modulates all channels DC current which is noted as IOUT in 256 steps.

6Eh (GCCG) is for G-group channels (OUT1, OUT4…OUT34). 6Fh (GCCR) is for R-group channels (OUT2, OUT5…OUT35). 70h (GCCB) is for B-group channels (OUT3, OUT6…OUT36).

GCCx control the I_{OUT} as shown in Formula (1).

$$GCCx = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (5)$$

If GCCx=0xFF,

$$I_{OUTx} = I_{OUT\,(MAX)} \times \frac{255}{256}$$

If GCCx=0x01,

$$I_{OUTx} = I_{OUT\,(MAX)} \times \frac{1}{256}$$

Where x = R, G or B, $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information).

Table 12 71h Phase Delay and Clock Phase Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PDE	HLS	PS6	PS5	PS4	PS3	PS2	PS1
Default	0	0	0	0	0	0	0	0

IS31FL3246 features a 6 phase delay function, when this bit is set, the phase delay function is enabled.

HLS Group Phase Delay Select
0 6 Group Phase Delay operate at low frequency PWM (LFP)
1 6 Group Phase Delay operate at high frequency PWM (HFP)

PDE Phase Delay Enable
0 Phase delay disable
1 Phase delay enable

PS[n] Clock Phase Select
0 Clock Phase Select disable
1 Clock Phase Select enable

Phase Delay separates 36 outputs as 6 groups, OUT1~OUT6 as group 1, OUT7~OUT12 as group 2…OUT31~OUT36 as group 6. When Phase Delay is enabled, group 2 has a 1/(6×f_{OUT}) time delay than group 1, group 3 also has a 1/(6×f_{OUT}) time delay than group 2, group 4 also has a 1/(6×f_{OUT}) time delay than group 3, and so on.

For each group of 6 outputs there is a Clock Phase option PS[n] (n=1~6), when PSn is set to “1”, OUT[1+(n-1)×6], OUT[3+(n-1)×6], OUT[5+(n-1)×6] keep the phase, phase 1, the turning on edge of the PWM pulse is fixed from starting of PWM cycle, but OUT[2+(n-1)×6], OUT[4+(n-1)×6], OUT[6+(n-1)×6] change to phase 2, the turning off edge of the PWM pulse is fixed from ending of PWM cycle as fiure 13, the rising and falling edges will cancel the power ripple.

IS31FL3742 operates both at PWM frequency at 127Hz~504Hz (LFP) and 32kHz~128kHz, HLS bit can select the Group Phase Delay function operating frequency. When HLS= “0”, 6 Group Phase Delay operate at low frequency PWM (LFP), When HLS= “1”, 6 Group Phase Delay operate at high frequency PWM (HFP).

Phase Delay feature and Clock Phase options can work together to minimize the voltage ripple of LED power supply. Check Phase Delay and Clock Phase section for more information

7Fh Reset Register

A write of “0000 0000” to 7Fh will reset all registers to their default values.

APPLICATION INFORMATION

RISET

The maximum output current $I_{OUT(MAX)}$ of OUT1~OUT36 can be adjusted by the external resistor, R_{ISET}, as described in Formula (8).

$$I_{OUT\ (MAX\ )} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (8)$$

x = 78.25, V_{ISET} = 0.97V.

The recommended minimum value of R_{ISET} is 3kΩ.

When R_{ISET}=3.3kΩ, $I_{OUT(MAX)}$=23mA

When R_{ISET}=3kΩ, $I_{OUT(MAX)}$=25.3mA

CURRENT SETTING

The maximum output current is set by the external resistor R_{ISET}. The Global Current Control register GCCX can be used to set a lower current than set by R_{ISET}.

The IS31FL3246 provides independent gradation control for each of the red, green and blue colors. The Global Current Control Register modulates all channels DC current which is noted as IOUT in 256 steps.

6Eh is for G-group channels (OUT1, OUT4…OUT34).
6Fh is for R-group channels (OUT2, OUT5…OUT35).
70h is for B-group channels (OUT3, OUT6…OUT36).

PWM CONTROL

Each channel can be (PWM) by total 8bits+10bits (261890 steps) for smooth LED brightness control or color mixing control, 8 bits PWM (LFP) operate at 127Hz (can be disabled), 10 bits (HFP) operate at 32kHz.

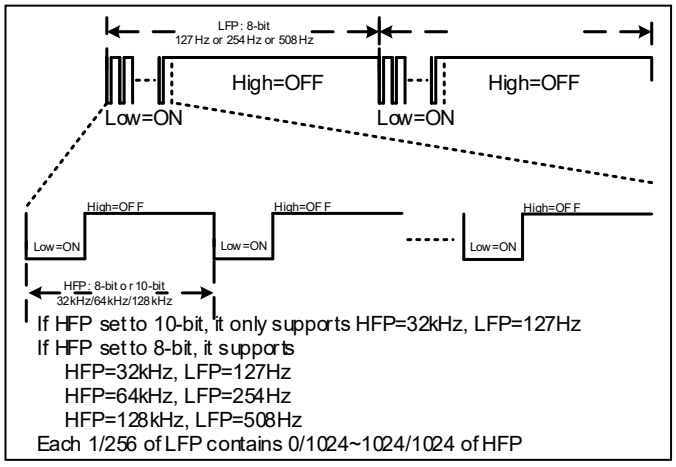


Figure 9 PWM Timing Diagram

The Low Frequency PWM Duty Registers (49h~6Ch) can change a low frequency PWM (LFP) duty with between 0/256 and 255/256. Each of the LFP's 1/256 unit contain another PWM method, HFP, 8-bit or 10-bit, work at 32kHz or higher frequency, change the PWM duty from 0/1024~1023/1024. When LFP and HFP work together, the total PWM steps are 8-bit+10-bit (261890 steps).

Writing new data continuously to the PWM registers can modulate the brightness of the LEDs to achieve color mixing and breathing effect.

PWM FREQUENCY SELECT

The IS31FL3246 output channels operate with a default 8 bit PWM resolution mode and the low frequency PWM at 127Hz and high frequency at 32kHz (the oscillator frequency is 8MHz). Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 200Hz to 18kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3246's output PWM frequency above/below the audible range. The Control Register (00h) can be used to set the switching frequency to 127Hz~504Hz as shown in Table 4, all the high frequency PWM (HFP) is higher than 20kHz, and can select lower low frequency PWM (LFP) to reduce the audible hum.

12 RGB COMBINATIONS

36 channels control by independent PWM registers as show in Table 7, or 36 channels compose into 12 RGB combinations. All 3 channels in one RGB combinations (OUT1~3, OUT4~6...OUT34~36) controlled by the same PWM register. PWM map in 12 RGB as show in Table 8.

PHASE DELAY and CLOCK PHASE

To reduce audible noise due to PWM switching, the IS31FL3246 features Phase Delay and Clock Phase schemes. When Phase Delay and Clock Phase are disabled (default) all of the outputs turn on simultaneously causing large current draw from the ceramic capacitors and pausible audible noise.

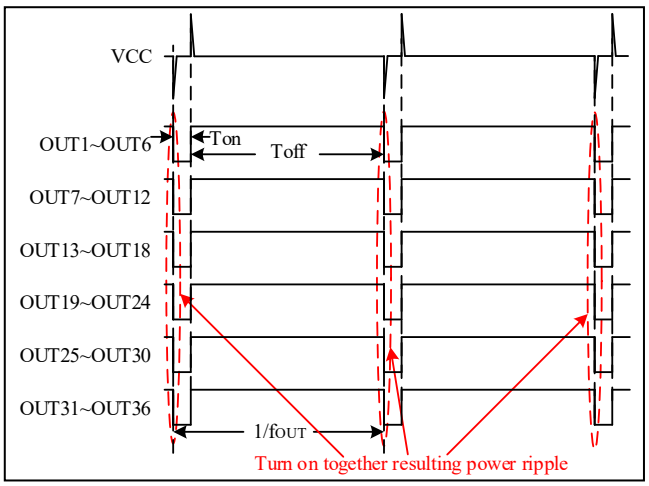


Figure 10 Phase Delay and Clock Phase disable for both LFP and HFP

The PDE bit of register 71h will enable the Phase Delay function so at power-on the OUTx channel will not all turn on at the same time to minimize peak load current, resulting in reduced voltage ripple on the LED power supply rail. Phase Delay separates the 36 outputs as 6 groups, OUT1~OUT6 as group 1, OUT7~OUT12 as group 2…OUT31~OUT36 as group 6, when Phase Delay is enabled, group 2 will have a 1/(6×f_{OUT}) time delay than group 1, group 3 will also have a 1/(6×f_{OUT}) time delay than group 2, and so on.

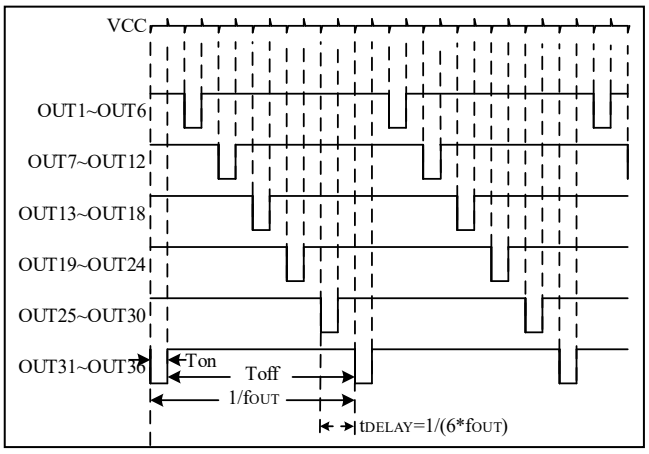


Figure 11 PDE= "1" Phase Delay Enable

The HLS bit of register 71h can select the Group Phase Delay schemes to apply on low frequency PWM (LFP) or high frequency PWM (HFP), if it applys on LFP, it redudes the LED power supply rail voltage ripple of low frequency (127Hz~504Hz), if it applys on HFP, it redudes the LED power supply rail voltage ripple of high frequency (32kHz~128Hz). Since HFP frequency is higher than 20kHz and enough to avoid the audible, it is recommend to choose the schemes to apply on LFP to reduce the the LED power supply rail voltage ripple of low frequency (127Hz~504Hz).

Also in each group of outputs, there is a Clock Phase option PS[n](n=1~6), when PSn of 71h register is set to "0" (default), all outputs in group n keep the phase 1.

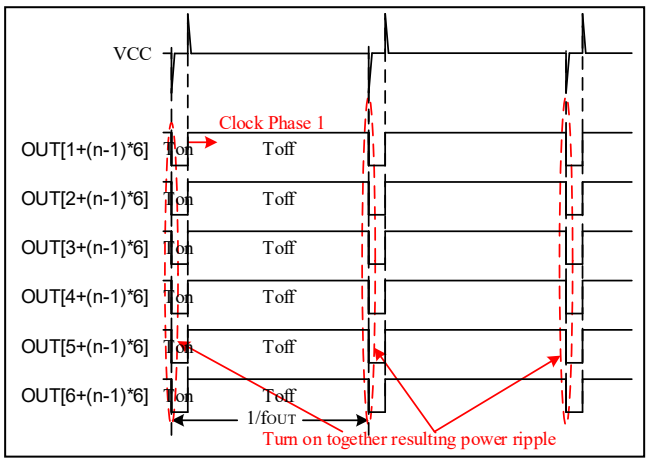


Figure 12 PSn= "0" Clock Phase disable

When PSn is set to "1", OUT[1+(n-1)×6], OUT[3+(n-1)×6], OUT[5+(n-1)×6] will keep the phase 1, the turning on edge of the PWM pulse is fixed from starting of PWM cycle as below, but OUT[2+(n-1)×6], OUT[4+(n-1)×6], OUT[6+(n-1)×6] will change to phase 2, the turning off edge of the PWM pulse is fixed from ending of PWM cycle as below, the rising and falling edges will cancel the power ripple.

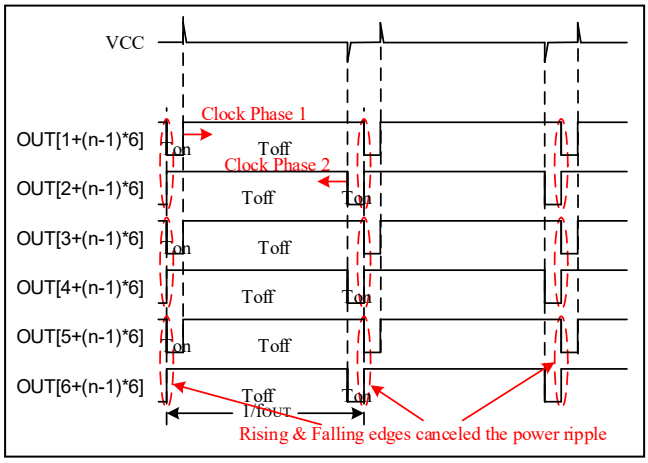


Figure 13 PSn= "1" Clock Phase enable

Phase Delay feature and Clock Phase options can work together to minimize the voltage ripple of LED power supply.

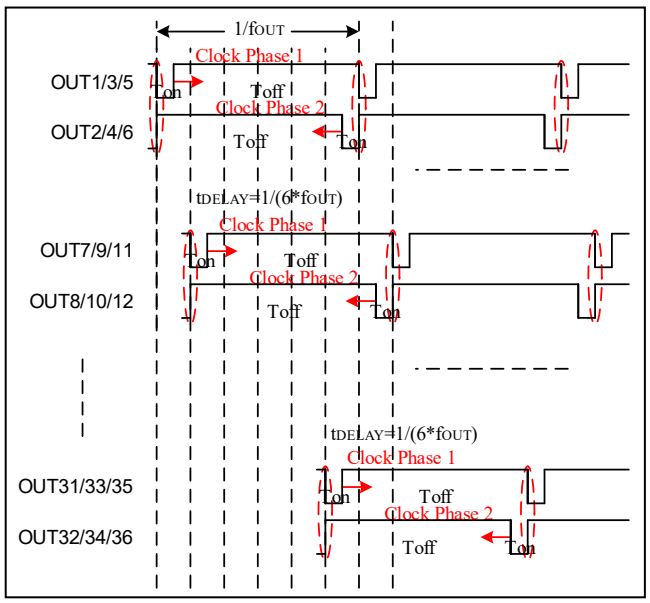


Figure 14 PDE= "1" Phase Delay enable, PSn= "1" (n=1~6) Clock Phase Enable

Phase Delay feature and Clock Phase options can work together to minimize the voltage ripple of LED power supply.

OPERATING MODE

IS31FL3246 can operate in PWM Mode or DC Mode. The brightness of each LED can be modulated with 261890 steps by PWM registers. In DC Mode, there is no PWM and Iout=Iout(MAX) always.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting the SSD bit of the Control Register (00h) to "0", the IS31FL3246 will operate in software shutdown mode. When the IS31FL3246 is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers accessible. Typical current consume is 0.9μA (V_{CC}=3.6V).

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consumption is 0.9μA (V_{CC}=3.6V).

The chip releases hardware shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but the register information is retained. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS31FL3246 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout, the first pcb trace to consider is the power supply trace and GND connections, especially those traces with high current. Also the digital and analog blocks' supply line and GND should be separated to avoid noise from digital block affecting the analog block.

At least one 0.1μF capacitor, if possible with a 1μF capacitor is recommended to connected to the ground at power supply pin of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

R_{ISET}

R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. The thermal pad of IS31FL3246 should connect to GND net and need to use 9 or 16 vias connect to GND copper area, the GND area should be as large area as possible to help radiate the heat from the IS31FL3246.

Current Rating Example

For a R_{ISET}=3.3kΩ application, the current rating for each net is as follows:

• VCC pin maximum current is lower than 10mA when V_{CC}=5V, but the VLED+ net is provide total current of all outputs, its current can as much as 23mA×36=828mA, recommend trace width for VCC pin: 0.20mm~0.3mm, recommend trace width for VLED+ net: 0.30mm~0.5mm

• Output pins=23mA, recommend trace width is 0.2mm~0.254mm

• All other pins<3mA, recommend trace width is 0.15mm~0.254mm

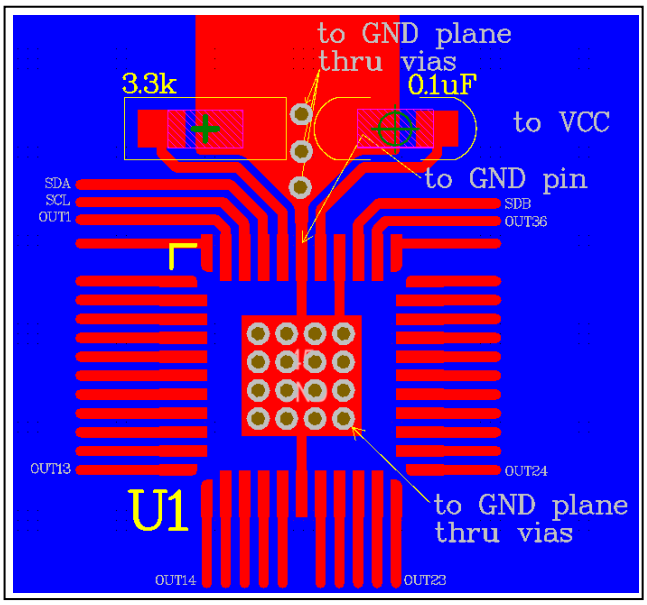


Figure 15 Layout Example (QFN)

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

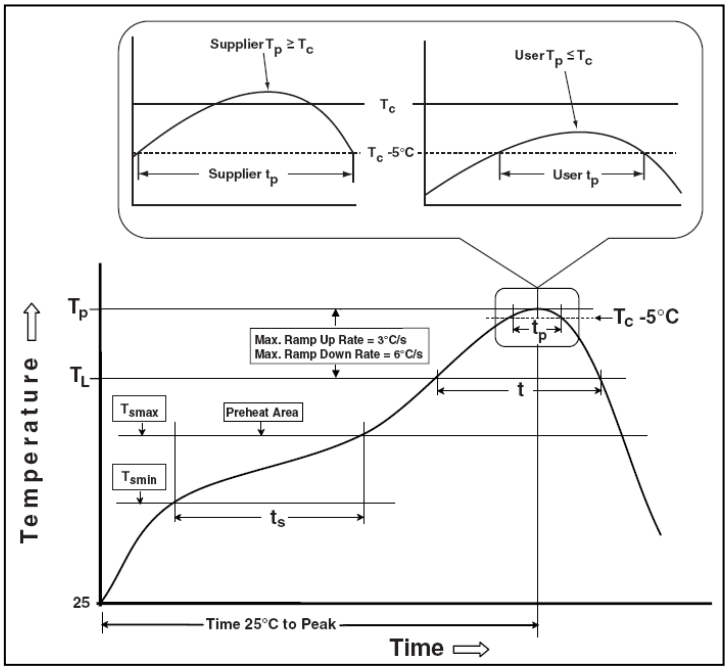
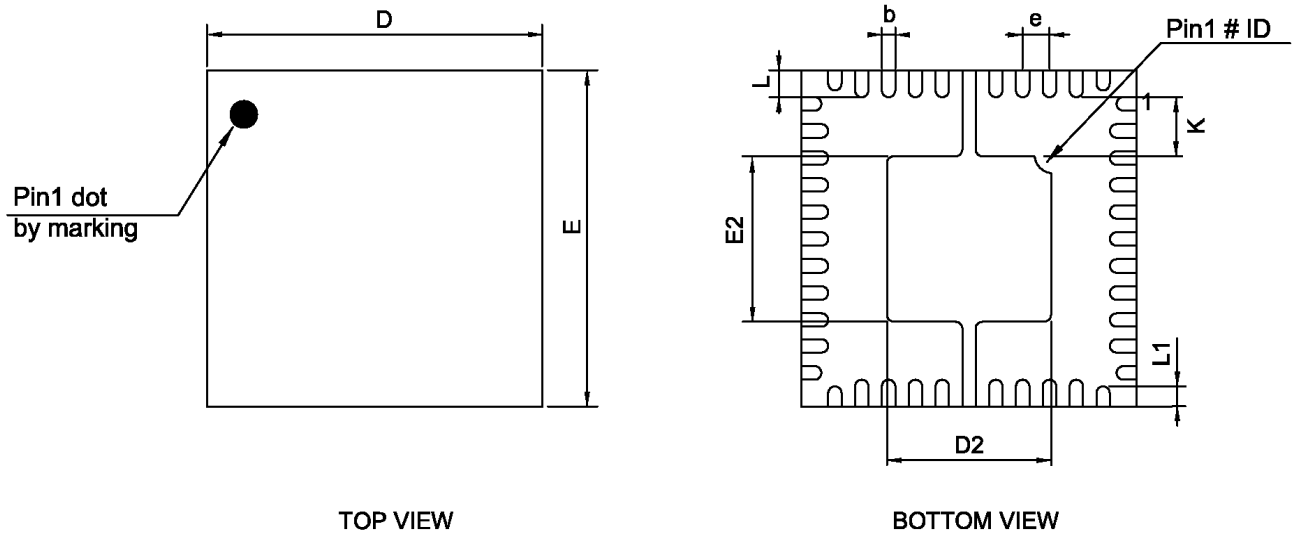


Figure 16 Classification Profile

PACKAGE INFORMATION

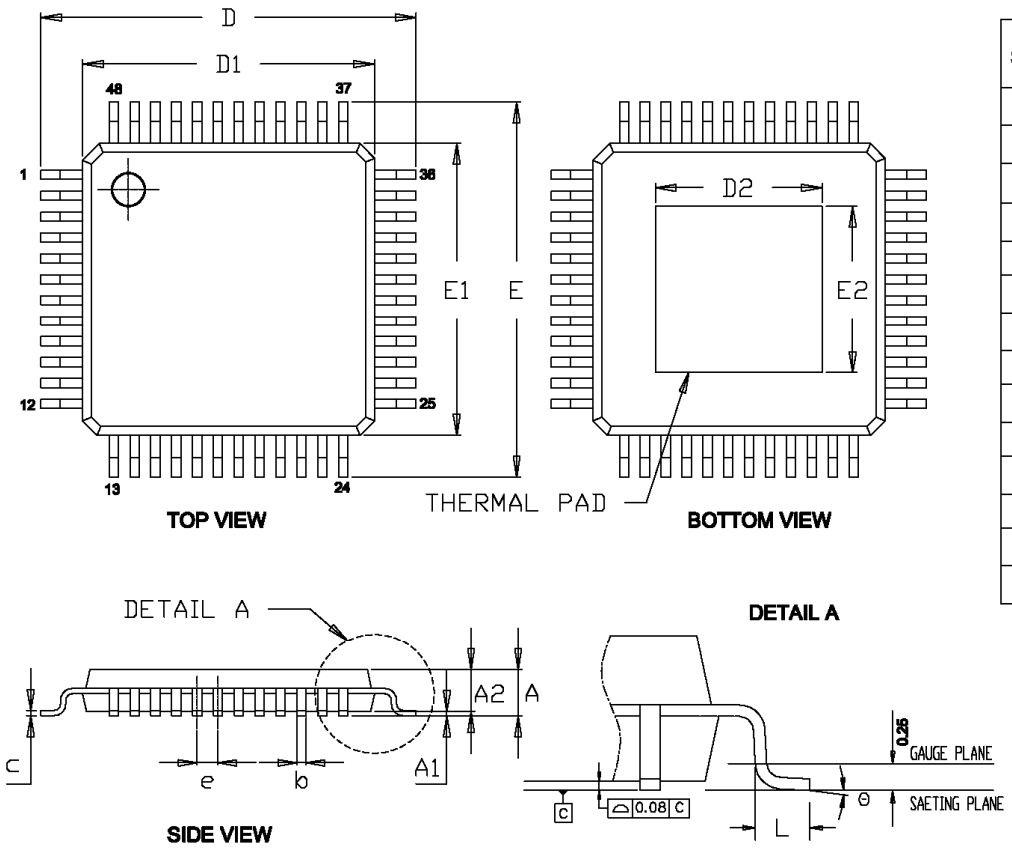
QFN-44



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.20REF		
D	4.90	5.00	5.10
E	4.90	5.00	5.10
E2	2.30	2.45	2.55
D2	2.30	2.45	2.55
b	0.15	0.20	0.25
L	0.30	0.40	0.50
L1	0.20	0.30	0.40
K	0.20	—	—
e	0.40BSC		

NOTES:
1.CONTROLLING DIMENSION:MM
2.REFERENCE DOCUMENT:NA CLOSE TOOL
3.THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHARP AMONG DIFFERENT FACTORIES.

eTQFP-48



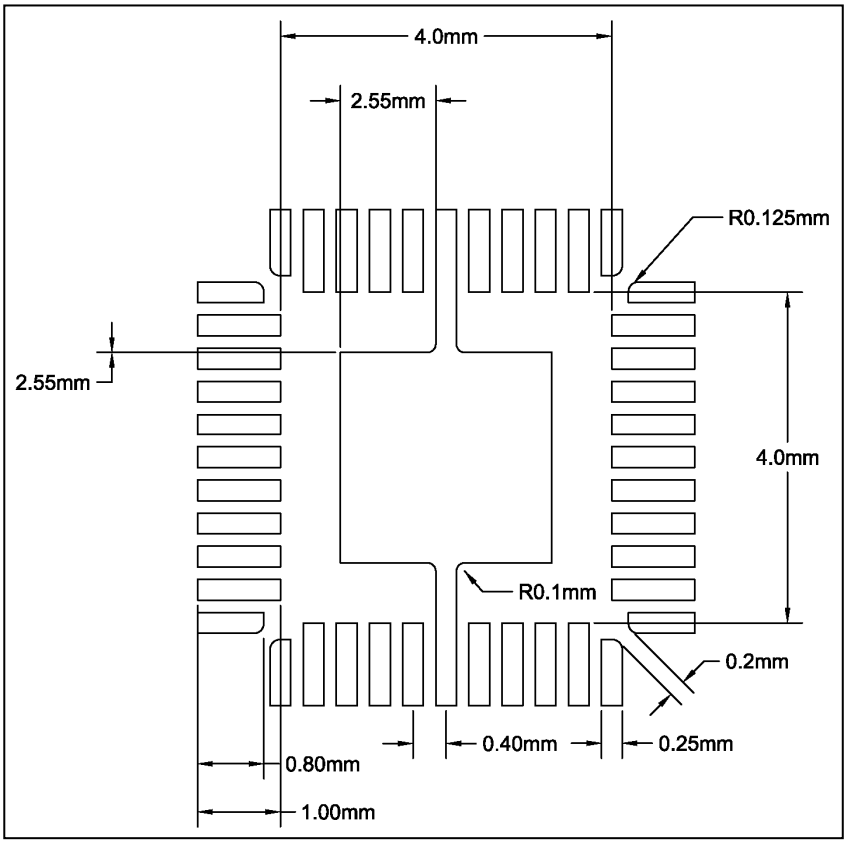
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D		9.00 BSC	
D1		7.00 BSC	
D2	4.00	—	4.21
E		9.00 BSC	
E1		7.00 BSC	
E2	4.00	—	4.21
L	0.45	0.60	0.75
b	0.17	0.22	0.27
e		0.50 BSC	
c	0.09	—	0.20
θ	0°	—	7°

NOTES:

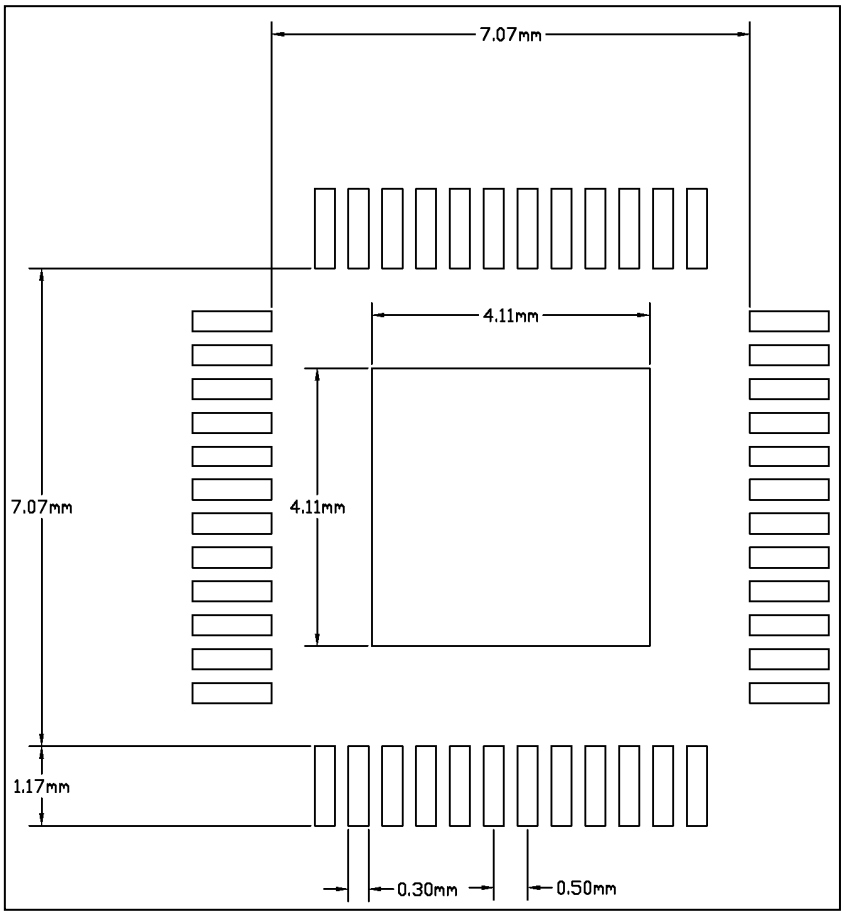
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

QFN-44



eTQFP-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2020.07.10
B	Add eTQFP-48 package, update figure 8 and figure 9	2020.09.07
C	Update QFN-44 land pattern and note 2	2021.10.08

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