# IS31FL3205

## 12-CHANNEL LED DRIVER WITH 16-BIT PWM

**March 2020**

### GENERAL DESCRIPTION

The IS31FL3205 is an LED driver with 12 constant current channels. Each channel can be pulse width modulated (PWM) by 16 bits for smooth LED brightness control. In addition, each channel has an 8-bit output current control register which allows fine tuning the current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel can be adjusted by one 8-bit global control register.

Proprietary programmable algorithms are used in IS31FL3205 to minimize audible noise caused by the MLCC decoupling capacitor. All registers can be programmed via a high speed I2C (1MHz).

IS31FL3205 can be turned off with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature.

IS31FL3205 is available in QFN-20 (3mm × 3mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

### FEATURES

- 2.7V to 5.5V supply
- Accuracy between channels and ICs: < ±6% (Max.)
- 1MHz I2C interface, automatic address increment function with readout function
- Four selectable I2C addresses
- Accurate color rendition
  - Selectable 8-bit/10-bit/12-bit/16-bit PWM
  - 8-bit dot correction
  - 8-bit global current adjust
- Open/Short detect function
- 62kHz PWM frequency (8-bit PWM)
- Temperature detect function
- EMI reduction technology
  - Spread spectrum
  - Selectable Phase Delay
  - Selectable 180 degree Clock Phase
- -40°C to +125°C temperature range
- QFN-20 (3mm×3mm) package

### APPLICATIONS

- Hand-held devices for LED display
- AI-speakers and smart home devices
- LED in home appliances

### TYPICAL APPLICATION CIRCUIT

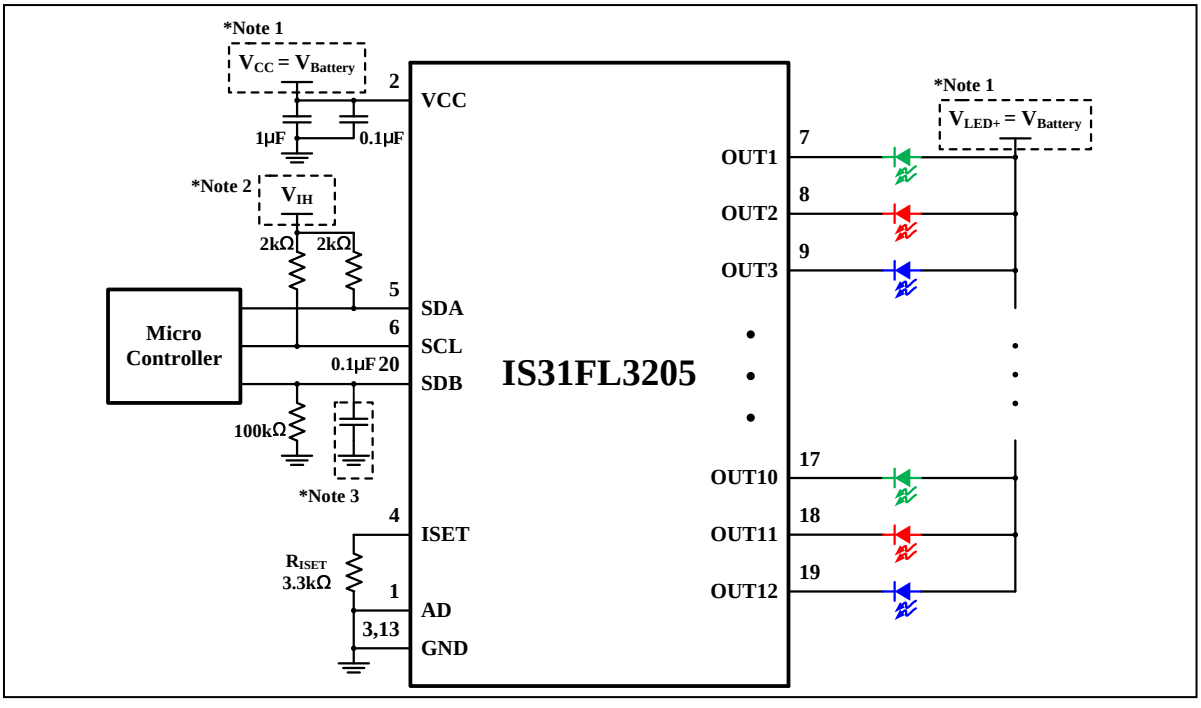



**Figure 1** Typical Application Circuit

## TYPICAL APPLICATION CIRCUIT (CONTINUED)

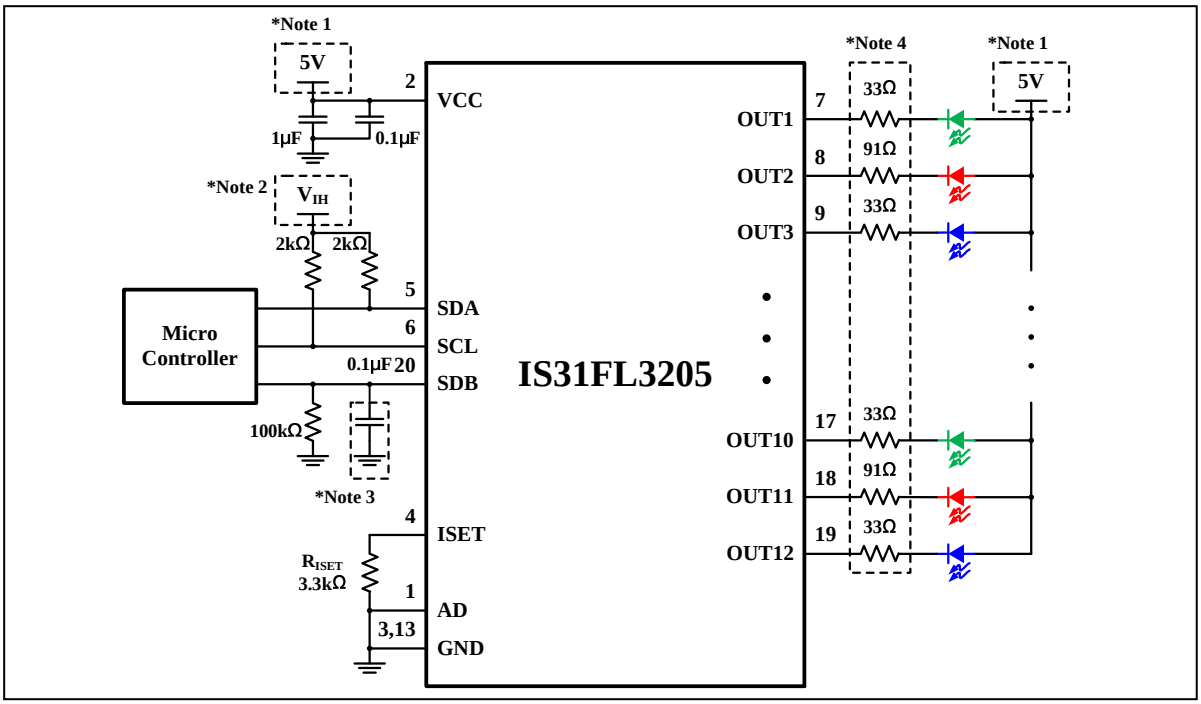



**Figure 2** Typical Application Circuit ($V_{CC}$= 5V)

**Note 1**: $V_{LED+}$ should be same as VCC voltage.

**Note 2**: $V_{IH}$ is the high level voltage for IS31FL3205, which is usually same as $V_{CC}$ of Micro Controller, e.g. if $V_{CC}$ of Micro Controller is 3.3V, $V_{IH}$=3.3V. If $V_{CC}$=5V and $V_{IH}$ is lower than 2.8V, recommend to add a level shift circuit for SDA and SCL.

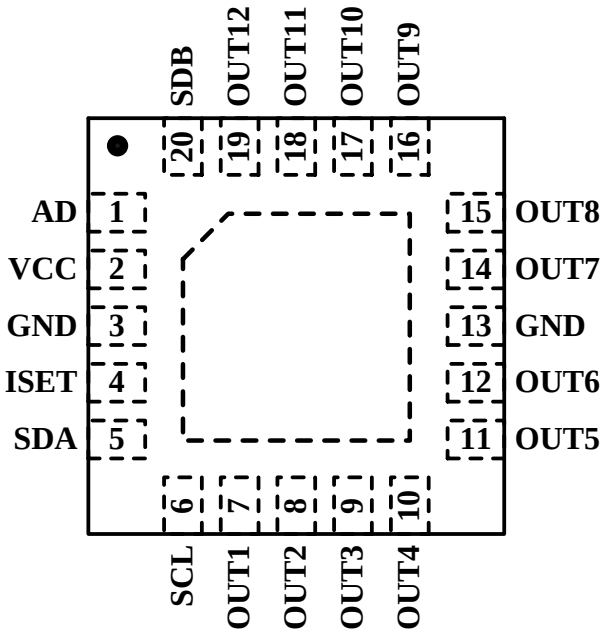
**Note 3**: A 0.1μF capacitor is necessary for passing the EFT test.

**Note 4**: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3205.

**Note 5**: The maximum output current is set to 38.25mA when $R_{ISET}$= 2kΩ. Please refer to the detail application information in $R_{ISET}$ section.

**Note 6**: The IC and LED should be placed far away from the antenna in order to prevent the EMI.

## PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---|---|
| QFN-20 |  |



## PIN DESCRIPTION

| No. | Pin | Description |
|---|---|---|
| 1 | AD | I2C address setting. |
| 2 | VCC | Power supply. |
| 3, 13 | GND | Ground. |
| 4 | ISET | Input terminal used to connect an external resistor. This regulates the global output current. |
| 5 | SDA | I2C serial data. |
| 6 | SCL | I2C serial clock. |
| 7~12 | OUT1~OUT6 | Output channel 1~6 for LEDs. |
| 14~19 | OUT7 ~ OUT12 | Output channel 7~12 for LEDs. |
| 20 | SDB | Shutdown the chip when pulled low. |
| | Thermal Pad | Connect to GND. |

## ORDERING INFORMATION

**Industrial Range: -40°C to +125°C**

| Order Part No. | Package | QTY/Reel |
|---|---|---|
| IS31FL3205-QFLS4-TR | QFN-20, Lead-free | 2500 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | -0.3V ~ +6.0V |
| Voltage at SCL, SDA, SDB, AD, OUT1 to OUT12 | -0.3V ~ $V_{CC}$+0.3V |
| Maximum junction temperature, $T_{JMAX}$ | +150°C |
| Storage temperature range, $T_{STG}$ | -65°C ~ +150°C |
| Operating temperature range, $T_A$=$T_J$ | -40°C ~ +125°C |
| Package thermal resistance (Mounted on JEDEC standard 4 layer (2s2p) PCB test board), $\theta_{JA}$ | 58°C/W |
| ESD (HBM)<br>ESD (CDM) | ±7kV<br>±750V |

**Note 7:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

Typical values are $T_A$ = 25°C, $V_{CC}$ = 5V.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | | 5.5 | V |
| $I_{MAX}$ | Output current | $V_{CC}$= 5V, $V_{OUT}$= 0.8V, $R_{ISET}$= 2kΩ, GCC= 0xFF, Scaling= 0xFF (Note 8) | | 38 | | mA |
| $I_{OUT}$ | Output current | $V_{CC}$= 5V, $V_{OUT}$= 0.6V, $R_{ISET}$= 3.3kΩ, GCC= 0xFF, SL= 0xFF | 21.39 | 23 | 24.61 | mA |
| $\Delta I_{MAT}$ | Output current mismatch between channels | $R_{ISET}$= 3.3kΩ, GCC= 0xFF, $V_{OUT}$= 0.4V, SL= 0xFF (Note 9) | -6 | | 6 | % |
| $V_{HR}$ | Headroom voltage | GCC= 0xFF,$R_{ISET}$= 3.3kΩ, $I_{OUT}$= 20mA, SL= 0xFF | | 0.3 | 0.5 | V |
| $I_{CC}$ | Quiescent power supply current | $V_{CC}$= 5V, $R_{ISET}$= 3.3kΩ, GCC= 0xFF, SL = 0xFF, $I_{OUT}$= 23mA, PWM= 0x00 | | 3.3 | 5 | mA |
| | | $V_{CC}$= 3.6V, $R_{ISET}$= 3.3kΩ, GCC= 0xFF, SL = 0xFF, $I_{OUT}$= 23mA, PWM= 0x00 | | 2.7 | 4 | mA |
| $I_{SD}$ | Shutdown current | $V_{CC}$= 5V, $R_{ISET}$= 3.3kΩ, $V_{SDB}$= 0V or software shutdown | | 2 | 3 | μA |
| | | $V_{CC}$= 3.6V, $R_{ISET}$= 3.3kΩ, $V_{SDB}$= 0V or software shutdown | | 1 | 2 | μA |
| $f_{OUT}$ | PWM frequency of output | PWM resolution 8-bit, OSC clock 8MHz | | 32 | | kHz |
| $I_{OZ}$ | Output leakage current | $V_{SDB}$ = 0V or software shutdown, $V_{OUT}$ = 5.5V | | | 0.1 | μA |
| $T_{SD}$ | Thermal shutdown | (Note 10) | | 160 | | °C |
| $T_{SD\_HY}$ | Thermal shutdown hysteresis | (Note 10) | | 13 | | °C |
| $V_{ISET}$ | Output voltage of ISET pin | | | 1.0 | | V |
| **Logic Electrical Characteristics (SDA, SCL, SDB, AD)** | | | | | | |
| $V_{IL}$ | Logic "0" input voltage | $V_{CC}$ = 2.7V~5.5V | | | 0.4 | V |
| $V_{IH}$ | Logic "1" input voltage | $V_{CC}$ = 2.7V~5.5V | 1.4 | | | V |
| $I_{IL}$ | Logic "0" input current | $V_{INPUT}$ = 0V (Note 10) | | 5 | | nA |
| $I_{IH}$ | Logic "1" input current | $V_{INPUT}$ = $V_{CC}$ (Note 10) | | 5 | | nA |

## DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 10)

| Symbol | Parameter | Fast Mode | | | Fast Mode Plus | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $f_{SCL}$ | Serial-clock frequency | - | | 400 | - | | 1000 | kHz |
| $t_{BUF}$ | Bus free time between a STOP and a START condition | 1.3 | | - | 0.5 | | - | μs |
| $t_{HD, STA}$ | Hold time (repeated) START condition | 0.6 | | - | 0.26 | | - | μs |
| $t_{SU, STA}$ | Repeated START condition setup time | 0.6 | | - | 0.26 | | - | μs |
| $t_{SU, STO}$ | STOP condition setup time | 0.6 | | - | 0.26 | | - | μs |
| $t_{HD, DAT}$ | Data hold time (Note 11) | - | | - | - | | - | μs |
| $t_{SU, DAT}$ | Data setup time (Note 12) | 100 | | - | 50 | | - | ns |
| $t_{LOW}$ | SCL clock low period | 1.3 | | - | 0.5 | | - | μs |
| $t_{HIGH}$ | SCL clock high period | 0.7 | | - | 0.26 | | - | μs |
| $t_R$ | Rise time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |
| $t_F$ | Fall time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |

**Note 8:** The recommended minimum value of $R_{ISET}$ is 2kΩ, or it may cause a large current.

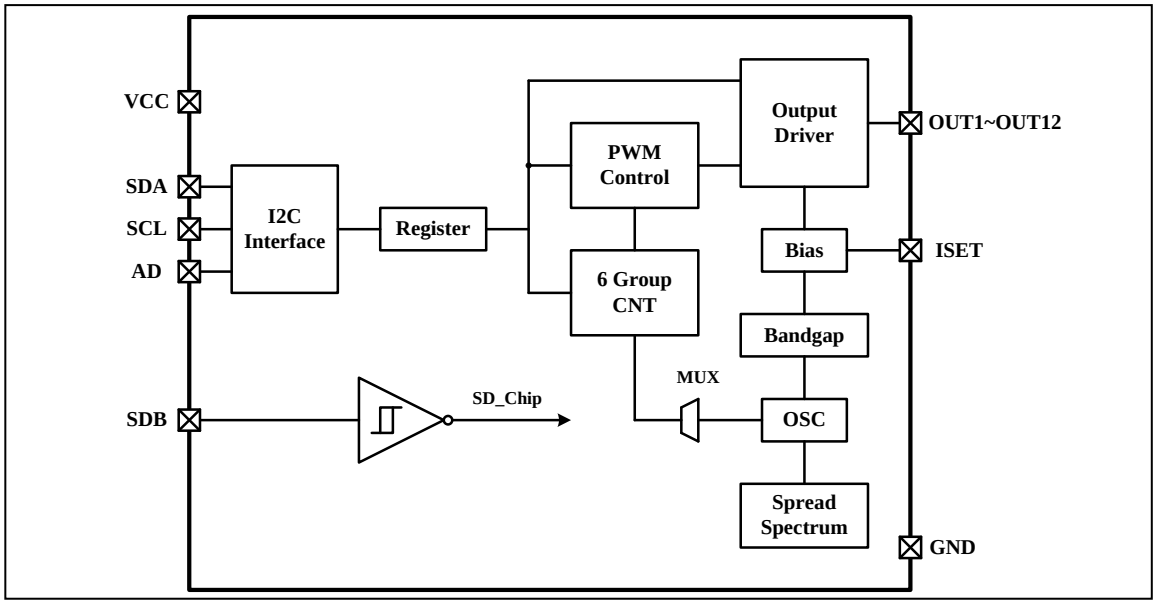
**Note 9:** $\Delta I_{MAT} = (I_{OUT} - I_{AVG})/I_{AVG} \times 100\%$. $I_{AVG} = (I_{OUT1}+I_{OUT2}+\ldots I_{OUT12})/12$.

**Note 10:** Guaranteed by design.

**Note 11:** The minimum $t_{HD, DAT}$ measured start from $V_{IL}$(Max.) of SCL signal. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. $V_{IL}$(Max.)

**Note 12:** A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU,DAT} \geq$ 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_R$ max + $t_{SU,DAT}$ = 1000 + 250 = 1250ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

## FUNCTIONAL BLOCK DIAGRAM



## DETAILED DESCRIPTION

### I2C INTERFACE

The IS31FL3205 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3205 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin. The complete slave address is:

**Table 1 Slave Address (Write Only):**

| Bit | A7:A3 | A2:A1 | A0 |
|---|---|---|---|
| Value | 01101 | AD | 0 |

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drian) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3205.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3205's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3205 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3205, the register address byte is sent, most significant bit first. IS31FL3205 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3205 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

### ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3205, load the address of the data register that the first data byte is intended for. During the IS31FL3205 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3205 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3205 (Figure 6).

### READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3205 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3205 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3205 to the master (Figure 7).

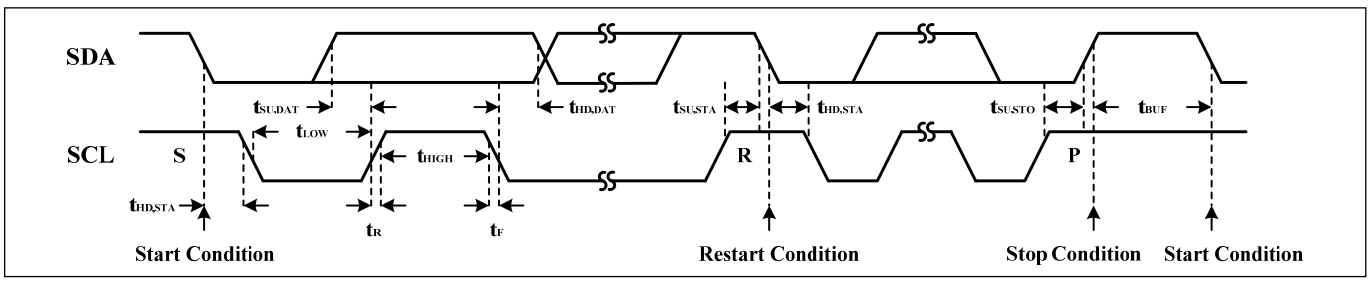



**Figure 3** Interface Timing

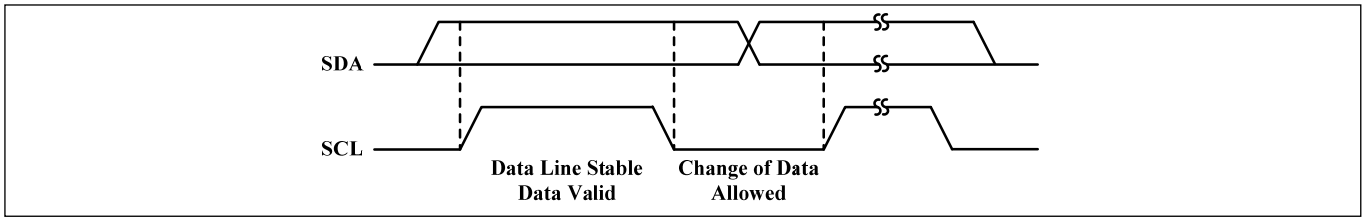



**Figure 4** Bit Transfer

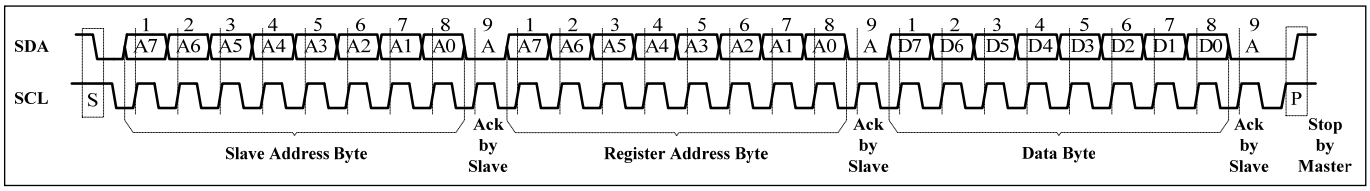



**Figure 5** Writing to IS31FL3205 (Typical)

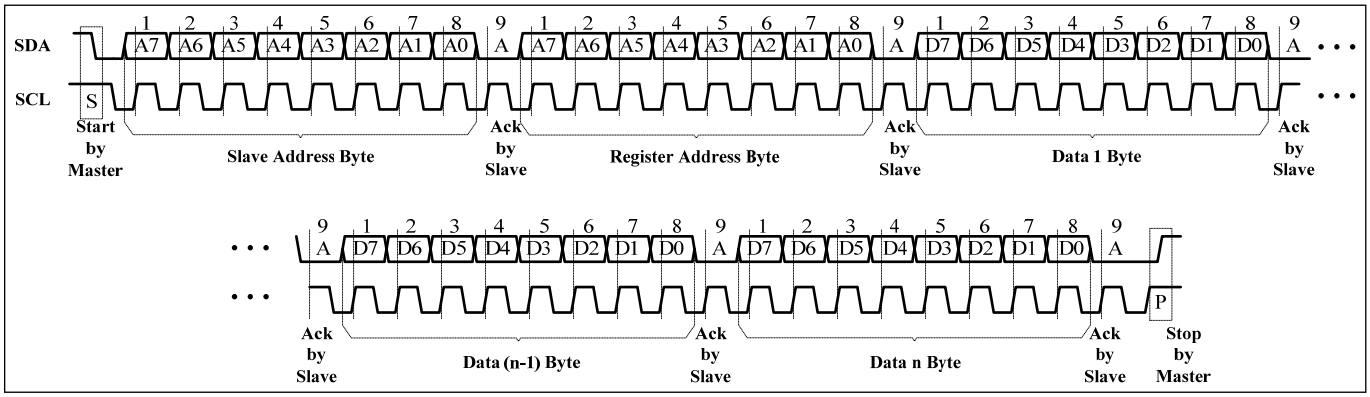



**Figure 6** Writing to IS31FL3205 (Automatic Address Increment)

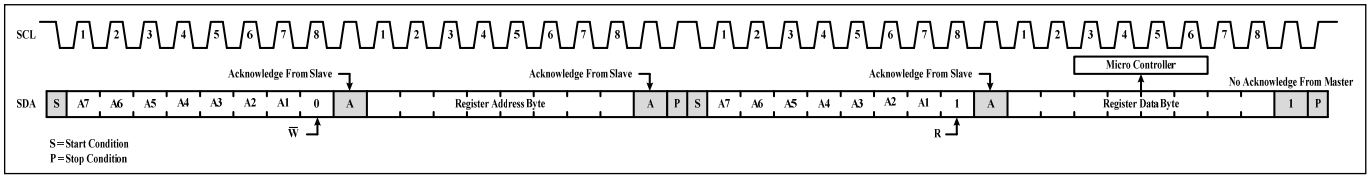



**Figure 7** Reading from IS31FL3205

## REGISTER DEFINITIONS

**Table 2 Register Function**

| Address | Name | Function | R/W | Table | Default |
|---|---|---|---|---|---|
| 00h | Control Register | Power control register | R/W | 3 | 0000 0000 |
| 07h~1Eh | PWM Register | Channel [12:1] PWM register byte | R/W | 5 | |
| 49h | Update Register | Update the PWM and Scaling data | W | - | |
| 4Dh~58h | LED Scaling Register | Control each channel's DC current | R/W | 7 | |
| 6Eh | Global Current Control Register | Control Global DC current/SSD | R/W | 8 | |
| 70h | Phase Delay and Clock Phase Register | Phase Delay and Clock Phase | R/W | 9 | |
| 71h | Open Short Detect Enable Register | Open short detect enable | R/W | 10 | |
| 72h~73h | LED Open/Short Register | Open short information | R/W | 11 | |
| 77h | Temperature Sensor Register | Temperature information | R/W | 12 | |
| 78h | Spread Spectrum Register | Spread spectrum control register | R/W | 13 | |
| 7Fh | Reset Register | Reset all registers | W | - | |

**Table 3 00h Control Register**

| Bit | D7 | D6:D4 | D3 | D2:D1 | D0 |
|---|---|---|---|---|---|
| Name | - | OSC | - | PMS | SSD |
| Default | 0 | 000 | 0 | 00 | 0 |

The Control Register sets software shutdown mode, internal oscillator clock frequency and PWM resolution. The internal oscillator clock frequency and the PWM resolution will decide the output PWM frequency. Recommend selecting PWM frequency higher than 20kHz to avoid MLCC audible noise as shown in Table 4.

**SSD** Software Shutdown Enable
0 Software shutdown mode
1 Normal operation

**PMS** PWM Resolution
00 N=256, 8-bit
01 N=1024, 10-bit
10 N=4096, 12-bit
11 N=65536, 16-bit

**OSC** Oscillator Clock Frequency Selection
000 16MHz
001 8MHz
010 1MHz
011 500kHz
100 250kHz
101 125kHz
110 62kHz
111 31kHz

**Table 4 PWM Frequency**

| PWM Resolution | 16M | 8M | 1M | 500k | 250k | 125k | 62k | 31k |
|---|---|---|---|---|---|---|---|---|
| 8bit | 62k | 32k | 4k | 2k | 1k | 0.5k | 244 | 122 |
| 10bit | 16k | 8k | 1k | 0.5k | 244 | 122 | NA | NA |
| 12bit | 4k | 2k | 244 | 122 | NA | NA | NA | NA |
| 16bit | 244 | 122 | NA | NA | NA | NA | NA | NA |

**Table 5 07h~1Eh PWM Register**

| Reg | 08h (0Ah, 0Ch…) | 07h (09h, 0Bh…) |
|---|---|---|
| Bit | D7:D0 | D7:D0 |
| Name | PWM_H | PWM_L |
| Default | 0000 0000 | 0000 0000 |

Each output has 2 bytes to modulate the PWM duty in 256/1024/4096/65536 steps. If using 8 bit PWM resolution, only PWM_L bits need to be set.
The value of the SL (Scaling Register) decides the peak current of each LED noted as $I_{OUT}$.
$I_{OUT}$ and the value of the PWM Registers decide the average current of each LED noted as $I_{LED}$.
$I_{OUT}$ is computed by Formula (1):

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (1)$$

$I_{LED}$ computed by Formula (2):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT} \qquad (2)$$

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$

N=1024: $PWM = \sum_{n=0}^{9} D[n] \cdot 2^n$

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$

N=65536: $PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$ (3)

Where $I_{OUT(MAX)}$ is the maximum output current decided by $R_{ISET}$ (Check $R_{ISET}$ section for more information), GCC is the global current setting (6Eh), and SL is the scaling of each output (4Ah~6Dh), N=256/1024/4096/65536(8/10/12/16 bit PWM resolution).

For example: $R_{ISET}$=3.3kΩ, GCC=0xFF, SL=0xFF, PMS= "11" (16-bit PWM resolution), PWM_H=0xFF, PWM_L=0xFF, $I_{OUT(MAX)}$= 23.18mA

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{255}{256} \times \frac{255}{256} = 23mA \quad (1)$$

$$PWM = \sum_{n=0}^{15} D[n] \cdot 2^n = 65535 \quad (3)$$

N= 65536

$$I_{LED} = \frac{65535}{65536} \times 23mA = 23mA \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by $R_{ISET}$ (Check $R_{ISET}$ section for more information)

The $I_{OUT}$ of each channel is set by the SL bits of LED Scaling Register (4Ah~6Dh). Please refer to the detail information in Table 7.

If $R_{ISET}$=3.3kΩ, GCC=0xFF, SL=0xFF, PMS= "00" (8-bit PWM resolution, only use the PWM_L, the PWM_H will be ignored), PWM_H=0x77, PWM_L=0xAA,

$I_{OUT(MAX)}$ = 23.18mA

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{255}{256} \times \frac{255}{256} = 23mA \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n = 170 \quad (3)$$

N= 256

$$I_{LED} = \frac{170}{256} \times 23mA \quad (2)$$

**Table 6 PWM and Scaling Register Map**

| OUT | PWM | | SL |
|---|---|---|---|
| | PWM_H | PWM_L | |
| 1 | 08h | 07h | 4Dh |
| 2 | 0Ah | 09h | 4Eh |
| 3 | 0Ch | 0Bh | 4Fh |
| 4 | 0Eh | 0Dh | 50h |
| 5 | 10h | 0Fh | 51h |
| 6 | 12h | 11h | 52h |
| 7 | 14h | 13h | 53h |
| 8 | 16h | 15h | 54h |
| 9 | 18h | 17h | 55h |
| 10 | 1Ah | 19h | 56h |
| 11 | 1Ch | 1Bh | 57h |
| 12 | 1Eh | 1Dh | 58h |

### 49h Update Register

When SDB = "H" and SSD = "1", a write of "0000 0000" to 49h is to update the PWM Registers (07h~1Eh) values.

**Table 7 4Dh~58h LED Scaling Register**

| Bit | D7:D0 |
|---|---|
| Name | SL |
| Default | 0000 0000 |

Each output has 8 bits to modulate DC current in 256 steps.

The value of the LED Scaling Registers decides the DC peak current of each LED noted $I_{OUT}$.

$I_{OUT}$ is computed by Formula (1):

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (1)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (4)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by $R_{ISET}$, GCC is the global current setting (6Eh)

4Dh~58h don't need to update by 49h, each register will be updated immediately when it is written.

**Table 8 6Eh Global Current Control Register**

| Bit | D7:D0 |
|---|---|
| Name | GCC |
| Default | 0000 0000 |

GCC and SL control the $I_{OUT}$ as shown in Formula (1).

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (5)$$

If GCC=0xFF, SL=0xFF, $I_{OUT}=I_{OUT(MAX)}$
If GCC=0x01, SL=0xFF,

$$I_{OUT} = I_{OUT\ (MAX)} \times \frac{1}{256} \times \frac{255}{256}$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by $R_{ISET}$ (Check $R_{ISET}$ section for more information).

**Table 9 70h Phase Delay and Clock Phase Register**

| Bit | D7 | D6:D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| Name | PDE | - | PS3 | PS2 | PS1 |
| Default | 0 | 0000 | 0 | 0 | 0 |

IS31FL3205 features a 3 phase delay function, when PDE bit is set, the phase delay function is enabled.

Phase Delay separates 12 outputs as 3 groups, OUT1~OUT3 as group 1, OUT4~OUT9 as group 2, OUT10~OUT12 as group 3. When Phase Delay is enabled, group 2 has a $1/(3*f_{OUT})$ time delay than group 1, group 3 also has a $1/(3*f_{OUT})$ time delay than group 2.

Phase Delay feature and Clock Phase options can work together to minimize the voltage ripple of LED power supply.

**PDE** Group Phase Delay Enable
0 Phase delay disable
1 Phase delay enable

**PS1** OUT1~OUT3 Phase Select
0 Phase delay 0 Degree
1 Phase delay 180 Degree

**PS2** OUT4~OUT9 Phase Select
0 Phase delay 0 Degree
1 Phase delay 180 Degree

**PS3** OUT10~OUT12 Phase Select
0 Phase delay 0 Degree
1 Phase delay 180 Degree

**Table 10 71h Open Short Detect Enable Register**

| Bit | D7:D2 | D1:D0 |
|---|---|---|
| Name | - | OSDE |
| Default | 0000 00 | 00 |

OSDE enables the open and/or short LED channel detection with the result stored in 72h~76h, note either open or short information is saved not both.

**OSDE** Open Detect Enable
00 Detect disable
01 Detect disable
10 Short detect enable
11 Open detect enable

**Table 11-1 72h LED Open/Short Register**

| Bit | D7:D3 | D2:D0 |
|---|---|---|
| Name | OP/ST[5:1] | - |
| Default | 0000 0 | xxx |

**Table 11-2 73h LED Open/Short Register**

| Bit | D7 | D6:D0 |
|---|---|---|
| Name | - | OP/ST[12:6] |
| Default | x | 000 0000 |

Open or short status is stored in 72h to 73h.

**OP[12:1]** Open Information of OUT12:OUT1
0 Open not detected
1 Open detected

**ST[12:1]** Short Information of OUT12:OUT1
0 Short not detected
1 Short detected

**Table 12 77h Temperature Sensor Register**

| Bit | D7:D6 | D5 | D4 | D3:D2 | D1:D0 |
|---|---|---|---|---|---|
| Name | TROF | - | T_Flag | - | TS |
| Default | 00 | 0 | 0 | 00 | 00 |

TS stores the temperature/thermal roll-off point. TROF stores percentage of output current of the thermal rool-off function.

Read T_Flag can indicate if the die temperature exceeds the setting point (TS). Before each reading of 77h register, TROF and TS need to be re-written.

**TROF** Thermal roll off percentage of output current
00 100%
01 75%
10 55%
11 30%

| | |
|---|---|
| **T_Flag** | Temperature Flag |
| 0 | Temperature point not exceeded |
| 1 | Temperature point exceeded |

| | |
|---|---|
| **TS** | Temperature Point, Thermal roll off start point |
| 00 | 140°C |
| 01 | 120°C |
| 10 | 100°C |
| 11 | 90°C |

**Table 13 78h Spread Spectrum Register**

| Bit | D7:D5 | D4 | D3:D2 | D1:D0 |
|---|---|---|---|---|
| Name | DCPWM | SSP | RNG | CLT |
| Default | 000 | 0 | 00 | 00 |

When DCPWM is set to “0”, the PWM outputs are decided by 01h~1Eh, and the PWM range is 0/256~255/256(8-bit PWM, 0/1024~1023/1024 for 10 bit PWM, 0/4096~4095/4096 for 12 bit PWM, 0/65536~65535/65536 for 16 bit PWM), still the 1/256(8-bit PWM, 1/1024 for 10 bit PWM, 1/4096 for 12 bit PWM, 1/65536 for 16 bit PWM), can’t be turned on. When the DCPWM is set to “1”, PWM dimming is disabled and dimming will be done by current adjust GCC and SL registers.

Spread spectrum register configures the spread spectrum function, adjust the cycle time and range.

| | |
|---|---|
| **DCPWM** | Setting the output to work in DC mode |
| xx0 | Output 1~9 PWM data set by registers 01h~18h |
| xx1 | Output 1~9 set to turn on (PWM is disabled) |
| x0x | Output 10~12 PWM data set by registers 19h~1Eh |
| x1x | Output 10~12 set to turn on (PWM is disabled) |

| | |
|---|---|
| **SSP** | Spread Spectrum Enable |
| 0 | Disable |
| 1 | Enable |

| | |
|---|---|
| **RNG** | Spread Spectrum Range |
| 00 | ±5% |
| 01 | ±15% |
| 10 | ±24% |
| 11 | ±34% |

| | |
|---|---|
| **CLT** | Spread Spectrum Cycle Time |
| 00 | 1980μs |
| 01 | 1200μs |
| 10 | 820μs |
| 11 | 660μs |

### 7Fh Reset Register

When SDB = “H” and SSD = “1”, A write of “0000 0000” to 7Fh will reset all registers to their default values.

## APPLICATION INFORMATION

### RISET

The maximum output current $I_{OUT(MAX)}$ of OUT1~OUT12 can be adjusted by the external resistor, $R_{ISET}$, as described in Formula (6).

$$I_{OUT\ (MAX\ )} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (6)$$

x = 76.5, $V_{ISET}$ = 1.0V.

The recommended minimum value of $R_{ISET}$ is 2kΩ.

When $R_{ISET}$=3.3kΩ, $I_{OUT(MAX)}$=23.18mA

When $R_{ISET}$=2kΩ, $I_{OUT(MAX)}$=38.25mA

$R_{ISET}$ should be close to the chip and the ground side should well connect to the GND plane.

### CURRENT SETTING

The maximum output current is set by the external register $R_{ISET}$. The current of each output can also be set independently by the SL 8 bits of LED Scaling Register (4Dh~58h).

Some applications may require the IOUT of each channel need to be adjusted independently. For example, if OUT1 drives 1 LED and OUT2 drives 2 parallel LEDs, and they should have the same average current like 18mA, we can set the $I_{OUT(MAX)}$ to 36mA, and GCC=0xFF, 4Ah=0x80, 4Bh=0xFF, the OUT1 sinks about 18mA and OUT2 sinks 36mA which can have two LEDs in parallel.

Another example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED, with same $R_{ISET}$, GCC and same SL bits, when OUT1 OUT2 and OUT3 have the same PWM value, the LED may looks a litter pink, or not so white, in this case, the SL bits can be used to adjust the single IOUTx of some output and make it pure white color. We call this SL bits another name: white balance registers.

### PWM CONTROL

The PWM Registers (07h~1Eh) can modulate LED brightness of each 12 channels with 256/1024/4096/65536 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

### PWM FREQUENCY SELECT

The IS31FL3205 output channels operate with a default 8 bit PWM resolution and the PWM frequency of 62kHz (the oscillator frequency is 16MHz). Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 300Hz to 18kHz, To avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3205’s output PWM frequency above/below the audible range. The Control Register (00h) can be used to set the switching frequency to 122Hz~62kHz as shown in Table 4, some combine setting of the OSC and PMS bits will get different output PWM frequency, and higher than 20kHz or is out of the audible range.

### OPEN/SHORT DETECT FUNCTION

IS31FL3205 has open and short detect bit for each LED.

By setting the OSDE bit of Open Short Detect Enable Register (71h) from “00” to “10” (store short information) or “11” (store open information), the LED Open/Short Register will store the open/short information immediately the MCU can get the open/short information by reading the 72h~73h.

### SPREAD SPECTRUM FUNCTION

PWM current switching of LED outputs can be particularly troublesome when the EMI is concerned. To optimize the EMI performance, the IS31FL3205 includes a spread spectrum function. By setting the RNG bit of Spread Spectrum Register (78h), Spread Spectrum range can be choose from ±5% /±15% /±24% /±34%. The spread spectrum function will lower the total electromagnetic emitting energy by spreading the energy into a wider range to significantly degrade the peak energy of EMI. With spread spectrum, the EMI test is easier to pass with a smaller size and lower cost filter circuit.

### OPERATING MODE

IS31FL3205 can only operate in PWM Mode. The brightness of each LED can be modulated with 256/1024/4096/65536 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

## SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

### Software Shutdown

By setting the SSD bit of the Control Register (00h) to "0", the IS31FL3205 will operate in software shutdown mode. When the IS31FL3205 is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers accessible. Typical current consume is 1μA ($V_{CC}$=3.6V).

### Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consumption is 1μA ($V_{CC}$=3.6V).

The chip releases hardware shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but the register information retains. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

## LAYOUT

The IS31FL3205 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

### Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks' supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1μF capacitor, if possible with a 1μF capacitor is recommended to connected to the ground at power supply pin of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

### $R_{ISET}$

$R_{ISET}$ should be close to the chip and the ground side should well connect to the GND plane.

### Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. The thermal pad of IS31FL3205 should connect to GND net and need to use 4 or 9 vias connect to GND copper area, the GND area should be as large area as possible to help radiate the heat from the IS31FL3205.

### Current Rating Example

For a $R_{ISET}$=3.3kΩ application, the current rating for each net is as follows:

• VCC pin maximum current is 5mA when $V_{CC}$=5V, but the VLED+ net is provide total current of all outputs, its current can as much as 23mA×12=276mA, recommend trace width for VCC pin: 0.20mm~0.3mm, recommend trace width for VLED+ net: 0.25mm~0.4mm,

• Output pins=23mA, recommend trace width is 0.2mm~0.254mm

• All other pins<3mA, recommend trace width is 0.15mm~0.254mm

## CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|---|
| **Preheat & Soak**<br>Temperature min (Tsmin)<br>Temperature max (Tsmax)<br>Time (Tsmin to Tsmax) (ts) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3°C/second max. |
| Liquidous temperature (TL)<br>Time at liquidous (tL) | 217°C<br>60-150 seconds |
| Peak package body temperature (Tp)* | Max 260°C |
| Time (tp)** within 5°C of the specified classification temperature (Tc) | Max 30 seconds |
| Average ramp-down rate (Tp to Tsmax) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

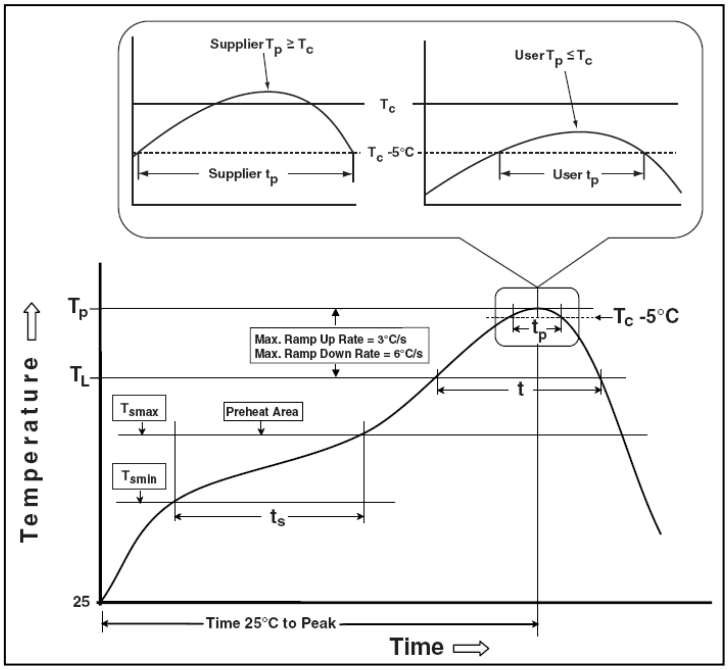
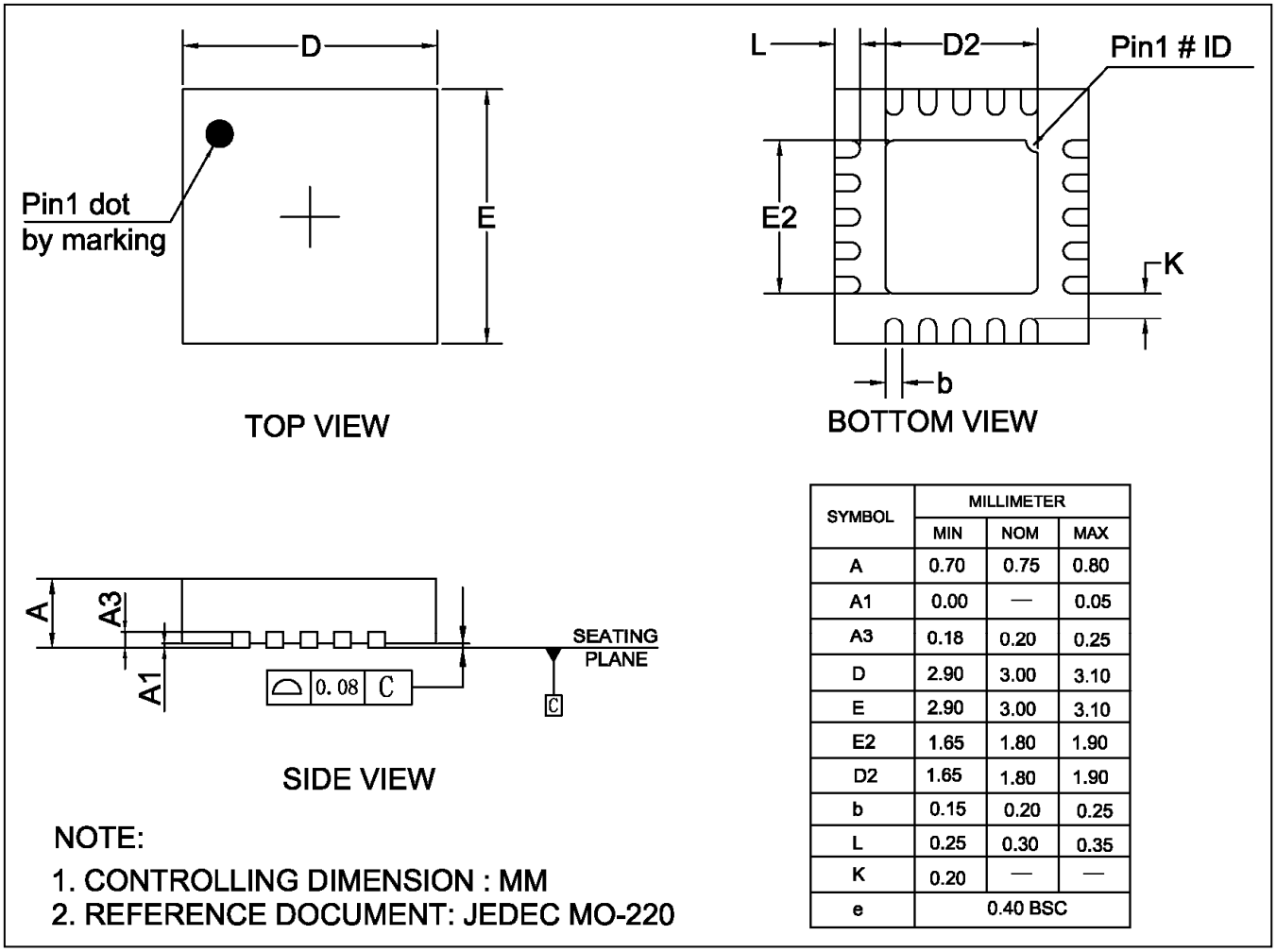



**Figure 8** Classification Profile

## PACKAGE INFORMATION

### QFN-20



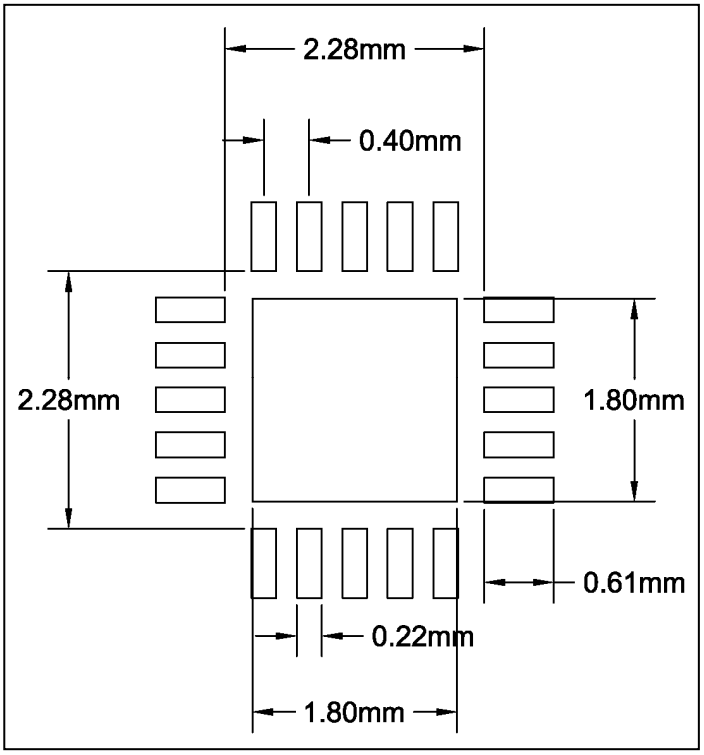

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | — | 0.05 |
| A3 | 0.18 | 0.20 | 0.25 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.65 | 1.80 | 1.90 |
| D2 | 1.65 | 1.80 | 1.90 |
| b | 0.15 | 0.20 | 0.25 |
| L | 0.25 | 0.30 | 0.35 |
| K | 0.20 | — | — |
| e | 0.40 BSC | | |

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

## RECOMMENDED LAND PATTERN

### QFN-20




**Note:**

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

## REVISION HISTORY

| Revision | Detail Information | Date |
|---|---|---|
| A | Initial release. | 2020.02.27 |

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