

1M x 36 and 2M x 18 36Mb, FLOW THROUGH 'NO WAIT' STATE BUS SRAM

FEBRUARY 2012

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single Read/Write control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{\text{CKE}}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP package
- Power supply:
NVF: $V_{\text{DD}} 2.5\text{V} (\pm 5\%)$, $V_{\text{DDQ}} 2.5\text{V} (\pm 5\%)$
NLF: $V_{\text{DD}} 3.3\text{V} (\pm 5\%)$, $V_{\text{DDQ}} 3.3\text{V}/2.5\text{V} (\pm 5\%)$
- Industrial temperature available
- Lead-free available

DESCRIPTION

The 36 Meg 'NLF/NVF' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 1M words by 36 bits and 2M words by 18 bits, fabricated with ISSI's advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{\text{CKE}}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{\text{WE}}$ is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

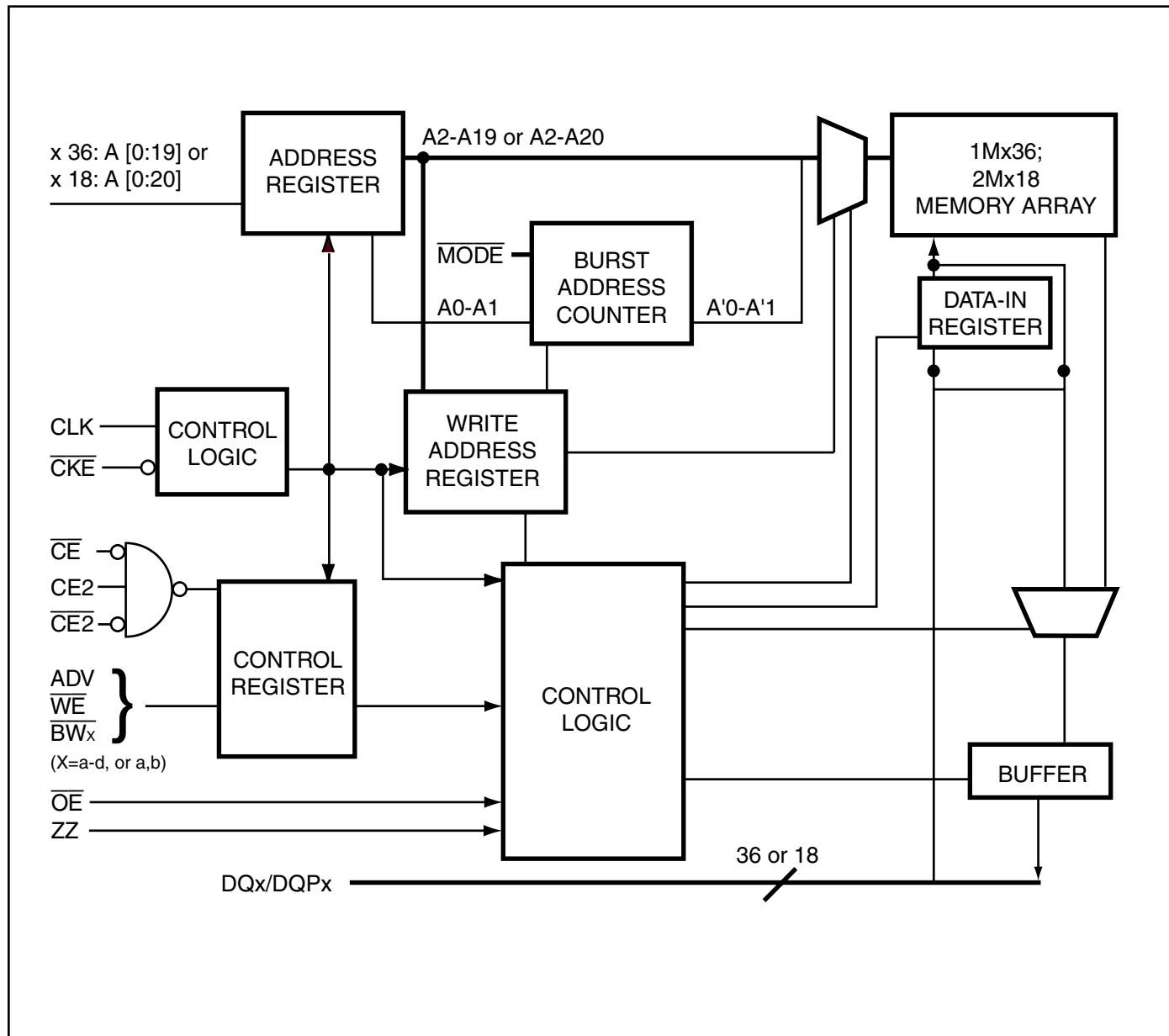
Symbol	Parameter	6.5	7.5	Units
t_{KQ}	Clock Access Time	6.5	7.5	ns
t_{KC}	Cycle Time	7.5	8.5	ns
	Frequency	133	117	MHz

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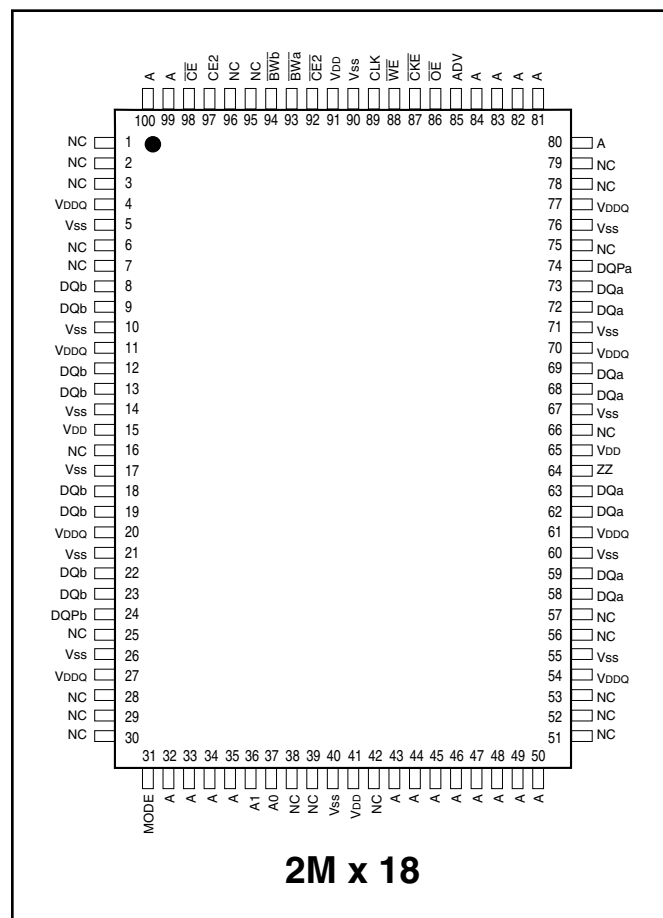
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

BLOCK DIAGRAM



Pinout diagram of the 1M x 36 DRAM chip. The chip is a square package with pins numbered 1 to 50 on the left and 80 to 31 on the right. The top edge has pins 100 to 81, and the bottom edge has pins 31 to 50. The diagram shows the pin numbers, the pin symbols, and the corresponding signal names. A black dot is located on pin 1.

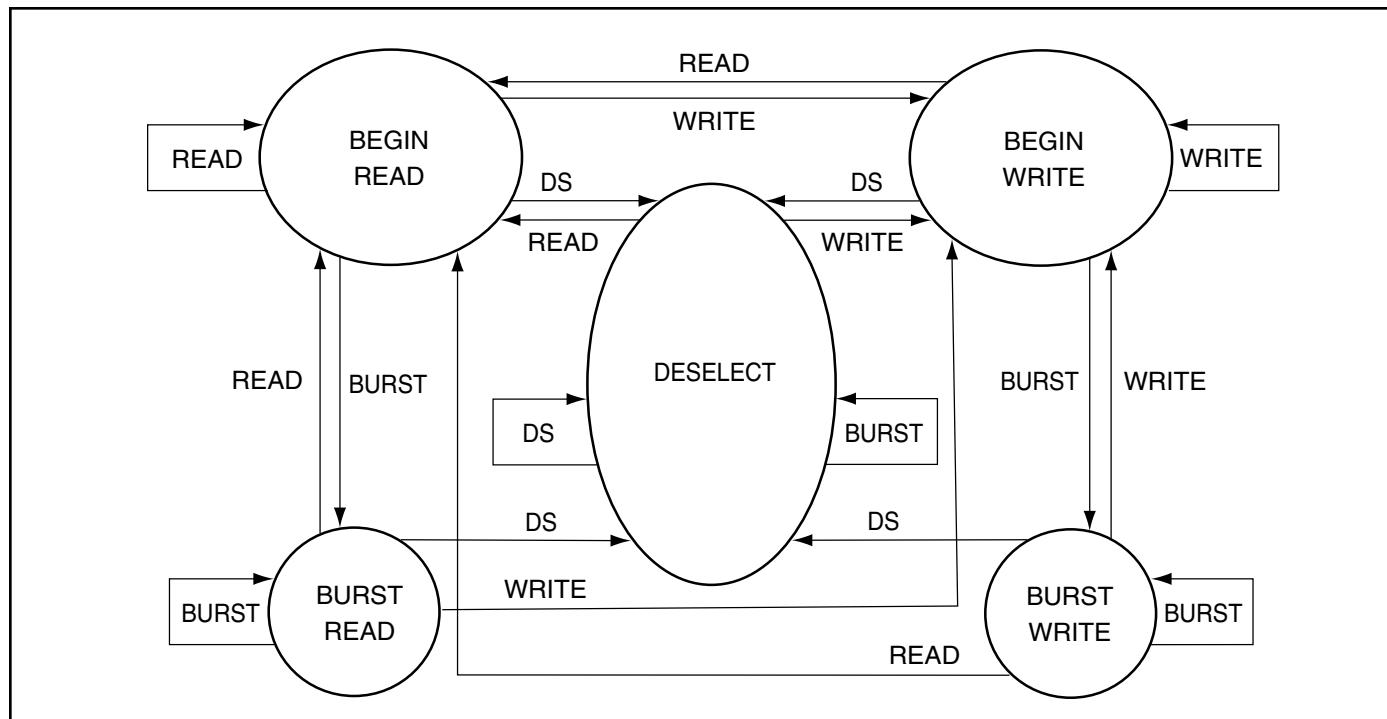
Pin	Signal	Pin	Signal
1	DQpC	80	DQpB
2	DQc	79	DQb
3	DQc	78	DQb
4	VDDQ	77	VDDQ
5	Vss	76	Vss
6	DQc	75	DQb
7	DQc	74	DQb
8	DQc	73	DQb
9	DQc	72	DQb
10	Vss	71	Vss
11	VDDQ	70	VDDQ
12	DQc	69	DQb
13	DQc	68	DQb
14	Vss	67	Vss
15	VDD	66	NC
16	NC	65	VDD
17	Vss	64	ZZ
18	DQd	63	DQa
19	DQd	62	DQa
20	VDDQ	61	VDDQ
21	Vss	60	Vss
22	DQd	59	DQa
23	DQd	58	DQa
24	DQd	57	DQa
25	DQd	56	DQa
26	Vss	55	Vss
27	VDDQ	54	VDDQ
28	DQd	53	DQa
29	DQd	52	DQa
30	DQpd	51	DQPa
31	MODE		
32	A		
33	A		
34	A		
35	A		
36	A1		
37	A0		
38	NC		
39	NC		
40	Vss		
41	VDD		
42	NC		
43	A		
44	A		
45	A		
46	A		
47	A		
48	A		
49	A		
50	A		



A0, A1	Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{\text{BWA}}\text{--}\overline{\text{BWd}}$	Synchronous Byte Write Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CKE}}$	Clock Enable
Vss	Ground for Core
NC	Not Connected

$\overline{\text{CE}}$, CE2 , $\overline{\text{CE2}}$	Synchronous Chip Enable
$\overline{\text{OE}}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data I/O
MODE	Burst Sequence Selection
V_{DD}	+3.3V/2.5V Power Supply
V_{SS}	Ground for output Buffer
V_{DDQ}	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE⁽¹⁾

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:

- "X" means don't care.
- The rising edge of clock is symbolized by ↑
- A continue deselect cycle can only be entered if a deselect cycle is executed first.
- $\overline{WE} = L$ means Write operation in Write Truth Table.
 $\overline{WE} = H$ means Read operation in Write Truth Table.
- Operation finally depends on status of asynchronous pins (ZZ and $\overline{OE}$).

ASYNCHRONOUS TRUTH TABLE⁽¹⁾

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTES	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36)

Operation	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTES	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

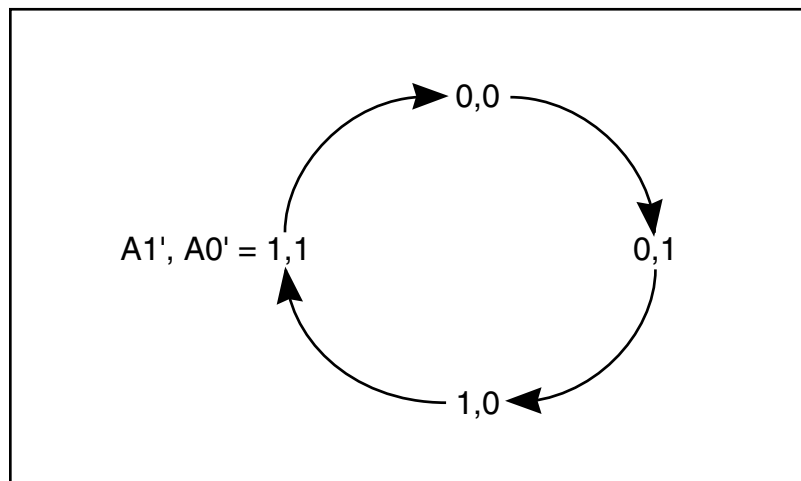
Notes:

1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	–65 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to V _{SS} for I/O Pins	–0.5 to V _{DDQ} + 0.3	V
V _{IN}	Voltage Relative to V _{SS} for for Address and Control Inputs	–0.3 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLFx)

Range	Ambient Temperature	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61NVF_x)

Range	Ambient Temperature	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	3.3V		2.5V		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0 mA (3.3V) I _{OH} = -1.0 mA (2.5V)	2.4	—	2.0	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{DD} + 0.3	1.7	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	-0.3	0.7	V
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{DD} ⁽¹⁾	-5	5	-5	5	μA
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{DDQ} , OE = V _{IH}	-5	5	-5	5	μA

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	6.5 MAX		7.5 MAX		Unit
				x18	x36	x18	x36	
I _{CC}	AC Operating Supply Current	Device Selected, OE = V _{IH} , ZZ ≤ V _{IL} , All Inputs ≤ 0.2V or ≥ V _{DD} - 0.2V, Cycle Time ≥ t _{kc} min.	Com. Ind. typ. ⁽²⁾	400 425 390	400 425	375 400 340	375 400	mA
I _{SB}	Standby Current TTL Input	Device Deselected, V _{DD} = Max., All Inputs ≤ V _{IL} or ≥ V _{IH} , ZZ ≤ V _{IL} , f = Max.	Com. Ind.	200 210	200 210	190 200	190 200	mA
I _{SBI}	Standby Current CMOS Input	Device Deselected, V _{DD} = Max., V _{IN} ≤ V _{SS} + 0.2V or ≥ V _{DD} - 0.2V f = 0	Com. Ind. typ. ⁽²⁾	100 105 40	100 105	100 105 40	100 105	mA

Note:

1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100 μA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} - 0.2V.
2. Typical values are measured at V_{CC} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

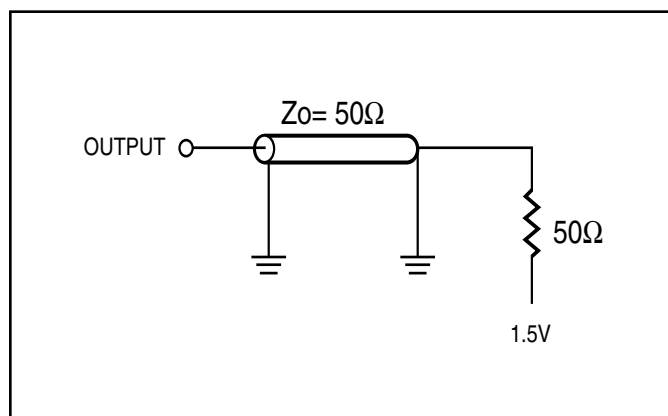


Figure 1

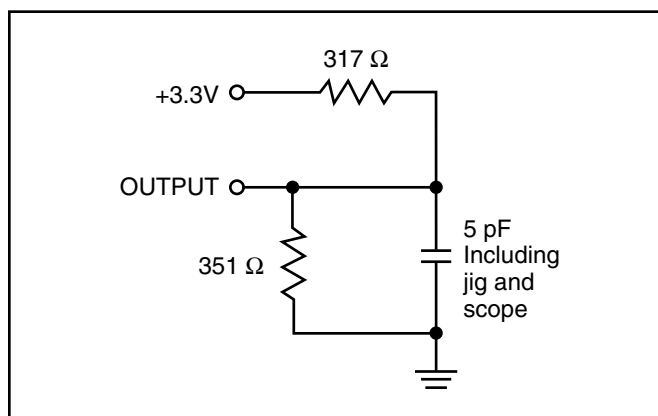


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

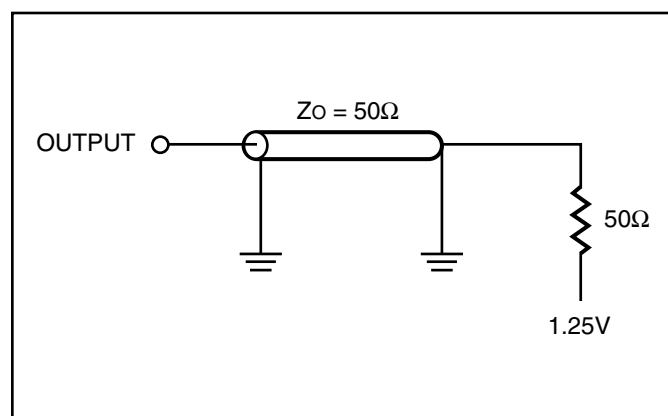


Figure 3

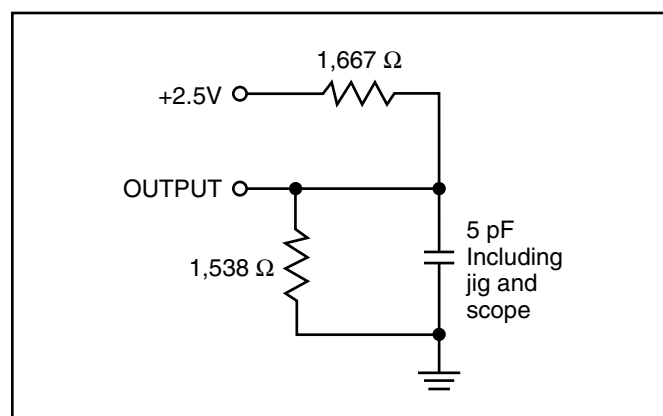


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	6.5		7.5		Unit
		Min.	Max.	Min.	Max.	
fmax	Clock Frequency	—	133	—	117	MHz
t _{KC}	Cycle Time	7.5	—	8.5	—	ns
t _{KH}	Clock High Time	2.2	—	2.5	—	ns
t _{KL}	Clock Low Time	2.2	—	2.5	—	ns
t _{KQ}	Clock Access Time	—	6.5	—	7.5	ns
t _{KQX} ⁽²⁾	Clock High to Output Invalid	2.5	—	2.5	—	ns
t _{KQLZ} ^(2,3)	Clock High to Output Low-Z	2.5	—	2.5	—	ns
t _{KQHZ} ^(2,3)	Clock High to Output High-Z	—	3.8	—	4.0	ns
t _{OEQ}	Output Enable to Output Valid	—	3.2	—	3.4	ns
t _{OELZ} ^(2,3)	Output Enable to Output Low-Z	0	—	0	—	ns
t _{OEHZ} ^(2,3)	Output Disable to Output High-Z	—	3.5	—	3.5	ns
t _{AS}	Address Setup Time	1.5	—	1.5	—	ns
t _{WS}	Read/Write Setup Time	1.5	—	1.5	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.5	—	ns
t _{SE}	Clock Enable Setup Time	1.5	—	1.5	—	ns
t _{ADVS}	Address Advance Setup Time	1.5	—	1.5	—	ns
t _{DS}	Data Setup Time	1.5	—	1.5	—	ns
t _{AH}	Address Hold Time	0.65	—	0.65	—	ns
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t _{ADVH}	Address Advance Hold Time	0.5	—	0.5	—	ns
t _{DH}	Data Hold Time	0.5	—	0.5	—	ns
t _{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t _{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

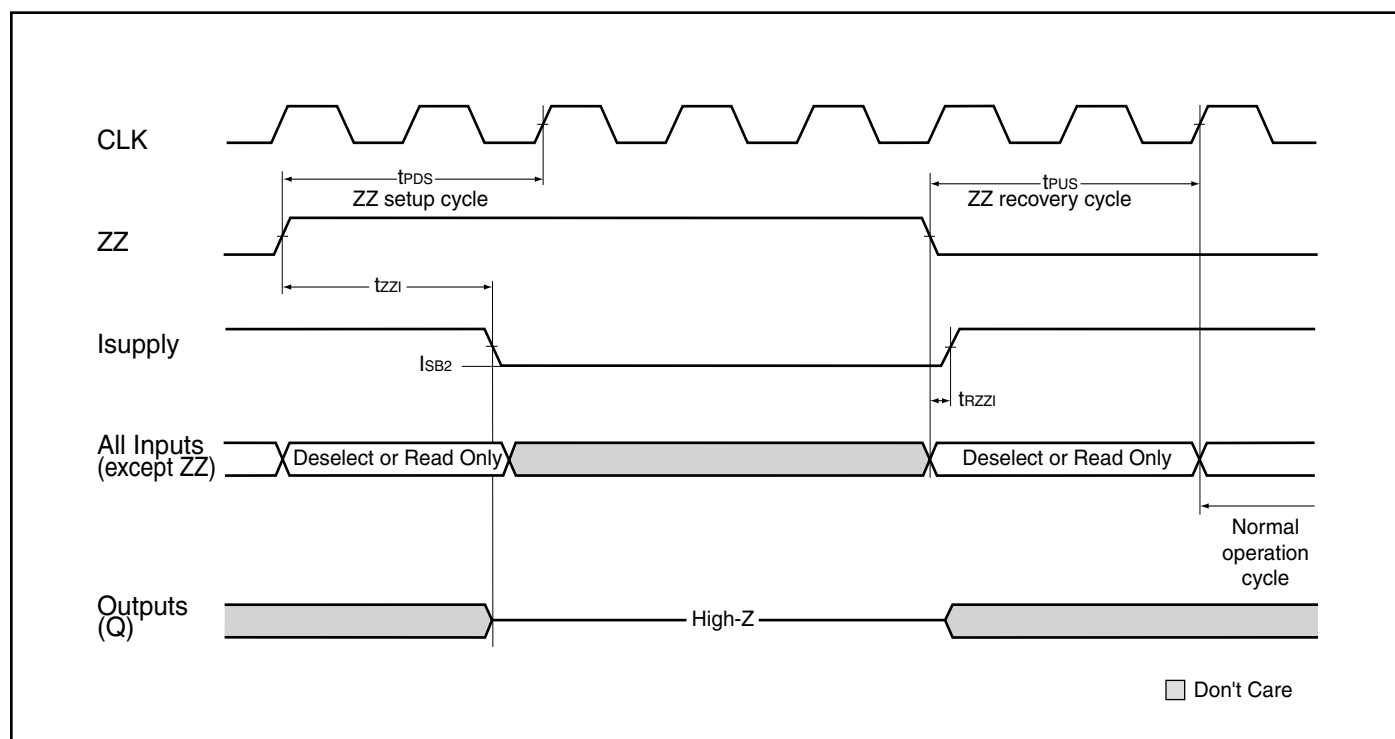
Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

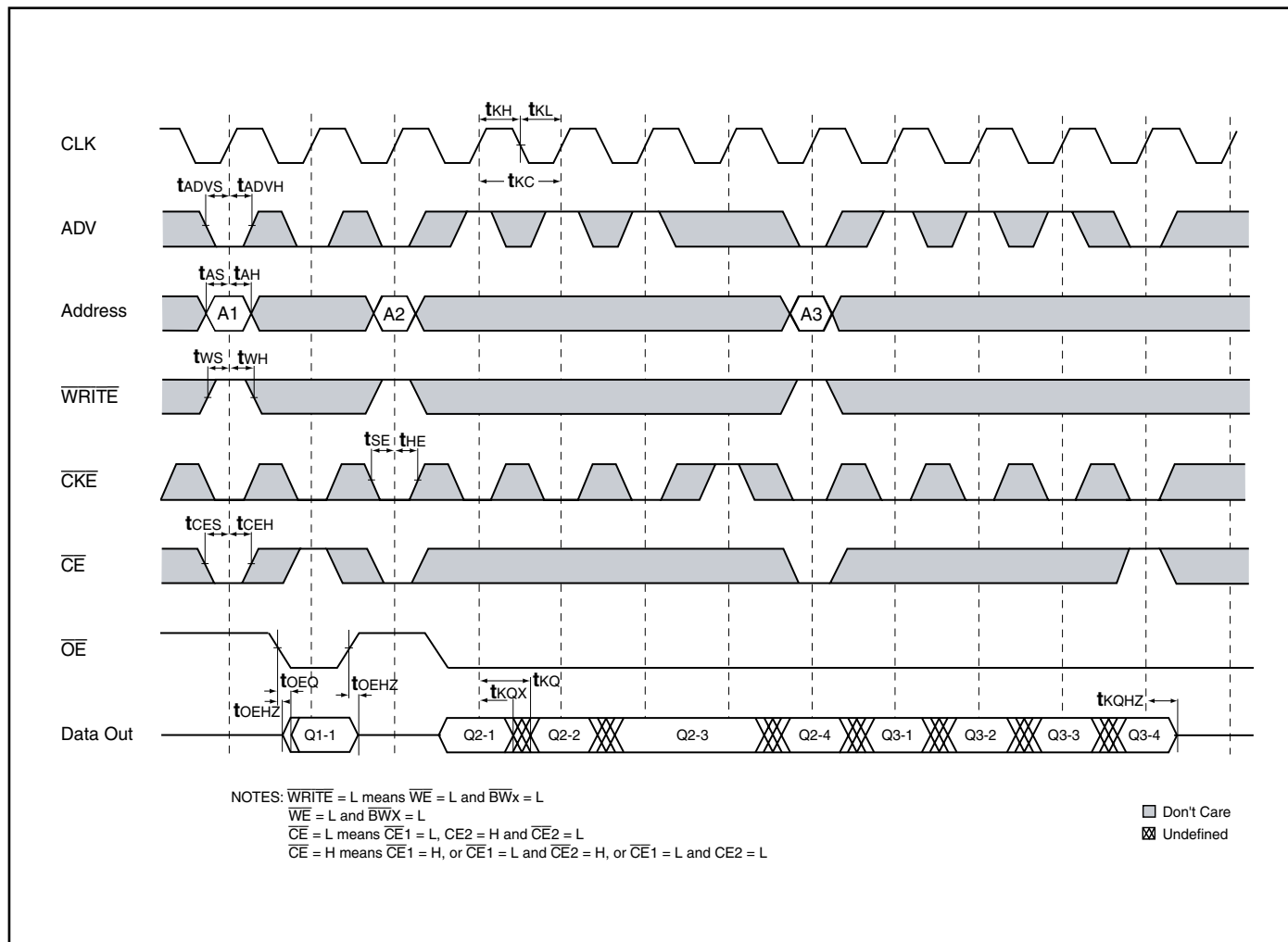
SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I _{SB2}	Current during SLEEP MODE	ZZ ≥ V _{IH}		80	mA
t _{PDS}	ZZ active to input ignored			2	cycle
t _{PUS}	ZZ inactive to input sampled		2		cycle
t _{ZZI}	ZZ active to SLEEP current		2		cycle
t _{ZZI}	ZZ inactive to exit SLEEP current		0		ns

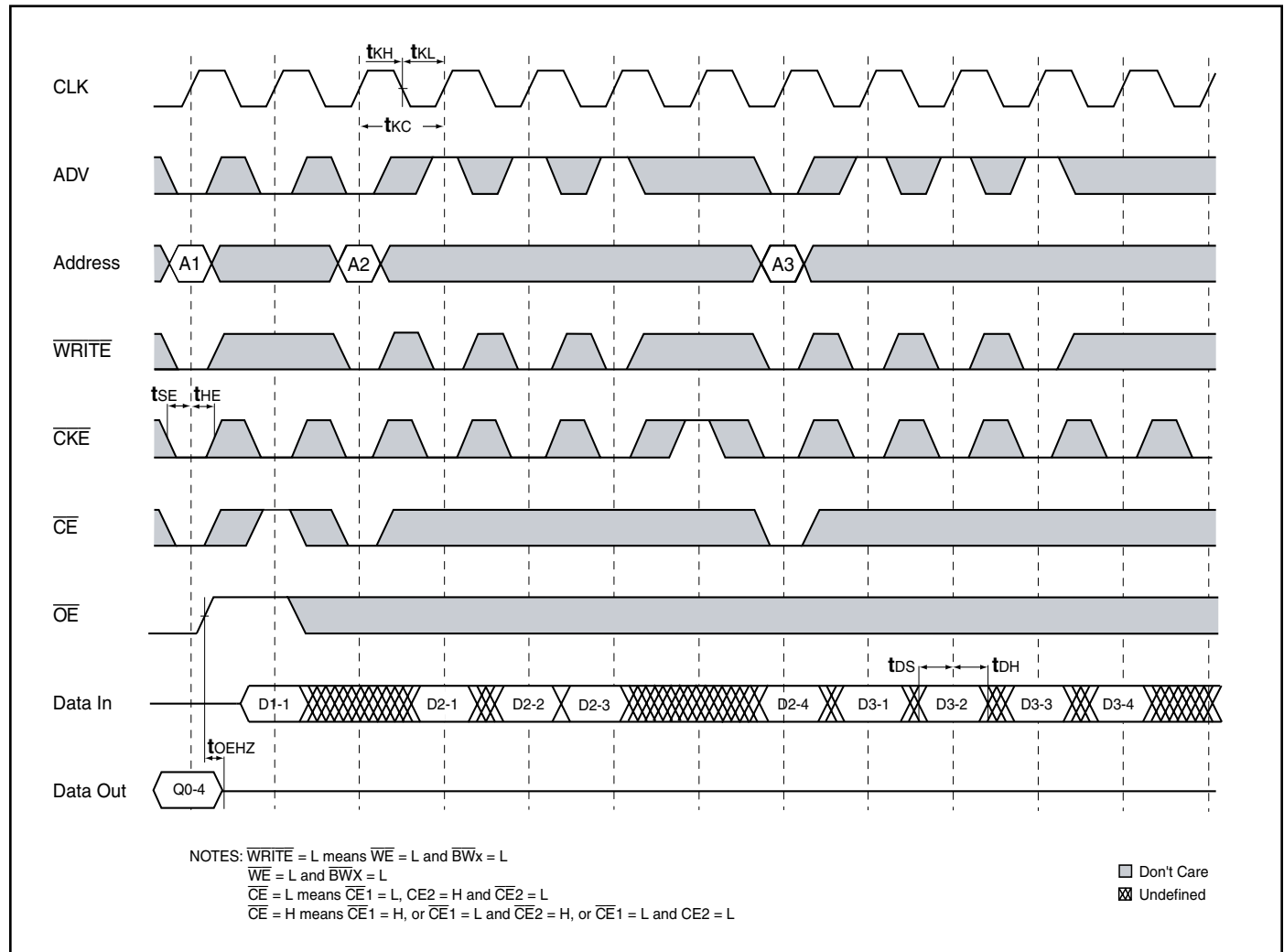
SLEEP MODE TIMING



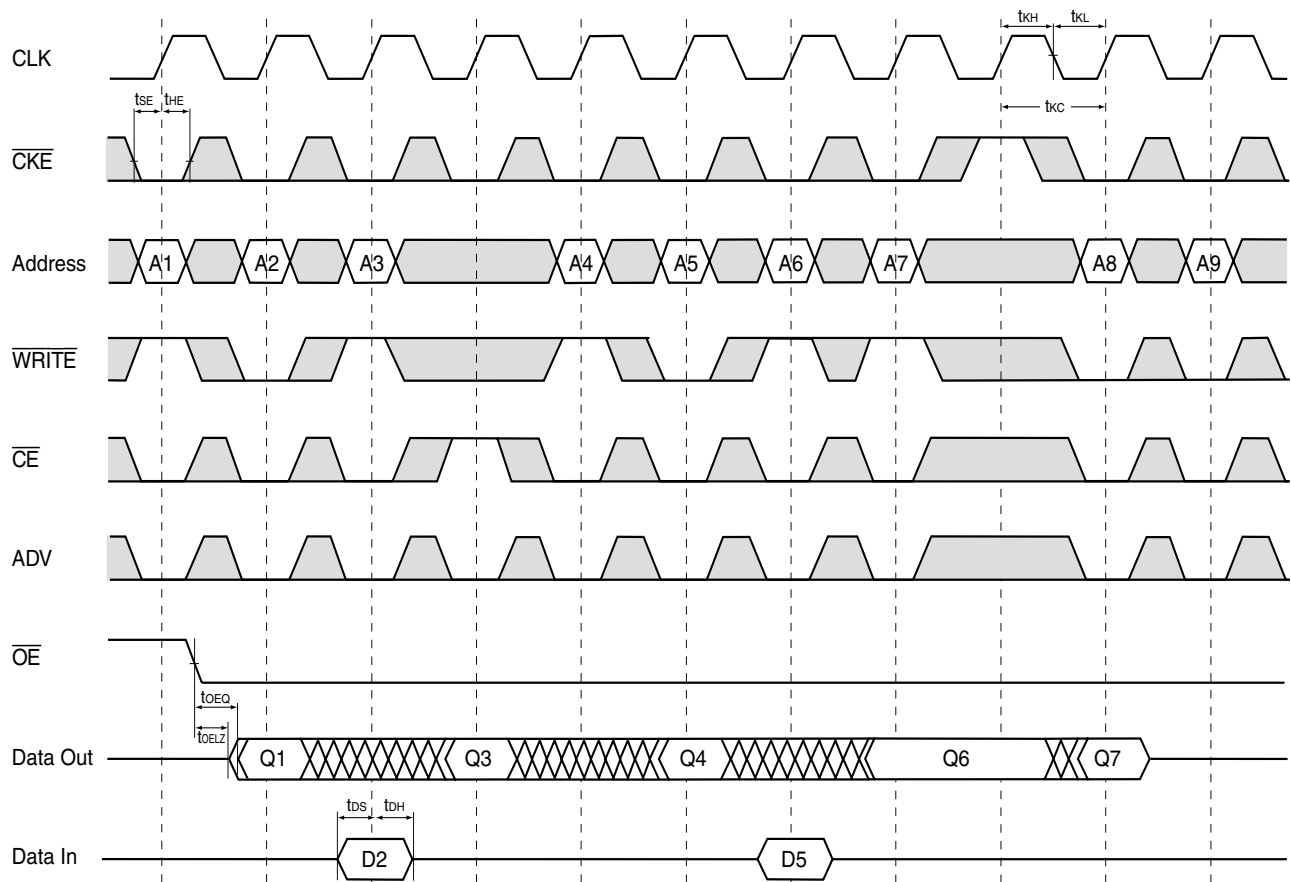
READ CYCLE TIMING



WRITE CYCLE TIMING



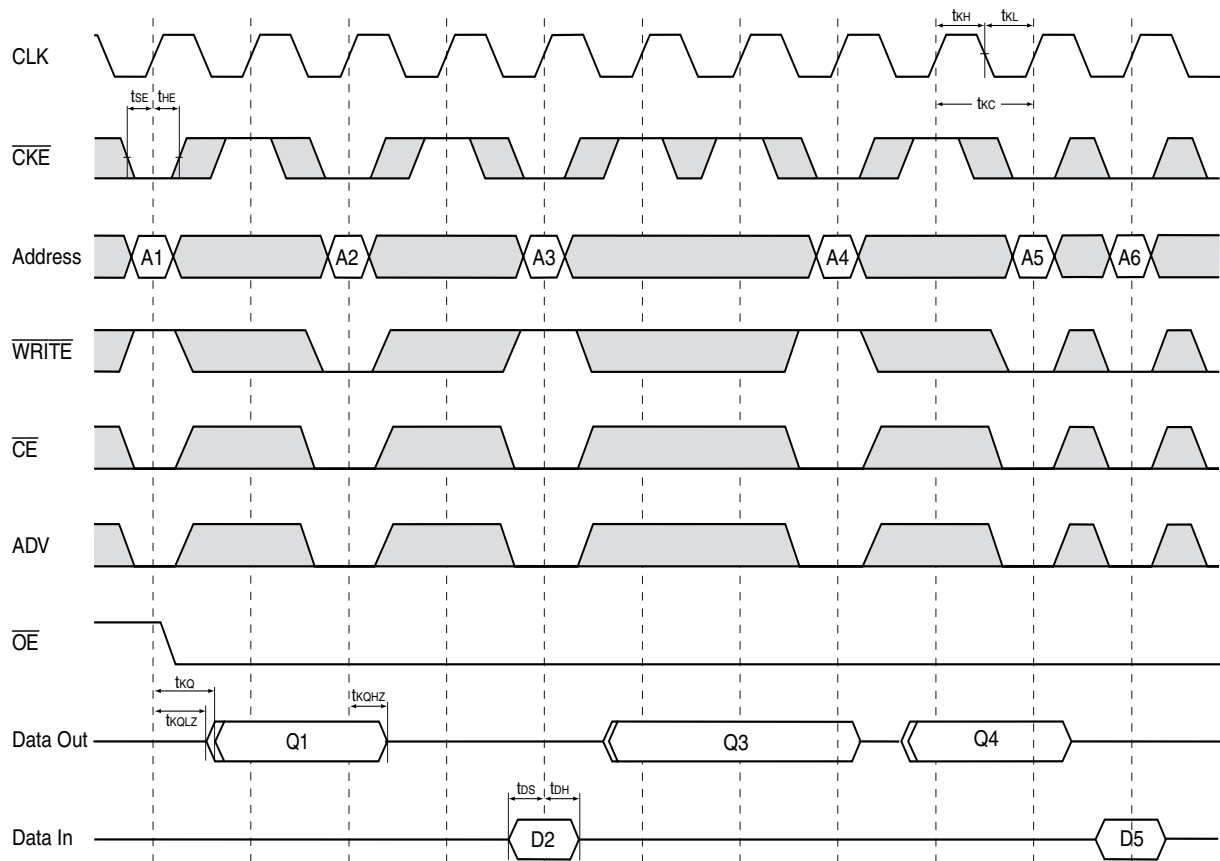
SINGLE READ/WRITE CYCLE TIMING



NOTES: $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$ and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CE}} = \text{L}$ means $\overline{\text{CE1}} = \text{L}$, $\overline{\text{CE2}} = \text{H}$ and $\overline{\text{CE2}} = \text{L}$
 $\overline{\text{CE}} = \text{H}$ means $\overline{\text{CE1}} = \text{H}$, or $\overline{\text{CE1}} = \text{L}$ and $\overline{\text{CE2}} = \text{H}$, or $\overline{\text{CE1}} = \text{L}$ and $\overline{\text{CE2}} = \text{L}$

□ Don't Care
 ▤ Undefined

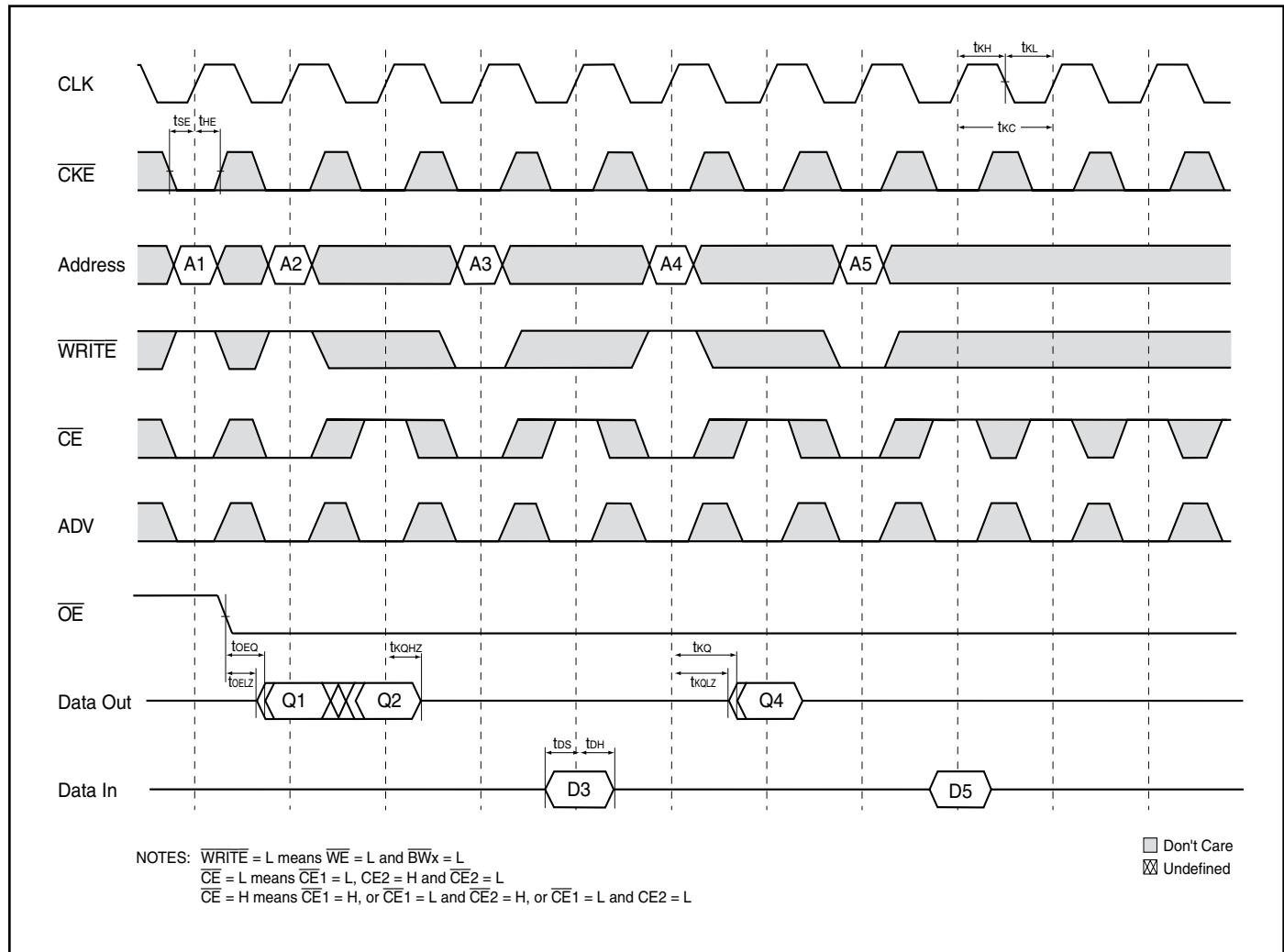
CKE OPERATION TIMING



NOTES: $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$ and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CE}} = \text{L}$ means $\overline{\text{CE1}} = \text{L}$, $\text{CE2} = \text{H}$ and $\overline{\text{CE2}} = \text{L}$
 $\overline{\text{CE}} = \text{H}$ means $\overline{\text{CE1}} = \text{H}$, or $\overline{\text{CE1}} = \text{L}$ and $\overline{\text{CE2}} = \text{H}$, or $\overline{\text{CE1}} = \text{L}$ and $\text{CE2} = \text{L}$

□ Don't Care
 ▨ Undefined

$\overline{CE}$ OPERATION TIMING



ORDERING INFORMATION ($V_{DD} = 3.3V/V_{DDQ} = 2.5V-3.3V$)

Commercial Range: 0°C to +70°C

Access Time	Order Part Number	Package
1Mx36		
6.5	IS61NLF102436A-6.5TQ	100 TQFP
7.5	IS61NLF102436A-7.5TQ	100 TQFP
2Mx18		
6.5	IS61NLF204818A-6.5TQ	100 TQFP
7.5	IS61NLF204818A-7.5TQ	100 TQFP

Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
1Mx36		
6.5	IS61NLF102436A-6.5TQI	100 TQFP
7.5	IS61NLF102436A-7.5TQI	100 TQFP
	IS61NLF102436A-7.5TQLI	100 TQFP, Lead-free
2Mx18		
6.5	IS61NLF204818A-6.5TQI	100 TQFP
7.5	IS61NLF204818A-7.5TQI	100 TQFP
	IS61NLF204818A-7.5TQLI	100 TQFP, Lead-free

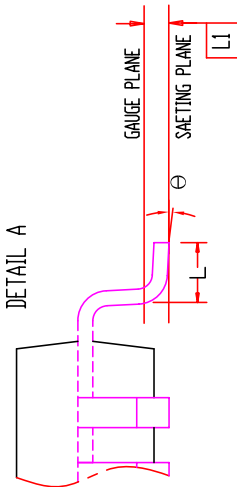
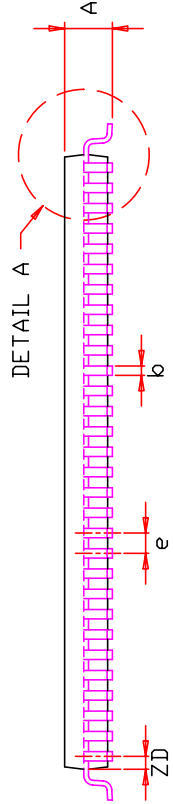
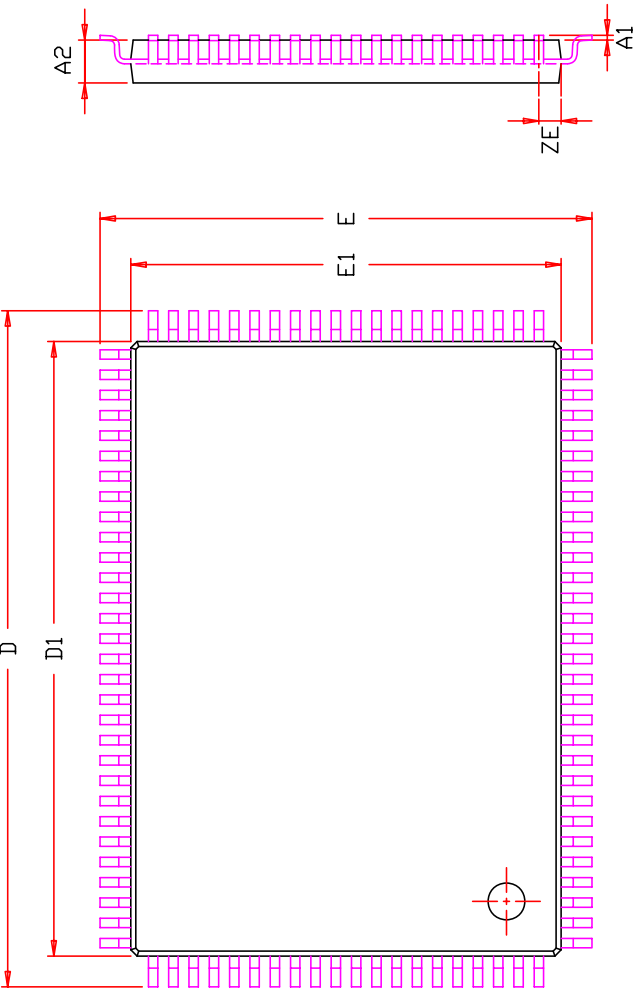
ORDERING INFORMATION ($V_{DD} = 2.5V/V_{DDQ} = 2.5V$)

Commercial Range: 0°C to +70°C

Access Time	Order Part Number	Package
1Mx36		
6.5	IS61NVF102436A-6.5TQ	100 TQFP
7.5	IS61NVF102436A-7.5TQ	100 TQFP
2Mx18		
6.5	IS61NVF204818A-6.5TQ	100 TQFP
7.5	IS61NVF204818A-7.5TQ	100 TQFP

Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
1Mx36		
6.5	IS61NVF102436A-6.5TQI	100 TQFP
7.5	IS61NVF102436A-7.5TQI	100 TQFP
2Mx18		
6.5	IS61NVF204818A-6.5TQI	100 TQFP
7.5	IS61NVF204818A-7.5TQI	100 TQFP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.40		1.60	0.055		0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.30	0.38	0.009	0.012	0.015
D	21.90	22.00	22.10	0.862	0.866	0.870
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.65 BSC.			0.026 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	0.25 BSC.			0.010 BSC.		
ZD	0.575 REF.			0.023 REF.		
ZE	0.825 REF.			0.032 REF.		
θ	0	3.5°	7°	0	3.5°	7°

NOTE :

- 1. CONTROLLING DIMENSION : MM
- 2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	100L 14x20x1.4mm LQFP (Footprint : 2.0 mm) Package Outline	REV.	F	DATE	09/01/2009
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280-600-011 REV.A

Mouser Electronics

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