

Applications

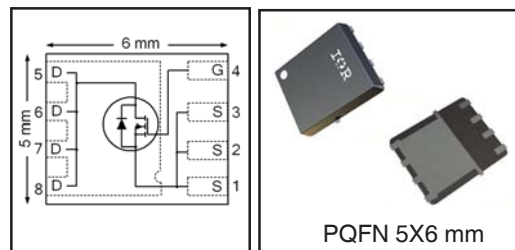
- Synchronous MOSFET for Notebook Processor Power
- Synchronous Rectifier MOSFET for Isolated DC-DC Converters in Networking Systems

HEXFET® Power MOSFET

V_{DS}	$R_{DS(on)}$ max	Qg
30V	4.8m Ω @ $V_{GS} = 10V$	17nC

Benefits

- Very low $R_{DS(ON)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- 100% Tested for R_G
- Lead-Free (Qualified up to 260°C Reflow)
- RoHS compliant (Halogen Free)
- Low Thermal Resistance
- Large Source Lead for more reliable Soldering



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	20	A
I_D @ $T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	16	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	54	
I_{DM}	Pulsed Drain Current ①	160	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation ⑤	3.1	W
P_D @ $T_A = 70^\circ\text{C}$	Power Dissipation ⑤	2.0	
	Linear Derating Factor ⑤	0.025	W/ $^\circ\text{C}$
T_J	Operating Junction and	-55 to + 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	5.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	40	

Notes ① through ⑤ are on page 9

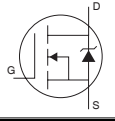
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

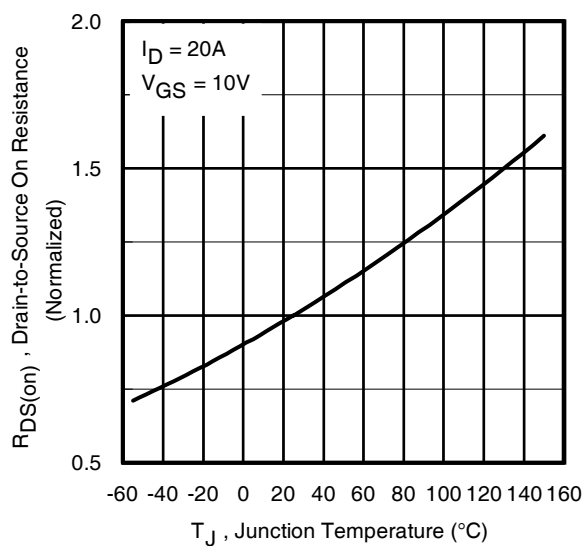
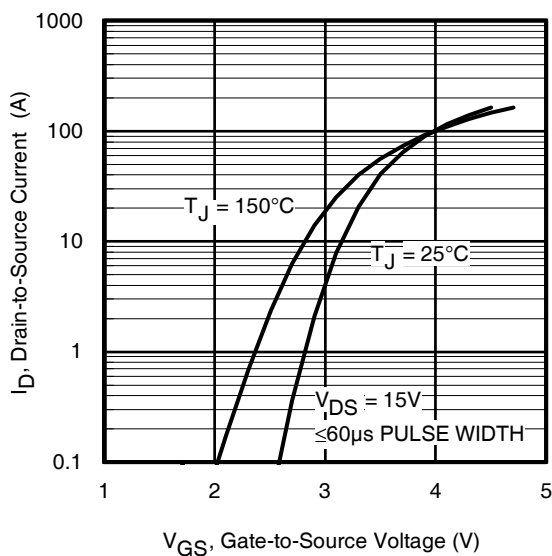
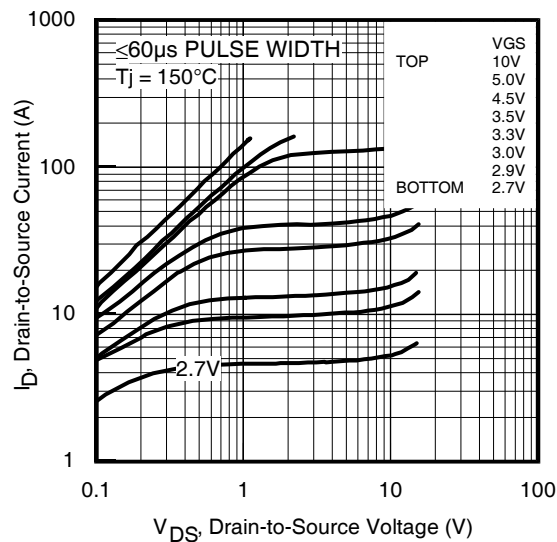
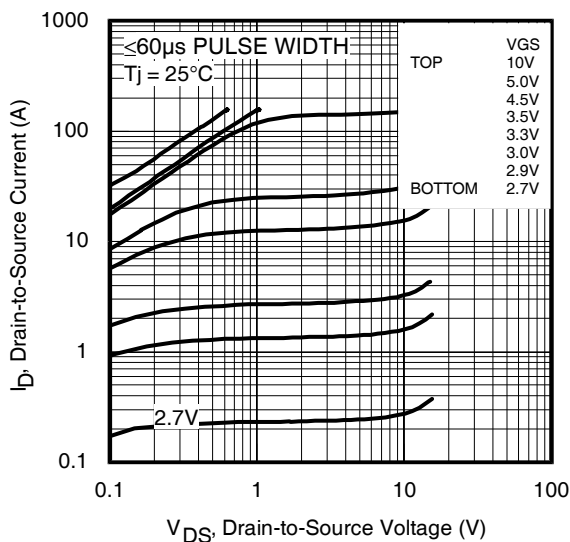
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.1	4.8	$m\Omega$	$V_{GS} = 10V, I_D = 20A$ ③
		—	6.0	6.8		$V_{GS} = 4.5V, I_D = 16A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-6.3	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	48	—	—	S	$V_{DS} = 15V, I_D = 16A$
Q_g	Total Gate Charge	—	17	26	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 16A$ See Fig.17 & 18
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	4.5	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	2.0	—		
Q_{gd}	Gate-to-Drain Charge	—	5.5	—		
Q_{godr}	Gate Charge Overdrive	—	5.0	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	7.5	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	9.0	—		
R_G	Gate Resistance	—	1.5	2.3	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ $I_D = 16A$ $R_G = 1.8\Omega$ See Fig.15
t_r	Rise Time	—	12	—		
$t_{d(off)}$	Turn-Off Delay Time	—	19	—		
t_f	Fall Time	—	7.0	—		
C_{iss}	Input Capacitance	—	2360	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	450	—		
C_{rss}	Reverse Transfer Capacitance	—	210	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	28	mJ
I_{AR}	Avalanche Current ①	—	16	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.9	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 16A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	14	21	ns	$T_J = 25^\circ\text{C}, I_F = 16A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	15	23	nC	$di/dt = 300A/\mu s$ ③ See Fig.16
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



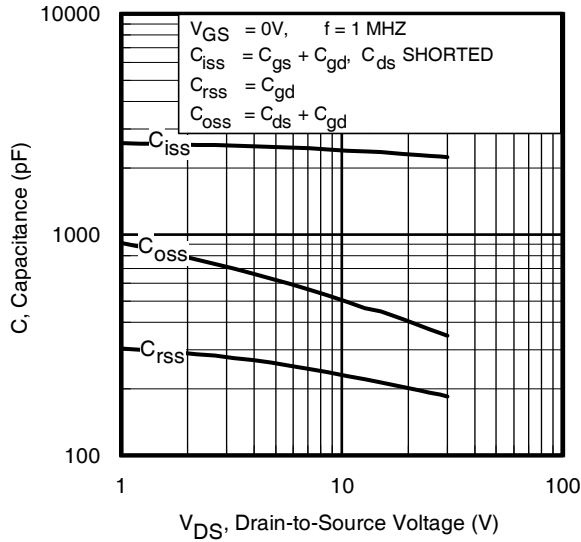


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

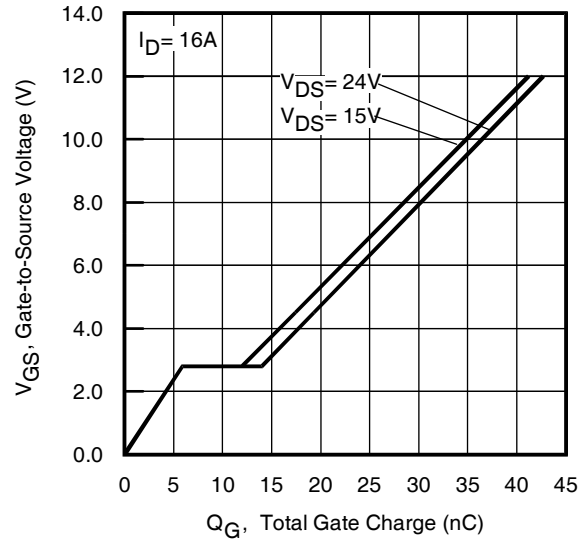


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

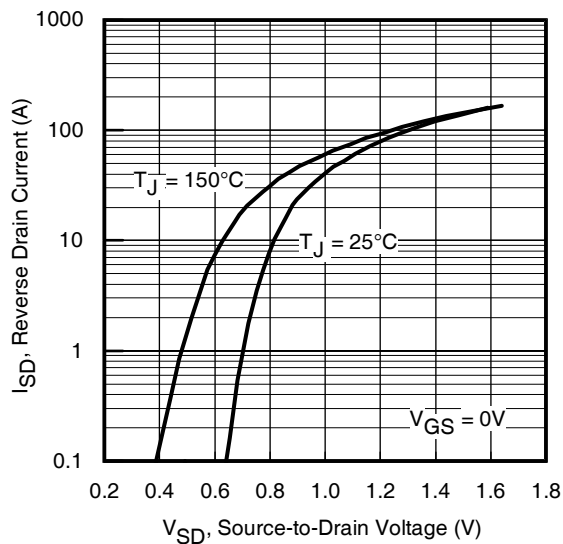


Fig 7. Typical Source-Drain Diode Forward Voltage

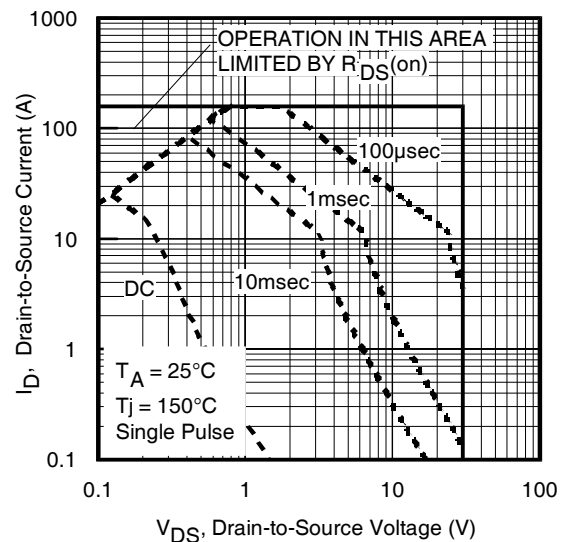


Fig 8. Maximum Safe Operating Area

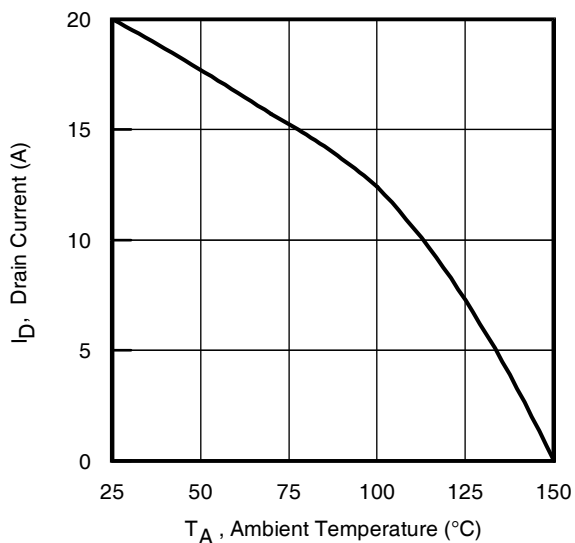


Fig 9. Maximum Drain Current vs. Ambient Temperature

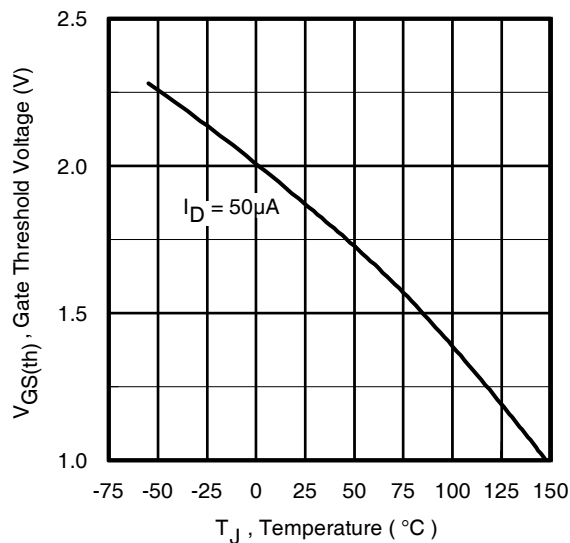


Fig 10. Threshold Voltage vs. Temperature

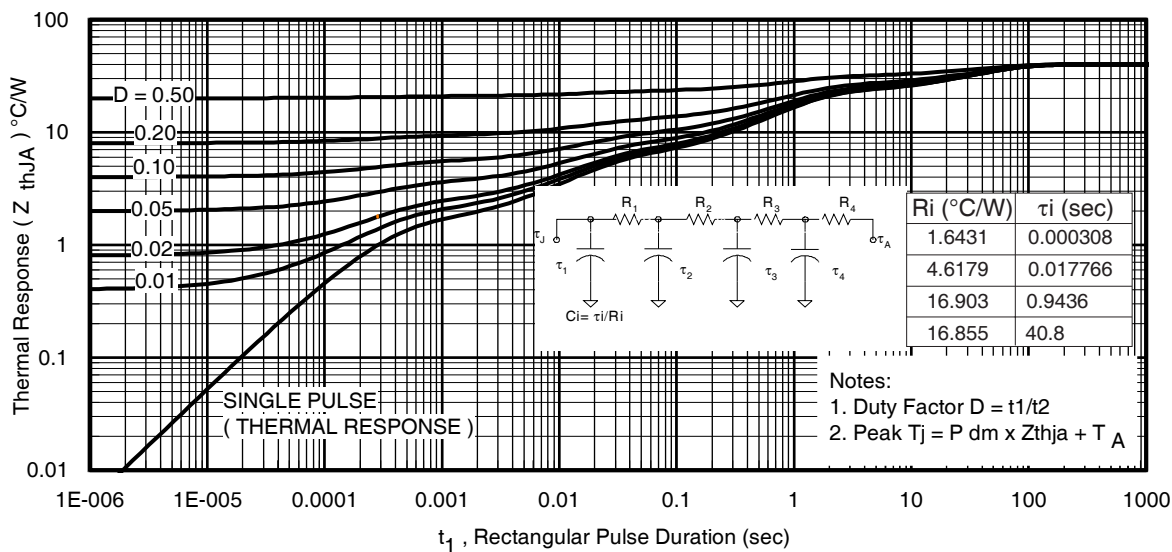
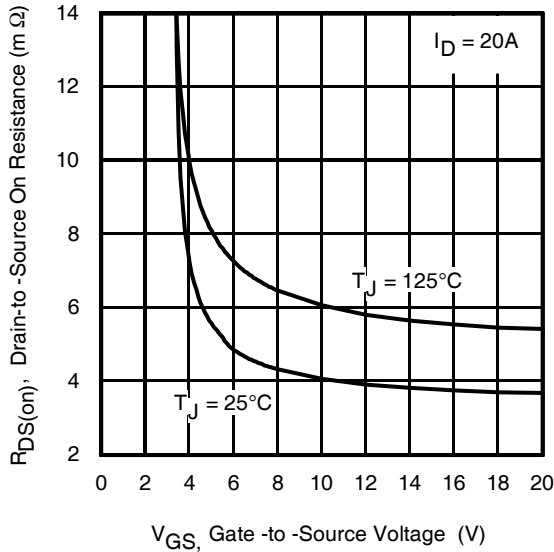
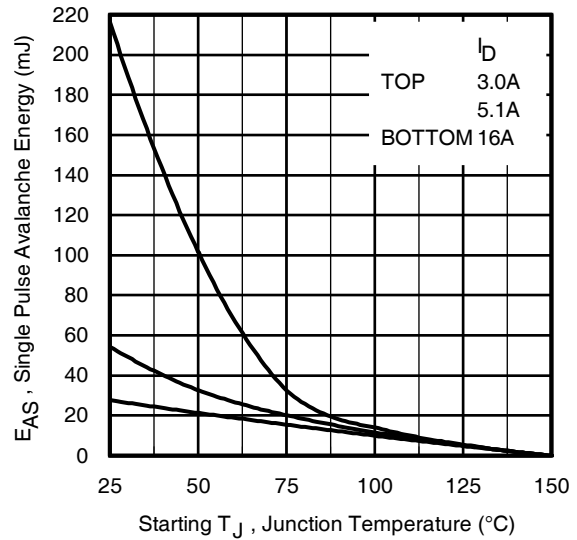
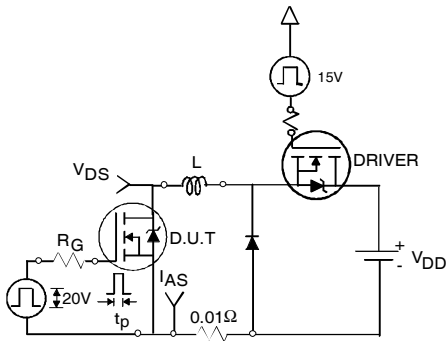
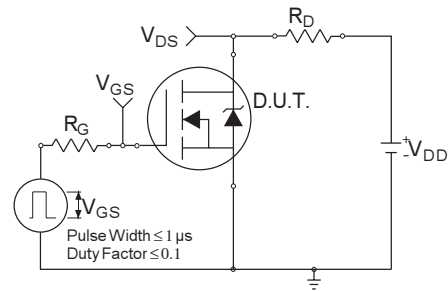
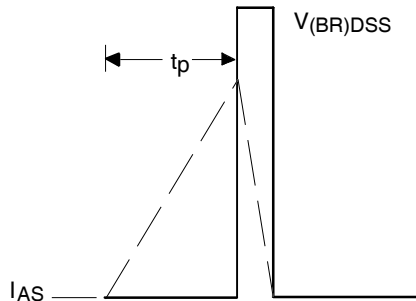
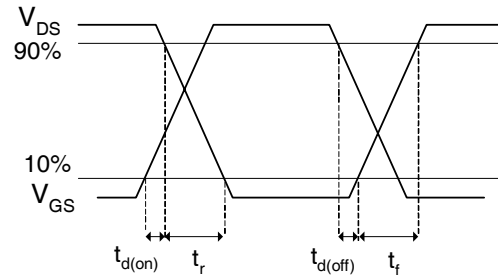


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14a. Unclamped Inductive Test Circuit

Fig 15a. Switching Time Test Circuit

Fig 14b. Unclamped Inductive Waveforms

Fig 15b. Switching Time Waveforms

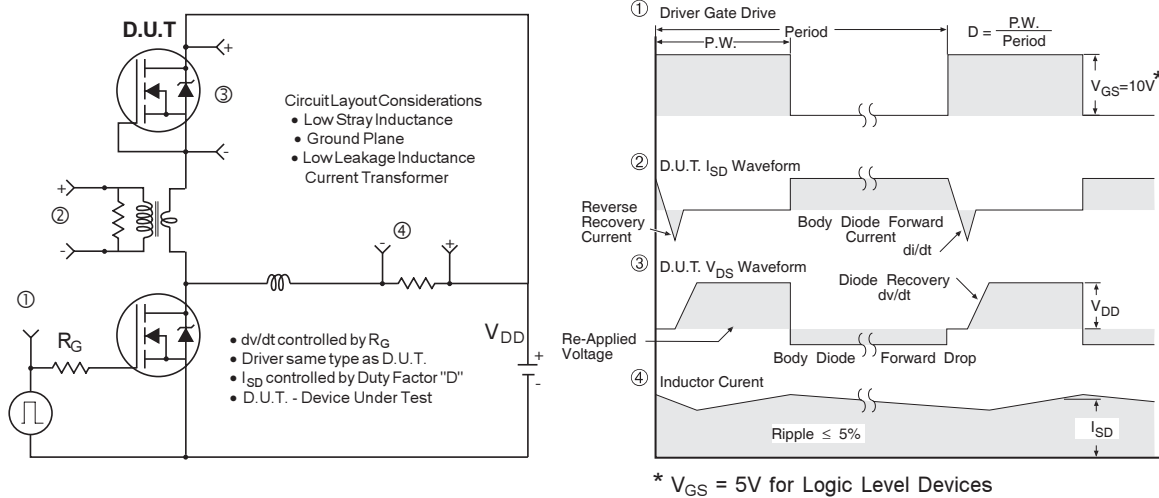


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

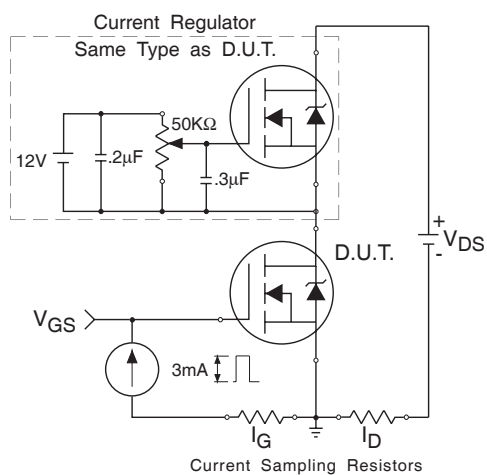


Fig 17. Gate Charge Test Circuit

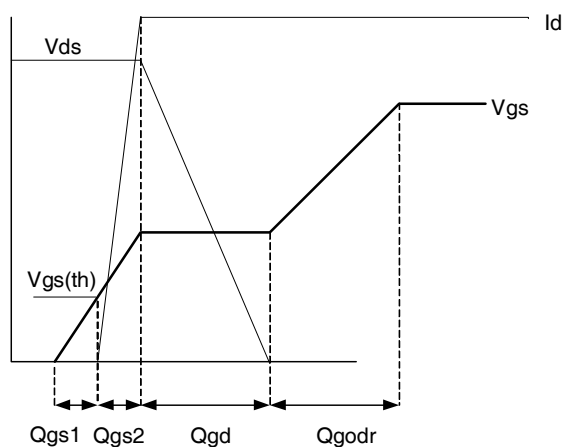
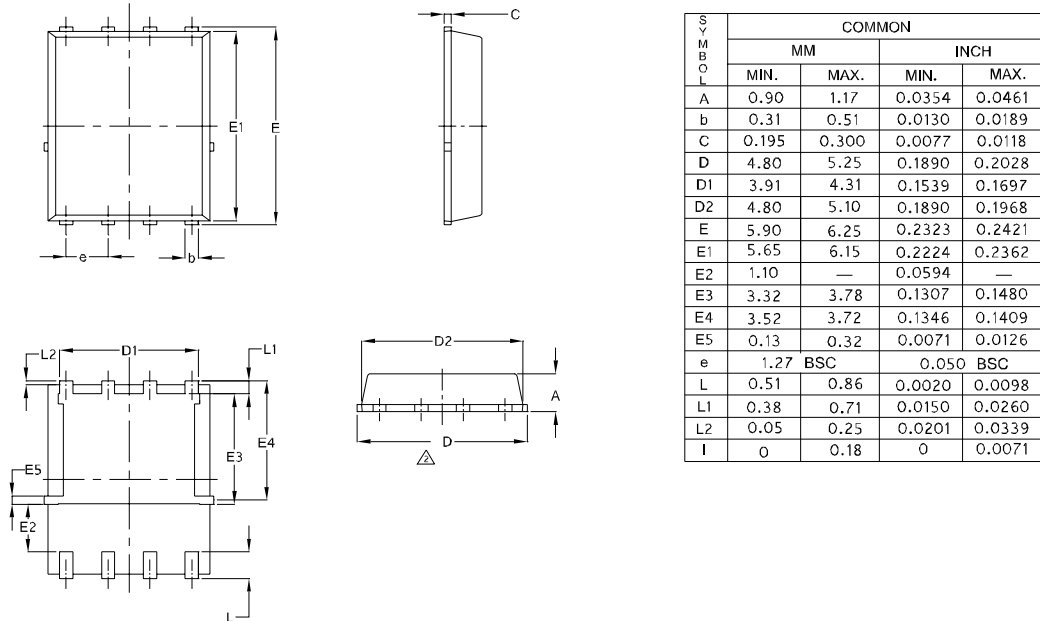
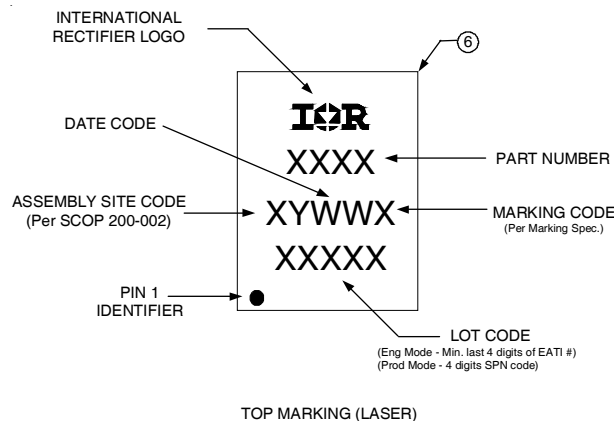


Fig 18. Gate Charge Waveform

PQFN 5x6 Option "E" Package Details

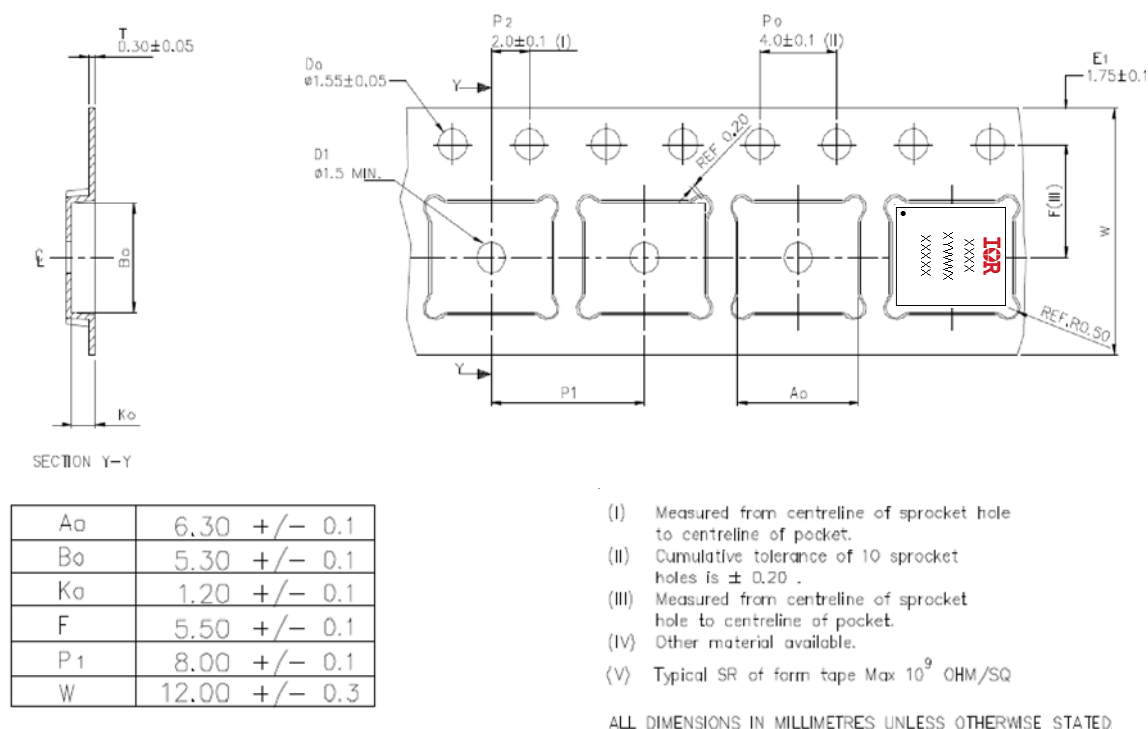


PQFN Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN Tape and Reel



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T_J = 25°C, L = 0.22mH, R_G = 25Ω, I_{AS} = 16A.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R_{thjc} is guaranteed by design
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.

Revision History

Date	Comments
08/08/2013	- Updated the package drawing, on page 1. - Updated the package outline drawing, on page 8. - This drawing change is related to PCN "Hana-GTBF-GEM 5x6 PQFN Public."

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