FEATURES

- Peak efficiency up to 94% at 1.2V
- Two pairs of control and synchronous MOSFETs in a single PQFN package
- Proprietary package minimizes package parasitic and simplifies PCB layout
- Input voltage (VIN) range of 4.5V to 21V
- Output current capability of 30A/phase
- Ultra-low Rg MOSFET technology minimizes switching losses for optimized high frequency performance
- Synchronous MOSFET with monolithic integrated Schottky diode reduces dead-time and diode reverse recovery losses
- Efficient dual side cooling
- Small 6mm x 8 mm x 0.9mm PQFN package
- Lead-free RoHS compliant package

APPLICATIONS

- High frequency, low profile DC-DC converters
- Voltage Regulators for CPUs, GPUs, and DDR memory arrays

DESCRIPTION

The IRF3546 dual integrated Power Block co-packages two pairs of high performance control and synchronous MOSFETs and is ideal for use in high-density two-phase synchronous buck converters. It is optimized internally for PCB layout, heat transfer and package inductance. Coupled with the latest generation of IR MOSFET technology, the IRF3546 provides higher efficiency at low output voltages required by cutting edge CPU, GPU and DDR memory designs.

High switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency. Integrating two phases in one package while still providing superior efficiency and thermal performance, the IRF3546 enables smallest size solutions.

The IRF3546 uses IR's latest generation of low voltage MOSFET technology characterized by ultra-low gate resistance (Rg, <0.5Ω) and charge that result in minimized switching losses. The synchronous MOSFET optimizes conduction losses and features a monolithic integrated Schottky to significantly reduce dead-time and diode conduction and reverse recovery losses.

The IRF3546 is optimized specifically for CPU core power delivery in 12V input applications like servers, certain notebooks, GPU and DDR memory designs.

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF3546	PQFN 6 mm x 8 mm	Tape and Reel	3000	IRF3546MTRPBF

PINOUT DIAGRAM

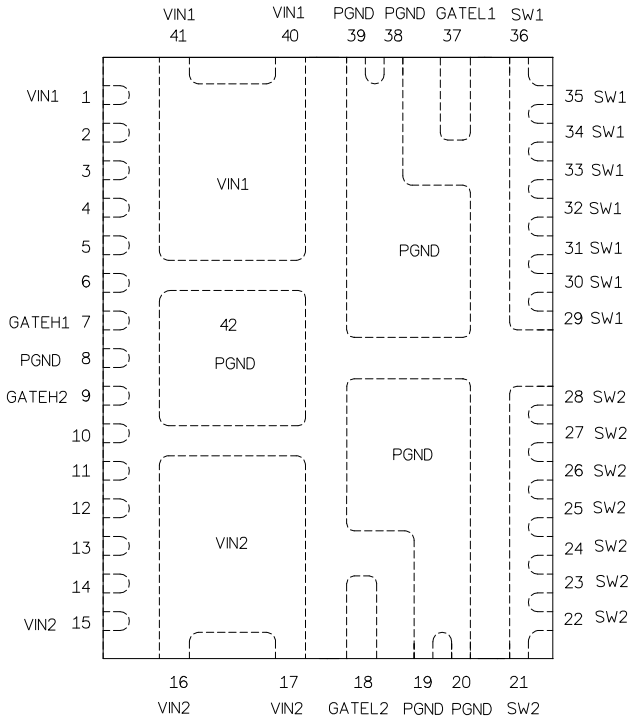


Figure 1: IRF3546 Top View

FUNCTIONAL BLOCK DIAGRAM

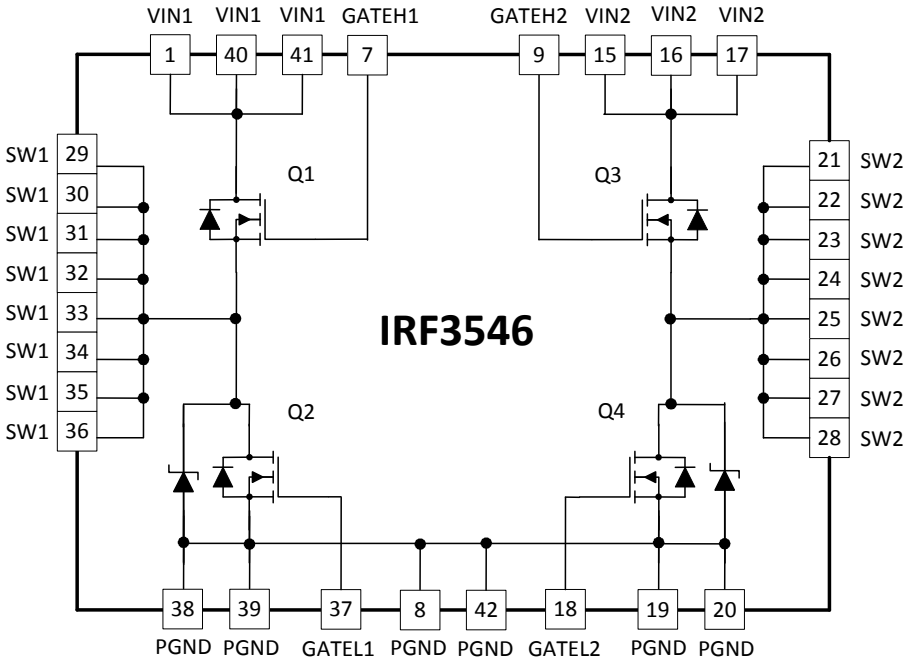


Figure 2: Block Diagram

TYPICAL APPLICATION

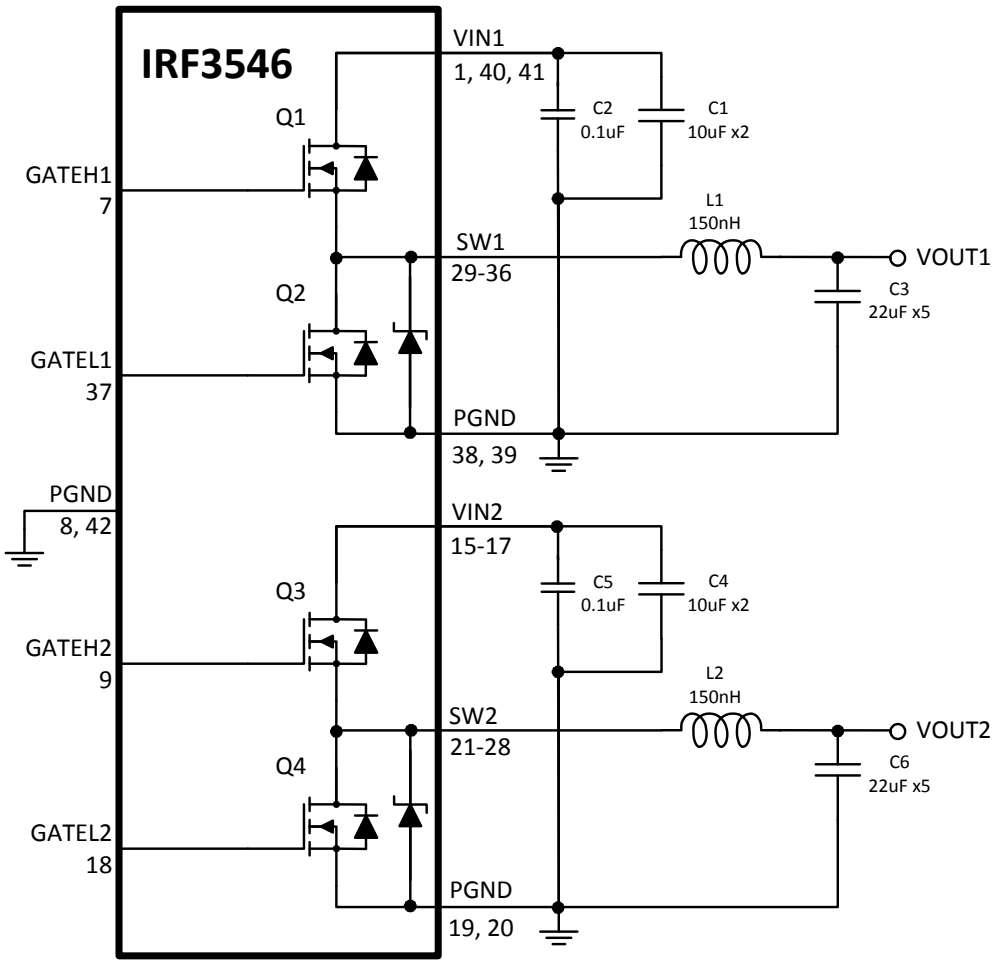


Figure 3: High Density Two Phase Voltage Regulator

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1, 40, 41	VIN1	High current input supply pads. Connected to Drains of Q1. Recommended operating range is 4.5V to 21V. Connect at least two 10uF 1206 ceramic capacitors and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN1 pins (40 and 41) and PGND pins (38 and 39). The 0.1uF 0402 capacitor should be on the same side of the PCB as the IRF3546.
2-6, 10-14	No Connect	No connects. These pins can be connected to the VIN planes to reduce PCB trace resistances.
7	GATEH1	Gate connection of the Channel 1 control MOSFET Q1.
8, 19, 20, 38, 39, 42	PGND	High current Power Ground. Connected to Sources of Q2 and Q4. Note all pads are internally connected in the package. Provide low resistance connections to the ground plane and respective output capacitors.
9	GATEH2	Gate connection of the Channel 2 control MOSFET Q3.
15-17	VIN2	High current input supply pads. Connected to Drains of Q3. Recommended operating range is 4.5V to 21V. Connect at least two 10uF 1206 ceramic capacitors and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN2 pins (16 and 17) and PGND pins (19 and 20). The 0.1uF 0402 capacitor should be on the same side of the PCB as the IRF3546.
18	GATEL2	Gate connection of the Channel 2 synchronous MOSFET Q4.
21-28	SW2	High Current Switch Node output for Channel 2. Connected to Source of Q3 and Drain of Q4.
29-36	SW1	High Current Switch Node output for Channel 1. Connected to Source of Q1 and Drain of Q2.
37	GATEL1	Gate connection of the Channel 1 synchronous MOSFET Q2.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

	Parameter	Q1 and Q3 Max.	Q2 and Q4 Max.	Units
V_{DS}	Drain-to-Source Voltage	25		V
V_{GS}	Gate-to-Source Voltage	±20		V
I_D @T_C = 25° C	Continuous Drain Current, V_{GS} @ 10V	16	20	A
I_D @T_C = 70° C	Continuous Drain Current, V_{GS} @ 10V	13	16	A
I_{DM}	Pulse Drain Current	130	160	A
E_{AS}	Single Pulse Avalanche Energy	50 NOTE 1	200 NOTE 2	mJ

THERMAL INFORMATION	
Thermal Resistance, Junction to Top (θ_{JC_TOP})	11.3 °C/W
Thermal Resistance, Junction to PCB (pin 28) (θ_{JB})	1.6 °C/W
Thermal Resistance (θ_{JA}) NOTE 3	18.4 °C/W
Maximum Operating Junction Temperature	-40°C to 150°C
Maximum Storage Temperature Range	-55°C to 150°C
MSL Rating	MSL3
Reflow Temperature	260°C

Notes

1. T_J =25°C, L =100uH, R_G =50Ω, I_{AS} =32A.
2. T_J =25°C, L =100uH, R_G =50Ω, I_{AS} =63A.
3. Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air. Refer to International Rectifier Application Note AN-994 for details.

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency						
Power Block per-channel Peak Efficiency	η	Note 2		94		%
		Note 3		93		%
Control MOSFETs (Q1 and Q3)						
Drain-to-Source On-Resistance	$R_{DS(ON)\_4.5V\_25°C}$	V_{GS}=4.5V, I_D=13A, T_J=25°C		4.1	4.8	mΩ
Drain-to-Source On-Resistance	$R_{DS(ON)\_10V\_25°C}$	V_{GS}=10V, I_D=27A, T_J=25°C		3.2	3.9	mΩ
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA, T_J=25°C	25			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	T_J=25°C -125°C, Note 1		0.02		V/°C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V, T_J=25°C			1	µA
Gate-to-Source Forward Leakage Current	I_{GSS}	V_{GS}=16V			100	nA
Gate-to-Source Reverse Leakage Current	I_{GSS}	V_{GS}=-16V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=35uA	1.1	1.6	2.1	V
Gate Threshold Voltage Coefficient	$\Delta V_{GS(th)}$	V_{DS}= V_{GS}, I_D=35uA		-5.7		mV/°C
Total Gate Charge	Q_g	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A, Note 1		9.7	15	nC
Pre-Vth Gate-to-Source Charge	Q_{gs1}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		2.3		nC
Post-Vth Gate-to-Source Charge	Q_{gs2}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		1.8		nC
Gate-to-Drain Charge	Q_{gd}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		3.1		nC
Gate Charge Overdrive	Q_{godr}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		2.9		nC
Switch Charge (Q_{gs2} +Q_{gd})	Q_{SW}	V_{DS}= 13V, V_{GS}=4.5V, I_D=13A		4.9		nC
Output Charge	Q_{oss}	V_{DS}= 16V, V_{GS}=0V		13		nC
Gate Resistance	R_g			0.6		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD}= 13V, V_{GS}=4.5V, I_D=13A, R_G=1.8 Ω		7.5		ns
Rise Time	t_r	V_{DD}= 13V, V_{GS}=4.5V, I_D=13A, R_G=1.8 Ω		12		ns
Turn-Off Delay Time	t_d	V_{DD}= 13V, V_{GS}=4.5V, I_D=13A, R_G=1.8 Ω		6.7		ns
Fall Time	t_f	V_{DD}= 13V, V_{GS}=4.5V, I_D=13A, R_G=1.8 Ω		4.2		ns
Input Capacitance	C_{iss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		1310		pF
Output Capacitance	C_{oss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		380		pF
Reverse Transfer Capacitance	C_{rss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		90		pF
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=13A, T_J=25°C	0.72	0.80	0.88	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		15	23	ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		10	15	nC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Synchronous MOSFETs (Q2 and Q4)						
Drain-to-Source On-Resistance	$R_{DS(ON)\_4.5V\_25°C}$	V_{GS}=4.5V, I_D=16A, T_J=25°C		1.8	2.2	mΩ
Drain-to-Source On-Resistance	$R_{DS(ON)\_10V\_25°C}$	V_{GS}=10V, I_D=30A, T_J=25°C		1.35	1.8	mΩ
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=1mA, T_J=25°C	25			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	T_J=25°C -125°C, Note 1		0.02		V/°C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V, T_J=25°C			250	uA
Gate-to-Source Forward Leakage Current	I_{GSS}	V_{GS}=16V			100	nA
Gate-to-Source Reverse Leakage Current	I_{GSS}	V_{GS}=-16V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=100uA	1.1	1.6	2.1	V
Gate Threshold Voltage Coefficient	$\Delta V_{GS(th)}$	V_{DS}= V_{GS}, I_D=1mA		-5.4		mV/°C
Total Gate Charge	Q_g	V_{DS}= 13V, V_{GS},=4.5V, I_D=30A, Note 1		22	33	nC
Pre-Vth Gate-to-Source Charge	Q_{gs1}	V_{DS}= 13V, V_{GS}=4.5V, I_D=30A		5.1		nC
Post-Vth Gate-to-Source Charge	Q_{gs2}	V_{DS}= 13V, V_{GS}=4.5V, I_D=30A		3.1		nC
Gate-to-Drain Charge	Q_{gd}	V_{DS}= 13V, V_{GS}=4.5V, I_D=30A		6.0		nC
Gate Charge Overdrive	Q_{godr}	V_{DS}= 13V, V_{GS}=4.5V, I_D=30A		6.7		nC
Switch Charge (Q_{gs2} +Q_{gd})	Q_{SW}	V_{DS}= 13V, V_{GS}=4.5V, I_D=30A		9.1		nC
Output Charge	Q_{oss}	V_{DS}= 16V, V_{GS}=0V		23		nC
Gate Resistance	R_g			0.4		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD}= 13V, V_{GS}=4.5V, I_D=16A, R_G=1.3 Ω		13		ns
Rise Time	t_r	V_{DD}= 13V, V_{GS}=4.5V, I_D=16A, R_G=1.3 Ω		15		ns
Turn-Off Delay Time	t_d	V_{DD}= 13V, V_{GS}=4.5V, I_D=16A, R_G=1.3 Ω		16		ns
Fall Time	t_f	V_{DD}= 13V, V_{GS}=4.5V, I_D=16A, R_G=1.3 Ω		6.6		ns
Input Capacitance	C_{iss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		2880		pF
Output Capacitance	C_{oss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		950		pF
Reverse Transfer Capacitance	C_{rss}	V_{GS}= 0V, V_{DS}=13V, f=1.0MHz		180		pF
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=30A, T_J=25°C	0.63	0.70	0.77	V
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=13A, T_J=25°C	0.54	0.60	0.66	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		23	35	ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, I_F=30A, V_{DD}=13V, di/dt=200A/us, Note 1		30	45	nC

Notes

1. Guaranteed by design but not tested in production
2. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 300kHz, L=210nH (0.29mΩ), VCC=6.8V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, 400LFM airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.
3. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=6.8V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, no airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.

TYPICAL OPERATING CHARACTERISTICS

T_A = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7” (L) x 2.6” (W), unless specified otherwise.

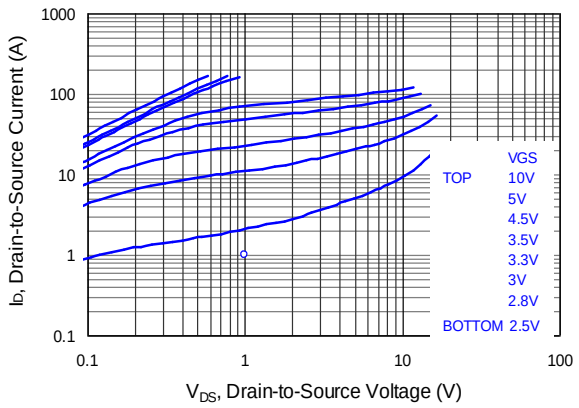


Figure 4: Q1 & Q3 Typical Output Characteristics

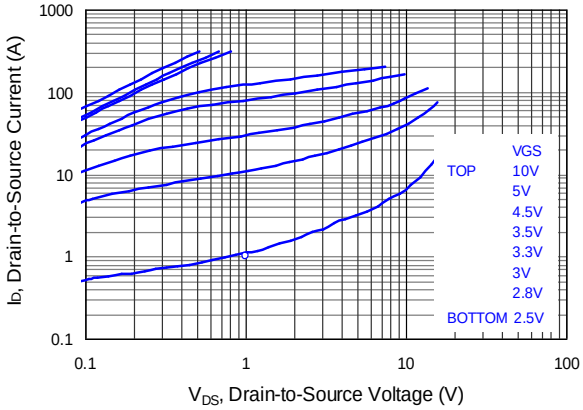


Figure 7: Q2 & Q4 Typical Output Characteristics

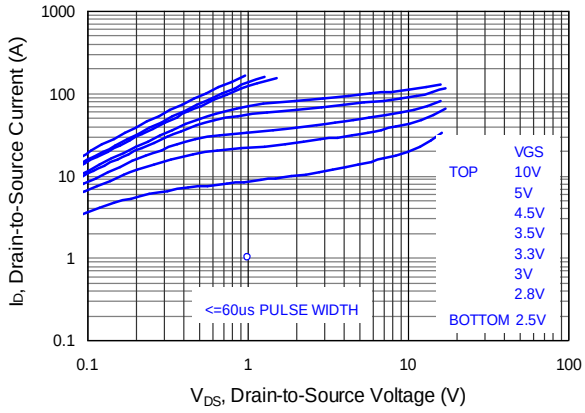


Figure 5: Q1 & Q3 Typical Output Characteristics @150°C

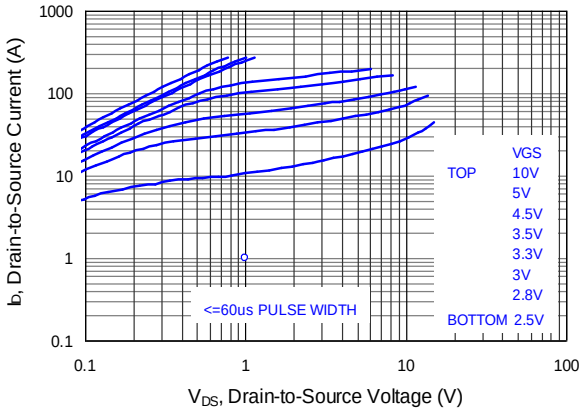


Figure 8: Q2 & Q4 Typical Output Characteristics @150°C

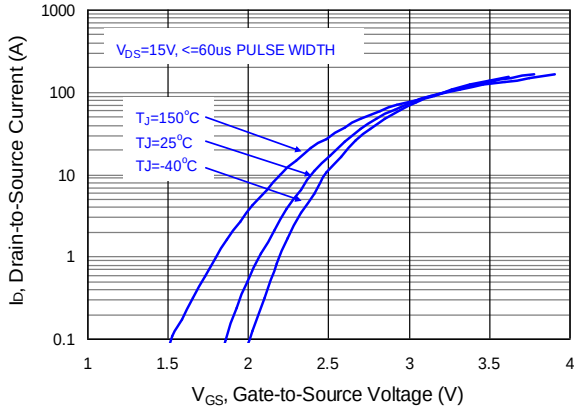


Figure 6: Q1 and Q3 Typical Transfer Characteristics

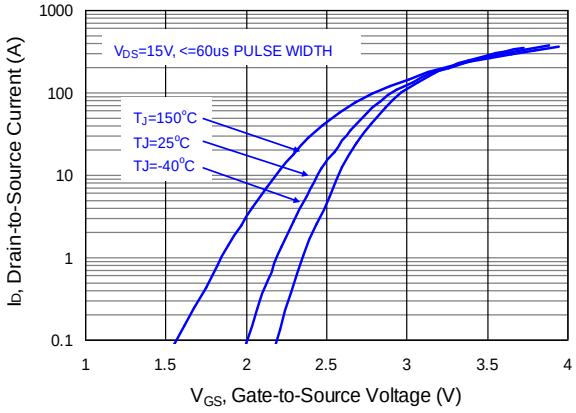


Figure 9: Q2 and Q4 Typical Transfer Characteristics

TYPICAL OPERATING CHARACTERISTICS (CONTINUE)

T_A = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), unless specified otherwise.

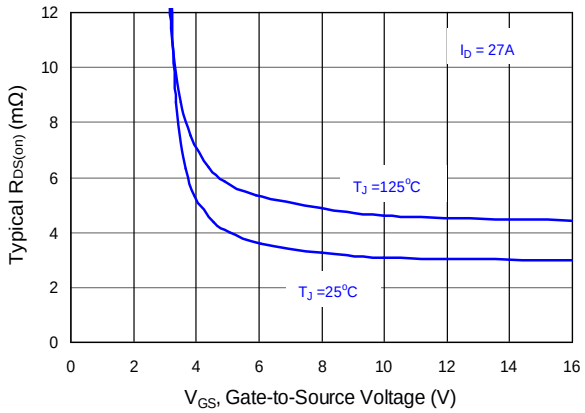


Figure 10: Q1 & Q3 Typical On-Resistance

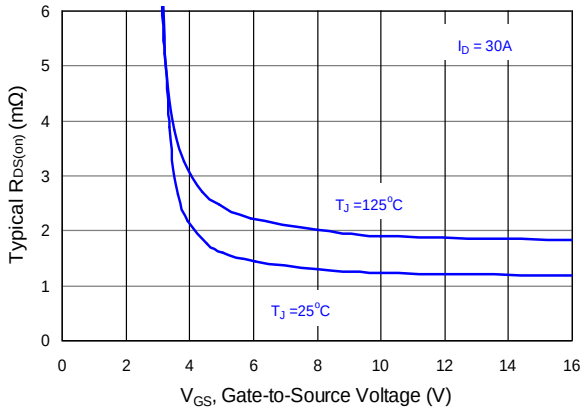


Figure 13: Q2 & Q4 Typical On-Resistance

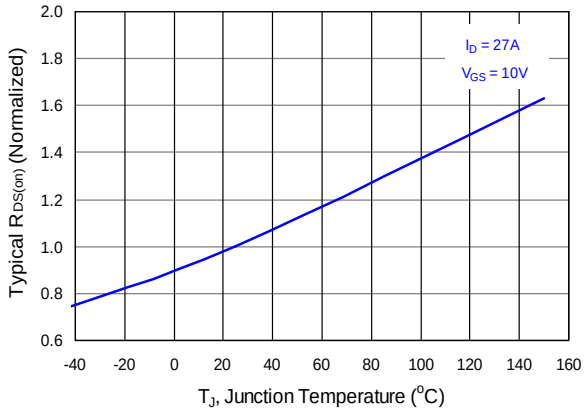


Figure 11: Q1 & Q3 On-Resistance vs. Temperature

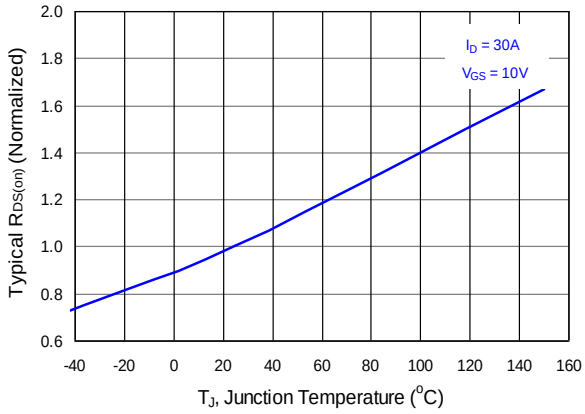


Figure 14: Q2 & Q4 On-Resistance vs. Temperature

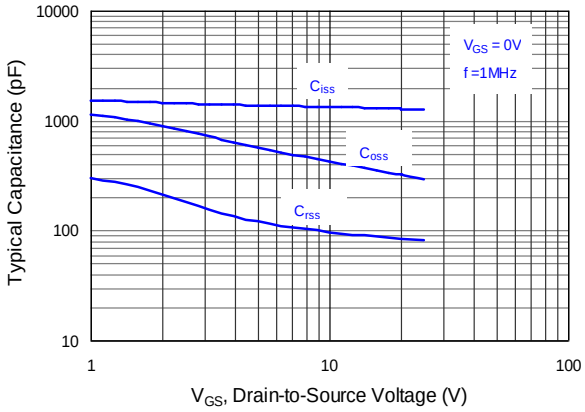


Figure 12: Q1 & Q3 Typical Capacitance vs. Drain-Source Voltage

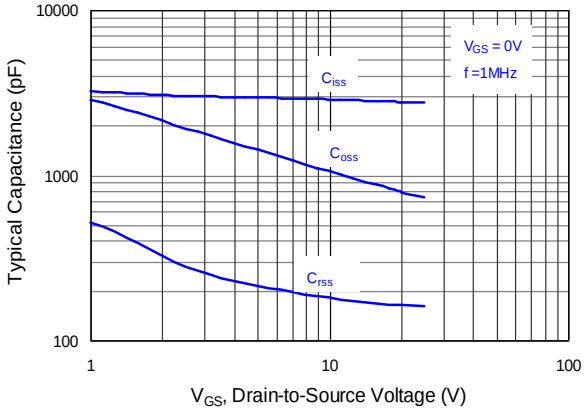


Figure 15: Q2 & Q4 Typical Capacitance vs. Drain-Source Voltage

TYPICAL OPERATING CHARACTERISTICS (CONTINUE)

T_A = 25°C, no heat sink, no air flow, 4-layer PCB board of 3.7" (L) x 2.6" (W), unless specified otherwise.

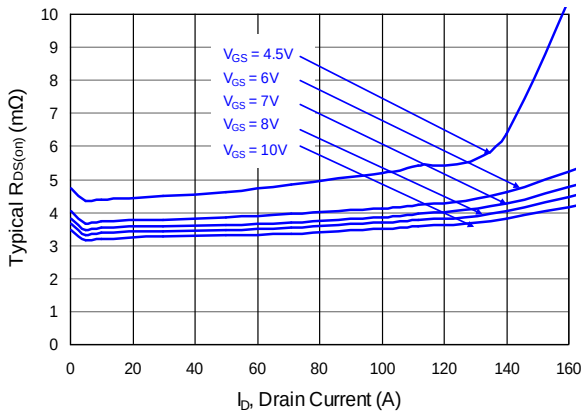


Figure 16: Q1 & Q3 Typical On-Resistance

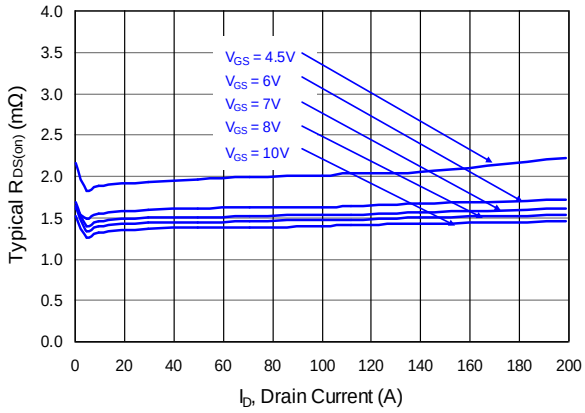


Figure 19: Q2 & Q4 Typical On-Resistance

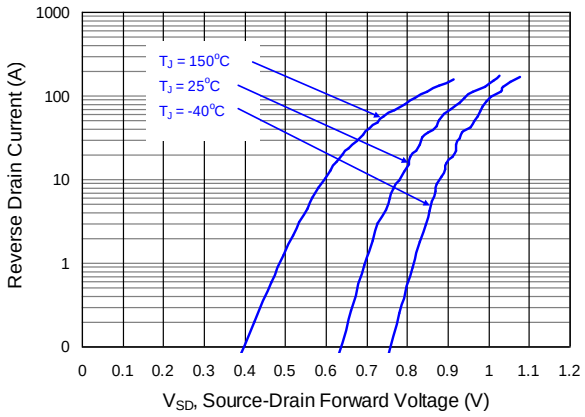


Figure 17: Q1 & Q3 Drain-Source Diode Characteristics

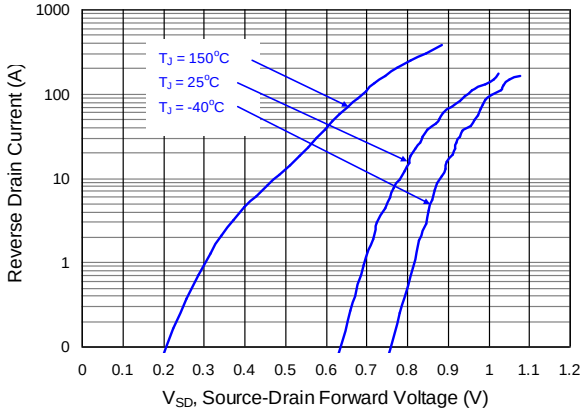


Figure 20: Q2 & Q4 Drain-Source Diode Characteristics

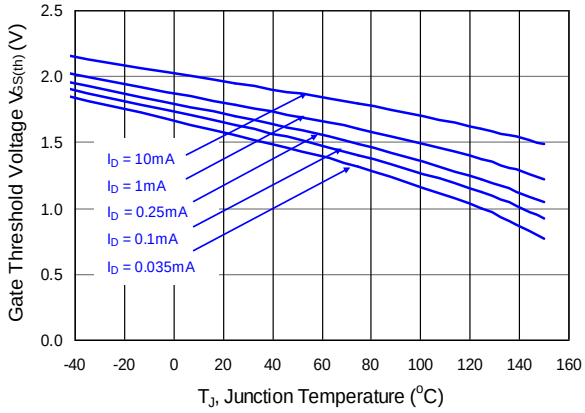


Figure 18: Q1 & Q3 Typical Threshold Voltage vs. Junction Temperature

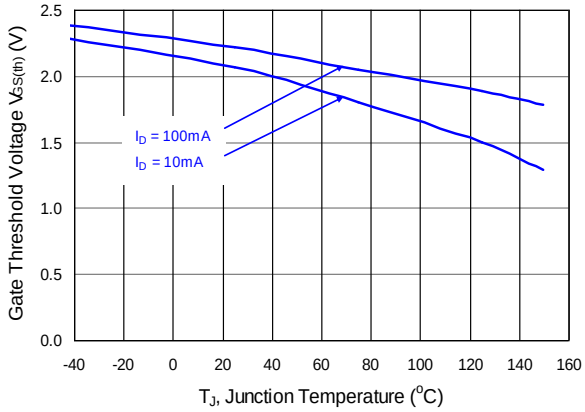


Figure 21: Q2 & Q4 Typical Threshold Voltage vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS (CONTINUE)

T_A = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), unless specified otherwise.

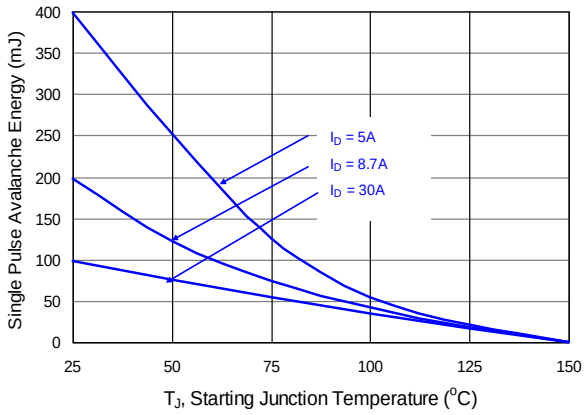


Figure 22: Q1 & Q3 Single Pulse Avalanche Energy

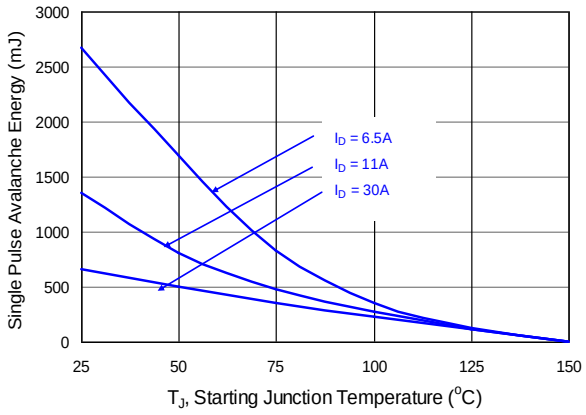


Figure 25: Q2 & Q4 Single Pulse Avalanche Energy

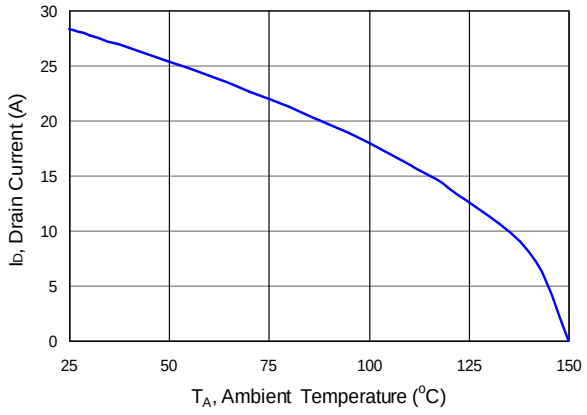


Figure 23: Q1 & Q3 Maximum Drain Current vs. Temperature

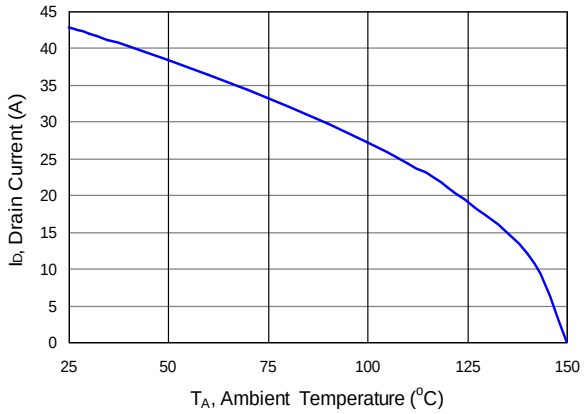


Figure 26: Q2 & Q4 Maximum Drain Current vs. Temperature

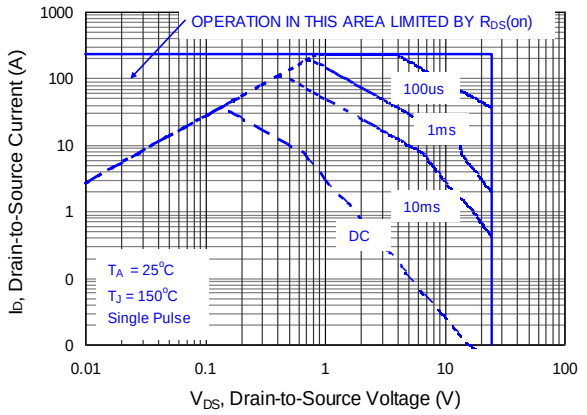


Figure 24: Q1 & Q3 Maximum Safe Operating Area

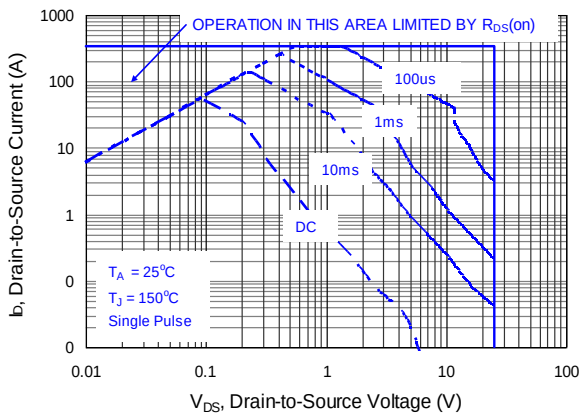


Figure 27: Q2 & Q4 Maximum Safe Operating Area

GENERAL DESCRIPTION

The IRF3546 contains two pairs of integrated high and low side N-channel MOSFETs. It is suitable for high switching frequency operation.

The IRF3546 can be driven as two independent power stages or as one power stage in a two-phase interleaved converter .

APPLICATION INFORMATION

Figure 3 shows a typical two phase, high density application circuit for the IRF3546.

SUPPLY DECOUPLING CAPACITOR

At least two 10uF 1206 ceramic capacitors and one 0.1uF 0402 ceramic capacitor are recommended for decoupling the VIN to PGND connection of each MOSFET pair. The 0.1uF 0402 capacitor should be on the same side of the PCB as the IRF3546 and next to the VIN and PGND pins. Adding additional capacitance and use of capacitors with lower ESR and mounted with low inductance routing will improve efficiency and reduce overall system noise, especially in high current applications.

PCB LAYOUT CONSIDERATION

PCB layout and design is important to driver performance in voltage regulator circuits due to the high current slew rate (di/dt) during MOSFET switching.

Locate all power components in each phase as close to each other as practically possible in order to minimize parasitics and losses, allowing for reasonable airflow.

Input supply decoupling capacitors should be physically located close to their respective pins.

High current paths like the gate driver traces should be as wide and short as practically possible.

GATEL1 and GATEL2 interconnect trace inductances should be minimized to prevent Cdv/dt turn-on of the low side MOSFET.

The ground connection should be as close as possible to the low-side MOSFET source.

Use of a copper plane under and around the device and thermal vias to connect to buried copper layers improves the thermal performance substantially.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length +0.15 - 0.3 mm outboard extension and 0 to + 0.05mm inboard extension. The outboard extension ensures a large and visible toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width.
- Only 0.30mm diameter via shall be placed in the area of the power pad lands and connected to power planes to minimize the noise effect and to improve thermal performance.

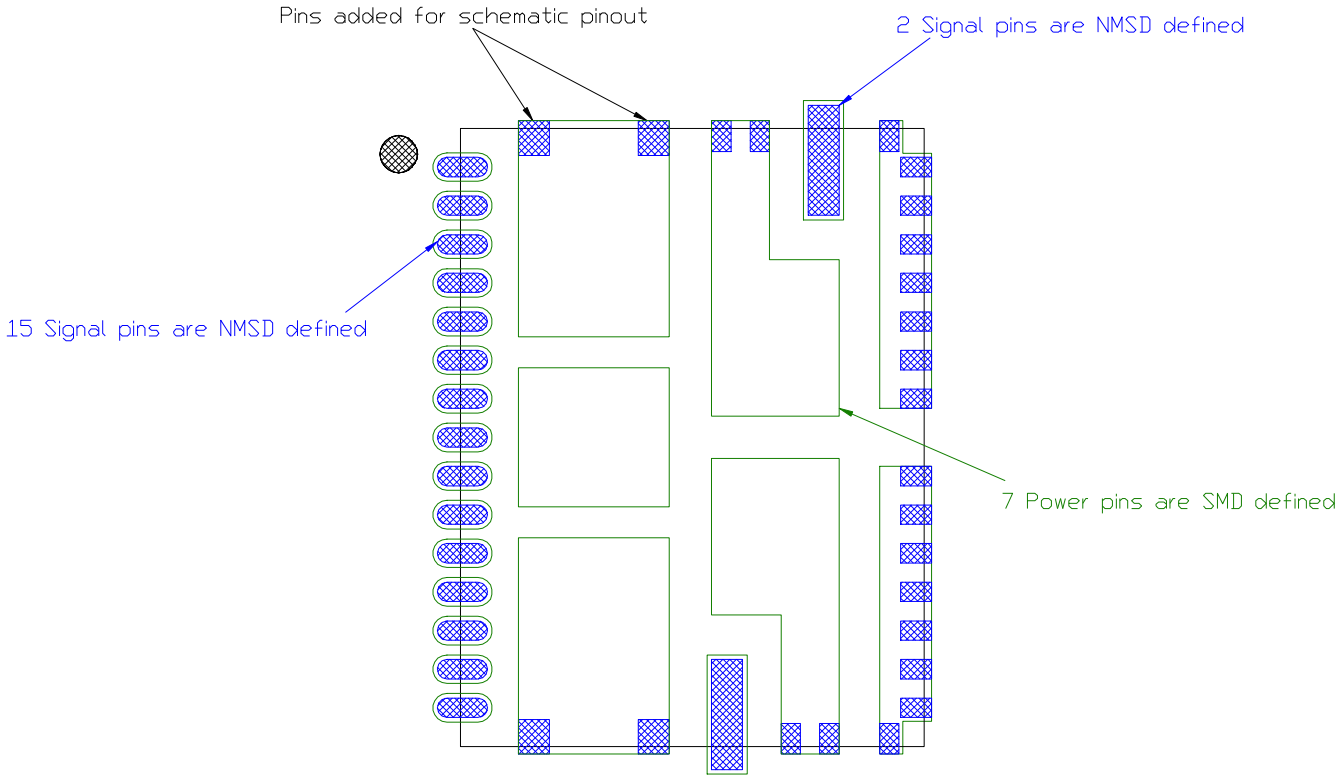


Figure 28: Metal and Component Placement

SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the low power signal lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm typical.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The power land pads VIN1, VIN2, PGND, SW1 and SW2 should be Solder Mask Defined (SMD).
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

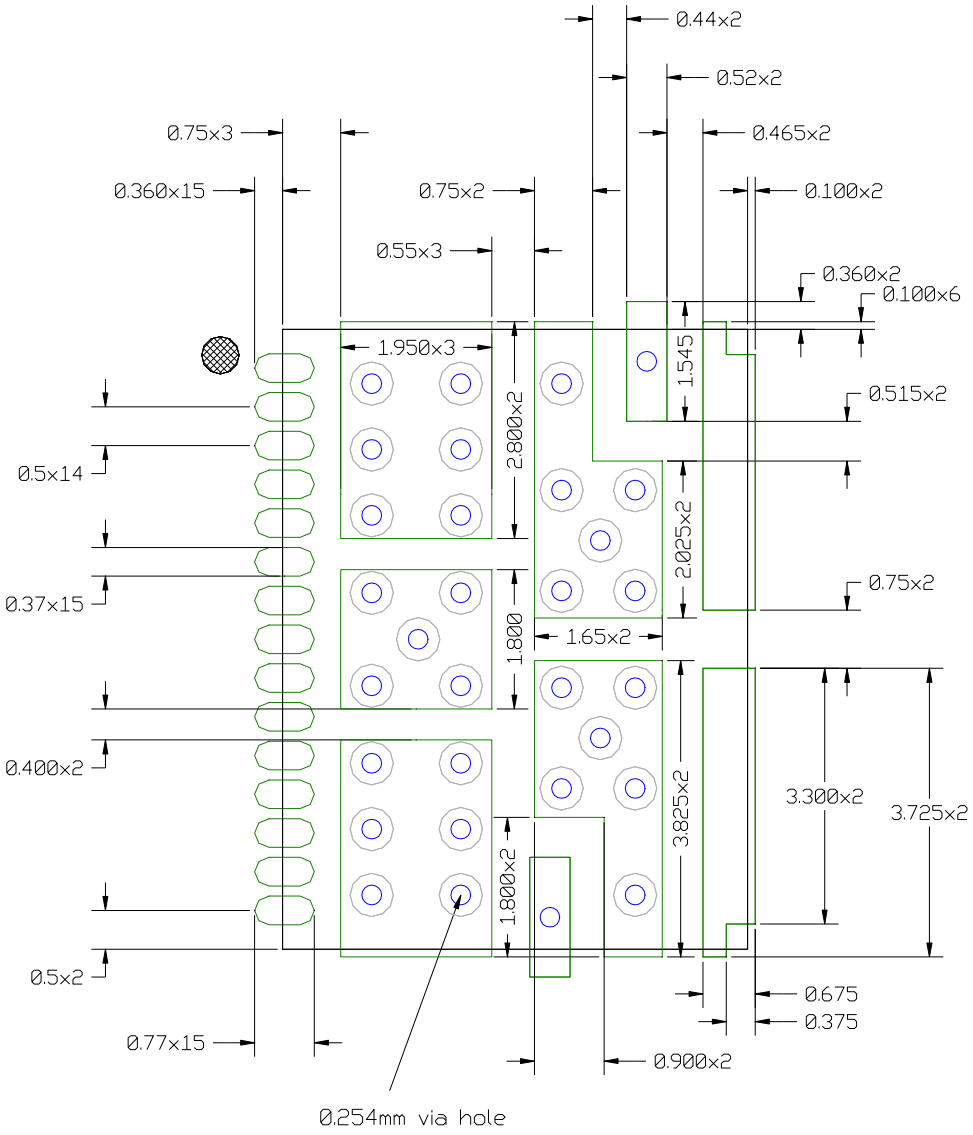


Figure 29: Solder Resist

STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 65% to 75% of the area of the lead lands depending on stencil thickness. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The low power signal stencil lead land apertures should therefore be shortened in length to keep area ratio of 65% to 75% while centered on lead land.
- The power pads VIN1, VIN2, PGND, SW1 and SW2, land pad apertures should be approximately 65% to 75% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open. Solder paste on large pads is broken down into small sections with a minimum gap of 0.2mm between allowing for out-gassing during solder reflow.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

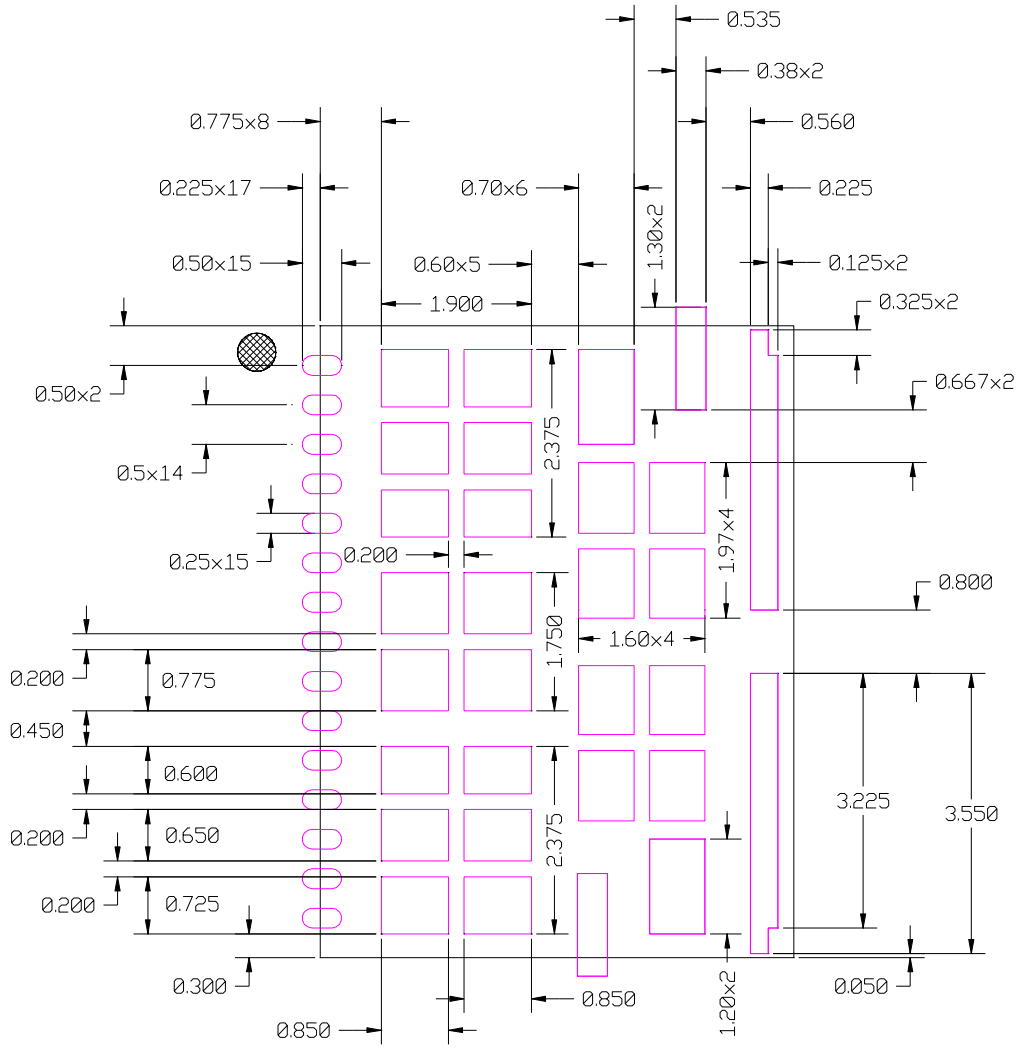


Figure 30: Stencil Design

MARKING INFORMATION

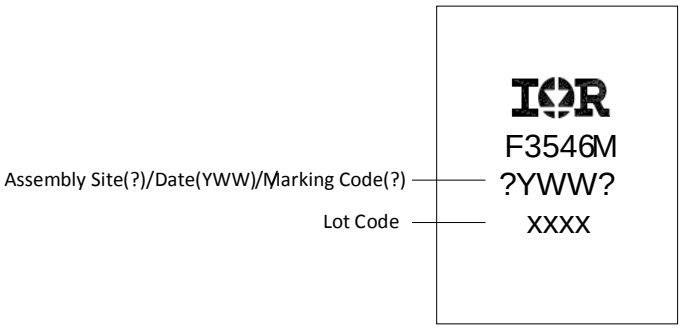
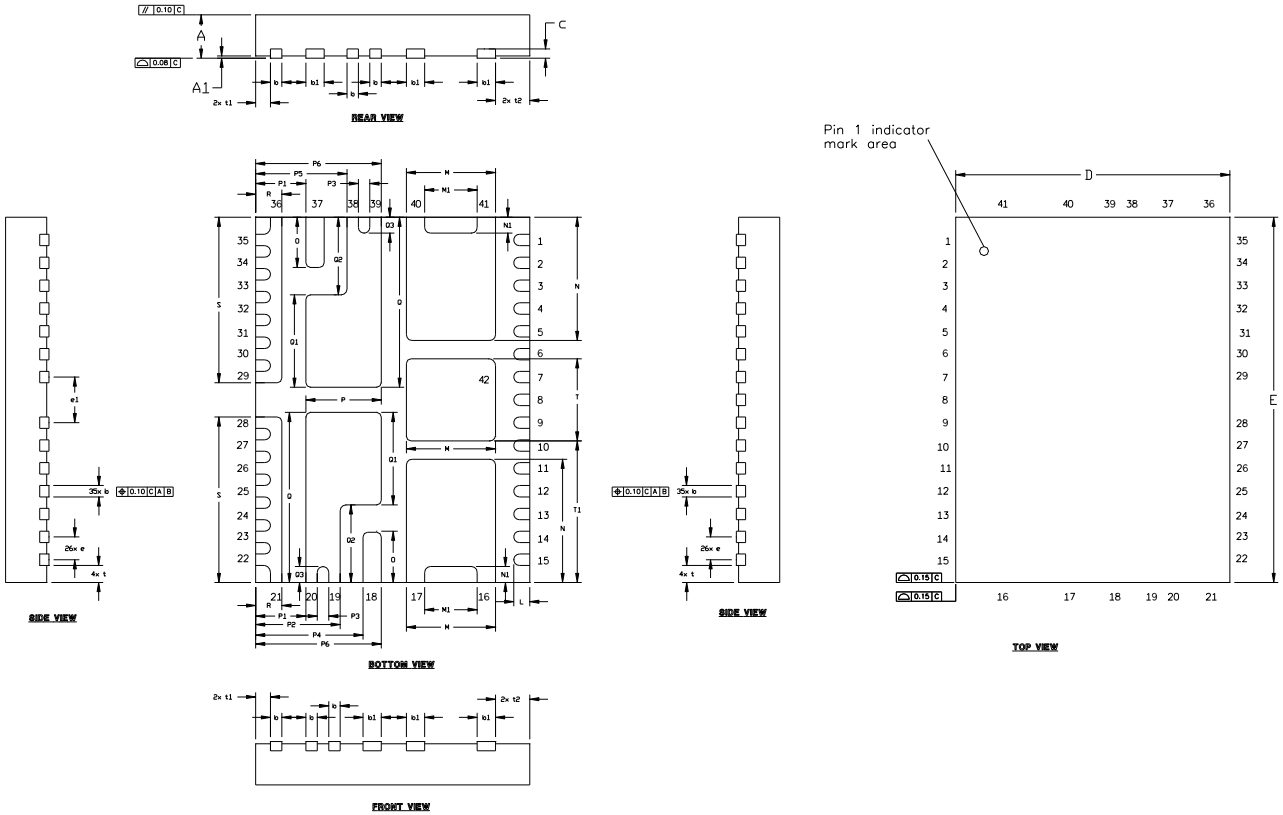


Figure 31: PQFN 6mm x 8mm

PACKAGE INFORMATION



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.200	0.300	.0079	.0118
b1	0.350	0.450	.0138	.0177
c	0.203 REF.		.0080 REF.	
D	6.000 BASIC		.2362 BASIC	
E	8.000 BASIC		.3150 BASIC	
e	0.500 BASIC		.0197 BASIC	
e1	1.000 BASIC		.0394 BASIC	
t	0.375 BASIC		.0148 BASIC	
t1	0.325 BASIC		.0128 BASIC	
t2	0.750 BASIC		.0295 BASIC	
L	0.300	0.400	.0118	.0157
M	1.900	2.000	.0748	.0787
M1	1.100	1.200	.0433	.0472
N	2.650	2.750	.1043	.1083
N1	0.300	0.400	.0118	.0157

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
O	1.050	1.150	.0413	.0453
P	1.600	1.700	.0630	.0669
P1	1.050	1.150	.0413	.0453
P2	1.800	1.900	.0709	.0748
P3	0.200	0.300	.0079	.0118
P4	2.300	2.400	.0906	.0945
P5	1.950	2.050	.0768	.0807
P6	2.700	2.800	.1063	.1102
Q	3.675	3.775	.1447	.1486
Q1	1.975	2.075	.0778	.0817
Q2	1.650	1.750	.0650	.0689
Q3	0.300	0.400	.0118	.0157
R	0.525	0.625	.0207	.0246
S	3.575	3.675	.1407	.1447
T	1.750	1.850	.0689	.0728
T1	3.050	3.150	.1201	.1240

Figure 32: PQFN 6mm x 8mm

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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