

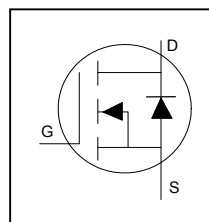
Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

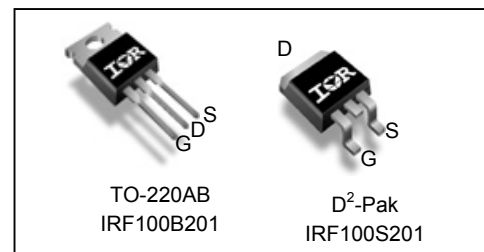
Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant, Halogen-Free

HEXFET® Power MOSFET



V_{DS}	100V
$R_{DS(on)}$ typ.	3.5mΩ
max	4.2mΩ
I_D (Silicon Limited)	192A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF100B201	TO-220	Tube	50	IRF100B201
IRF100S201	D²-Pak	Tape and Reel	800	IRF100S201

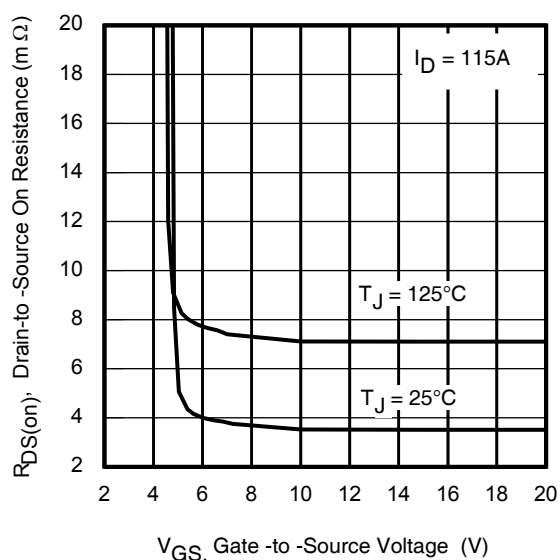


Fig 1. Typical On-Resistance vs. Gate Voltage

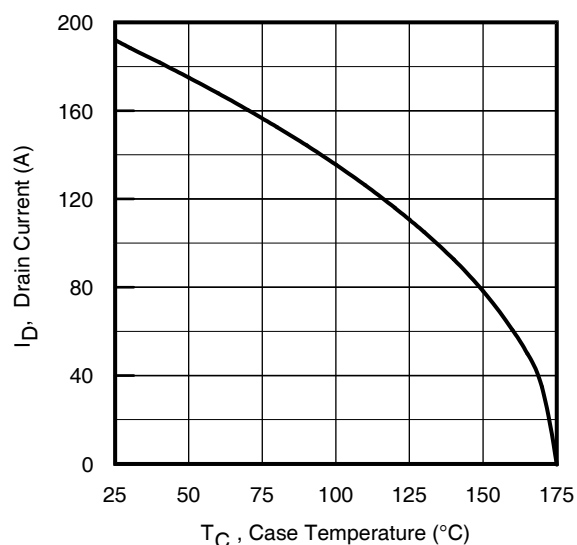


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	192	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	136	
I_{DM}	Pulsed Drain Current ①	690	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	441	W
	Linear Derating Factor	2.9	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	567	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ⑨	1005	
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑩	240	
I_{AR}	Avalanche Current ①	See Fig 15, 15, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	0.34	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.1	—	V/°C	Reference to 25°C , $I_D = 5\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.5	4.2	mΩ	$V_{GS} = 10\text{V}$, $I_D = 115\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Gate Resistance	—	2.2	—	Ω	

Notes:

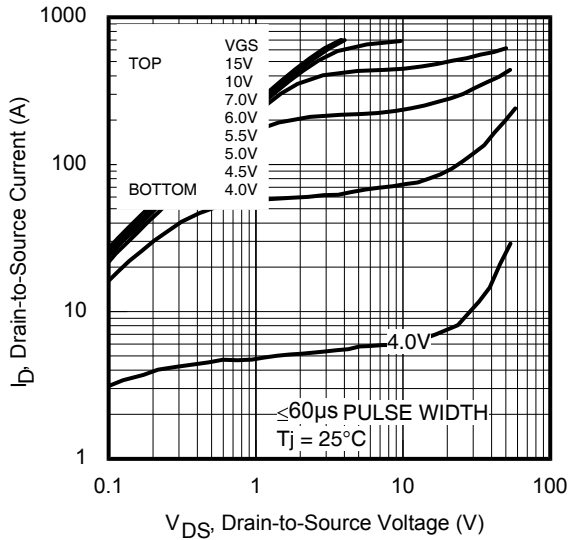
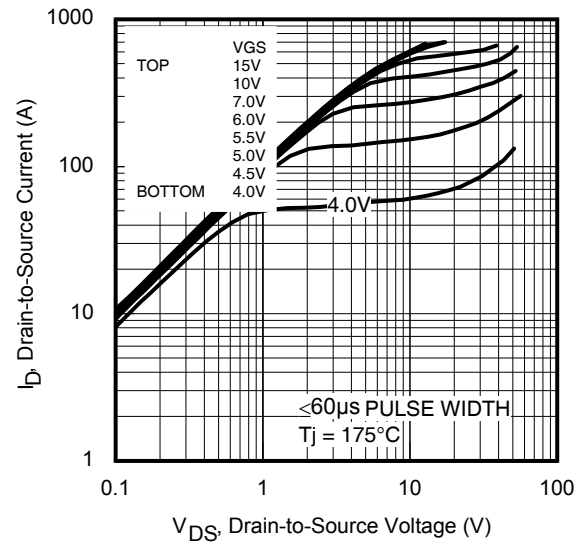
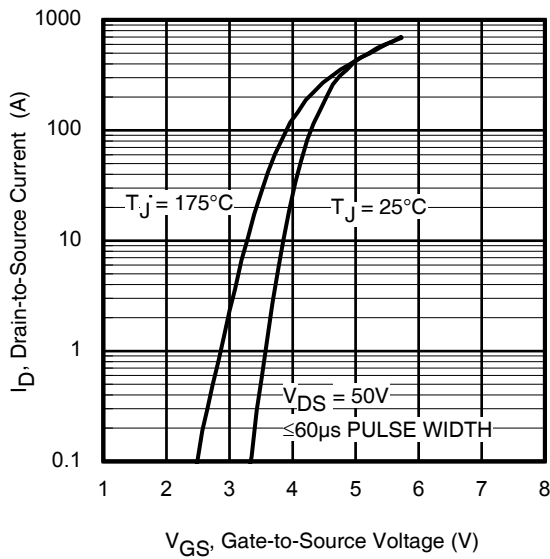
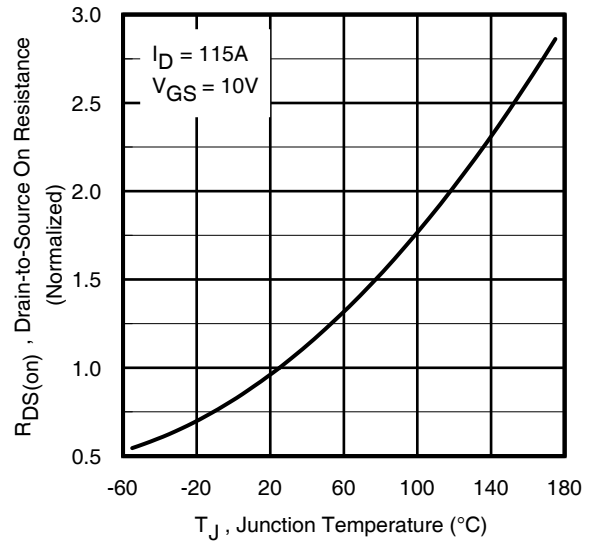
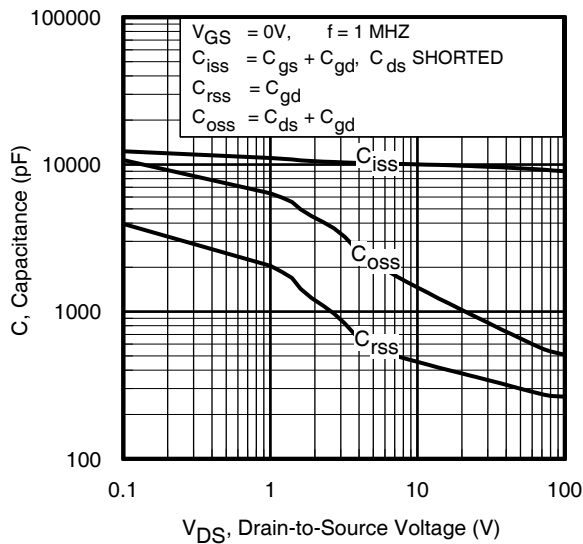
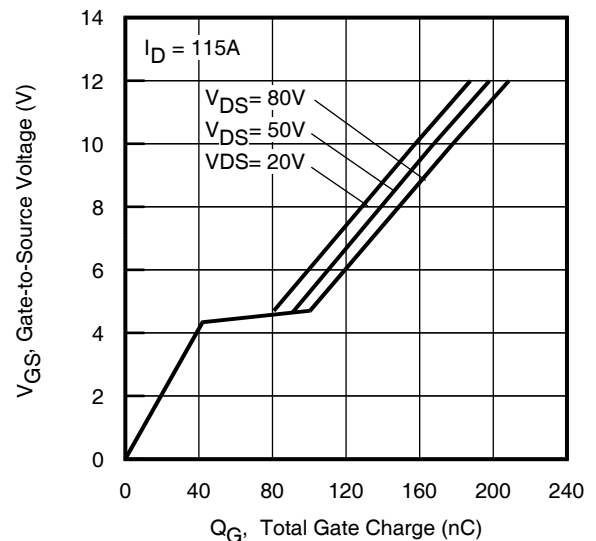
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 86\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 115\text{A}$, $V_{GS} = 10\text{V}$.
- ③ $I_{SD} \leq 115\text{A}$, $di/dt \leq 1400\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ R_θ is measured at T_J approximately 90°C .
- ⑧ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑨ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1.0\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 45\text{A}$, $V_{GS} = 10\text{V}$.
- ⑩ This value determined from sample failure population, starting $T_J = 25^\circ\text{C}$, $L = 86\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 115\text{A}$, $V_{GS} = 10\text{V}$.

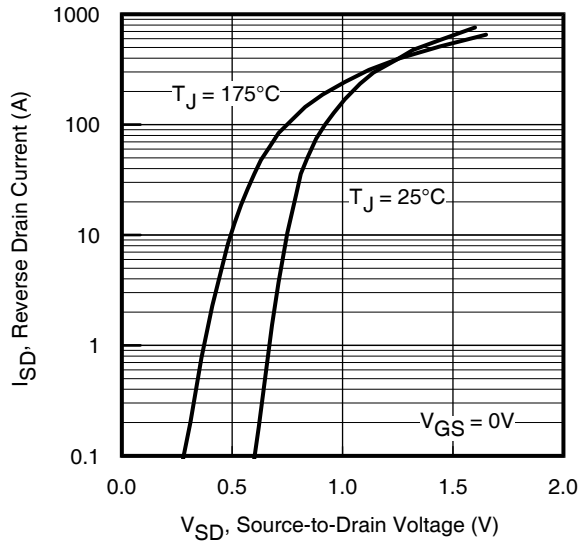
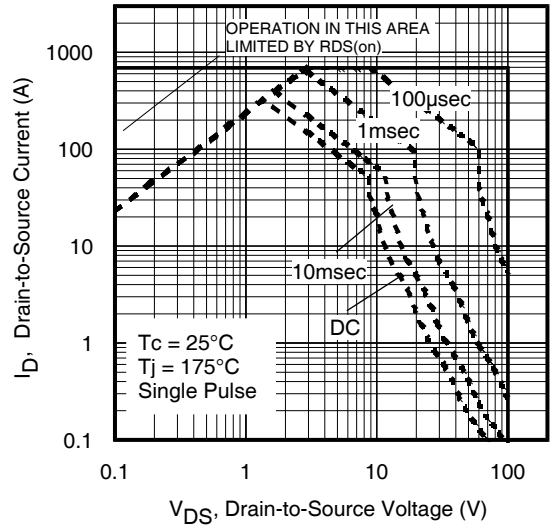
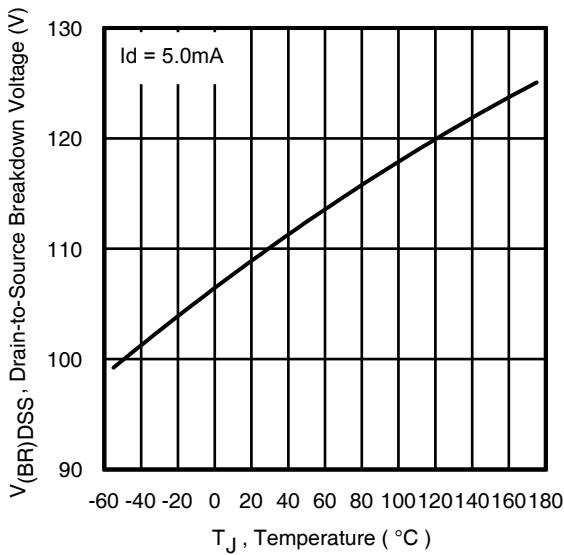
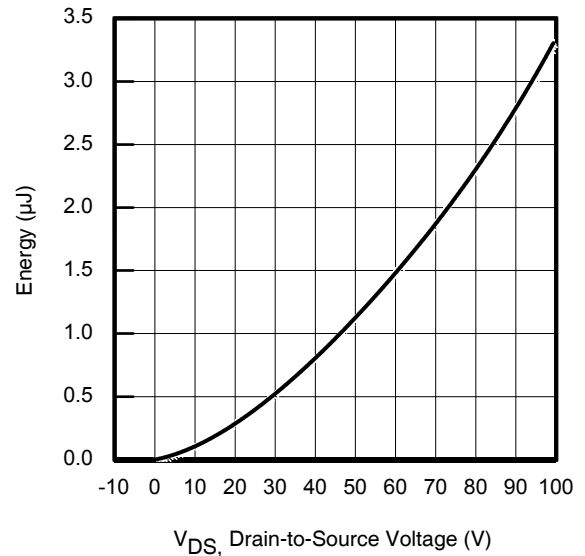
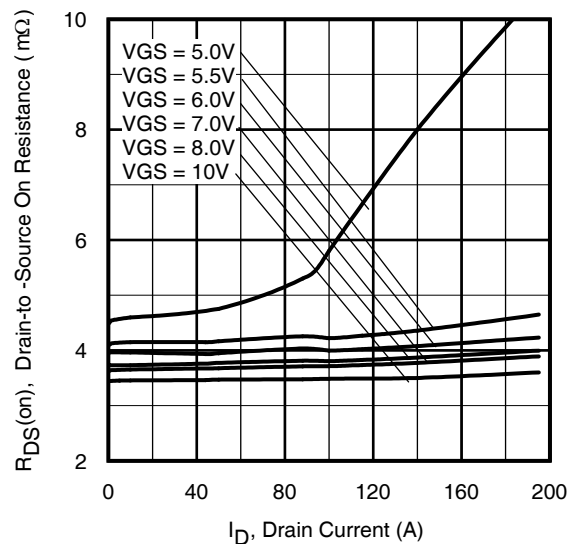
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	278	—	—	S	$V_{DS} = 10\text{V}$, $I_D = 115\text{A}$
Q_g	Total Gate Charge	—	170	255	nC	$I_D = 115\text{A}$
Q_{gs}	Gate-to-Source Charge	—	46	—		$V_{DS} = 50\text{V}$
Q_{gd}	Gate-to-Drain Charge	—	45	—		$V_{GS} = 10\text{V}$
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	125	—		
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 65\text{V}$
t_r	Rise Time	—	97	—		$I_D = 115\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	110	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	100	—		$V_{GS} = 10\text{V}^{(4)}$
C_{iss}	Input Capacitance	—	9500	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	660	—		$V_{DS} = 50\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	310	—		$f = 1.0\text{MHz}$, See Fig.TBD
$C_{oss\text{ eff.}(ER)}$	Effective Output Capacitance (Energy Related)	—	725	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to $80\text{V}^{(6)}$
$C_{oss\text{ eff.}(TR)}$	Output Capacitance (Time Related)	—	950	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to $80\text{V}^{(5)}$

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	192	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⁽¹⁾	—	—	690		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 115\text{A}$, $V_{GS} = 0\text{V}$ ⁽⁴⁾
dv/dt	Peak Diode Recovery dv/dt ⁽³⁾	—	18	—	V/ns	$T_J = 175^\circ\text{C}$, $I_S = 115\text{A}$, $V_{DS} = 100\text{V}$
t_{rr}	Reverse Recovery Time	—	47	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 85\text{V}$
		—	55	—		$T_J = 125^\circ\text{C}$ $I_F = 115\text{A}$,
Q_{rr}	Reverse Recovery Charge	—	90	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⁽⁴⁾
		—	123	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	3.5	—	A	$T_J = 25^\circ\text{C}$


Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Normalized On-Resistance vs. Temperature

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 9. Typical Source-Drain Diode Forward Voltage

Fig 10. Maximum Safe Operating Area

Fig 11. Drain-to-Source Breakdown Voltage

Fig 12. Typical C_{oss} Stored Energy

Fig 13. Typical On-Resistance vs. Drain Current

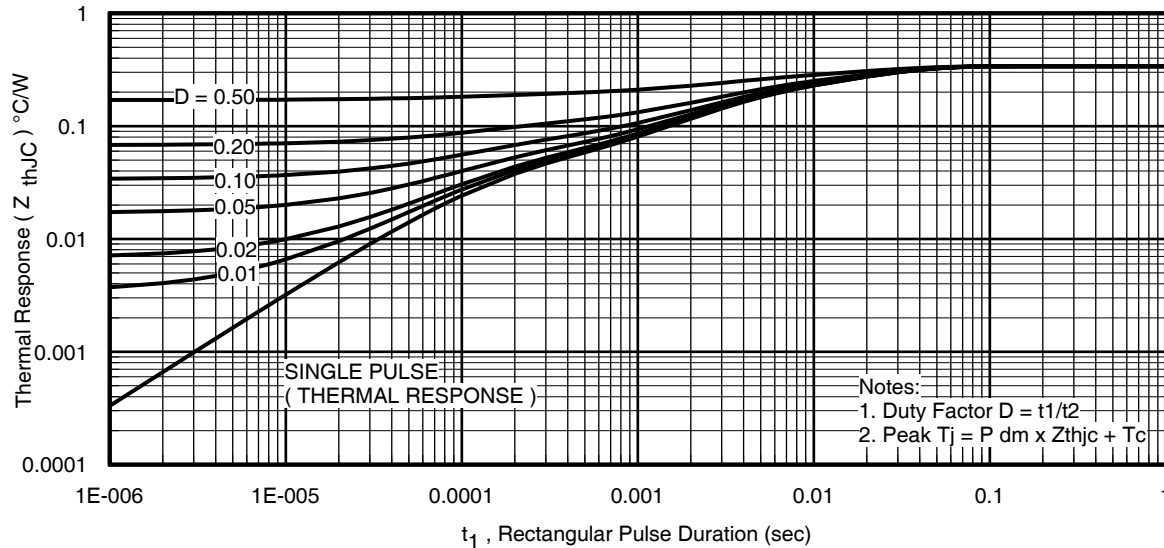


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

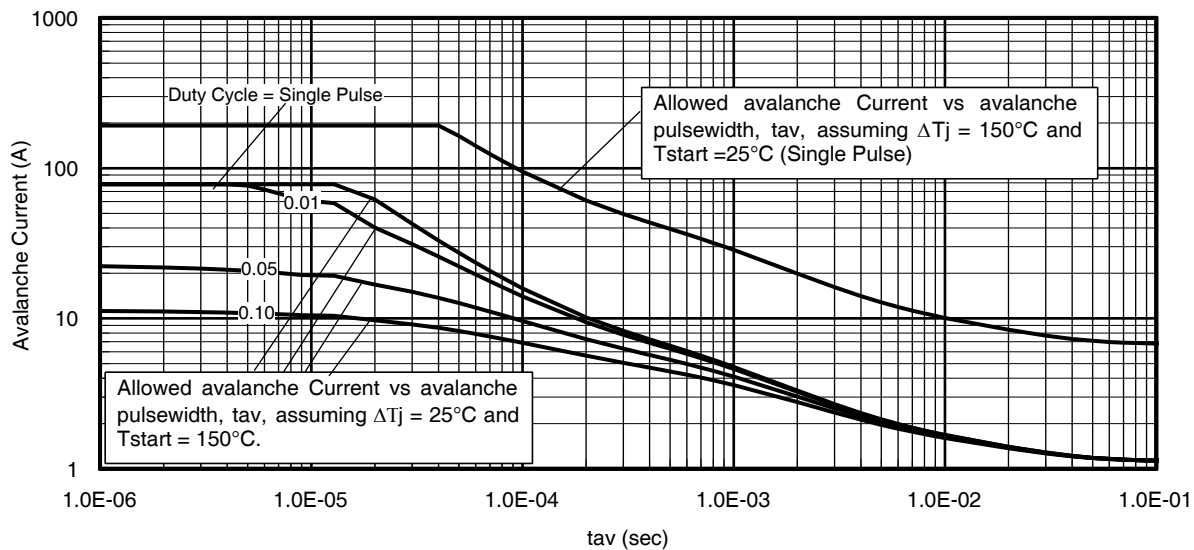


Fig 15. Avalanche Current vs. Pulse Width

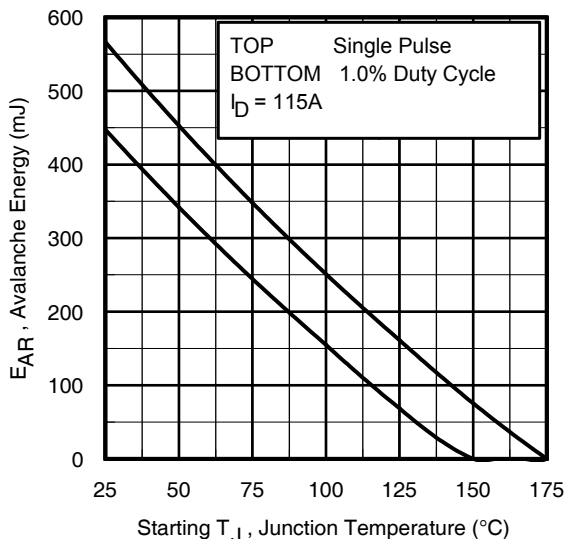
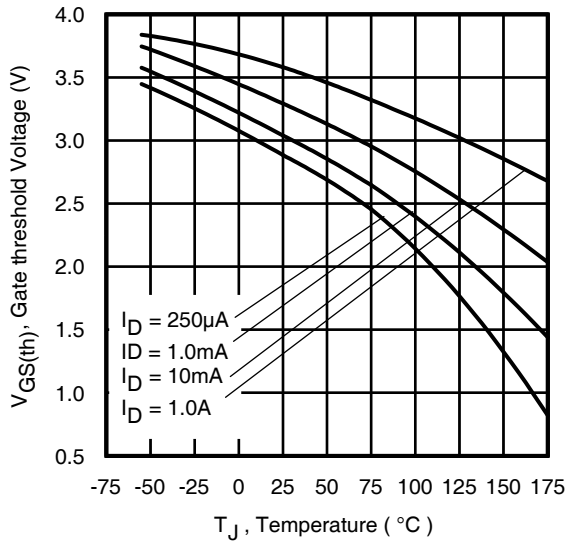
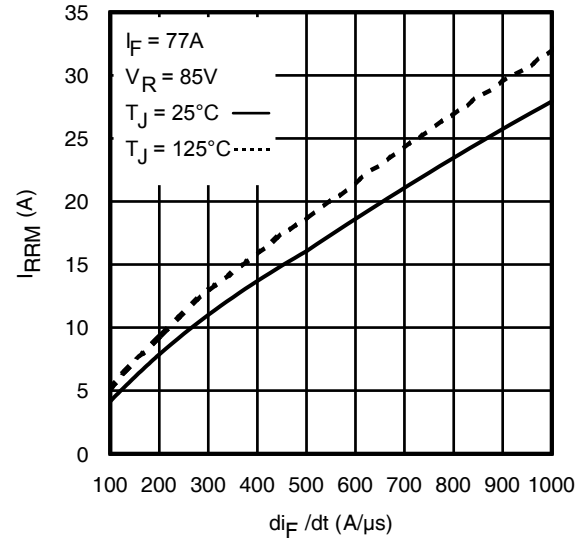
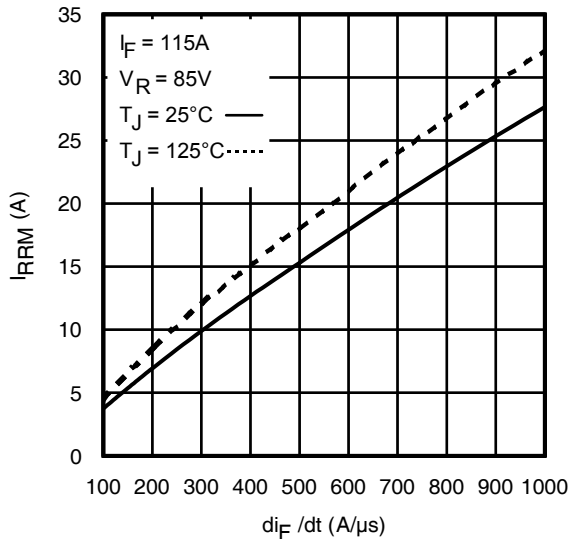
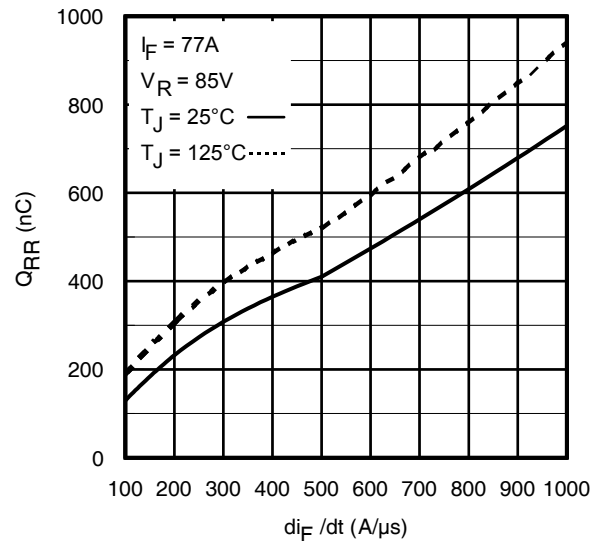
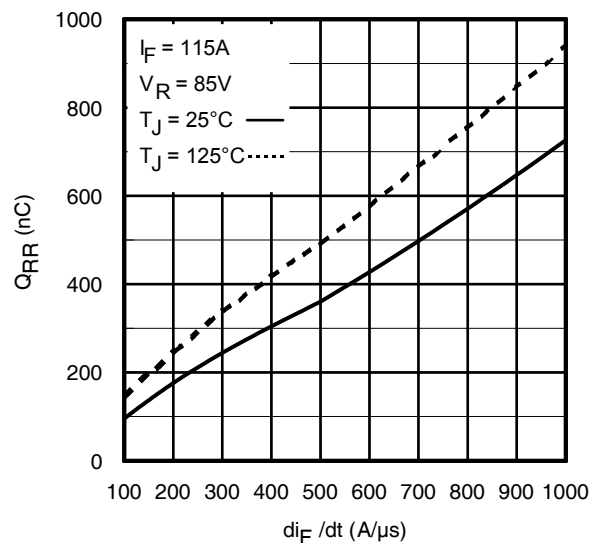


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


Fig 17. Threshold Voltage vs. Temperature

Fig 18. Typical Recovery Current vs. di_F/dt

Fig 19. Typical Recovery Current vs. di_F/dt

Fig 20. Typical Stored Charge vs. di_F/dt

Fig 21. Typical Stored Charge vs. di_F/dt

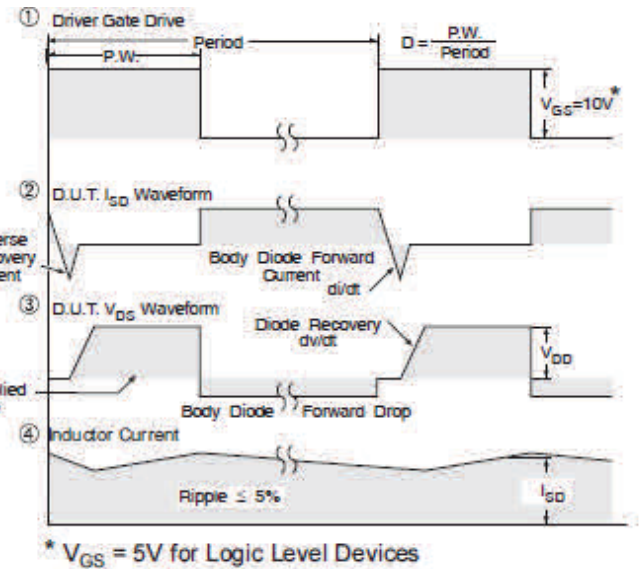
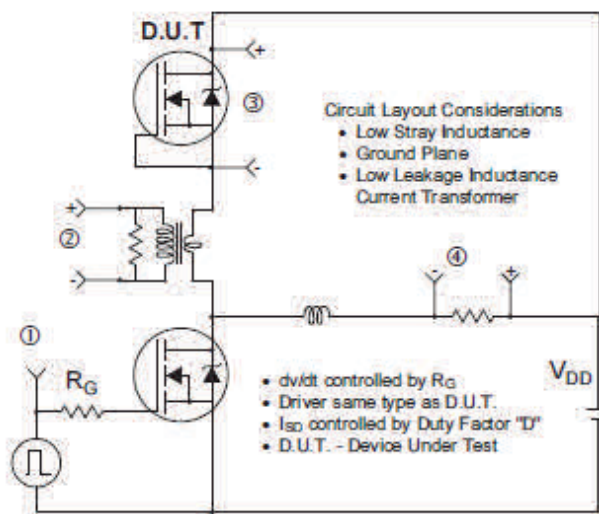


Fig 22. Peak Diode Recovery dV/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

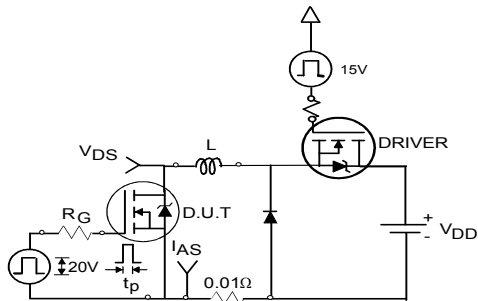


Fig 23a. Unclamped Inductive Test Circuit

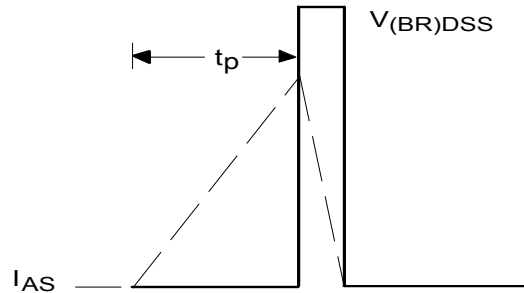


Fig 23b. Unclamped Inductive Waveforms

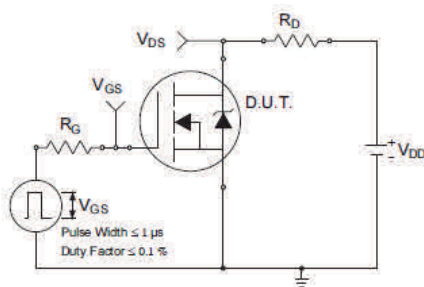


Fig 24a. Switching Time Test Circuit

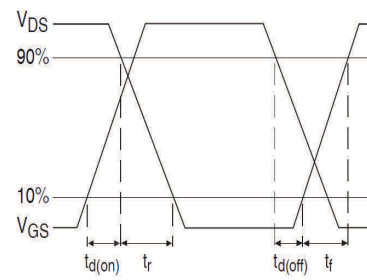


Fig 24b. Switching Time Waveforms

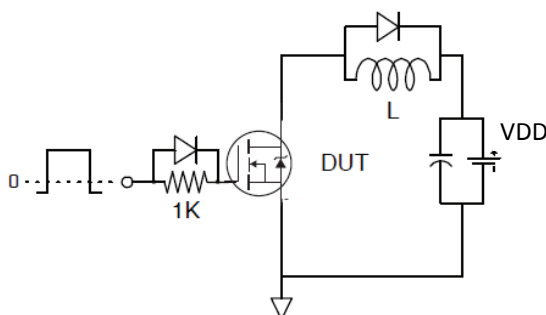


Fig 25a. Gate Charge Test Circuit

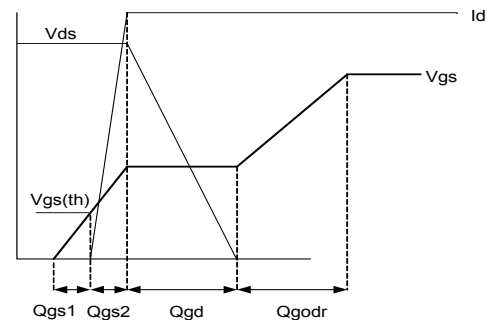
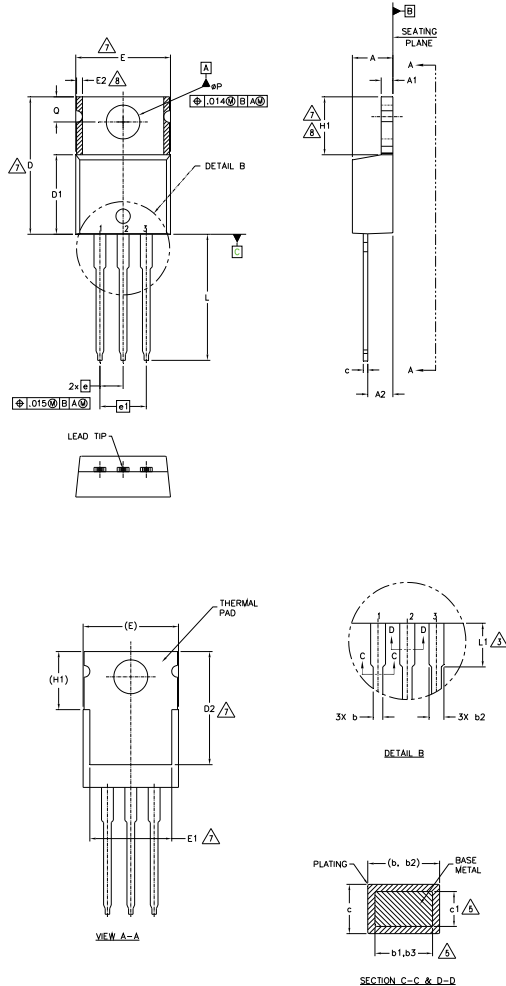


Fig 25b. Gate Charge Waveform

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	5
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	7
D2	11.68	12.88	.460	.507	
E	9.65	10.67	.380	.420	
E1	6.86	8.89	.270	.350	7
E2	—	0.76	—	.030	8
e	2.54 BSC		.100 BSC		7,8
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	3
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

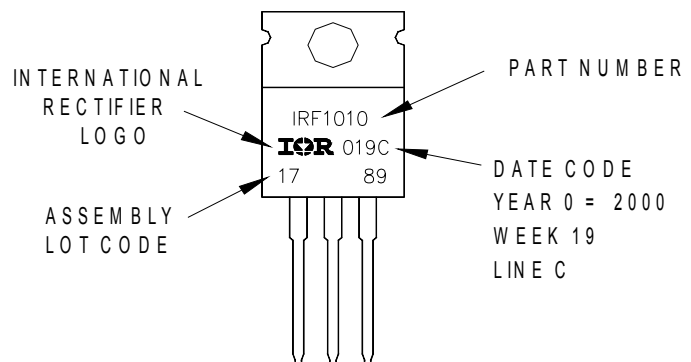
DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 2000
 IN THE ASSEMBLY LINE "C"

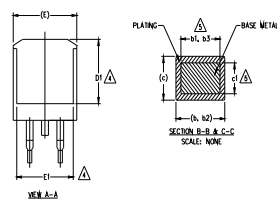
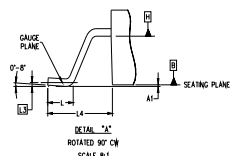
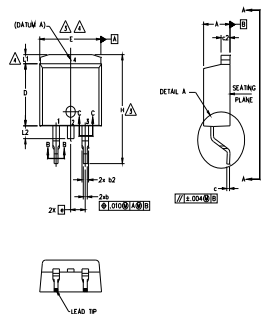
Note: "P" in assembly line position
 indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYM- BOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	4
L1	—	1.65	—	.066	
L2	1.27	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

DIODES

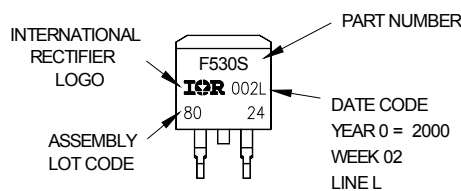
- 1.- ANODE *
2, 4.- CATHODE
3.- ANODE

* PART DEPENDENT.

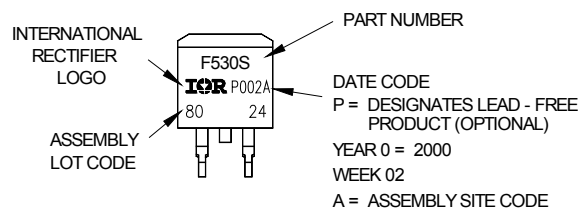
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

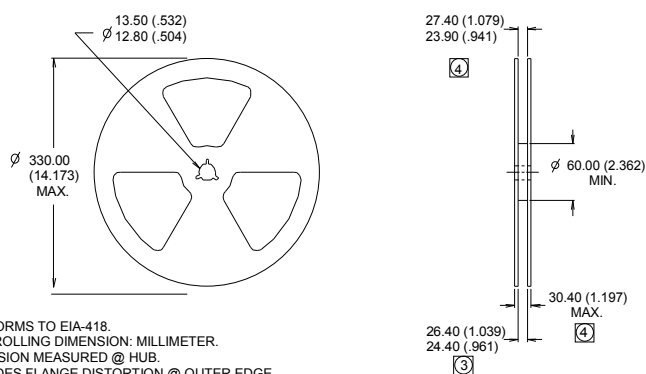
Figure 1 shows the dimensions of the TRR and TRL. The TRR (Top Right Resistor) and TRL (Top Left Resistor) are shown in cross-section. The dimensions are given in inches and millimeters.

TRR Dimensions:

- Top view: 1.60 (.063) x 1.50 (.059) (overall), 1.60 (.063) x 1.50 (.059) (inner square)
- Side view: 1.85 (.073) x 1.65 (.065) (overall), 4.10 (.161) x 3.90 (.153) (inner square)
- Bottom view: 11.60 (.457) x 11.40 (.449) (overall), 1.75 (.069) x 1.25 (.049) (inner square)

TRL Dimensions:

- Top view: 10.90 (.429) x 10.70 (.421) (overall), 16.10 (.634) x 15.90 (.626) (inner square)
- Side view: 15.42 (.609) x 15.22 (.601) (overall), 24.30 (.957) x 23.90 (.941) (inner square)
- Bottom view: 4.72 (.136) x 4.52 (.178) (overall), 0.368 (.0145) x 0.342 (.0135) (inner square)



NOTES :

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ☒ 3. DIMENSION MEASURED @ HUB.
- ☒ 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

March 26, 2015

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-220	N/A
	D ² Pak	MSL1
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
 To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[IRF100B201](#) [IRF100S201](#)