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## **Sup/IRBuck™**

### **USER GUIDE FOR IR3832W EVALUATION BOARD**

#### **DESCRIPTION**

The IR3832W is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 5mmx6mm Power QFN package.

Key features offered by the IR3832W include programmable soft-start ramp, Power Good, thermal protection, programmable switching frequency, tracking input, enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3832W evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3832W is available in the IR3832W data sheet.

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#### **BOARD FEATURES**

- $V_{in} = +12V$  (13.2V Max)
- $V_{cc} = +5V$  (5.5V Max)
- $V_{out} = +0.75V @ 0- \pm 4A$
- $F_s = 400kHz$
- $L = 1.50\mu H$
- $C_{in} = 2 \times 10\mu F$  (ceramic 1206) +  $330\mu F$  (electrolytic)
- $C_{out} = 6 \times 22\mu F$  (ceramic 0805)

## CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum  $\pm 4A$  load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3832W has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 4.5V-5.5V supply and it would be connected to Vcc+ and Vcc-.

If single 12V application is required, connect R7 ( zero Ohm resistor) which enables the on board bias regulator (see schematic). In this case there is no need of external Vcc supply.

The output tracks VDDQ input. The value of R14 and R28 can be selected to provide the desired ratio between the output voltage and the tracking input. For proper operation of IR3832W, the voltage at Vp pin should not exceed Vcc.

**Table I. Connections**

| Connection       | Signal Name                |
|------------------|----------------------------|
| VIN+             | V <sub>in</sub> (+12V)     |
| VIN-             | Ground of V <sub>in</sub>  |
| Vcc+             | Vcc input                  |
| Vcc-             | Ground for Vcc input       |
| VOUT-            | Ground of V <sub>out</sub> |
| VOUT+            | V <sub>out</sub> (+0.75V)  |
| Enable           | Enable                     |
| V <sub>DDQ</sub> | Tracking Input             |
| PGood            | Power Good Signal          |

## LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3832W SupIRBuck and all of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3832W. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

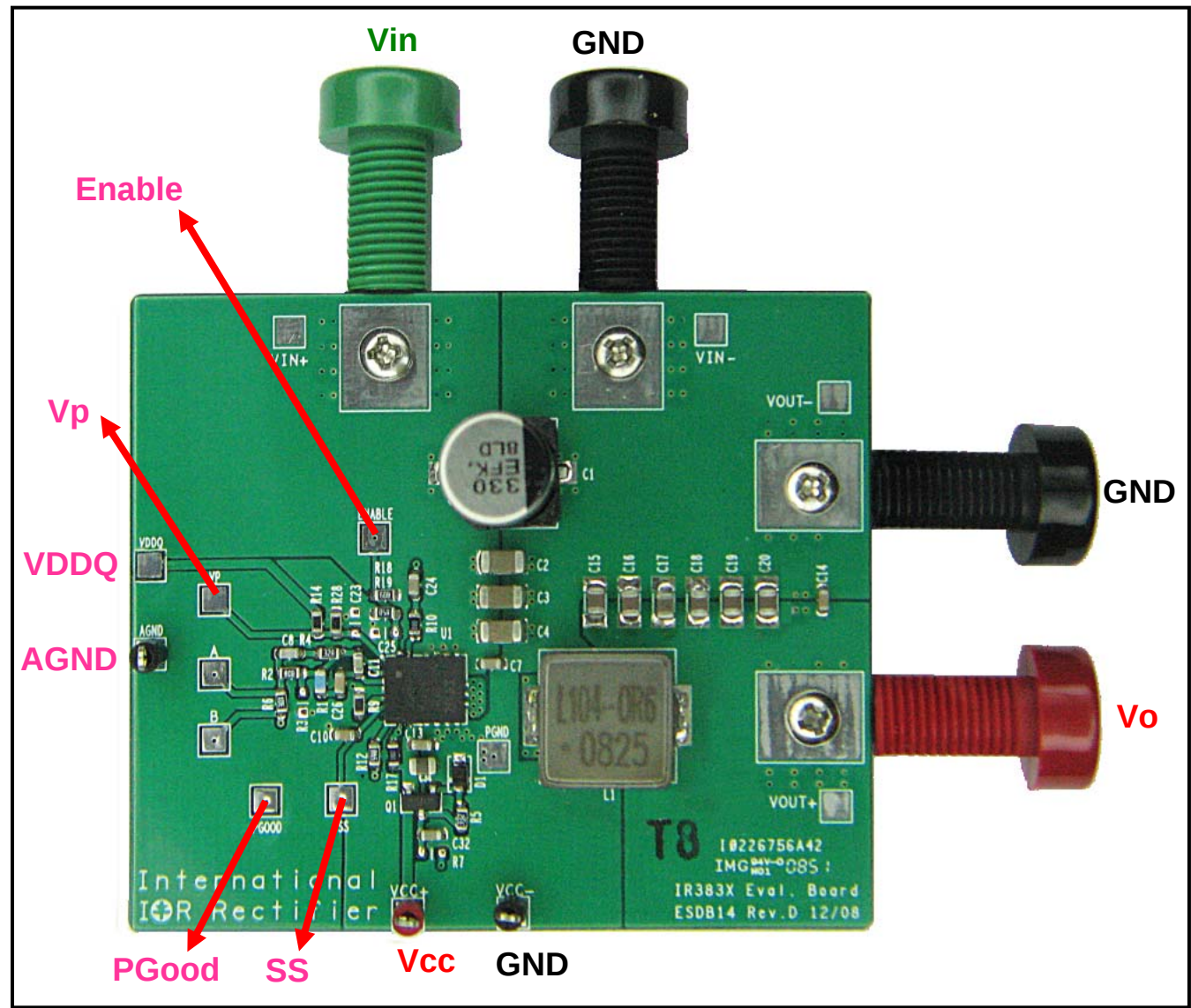


Fig. 1: Connection diagram of IR383xW evaluation boards

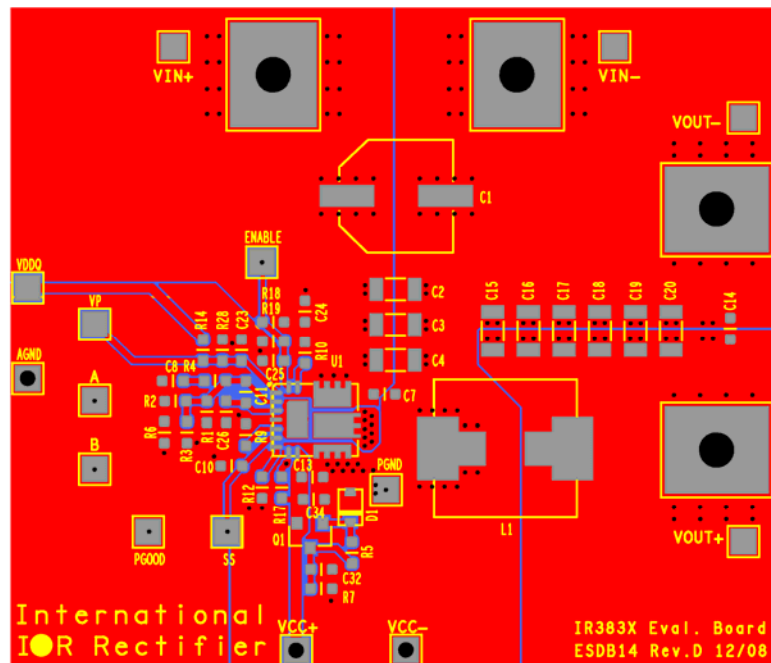


Fig. 2: Board layout, top overlay

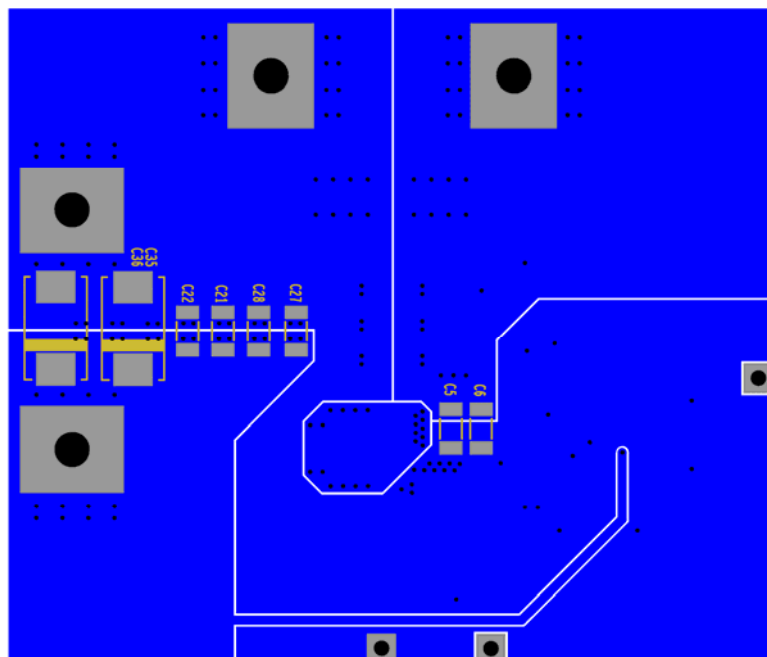
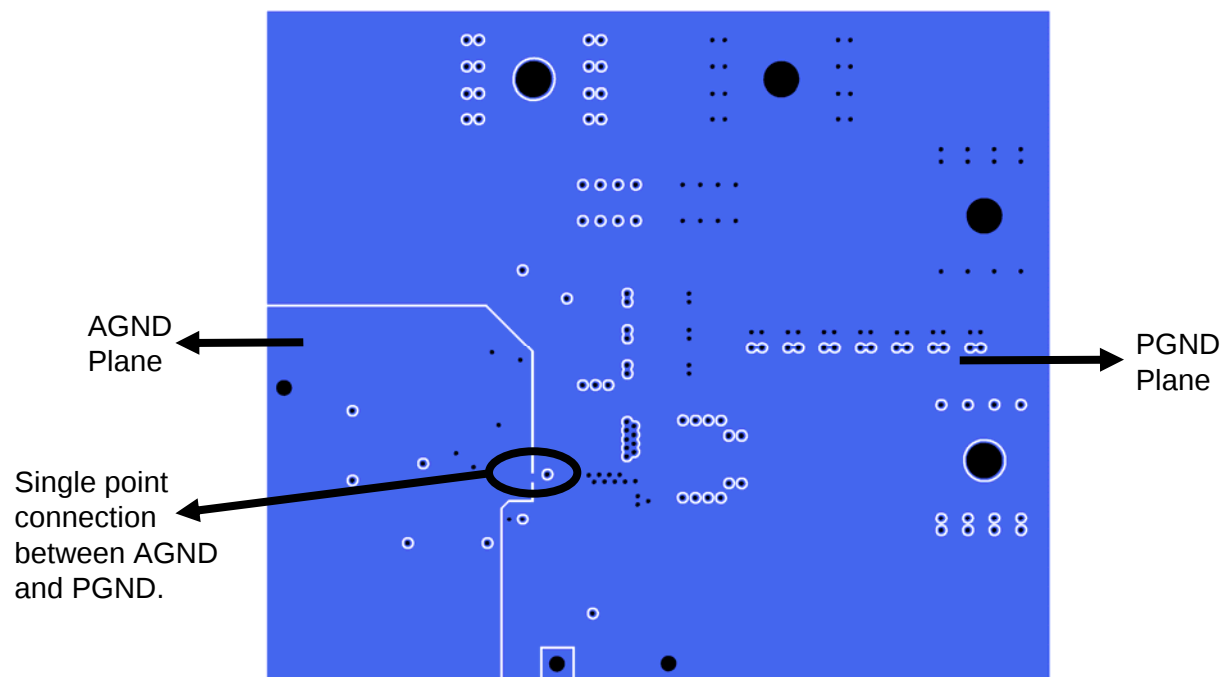
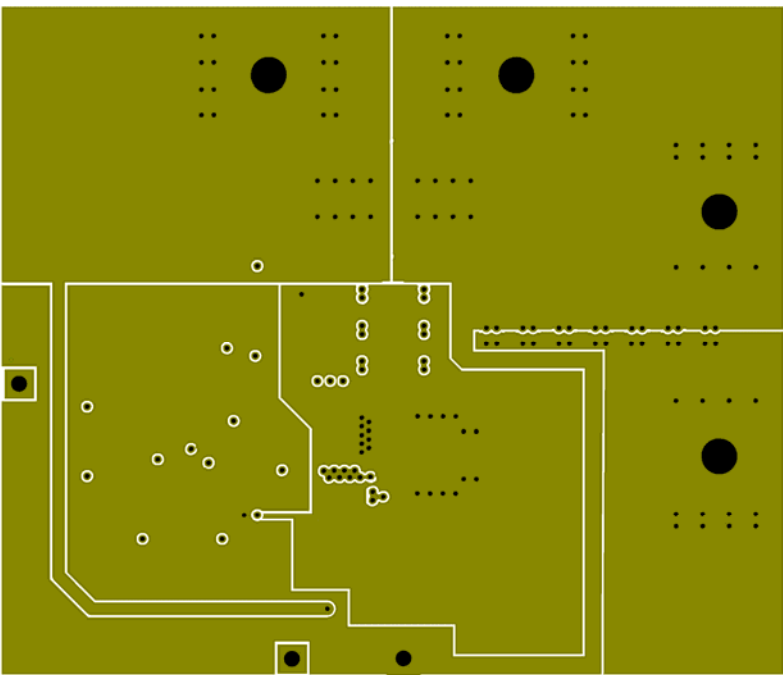


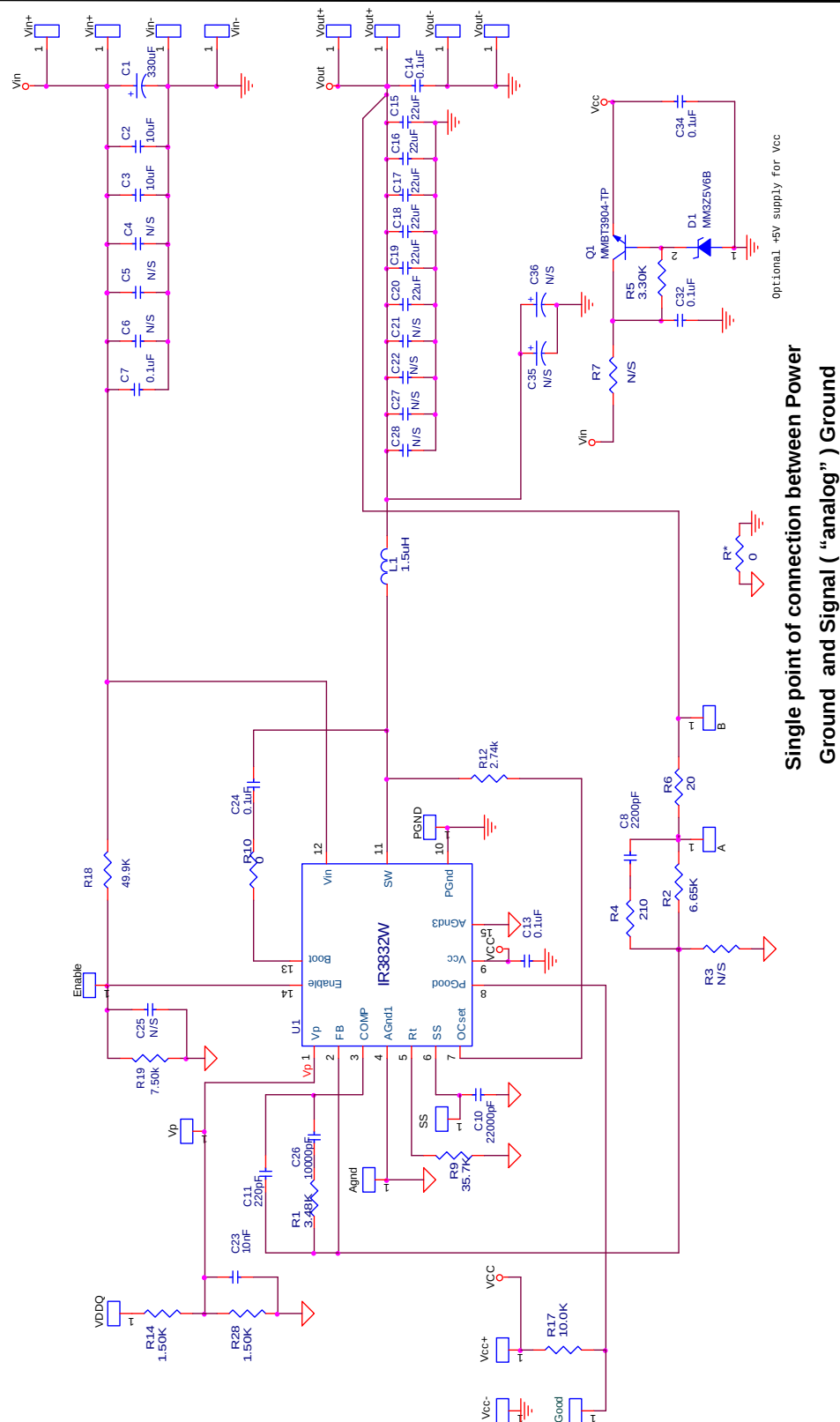
Fig. 3: Board layout, bottom overlay



**Fig. 4: Board layout, mid-layer I**



**Fig. 5: Board layout, mid-layer II**



**Fig. 6: Schematic of the IR3832W evaluation board**

## Bill of Materials

| Item | Quantity | Part Reference          | Value        | Description                      | Manufacturer            | Part Number        |
|------|----------|-------------------------|--------------|----------------------------------|-------------------------|--------------------|
| 1    | 1        | C1                      | 330uF        | SMD Elecrolitic, Fsize, 25V, 20% | Panasonic               | EEV-FK1E331P       |
| 2    | 2        | C2 C3                   | 10uF         | 1206, 16V, X5R, 20%              | Panasonic - ECG         | ECJ-3YB1C106M      |
| 3    | 1        | C10                     | 0.022uF      | 0603, 16V, X7R, 10%              | Panasonic- ECG          | ECJ-1VB1C223K      |
| 4    | 1        | C34                     | 10uF         | 0805, 10V, X5R, 20%              | Panasonic - ECG         | ECJ-GVB1A106M      |
| 5    | 5        | C7 C13 C14 C24 C32      | 0.1uF        | 0603, 25V, X7R, 10%              | Panasonic - ECG         | ECJ-1VB1E104K      |
| 6    | 1        | C8                      | 2200pF       | 0603, 50V, NP0, 5%               | Murata                  | GRM1885C1H222JA01D |
| 7    | 1        | C11                     | 220pF        | 0603, 50V, NP0, 5%               | Panasonic- ECG          | ECJ-1VC1H221J      |
| 8    | 6        | C15 C16 C17 C18 C19 C20 | 22uF         | 0805, 6.3V, X5R, 20%             | Panasonic- ECG          | ECJ-2FB0J226M      |
| 9    | 2        | C25, C26                | 10000pF      | 0603, 50V, X7R, 10%              | Panasonic - ECG         | ECJ-1VB1H103K      |
| 10   | 1        | D1                      | MM3Z5V6B     | Zener, 5.6V                      | Fairchild               | MM3Z5V6B           |
| 11   | 1        | L1                      | 1.5uH        | 11.5x10x4mm, 20%, 3.9mOhm        | Delta                   | MPO104-1R5IR       |
| 12   | 1        | Q1                      | MMBT3904/SOT | NPN, 40V, 200mA, SOT-23          | Fairchild               | MMBT3904/SOT       |
| 13   | 1        | R5                      | 3.3k         | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX3301     |
| 14   | 1        | R18                     | 49.9k        | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX4992     |
| 15   | 1        | R4                      | 210          | Thick Film, 0603,1/10W,1%        | Panasonic - ECG         | ERJ-3EKF2100V      |
| 16   | 1        | R6                      | 20           | Thick Film, 0603,1/10 W,1%       | Vishey/Dale             | CRCW060320R0FKEA   |
| 17   | 1        | R9                      | 35.7k        | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX3572     |
| 18   | 1        | R12                     | 2.74k        | Thick Film, 0603,1/10 W,1%       | Rohm                    | MCR03EZPFX2741     |
| 19   | 1        | R17                     | 10.0k        | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX1002     |
| 20   | 1        | R19                     | 7.5k         | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX7501     |
| 21   | 1        | R10                     | 0            | Thick Film, 0603,1/10W,1%        | Yageo                   | RC0603FR-100RL     |
| 22   | 1        | R1                      | 3.48k        | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX3481     |
| 23   | 1        | R2                      | 6.65k        | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX6651     |
| 24   | 2        | R14, R28                | 1.50k        | Thick Film, 0603,1/10W,1%        | Rohm                    | MCR03EZPFX1501     |
| 25   | 1        | U1                      | IR3832W      | 4A SuplIRBuck, 6mmx5mm           | International Rectifier | IR3832WMPbF        |

## TYPICAL OPERATING WAVEFORMS

$V_{in}=12.0V$ ,  $V_{cc}=5V$ ,  $V_o=0.75V$ ,  $I_o=0- \pm 4A$ , Room Temperature, No Air Flow

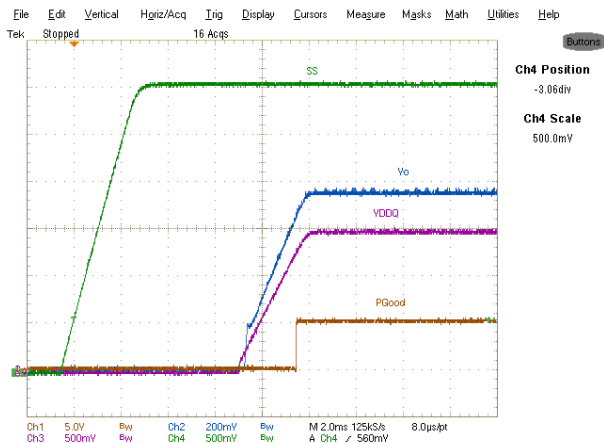


Fig. 7: Start up at 4A, sourcing current  
Ch<sub>1</sub>:PGood, Ch<sub>2</sub>:V<sub>out</sub>, Ch<sub>3</sub>:V<sub>DDQ</sub>, Ch<sub>4</sub>:SS

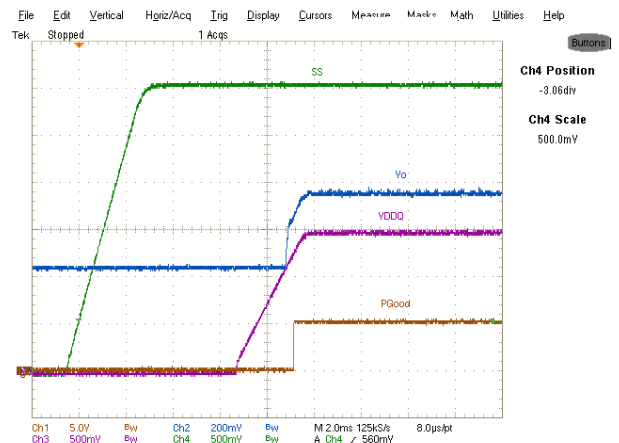


Fig. 8: Start up with Prebias, 0A Load  
Ch<sub>1</sub>:PGood, Ch<sub>2</sub>:V<sub>out</sub>, Ch<sub>3</sub>:V<sub>DDQ</sub>, Ch<sub>4</sub>:SS

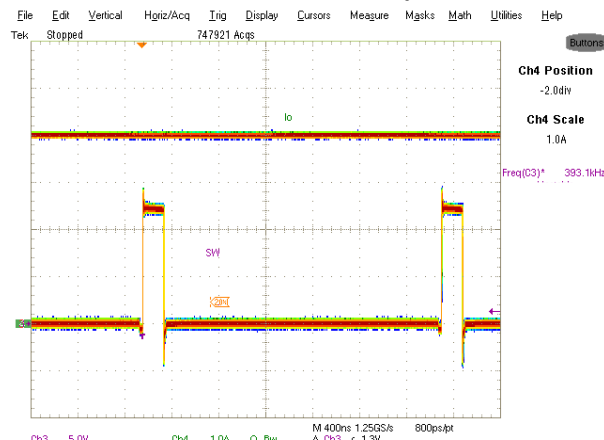


Fig. 9: Inductor node at 4A, sourcing current, Ch<sub>3</sub>:SW, Ch<sub>4</sub>:I<sub>out</sub>

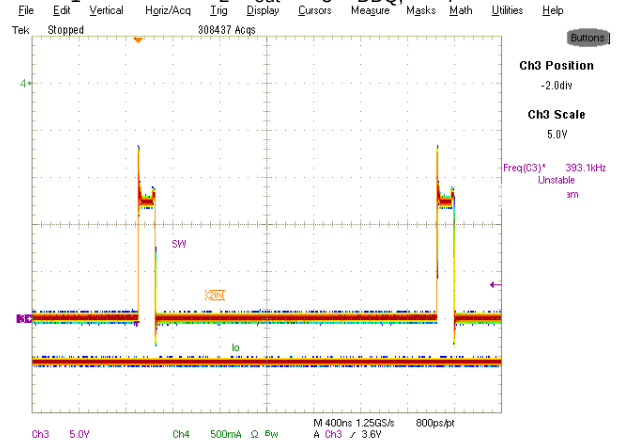


Fig. 10: Inductor node at -3A, sinking current, Ch<sub>3</sub>:SW, Ch<sub>4</sub>:I<sub>out</sub>

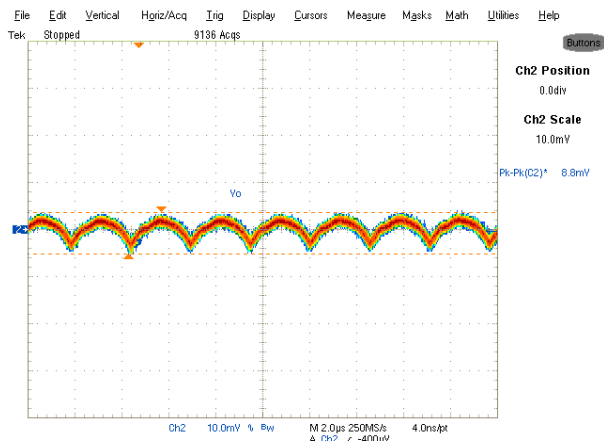


Fig. 11: Output Voltage Ripple, 4A, sourcing current, Ch<sub>2</sub>:V<sub>out</sub>

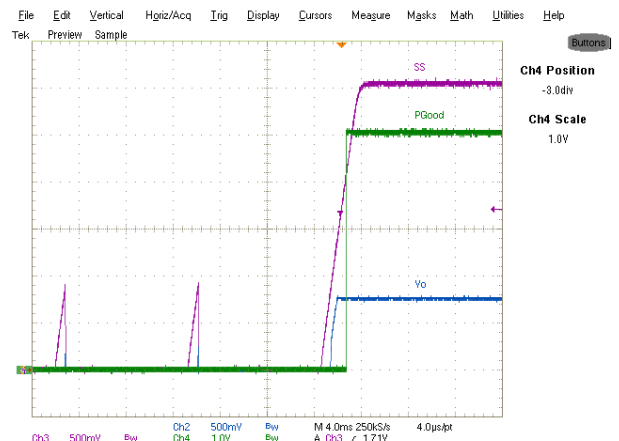


Fig. 12: Short (Hiccup) Recovery  
Ch<sub>2</sub>:V<sub>out</sub>, Ch<sub>3</sub>:V<sub>SS</sub>, Ch<sub>4</sub>:PGood

## TYPICAL OPERATING WAVEFORMS

$V_{in}=12V$ ,  $V_{cc}=5V$ ,  $V_o=0.75V$ , Room Temperature, No Air Flow

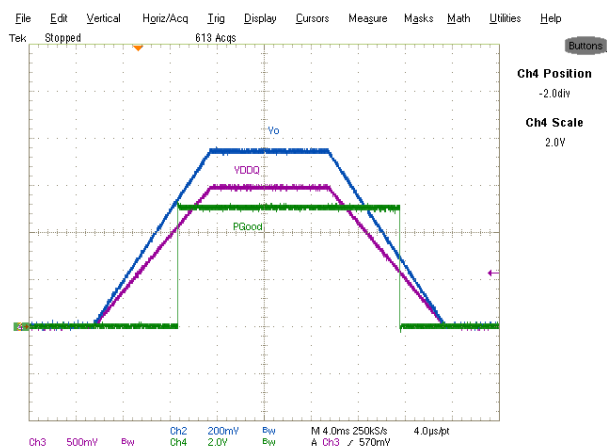


Fig. 13: Tracking 4A, sourcing current,  
 $Ch_2: V_{out}$ ,  $Ch_3: V_{DDQ}$ ,  $Ch_4: PGood$

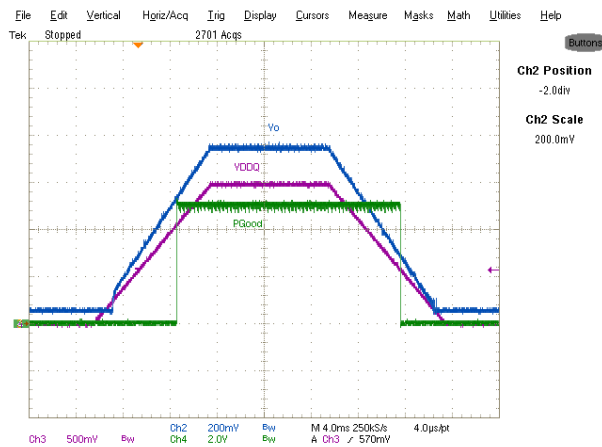


Fig. 14: Tracking -3A load, sinking current,  
 $Ch_2: V_{out}$ ,  $Ch_3: V_{DDQ}$ ,  $Ch_4: PGood$

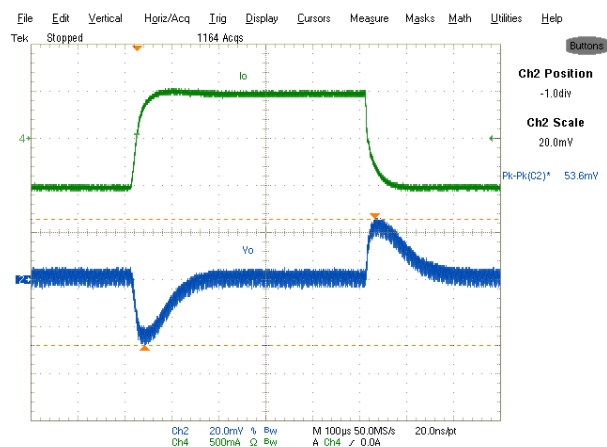


Fig. 15: Transient Response, 1A/us  
-0.5A to +0.5A load,  $Ch_2: V_{out}$ ,  $Ch_4: I_o$

**TYPICAL OPERATING WAVEFORMS**

Vin=12V, Vcc=5V, Vo=0.75V, Io=+4A, Room Temperature, No Air Flow

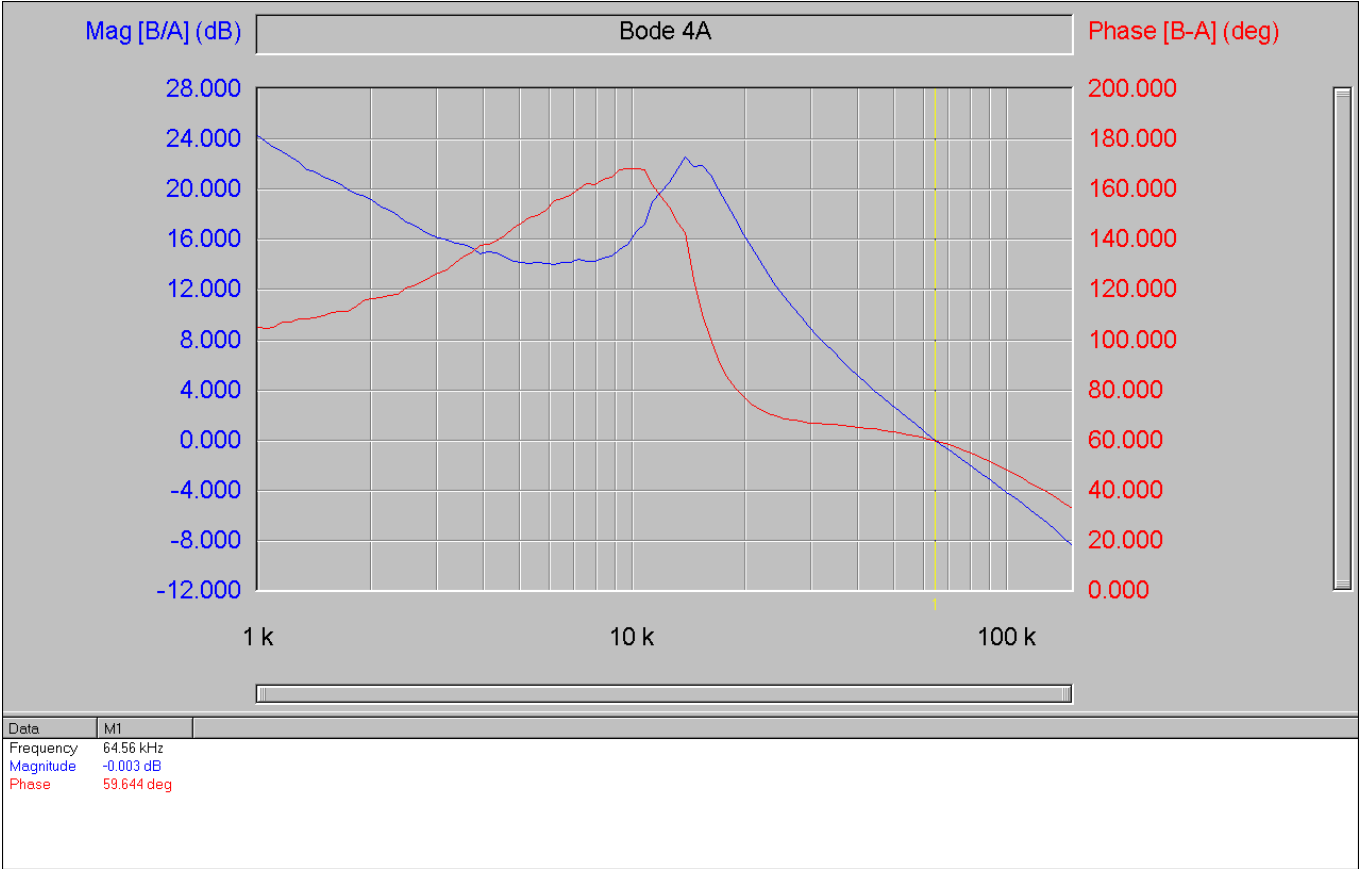


Fig.16: Bode Plot at 4A load (sourcing current) shows a bandwidth of 65kHz and phase margin of 60 degrees

**TYPICAL OPERATING WAVEFORMS**

**Vin=12V, Vo=0.75V, Io=0- +4A, Room Temperature, No Air Flow**

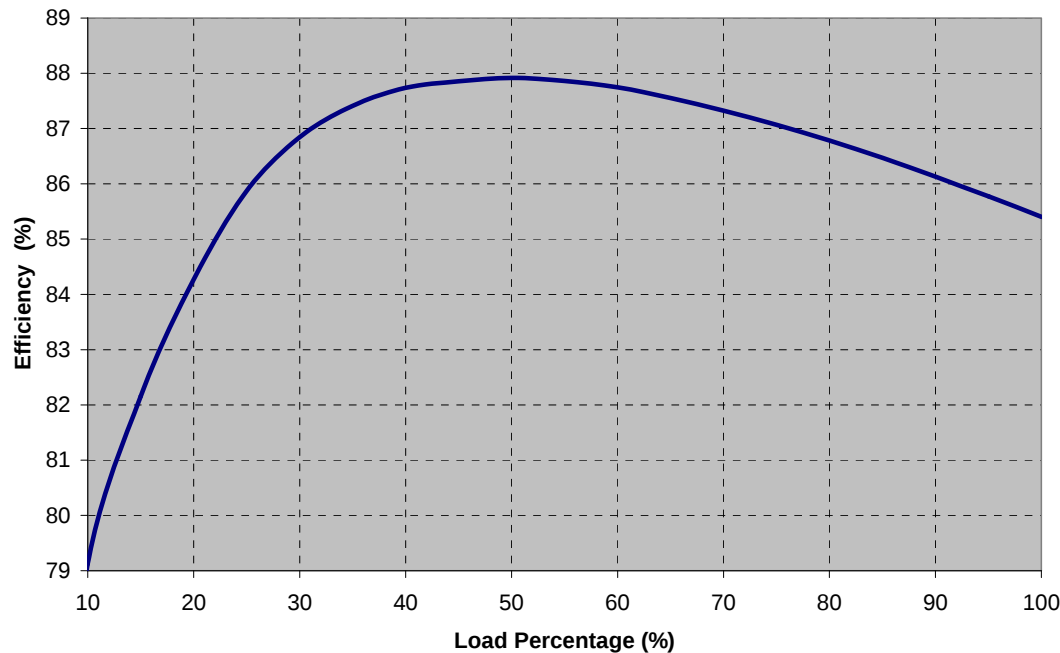


Fig.17: Efficiency versus load current

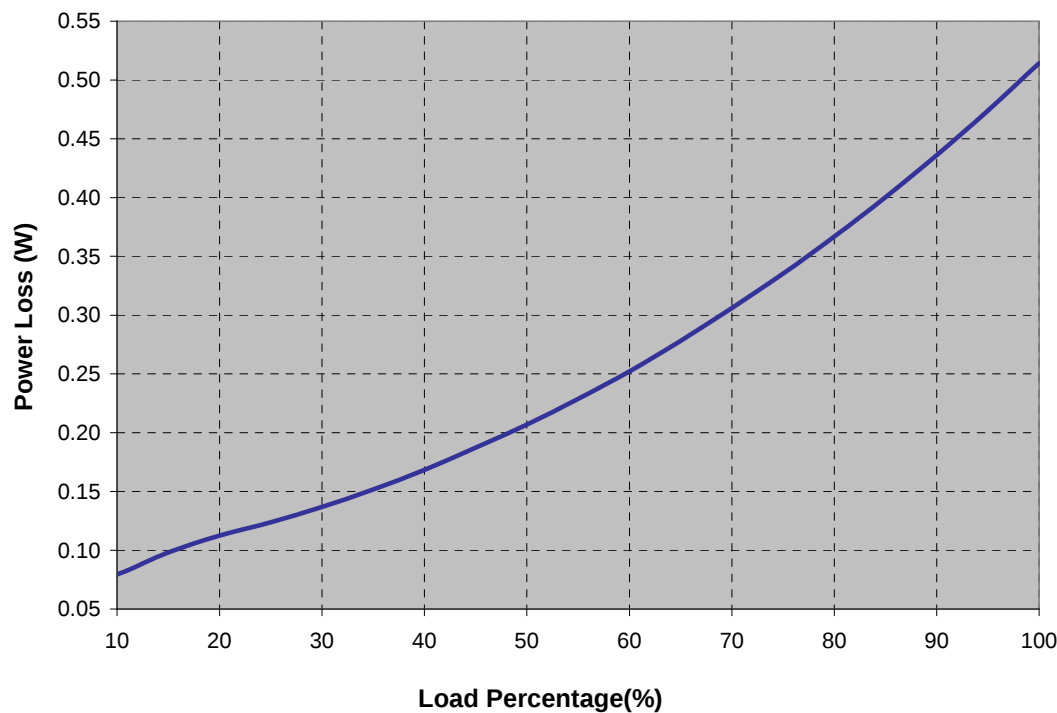


Fig.18: Power loss versus load current

THERMAL IMAGES

Vin=12V, Vo=0.75V, Io=+4A, Room Temperature, No Air Flow

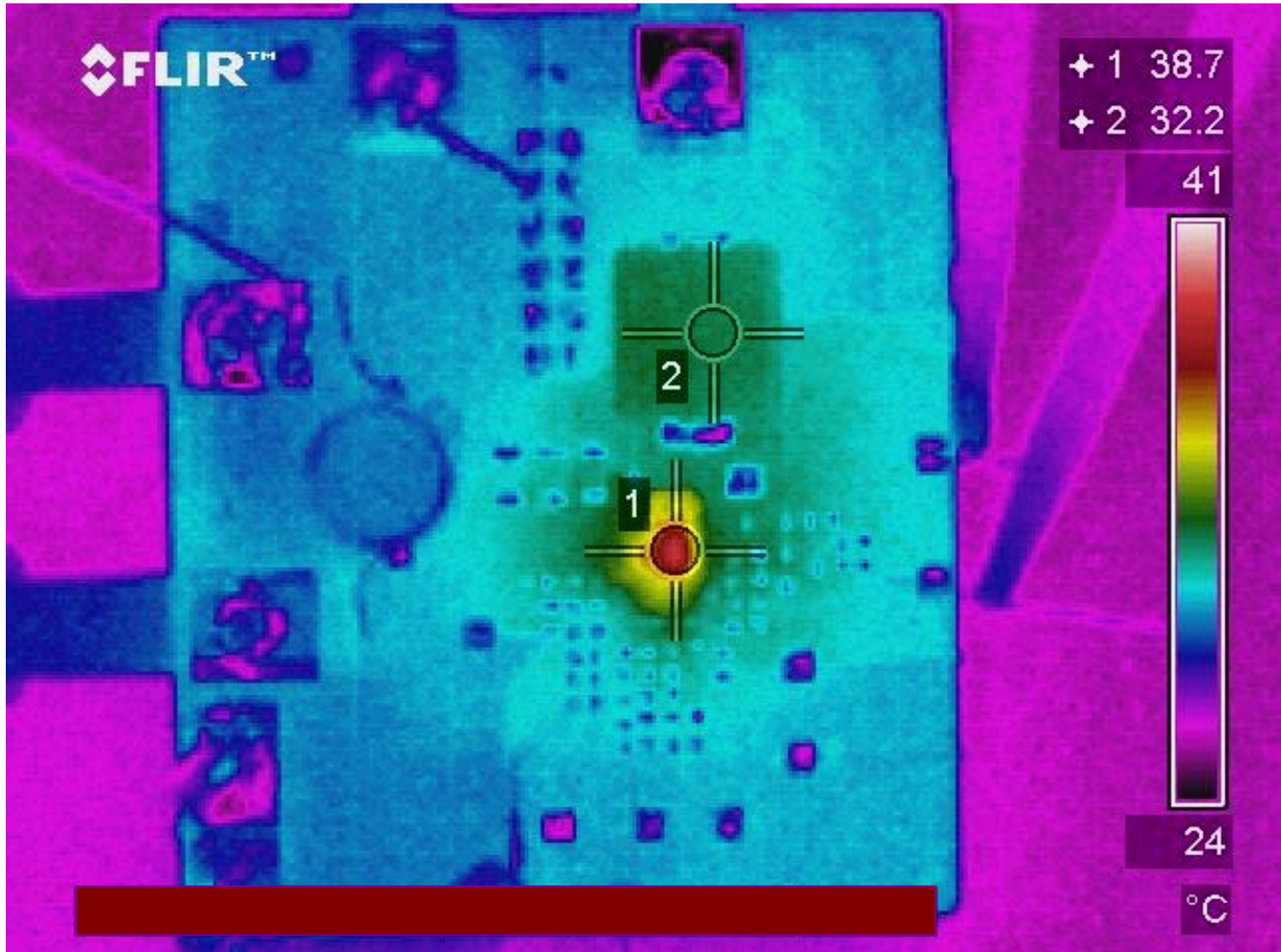


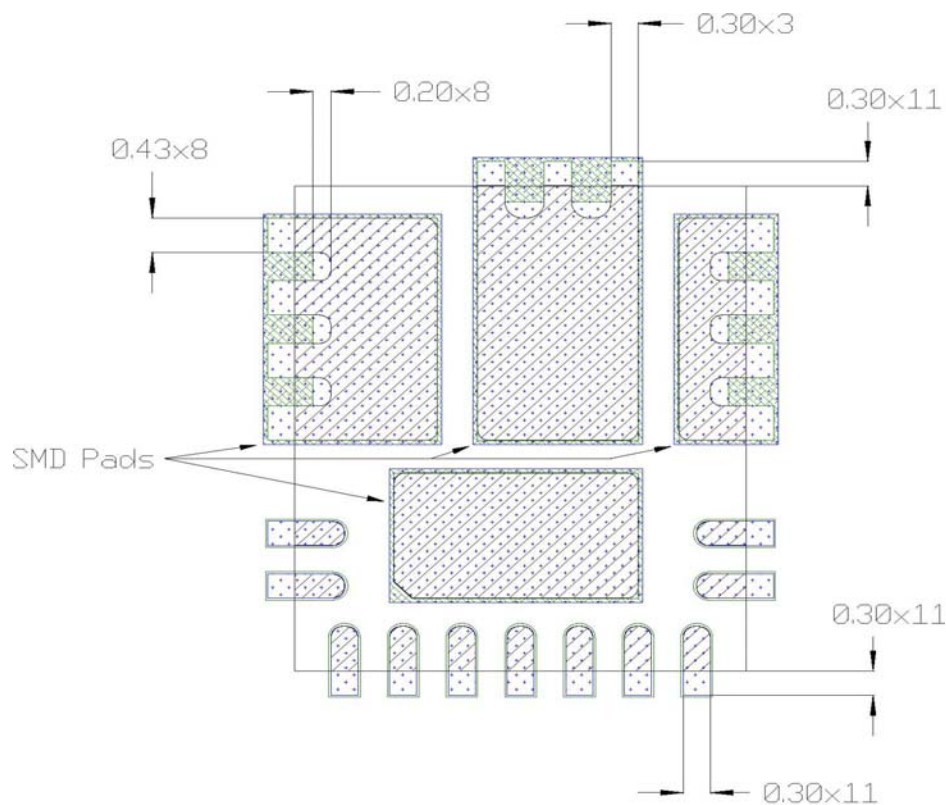
Fig.19: Thermal Image at 4A load  
Test Point 1: IR3832W, Test Point 2: Inductor

## PCB Metal and Components Placement

The lead lands (the 11 IC pins) width should be equal to the nominal part lead width. The minimum lead to lead spacing should be  $\geq 0.2\text{mm}$  to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

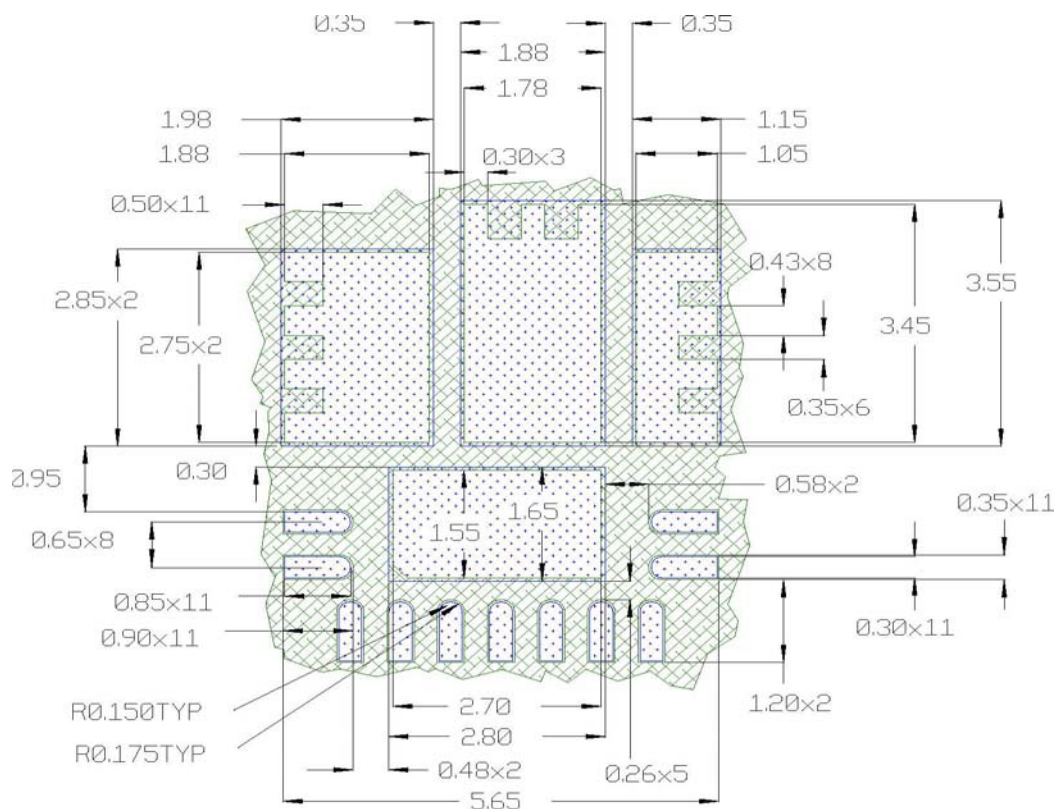


## Solder Resist

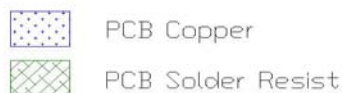
It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is  $\geq 0.15\text{mm}$  due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

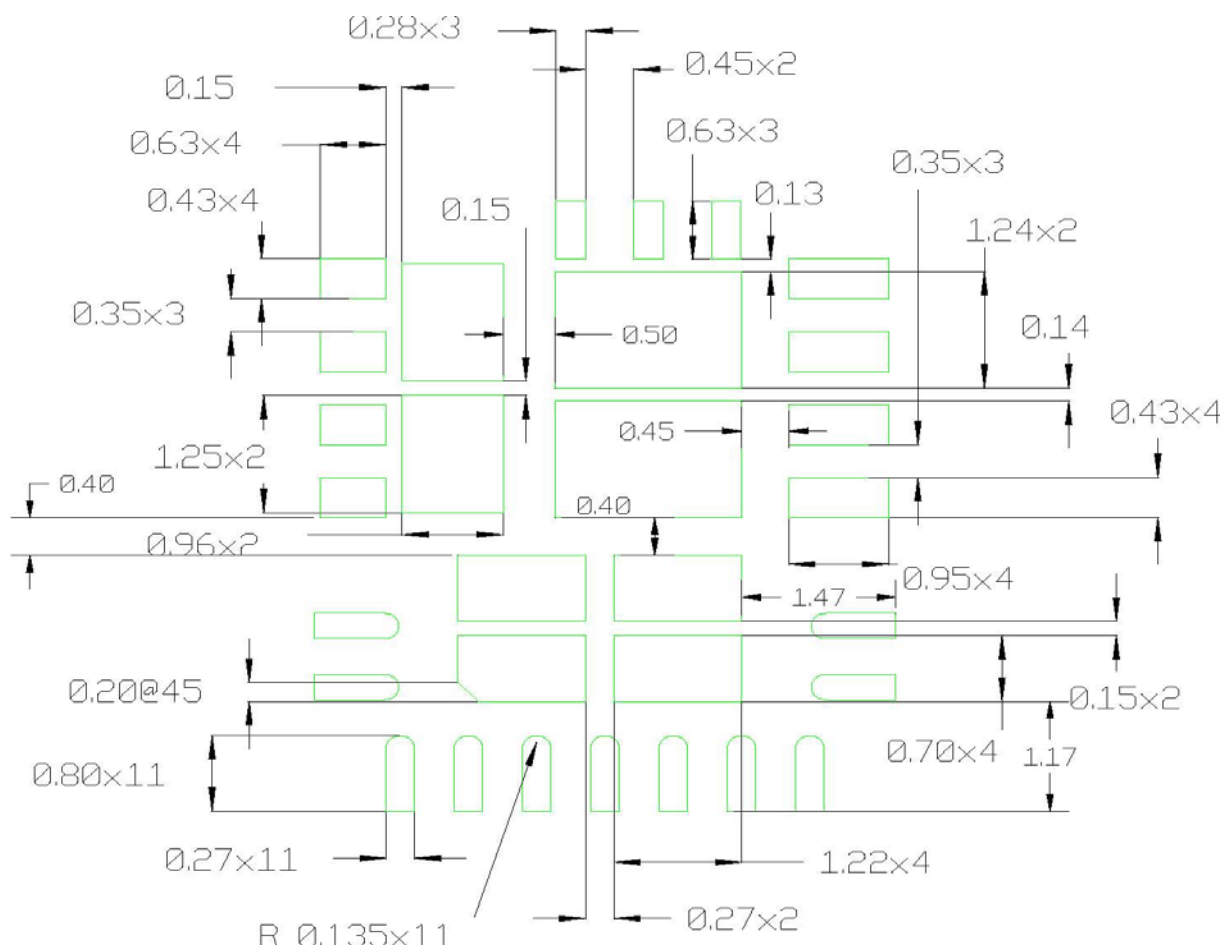


All Dimensions in mm

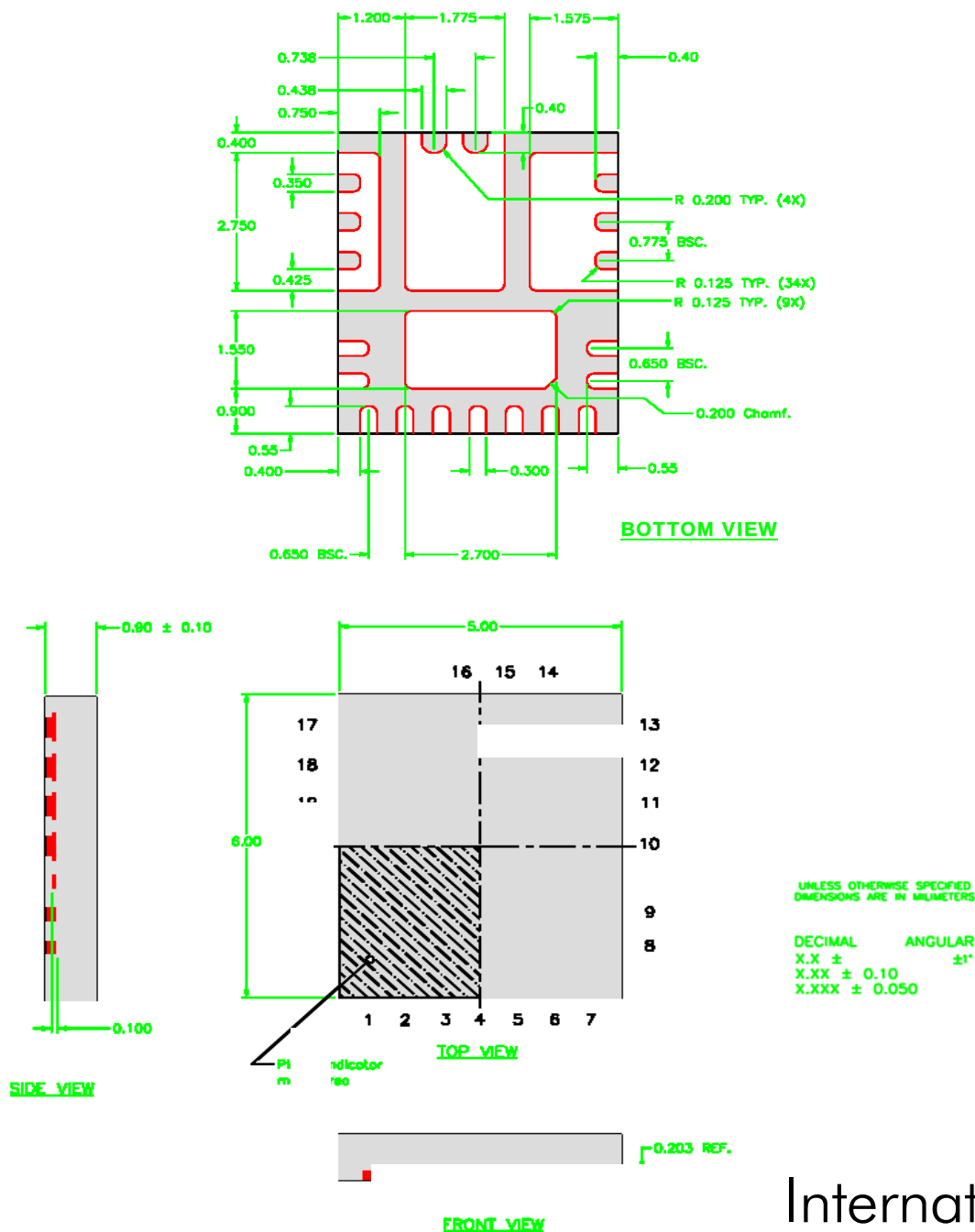


## Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture  
All Dimensions in mm



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