

# **IRAUDAMP7D**

# 25W-500W Scalable Output Power Class D Audio Power Amplifier Reference Design Using the IRS2092 Protected Digital Audio Driver

Ву

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#### **CAUTION:**

International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP7D Demo Board:

- Always wear safety glasses whenever operating Demo Board
- Avoid personal contact with exposed metal surfaces when operating Demo Board
- Turn off Demo Board when placing or removing measurement probes





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#### Introduction

The IRAUDAMP7D reference design is a two-channel Class D audio power amplifier that features output power scalability. The IRAUDAMP7D offers selectable half-bridge (stereo) and full-bridge (bridged) modes.

This reference design demonstrates how to use the IRS2092 Class D audio driver IC, along with IR's digital audio dual MOSFETs, such as IRFI4024H-117P, IRFI4019H-117P, IRFI4212H-117P and IRFI4020H-117P, on a single layer PCB. The design shows how to implement peripheral circuits on an optimum PCB layout using a single sided board.

The resulting design requires a small heatsink for normal operation (one-eighth of continuous rated power). The reference design provides all the required housekeeping power supplies and protections.

#### Unless otherwise noted, this user's manual is based on 150V model, IRAUDAMP7D-150,.

Other output power versions can be configured by replacing components given in the component selection of Table 5 on page 36

#### **Applications**

- AV receivers
- Home theater systems
- Mini component stereos
- Powered speakers
- Sub-woofers
- Musical Instrument amplifiers
- Automotive after market amplifiers

#### **Features**

Output Power: Scalable output power from 25W- 500W (see Table 1)

Residual Noise: 200 µV, IHF-A weighted, AES-17 filter

Distortion: 0.05 % THD+N @ 60W, 4  $\Omega$  Efficiency: 90 % @ 500W, 8  $\Omega$ , Class D stage

Multiple Protection Features: Over-current protection (OCP), high side and low side MOSFET

Over-voltage protection (OVP),

Under-voltage protection (UVP), high side and low side MOSFET

DC-protection (DCP),

Over-temperature protection (OTP)

PWM topology: Self-oscillating PWM, half-bridge or full-bridge topologies selectable



**Table 1** IRAUDAMP7D Specification Table Series

		Model Name			
Item		AMP7D-55	AMP7D-100	AMP7D-150	AMP7D-200
IR Power MOSFET	FET1A, FET1B	IRFI4024H-117P	IRFI4212H-117P	IRFI4019H-117P	IRFI4020H-117P
Half Bridge	8 Ω	25W x 2	60W x 2	125W x 2	250W x 2
Trail Bridge	4 Ω	50W x 2	120W x 2	250W x 2	Not Supported
Full Bridge	8 Ω	100W x 1	240W x 1	500W x 1	Not Supported
Nominal Supply Voltage	+B, -B	±25V	±35V	±50V	±70V
Min/Max Supply Voltage	+B, -B	±20V ~ ±28V	±28V ~ ±45V	±45V ~ ±60V	±60V ~ ±80V
Voltage Gain	Gv	20	30	36	40

#### Notes:

- All the power ratings are at clipping power (THD+N = 1 %). To estimate power ratings at THD+N=10%, multiply them by 1.33
- See Table 5 on page 36 for the complete listing of components table.

# **Specifications**

#### General Test Conditions for IRAUDAMP7D-150 (unless otherwise noted) Notes / Conditions

Power Supply Voltages	± 50V
Load Impedance	4 Ω
Self-Oscillating Frequency	400kHz
Voltage Gain	36

Electrical Data Typical Notes / Conditions

	71	
IR Devices Used IRS209	2, Protected digital audio	driver
IRFI402	24H-117P, IRFI4019H-1	17P, IRFI4212H-117P, IRFI4020H-
117P D	igital audio MOSFETs	
PWM Modulator Self-os	cillating, second order sig	gma-delta modulation, analog input
Power Supply Range	± 45V to ± 60V	Or see table 1 above
Output Power CH1-2: (1 % THD+N)	300W	1kHz
Output Power CH1-2: (10 % THD+N)	400W	1kHz
Rated Load Impedance	8 - 4 Ω	Resistive load
Standby Supply Current	+50 mA/-80 mA	No input signal
Total Idle Power Consumption	7W	No input signal
Channel Efficiency	90 %	Single-channel driven, 120W



### **Audio Performance**

	Before Demodulator	Class D Output	Notes / Conditions
THD+N, 1W	0.09 %	0.1 %	
THD+N, 10W	0.03 %	0.04 %	1kHz, Single-channel driven
THD+N, 60W	0.03 %	0.05 %	
THD+N, 100W	0.08 %	0.10 %	
Dynamic Range	100 dB	100 dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise	200 μV	200 μV	22 Hz – 20kHz, AES17 filter Self-oscillating frequency 400kHz
Damping Factor	2000	170	1kHz, relative to 4 Ω load
	95 dB	90 dB	100Hz
Channel Separation	85 dB	80 dB	1kHz
	75 dB	65 dB	10kHz
Frequency Response : 20 Hz- 20kHz	20 Hz-35kHz	±3 dB	1W, 4 Ω – 8 Ω Load

# Thermal Performance (T<sub>A</sub>=25 °C)

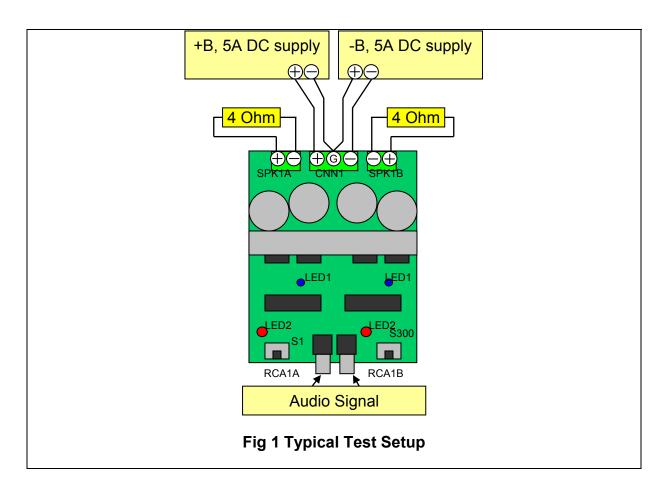
Condition	Typical	Notes / Conditions
Idling	T <sub>C</sub> =30 °C T <sub>PCB</sub> =37 °C	No signal input
2 ch x 15W (1/8 rated power)	T <sub>C</sub> =54 °C T <sub>PCB</sub> =67 °C	
2 ch x 120W (Rated power)	T <sub>C</sub> =80 °C T <sub>PCB</sub> =106 °C	OTP shutdown after 150 s

## **Physical Specifications**

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Dimensions	6"(L) x 4"(W) x 1.25"(H)
	150 mm (L) x 100 mm (W) x 35 mm(H)
Weight	0.330kgm

# **Test Setup**





# **Connector Description**

CH1 IN	RCA1A	Analog input for CH1
CH2 IN	RCA1B	Analog input for CH2
SUPPLY	CNN1	Positive and negative supply (+B / -B)
CH1 OUT	SPK1A	Output for CH1
CH2 OUT	SPK1B	Output for CH2

# **Switches Descriptions**

S1	Shutdown PWM
S300	Half bridge / Full bridge select

# **Indicator Description**

LED1A, B	PWM (presence of low side gate signal)
LED2A,B	Protection

### REFERENCE DESIGN



#### **Test Procedures**

### **Test Setup:**

- 1. On the unit under test (UUT), set switch S1 to OFF and S300 to Stereo positions.
- 2. Connect 4  $\Omega$ -200 W dummy loads to output connectors, SPKR1A and SPKR1B, as shown on Fig 1.
- 3. Set up a dual power supply ±50V with 5A current limit
- 4. Turn OFF the dual power supply before connecting to UUT.
- 5. Connect the dual power supply to CNN1, as shown in Fig 1.

#### Power up:

- 6. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time
- 7. The red LEDs (Protections) turn ON immediately and stay on as long as S1 is in OFF position. Blue LEDs stay OFF.
- 8. Quiescent current for the positive and negative supplies must be less than 50mA, while S1 is in OFF position. Under this condition, IRS2092 is in shutdown mode.
- Slide S1 to ON position; after one second delay, the two blue LEDs turn ON and the red LEDs turns off. The two blue LEDs indicate that PWM oscillation is present. This transition delay time is controlled by CSD pin of IRS2092, capacitor CP3
- 10. Under the normal operating condition with no input signal applied, quiescent current for the positive supply must be less than 50 mA; the negative supply current must be less than 100 mA.

# **Switching Frequency Test:**

11. With an oscilloscope, monitor switching waveform at test points VS1 of VS2 and L1B of CH2. Self oscillating frequency must be  $400kHz \pm 25kHz$ .

Note: The self-oscillating switching frequency is pre-calibrated to 400kHz by the value of R11. To change switching frequency, change the resistances of R11A and R11B for CH1 and CH2 respectively.

## **Audio Functionality Tests:**

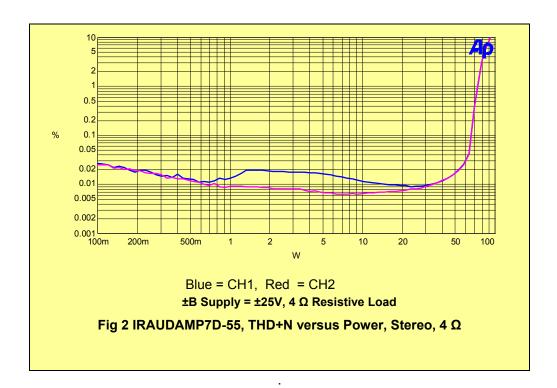
- 12. Set the signal generator to 1kHz, 20 mV<sub>RMS</sub> output.
- 13. Connect audio signal generators to RCA1A and RCA1B.
- 14. Sweep the audio signal voltage from 15 mV<sub>RMS</sub> to 1 V<sub>RMS</sub>.
- 15. Monitor the output signals at SPK1A/B with an oscilloscope. Waveform must be a non distorted sinusoidal signal.
- 16. Observe 1  $V_{RMS}$  input generates output voltage of 36  $V_{RMS}$ . The ratio, R8/(R7+R2), determines the voltage gain of IRAUDAMP7D.
- 17. Set switch S300 to Bridged position.
- 18. Observe that voltage gain doubles.



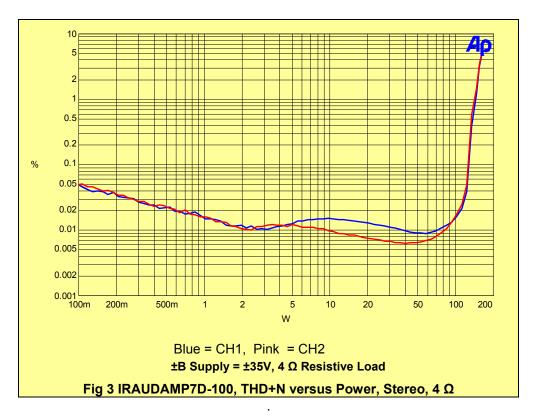
# **Test Setup using Audio Precision (Ap):**

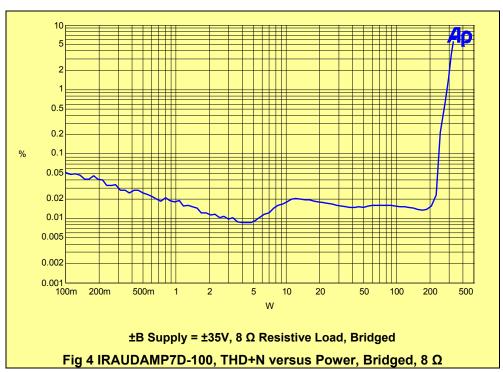
- 19. Use unbalance-floating signal generator outputs.
- 20. Use balanced inputs taken across output terminals, SPKR1A and SPKR1B.
- 21. Connect Ap frame ground to GND in terminal CNN1.
- 22. Place AES-17 filter for all the testing except frequency response.
- 23. Use signal voltage sweep range from 15 mV<sub>RMS</sub> to 1  $V_{RMS}$ .
- 24. Run Ap test programs for all subsequent tests as shown in Fig 2- Fig 13 below.

### **Test Results**

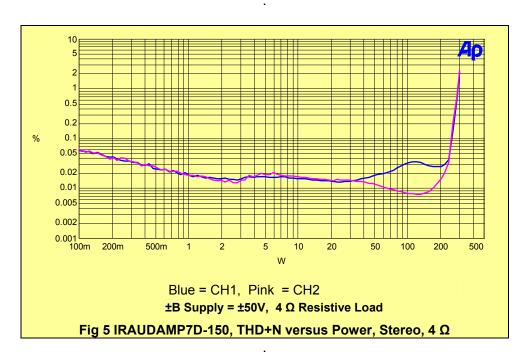


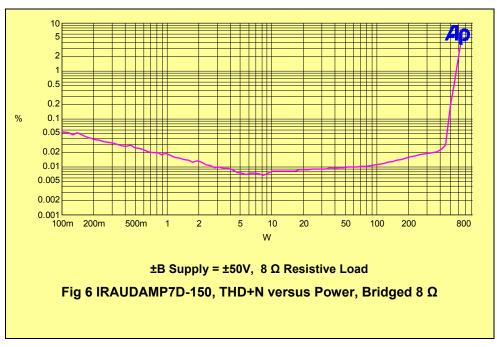




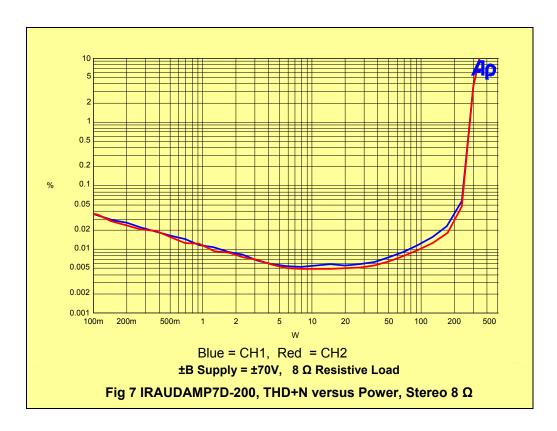


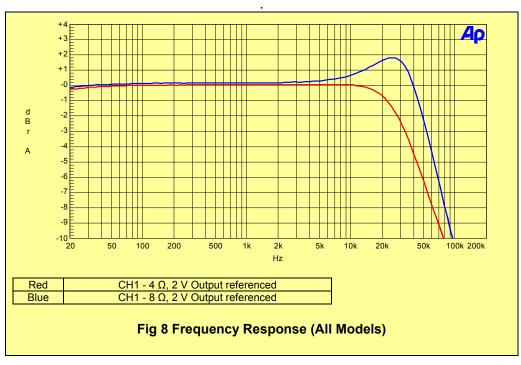




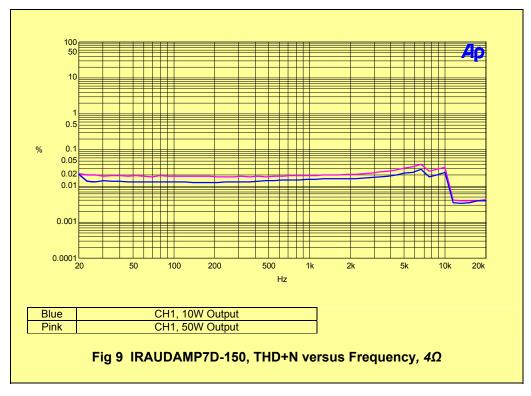


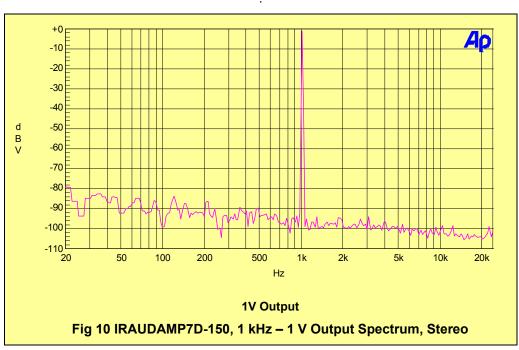




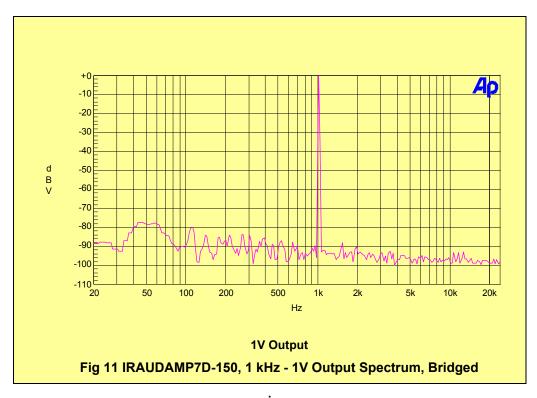


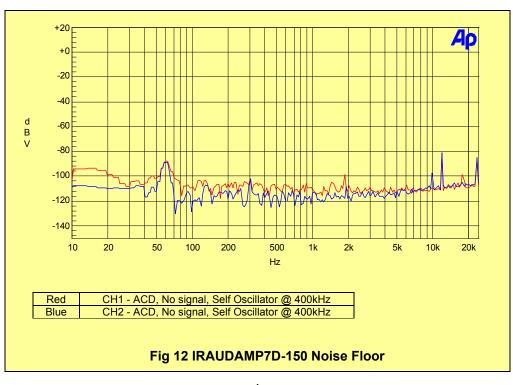




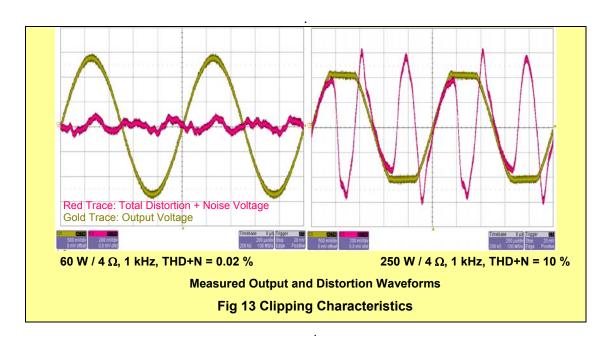








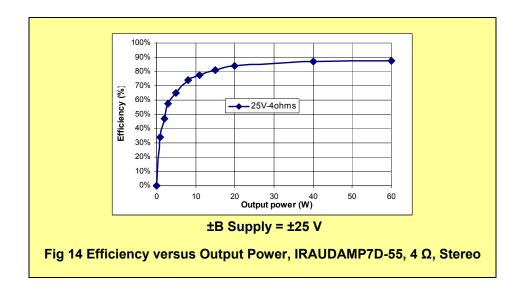




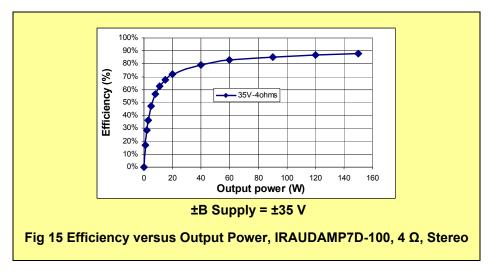
# **Efficiency**

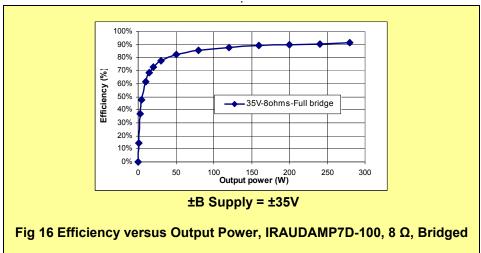
Figs 14-19 show efficiency characteristics of the IRAUDAMP7D. The high efficiency is achieved by following major factors:

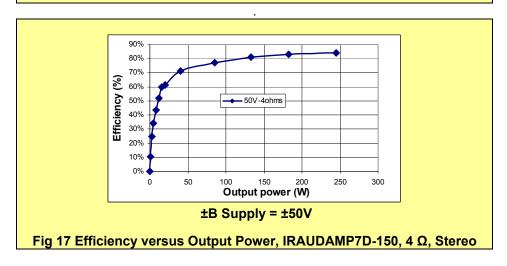
- 1) Low conduction loss due to the dual FETs offering low R<sub>DS(ON)</sub>
- 2) Low switching loss due to the dual FETs offering low input capacitance for fast rise and fall times
- 3) Secure dead-time provided by the IRS2092, avoiding cross-conduction



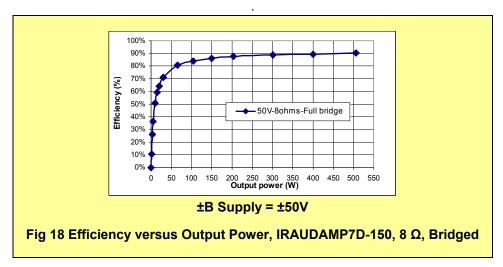


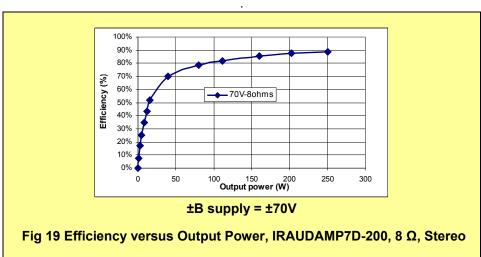












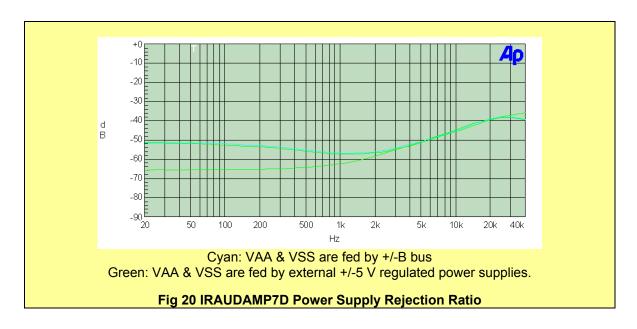
#### **Thermal Considerations**

With this high efficiency, the IRAUDAMP7D design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards, without additional heatsink or forced air-cooling.

#### **Power Supply Rejection Ratio (PSRR)**

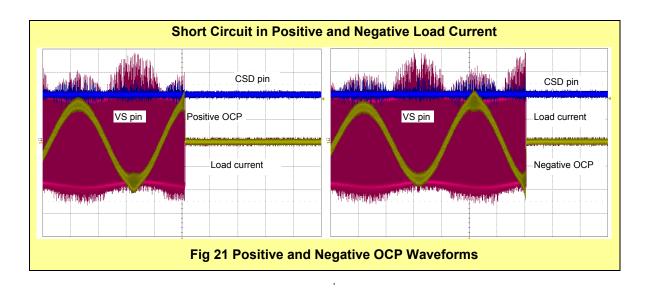
The IRAUDAMP7D obtains good power supply rejection ratio of -65 dB at 1kHz shown in Fig 20. With this high PSRR, IRAUDAMP7D accepts any power supply topology as far as the supply voltages fit in the min and max range.



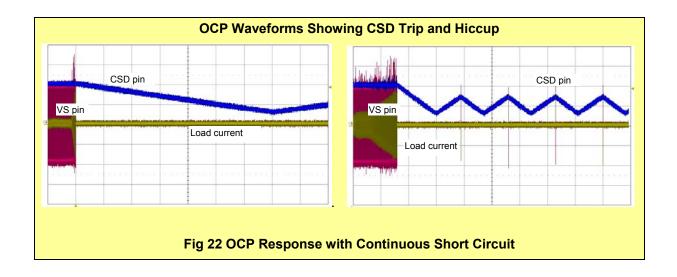


## **Short Circuit Protection Response**

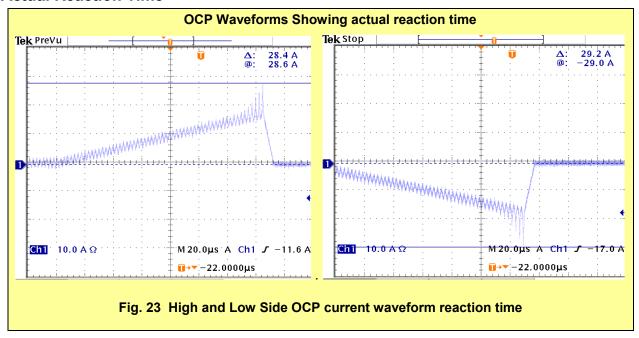
Figs 21-23 show over current protection reaction time of the IRAUDAMP7D in a short circuit event. As soon as the IRS2092 detects over current condition, it shuts down PWM. After one second, the IRS2092 tries to resume the PWM. If the short circuit persists, the IRS2092 repeats try and fail sequences until the short circuit is removed.







#### **Actual Reaction Time**



#### **IRAUDAMP7D Overview**

The IRAUDAMP7D features a self-oscillating type PWM modulator for the lowest component count, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The





benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP7D self-oscillating topology consists of following essential functional blocks.

- Front-end integrator
- PWM comparator
- Level shifters
- Gate drivers and MOSFETs
- Output LPF

### Integrator

Referring to Fig 24 below, the input operational amplifier of the IRS2092 forms a front-end secondorder integrator with R7, C4, C6, and R11. The integrator that receives a rectangular feedback signal from the PWM output via R8 and audio input signal via R7 generates quadratic carrier signal in COMP pin. The analog input signal shifts the average value of the quadratic waveform such that the duty cycle varies according to the instantaneous voltage of the analog input signal.

## **PWM Comparator**

The carrier signal in COMP pin is converted to PWM signal by an internal comparator that has threshold at middle point between VAA and VSS. The comparator has no hysteresis in its input threshold.

#### **Level Shifters**

The internal input level-shifter transfers the PWM signal down to the low-side gate driver section. The gate driver section has another level-shifter that level shifts up the high-side gate signal to the high-side gate driver section.

#### **Gate Drivers and MOSFETs**

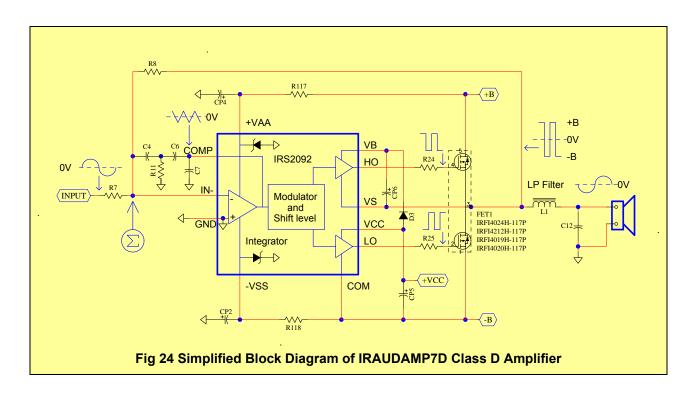
The received PWM signal is sent to the dead-time generation block where a programmable amount of dead time is added into the PWM signal between the two gate output signals of LO and HO to prevent potential cross conduction across the output power MOSFETs. The high-side level-shifter shifts up the high-side gate drive signal out of the dead-time block.

The IRS2092 drives two MOSFETs, high- and low-sides, in the power stage providing the amplified PWM waveform.

#### **Output LPF**



The amplified PWM output is reconstructed back to analog signal by the output LC LPF. Demodulation LC low-pass filter (LPF) formed by L1 and C12, filters out the Class D switching carrier signal leaving the audio output at the speaker load. A single stage output filter can be used with switching frequencies of 400 kHz and greater; a design with a lower switching frequency may require an additional stage of LPF.



# **Functional Descriptions**

#### **IRS2092 Gate Driver IC**

The IRAUDAMP7D uses IRS2092, a high-voltage (up to 200 V), high-speed power MOSFET driver with internal dead-time and protection functions specifically designed for Class D audio amplifier applications. These functions include OCP and UVP. The IRS2092 integrates bi-directional over current protection for both high-side and low-side MOSFETs. The dead-time can be selected for optimized performance according to the size of the MOSFET, minimizing dead-time while preventing shoot-through. As a result, there is no gate-timing adjustment required externally. Selectable dead-time through the DT pin voltage is an easy and reliable function which requires only two external resistors, R26 and R27 as shown on Fig 25 below.

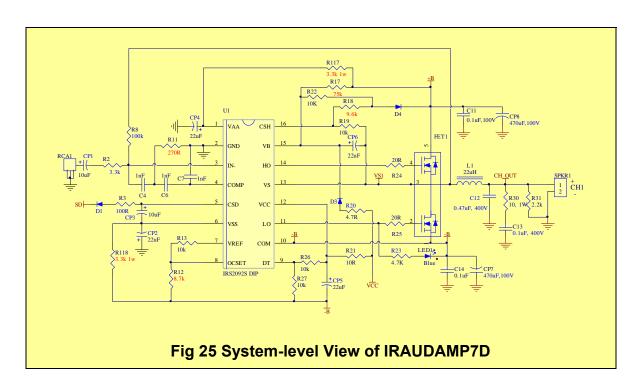
The IRS2092 offers the following functions.

PWM modulator



- Dead-time insertion
- Over current protection
- Under voltage protection
- Level shifters

Refer to IRS2092 datasheet and AN-1138 for more details.



### **Self-Oscillating Frequency**

Self-oscillating frequency is determined by the total delay time along the control loop of the system; the propagation delay of the IRS2092, the MOSFETs switching speed, the time-constant of front-end integrator (R7, R8, R11, C4, C6, C7). Variations in +B and -B supply voltages also affect the self-oscillating frequency.

The self-oscillating frequency changes with the duty ratio. The frequency is highest at idling. It drops as duty cycle varies away from 50%.

### Adjustments of Self-Oscillating Frequency

Use R11 to set different self-oscillating frequencies. The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute

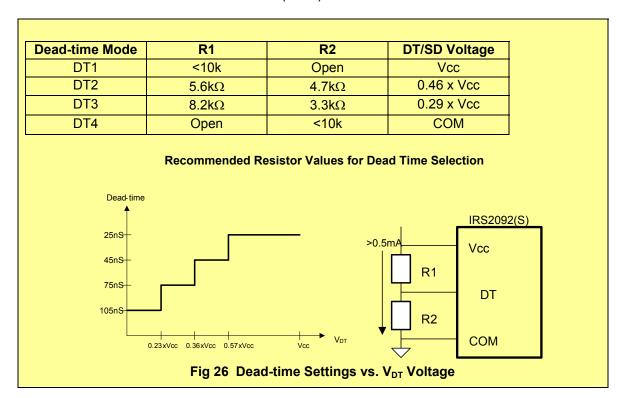


frequency and frequency relative to the other channels. In the absolute terms, at higher frequencies distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range.

Normally, when adjusting the self-oscillating frequency of the different channels, it is suggested to either match the frequencies accurately, or have them separated by at least 25kHz. Under the normal operating condition with no audio input signal, the switching-frequency is set around 400kHz in the IRAUDAMP7D.

#### Selectable Dead-time

The dead-time of the IRS2092 is set based on the voltage applied to the DT pin. Fig 26 lists the suggested component value for each programmable dead-time between 25 and 105 ns. All the IRAUDAMP7D models use DT2 (45ns) dead-time.



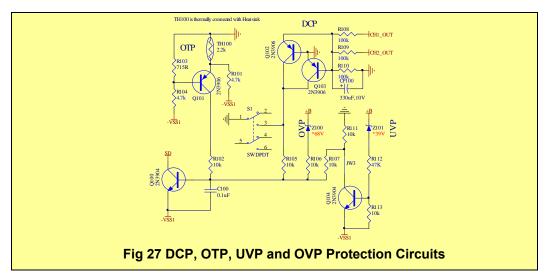
# **Protection System Overview**

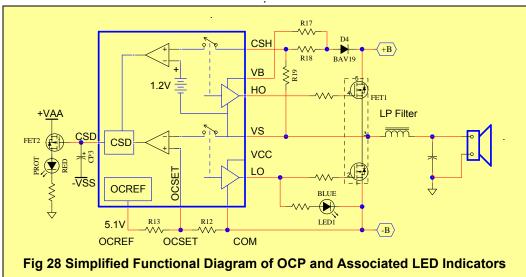
The IRS2092 integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), speaker DC offset



protection (DCP) and over temperature protection (OTP), are realized externally to the IRS2092 (Fig 27).

In the event that any of these external fault conditions are detected, the external shutdown circuit will disable the output by pulling down CSD pins, turning on red LEDs, and turning off blue LEDs (Fig 28). If the fault condition persists, the protection circuit stays in shutdown until the fault is removed. Once the fault is cleared, the blue LEDs turn on and red LEDs turn off.







# **Over-Current Protection (OCP)** Low-Side Current Sensing

The low-side current sensing feature protects the low side MOSFET from an overload condition in negative load current by measuring drain-to-source voltage across R<sub>DS(ON)</sub> during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage during low-side conduction gets higher than the OCSET voltage, the IRS2092 turns off outputs and pulls CSD down to -VSS.

### **High-Side Current Sensing**

The high-side current sensing protects the high side MOSFET from an overload condition in positive load current by measuring drain-to-source voltage across R<sub>DS(ON)</sub> during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side MOSFET while it is in the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider R19, R18 and R17 are used to program a threshold as shown in Fig 26. An external reverse blocking diode D4 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D4, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.

Table 2 Actual OCP table setting thresholds

Function	Device	Amp7-55	Amp7-100	Amp7-150	Amp7-200
OCSET	R12A R12B	1.3K	3.9K	7.5K	5.2K
Tested OCP curr	ent 25°C		23A	30A	23A
CSH	R18A R18B	0.0	4.7K	9.6K	8.2K
Tested OCP current 25°C			23A	29A	23A
Peak load current at rated power		6.0A	8.7A	12.2A	8.9A

### Over-Voltage Protection (OVP)

OVP is provided externally to the IRS2092. OVP shuts down the amplifier if the bus voltage between GND and +B exceeds 75V. The threshold is determined by a Zener diode Z100. OVP





protects the board from harmful excessive supply voltages, such as due to bus pumping at very low frequency continuous output in stereo mode.

### **Under-Voltage Protection (UVP)**

UVP is provided externally to the IRS2092. UVP prevents unwanted audible noise output from unstable PWM operation during power up and down. UVP shuts down the amplifier if the bus voltage between GND and +B falls below a voltage set by Zener diode Z101.

### **Speaker DC-Voltage Protection (DCP)**

DCP protects speakers against DC output current feeding to its voice coil. DC offset detection detects abnormal DC offset and shuts down PWM. If this abnormal condition is caused by a MOSFET failure because one of the high-side or low-side MOSFETs short circuited and remained in the on state, the power supply needs to be cut off in order to protect the speakers. Output DC offset greater than ±4V triggers DCP.

### Offset Null (DC Offset) Adjustment

The IRAUDAMP7D requires no output-offset adjustment. DC offsets are tested to be less than ±20 mV.

#### **Over-Temperature Protection (OTP)**

A NTC resistor, TH100 in Fig 25, is placed in close proximity to two dual MOSFETs on a heatsink to monitor heatsink temperature. If the heatsink temperature rises above 100 °C, the OTP shuts down both channels by pulling down CSD pins of the IRS2092. OTP recovers once the temperature has cooled down.

### **ON-OFF Switch**

OFF position of S1 forces the IRAUDAMP7D to stay in shutdown mode by pulling down the CSD pin. During the shutdown mode the output MOSFETs are kept off.

#### **Click and POP Noise Reduction**

Thanks to the click and pop elimination function built into the IRS2092, IRAUDAMP7D does not use any additional components for this function.





# **Power Supply Requirements**

For convenience, the IRAUDAMP7D has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies. Power supply voltage depends on the model and is shown in the power selection in Table 1.

# **House Keeping Power Supply**

The internally-generated housekeeping power supplies include  $\pm 5.6 V$  for analog signal processing, and  $\pm 12 V$  supply ( $V_{CC}$ ) referred to negative supply rail -B for MOSFET gate drive. The VAA and VSS supplying floating input section are fed from +B and -B power stage bus supplies via R117 and R118, respectively. Gate driver section of IRS2092 uses VCC to drive gates of MOSFETs. The  $V_{CC}$  is referenced to -B (negative power supply). D3 and CP6 form a bootstrap floating supply for the HO gate driver.

### **Bus Pumping**

When the IRAUDAMP7D is running in the stereo mode, bus pumping effect takes place with low frequency high output. Since the energy flowing in the Class D switching stage is bi-directional, there is a period where the Class D amplifier feeds energy back to the power supply. The majority of the energy flowing back to the supply is from the energy stored in the inductor in the output LPF. Usually, the power supply has no way to absorb the energy coming back from the load. Consequently the bus voltage is pumped up, creating bus voltage fluctuations.

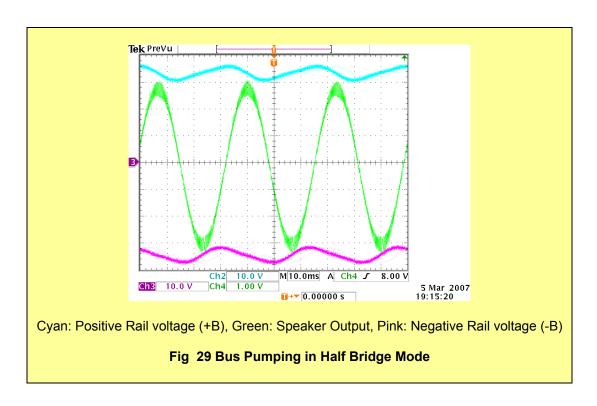
Following conditions make bus pumping worse:

- 1. Lower output frequencies (bus-pumping duration is longer per half cycle)
- 2. Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
- 3. Smaller bus capacitance (the same energy will cause a larger voltage increase)

The OVP protects IRAUDAMP7D from failure in case of excessive bus pumping. One of the easiest counter measures of bus pumping is to drive both of the channels in a stereo configuration out-of-phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection monitors only +B supply, assuming the bus pumping on the supplies is symmetric in +B and -B supplies.

There is no bus pumping effect in full bridge mode.



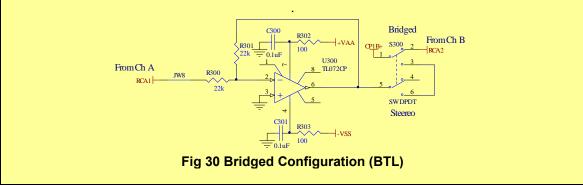


# **Bridged Configuration**

By selecting S300 to Bridged position, the IRAUDAMP7D realizes full bridge mode, also known as bridge-tied-load, or BTL configuration. Full bridge operation is achieved by feeding out-of-phase audio input signals to the two input channels as shown in the Fig 30 below.

In bridged mode, IRAUDAMP7D receives audio input signal from channel A only. The on-board inverter feed out-of-phase signal to Channel B. The speaker output must be connected between (+) of Channel A and (+) of Channel B in bridged mode.

In bridged mode, nominal load impedance is 8  $\Omega$ . (See power table in Table 1)





### **Load Impedance**

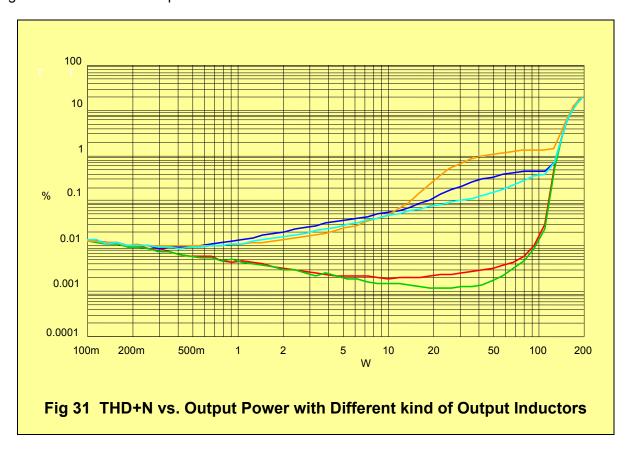
Each channel is optimized for a 4  $\Omega$  speaker load in half bridge and 8  $\Omega$  load in full bridge.

### **Output Filter Selection**

Since the output filter is not included in the control loop of the IRAUDAMP7D, the control loop has no ability to compensate performance deterioration caused by the output filter. Therefore, it is necessary to understand what characteristics are preferable when designing the output filter.

- 1) The DC resistance of the inductor should be minimized to 20 m $\Omega$  or less.
- The linearity of the output inductor and capacitor should be high with output current and voltage.

Fig 31 demonstrates THD performance difference with various inductors.

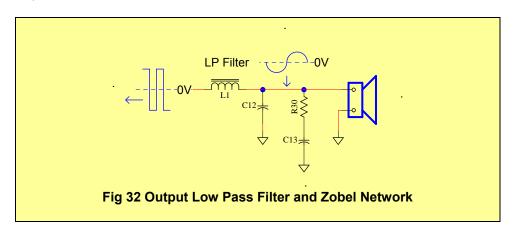




### Input Signal and Gain Setting

A proper input signal is an analog signal ranging from 20Hz to 20kHz with up to 3  $V_{\text{RMS}}$  amplitude with a source impedance of no more than 600  $\Omega.$  Input signal with frequencies from 30kHz to 60kHz may cause LC resonance in the output LPF, causing a large reactive current flowing through the switching stage, especially with greater than 8  $\Omega$  load impedances, and the LC resonance can activate OCP.

The IRAUDAMP7D has an RC network called Zobel network (R30 and C13) to damp the resonance and prevent peaking frequency response with light loading impedance. (Fig 32) The Zobel network is not thermally rated to handle continuous supersonic frequencies above 20kHz. These supersonic input frequencies can be filtered out by adding R2 and C2 as shown on main schematic Fig 33 and Fig 34. This RC filter works also as an input RF filter to prevent potential radio frequency interferences.

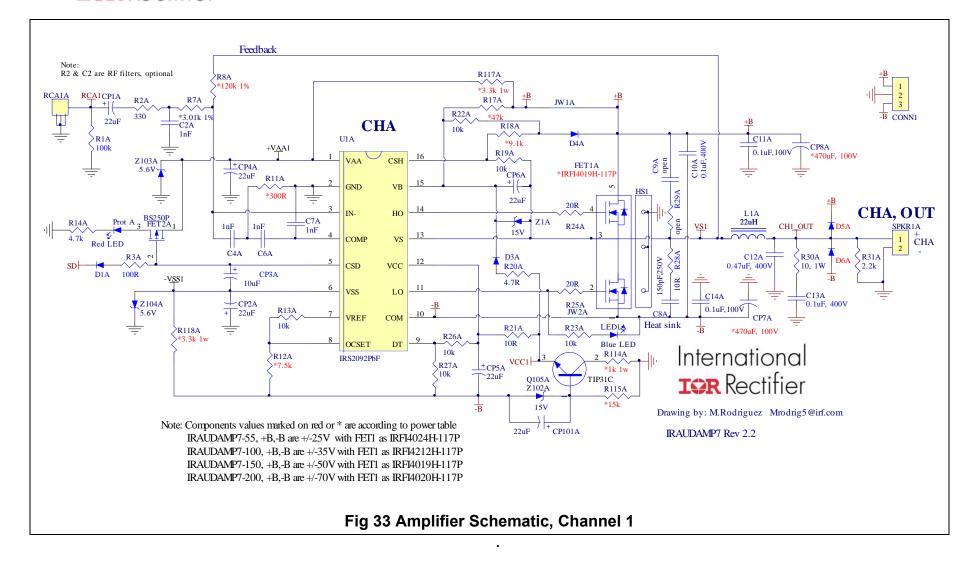


## **Gain Setting**

The ratio of resistors R8/R2 in Fig 23 sets voltage gain. The IRAUDAMP7D has no on board volume control. To change the voltage gain, change the input resistor term R2. Changing R8 affects PWM control loop design and may result poor audio performance.

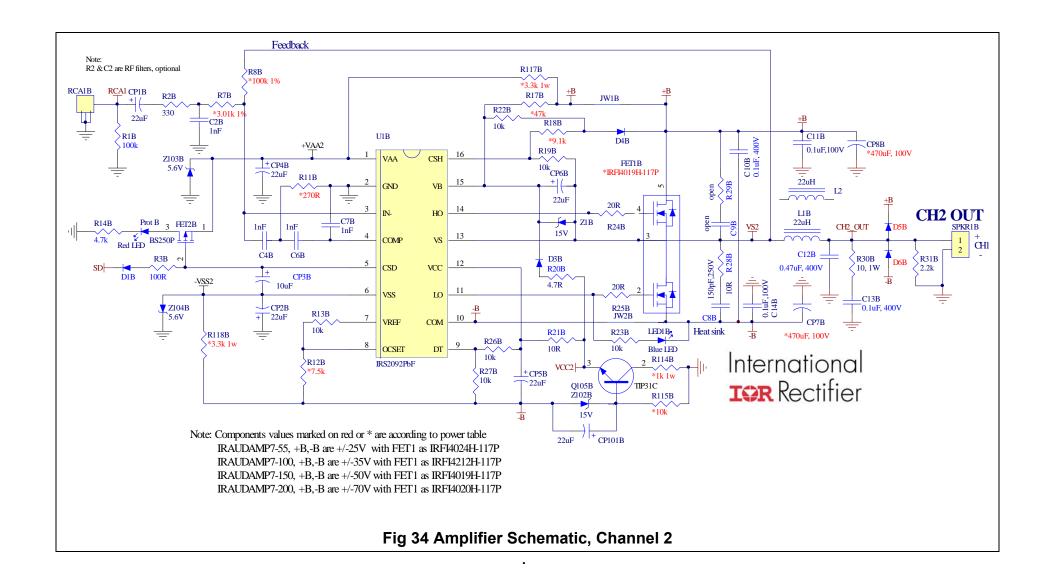


# REFERENCE DESIGN



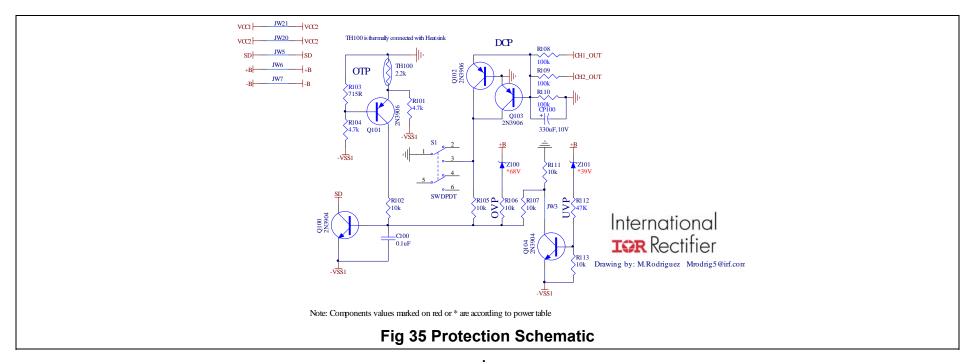
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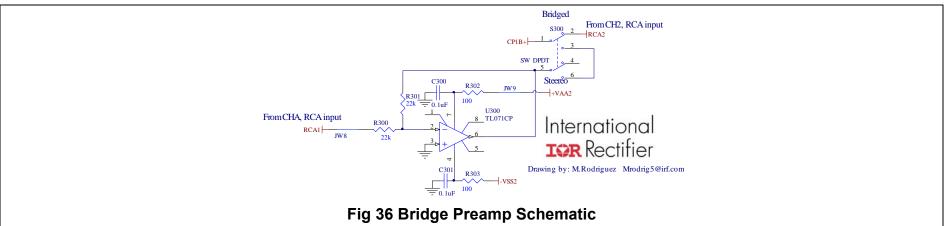




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# REFERENCE DESIGN







# **IRAUDAMP7D-150 Fabrication Materials**

# Table 3 IRAUDAMP7D-150 Electrical Bill of Materials

Quantit V	Value	Description	Designator	Digikey P/N	Vendor
8	1nF, 50V	CAP 1nF 50V POLYESTER 5%	C2A, C2B, C4A, C4B, C6A, C6B, C7A, C7B	P4551-ND	Panasonic - ECG
2	150 pF, 250V CERAMIC CAP 150PF 250 VAC CERAMIC 10 %		C8A, C8B	P11413TB-ND	Panasonic - ECG
2	Open	CERAMIC CAP 150PF 250 VAC CERAMIC 10%	C9A, C9B	P11413TB-ND	Panasonic - ECG
4	0.1uF, 400V	CAP .10UF 400V METAL POLYPROPYLANE	C10A, C10B, C13A, C13B	495-1311-ND	EPCOS Inc
4	0.1uF 100V	CAP .10UF 100V METAL POLYESTER	C11A, C11B, C14A, C14B	495-1147-ND	EPCOS Inc
2	0.47uF, 400V	CAP .47UF 400V METAL POLYPROPYLANE	C12A, C12B	495-1315-ND	EPCOS Inc
3	0.1uF 100V	CAP .10UF 100V METAL POLYESTER	C100, C300, C301	495-1147-ND	EPCOS Inc
1	ED365/3	TERMINAL BLOCK 7.50MM 3POS PCB	CONN1	ED2355-ND	On Shore Technology
12	22uF	CAP 22UF 25V ELECT VR RADIAL	CP1A, CP1B, CP2A, CP2B, CP4A, CP4B, CP5A, CP5B, CP6A, CP6B, CP101A, CP101B	493-1058-ND	Nichicon
2	10uF, 16V	CAP ELECT 10UF 16V KS RADIAL	CP3A, CP3B	P966-ND	Panasonic - ECG
4	470uF/100V	CAP 470UF 100V ELECT PW RADIAL	CP7A, CP7B, CP8A, CP8B	493-1985-ND	Nichicon
1	330uF, 10V	CAP 330UF 10V ALUM LYTIC RADIAL	CP100	P5125-ND	Panasonic - ECG
2	1N4148T-73	DIODE SWITCH 100V 150MA DO-35	D1A, D1B	1N4148T-73CT-ND	Rohm
4	MUR120RLG	DIODE ULTRA FAST 1A 200V AXIAL DO-41	D3A, D3B, D4A, D4B	MUR120RLGOSCT -ND	ON Semiconducto r
4	1N4003	DIODE GEN PURPOSE 200V 1A DO41	D5A, D5B, D6A, D6B	1N4003FSCT-ND	Fairchild Semiconducto r
2	*IRFI4019H- 117P	IRFI4019H-117P, Dual MOSFET TO-220-5	FET1A, FET1B	IR's Part No.	International Rectifier
2	BS250P	MOSFET P-CH 45V 230MA TO-92	FET2A, FET2B	BS250P-ND	Zetex Inc
1	Heat sink	Aluminum heat spreader	HS1	Drawing IRHS_Amp1	Custom made
4	Wire 0.400"	AXIAL JUMPER RES 0.0 OHM	JW1A, JW1B, JW2A, JW2B	P0.0BACT-ND	Panasonic - ECG
1	Wire 0.300"	AXIAL JUMPER RES 0.0 OHM	JW3	P0.0BACT-ND	Panasonic - ECG
1	Wire 1.640"	Wire Jumper #20 AWG insulated	JW5	Custom	Custom
2	Wire 1.800"	Wire Jumper #20 AWG insulated	JW6, JW7	Custom	Custom
1	Wire 1.240"	Wire Jumper #20 AWG insulated	JW8	Custom	Custom
1	Wire 1.200"	Wire Jumper #20 AWG insulated	JW9	Custom	Custom
2	Wire 0.800"	Wire Jumper #20 AWG insulated	JW20, JW21	Custom	Custom
2	22uH, 13A	Class D Inductor, 22UH	L1A, L1B	Sagami 7G17A-	Sagami



# REFERENCE DESIGN

		13A		220M-R	
2	Blue LED	LED 3MM DUAL	LED1A, LED1B	160-1600-ND	LITE-ON INC
2 Red LED LED 3MM HI-		FLANGE BLUE CLEAR LED 3MM HI-EFF RED TRANSPARENT	Prot A, Prot B	160-1140-ND	LITE-ON INC
2	2N3904-AP	TRANSISTOR NPN GP 40V TO92	Q100, Q104	2N3904-APCT-ND	Micro Commercial Co.
3	2N3906-AP	TRANSISTOR PNP GP 40V TO92	Q101, Q102, Q103	2N3906-APCT-ND	Micro Commercial Co.
2	TIP31C	TRANS NPN EPITAX 100V 3A TO-220	Q105A, Q105B	TIP31CFS-ND	Fairchild Semiconducto r
4	100k	RES 100K OHM CARBON FILM 1/4W 5%	R1A, R1B, R108, R110	P100KBACT-ND	Panasonic - ECG
2	330	AXIAL RES 330 OHM CARBON FILM 1/4W 5%	R2A, R2B	P330BACT-ND	Panasonic - ECG
2	100 Ohms	AXIAL RES 100 OHM CARBON FILM 1/4W 5%	R3A, R3B	P100BACT-ND	Panasonic - ECG
2	3k 1%	AXIAL RES METAL FILM 3.00K OHM 1/4W 1%	R7A, R7B	P3.00KCACT-ND	Panasonic - ECG
2	120k 1%	AXIAL RES METAL FILM 120K OHM 1/4W 1%	R8A, R8B	P120KCACT-ND	Panasonic - ECG
2	300 Ohms	AXIAL RES 300 OHM CARBON FILM 1/4W 5%	R11A, R11B	P300BACT-ND	P300BACT- ND
2	7.5k	AXIAL RES 7.5K OHM CARBON FILM 1/4W 5%	R12A, R12B	P7.5KBACT-ND	Yageo
18	10k	AXIAL RES 10k OHM CARBON FILM 1/4W 5%	R13A, R13B, R19A, R19B, R22A, R22B, R23A, R23B, R26A, R26B, R27A, R27B, R102, R105, R106, R107, R111, R113	P10KBACT-ND	Panasonic - ECG
4	4.7k	AXIAL RES 4.7K OHM CARBON FILM 1/4W 5%	R14A, R14B, R101, R104	P4.7KBACT-ND	Panasonic - ECG
2	47k	AXIAL RES 47K OHM CARBON FILM 1/4W 5%	R17A, R17B	P47KBACT-ND	Panasonic - ECG
2	9.1k	AXIAL RES 9.1K OHM CARBON FILM 1/4W 5%	R18A, R18B	P9.1KBACT-ND	Panasonic - ECG
2	4.7 Ohms	AXIAL RES 4.7 OHM CARBON FILM 1/4W 5%	R20A, R20B	P4.7BACT-ND	Panasonic - ECG
4	10 Ohms	AXIAL RES METAL FILM 10.0 OHM 1/2W 1%	R21A, R21B, R28A, R28B	PPC10.0XCT-ND	Vishay/BC Components
4	20R	AXIAL RES METAL FILM 20.0 OHM 1/2W 1%	R24A, R24B, R25A, R25B	PPC20.0XCT-ND	Vishay/BC Components
2	open	AXIAL RES METAL FILM 10.0 OHM 1/2W 1%	R29A, R29B	PPC10.0XCT-ND	Vishay/BC Components
2	2.2k 1W	AXIAL RES 10 OHM 1W 5% METAL OXIDE	R30A, R30B	10W-1-ND	Yageo
2	2.2k 1W	AXIAL RES 2.2K OHM 1W 5% METAL OXIDE	R31A, R31B	2.2KW-1-ND	Yageo
1	715 1%	AXIAL RES 715 OHM 1% 50PPM 1/4W	R103	CMF715QFCT-ND	Vishay/Dale





1	100k	RES 100K OHM CARBON FILM 1/4W 5%	R109	P100KBACT-ND	Panasonic - ECG
1	AXIAL RES 47K OHM 47k CARBON FILM 1/4W 5%		R112	P47KBACT-ND	Panasonic - ECG
2	1k 1W	AXIAL RES 1.0K OHM 1W 5% METAL OXIDE	R114A, R114B	1.0KW-1-ND	Yageo
2	15k	AXIAL RES 15k OHM CARBON FILM 1/4W 5%	R115A, R115B	P15KBACT-ND	Panasonic - ECG
4	3.3k 1W	AXIAL RES 3.3K OHM 1W 5% METAL OXIDE	R117A, R117B, R118A, R118B	3.3KW-1-ND	Yageo
2	22k	AXIAL RES 22K OHM CARBON FILM 1/4W 5%	R300, R301	P22KBACT-ND	Panasonic - ECG
2	100 Ohms	AXIAL RES 100 OHM CARBON FILM 1/4W 5%	R302, R303	P100BACT-ND	Panasonic - ECG
1	RCJ-013 (White CH2)	CONN RCA JACK METAL R/A WHT PCB	RCA1A	CP-1402-ND (White)	CUI Inc
1	RCJ-012 (Red CH1)	CONN RCA JACK METAL R/A WHT PCB	RCA1B	CP-1401-ND (Red)	CUI Inc
2	EG2209A	SWITCH SLIDE DPDT 12V .1A L=4	S1, S300	EG1908-ND	E-Switch
2	ED365/2	TERMINAL BLOCK 7.50MM 2POS PCB	SPKR1A, SPKR1B	ED2354-ND	On Shore Technology
1	2.2k at 25C	THERMISTOR NTC 2.2K OHM LEADED	TH100	BC2304-ND	Vishay/BC Components
2	IRS2092PbF	Class D Controller, IRS2092PbF DIP-16, Class D Controller, IRS2092PbFDIP-16	U1A, U1B	IR's P/N	International Rectifier
1	TL071CP	IC LN JFET-IN GP OP AMP 8-DIP	U300	296-7186-5-ND	Texas Instruments
4	15V	15V DIODE Zener 500MW Z1A, Z1B, Z102A, 1N5245B-TF ND	1N5245B-TPCT- ND	Micro Commercial Co.	
1	68V	DIODE Zener 500MW 68V DO35	Z100	1N5266B-TPCT- ND	Micro Commercial Co.
1	39V	DIODE Zener 500MW 39V DO35	Z101	1N5259BDICT-ND	Micro Commercial Co.
4	5.6V	DIODE Zener 500MW 5.6V DO35	Z103A, Z103B, Z104A, Z104B	1N5232B-TPCT- ND	Micro Commercial Co.
Note all ½ W and 1W resistors are flame proof part numbers					

# **Table 4 IRAUDAMP7D Mechanical Bill of Materials**

Quantit y	Value	Description	DLDER TAIL DIP IC Socket 1		Vendor
1	16-DIP Socket	16 PIN SOLDER TAIL DIP SOCKET			Aries Electro- nics
5	Washer #4 SS	WASHER LOCK INTERNAL #4 SS	Lock washer 1, Lock washer 2, Lock washer 3, Lock washer 4, Lock washer 5	H729- ND	Building Fasteners
1	РСВ	Print Circuit Board IRAUDAMP7D_Rev 2.2 .PCB	PCB 1		Custom
12	Screw 4- 40X5/16	SCREW MACHINE PHILLIPS 4-40X5/16	Screw 1, Screw 2, Screw 3, Screw 4, Screw 5, Screw 6, Screw 7, Screw 8, Screw 9, Screw 10, Screw 11, Screw 12	H343- ND	Building Fasteners



# REFERENCE DESIGN

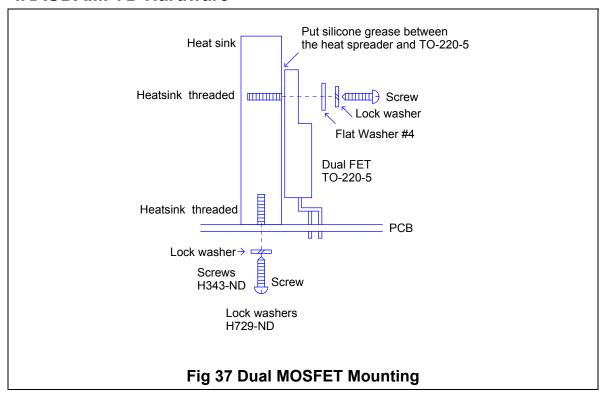
4	Stand off 0.5"	STANDOFF HEX 4- 40THR .500"L ALUM	Stand Off 1, Stand Off 2, Stand Off 3, Stand Off 4	1893K- ND	Keystone Electro- nics
1	Stand off 0.5"	STANDOFF HEX M/F 4- 40 .500" ALUM, Chassis GND	Stand Off 5	8401K- ND	Keystone Electro- nics
1	AAVID 4880G	Thermalloy TO-220 mounting kit with screw	TO-220 mounting kit 1	Newuar k 82K609 6	Therm- alloy

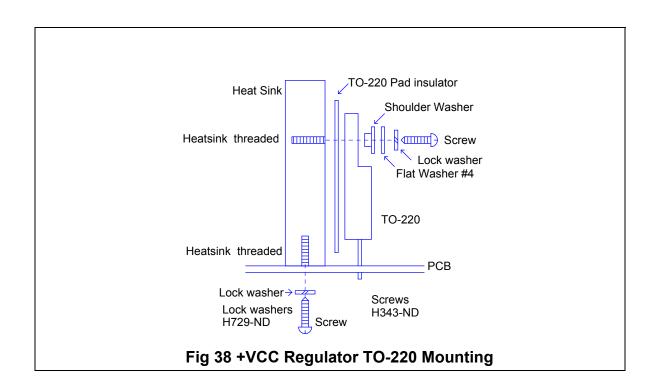
# **Table 5 IRAUDAMP7D Models Differential Table**

Model Name						
Ite	m	AMP7D-55	AMP7D-100	AMP7D-150	AMP7D-200	Notes
IR Power MOSFETS	FET1	IRFI4024H-117P	IRFI4212H-117P	IRFI4019H-117P	IRFI4020H- 117P	
Half Bridge	8 Ω	25 W x 2	60 W x 2	125 W x 2	250 W x 2	Stereo
Output	4 Ω	50 W x 2	120 W x 2	250 W x 2	N/A	Stereo
Full Bridge Output	8 Ω	100 W x 1	240 W x 1	500 W x 1	N/A	Bridged
Power	+B, -B	±25 V	±35 V	±50 V	±70 V	
Supply	±B Voltage Range	±3 V	±5 V	±8 V	±10 V	
Audio Gain	Gain	20	30	36	40	
Feedback	R8A,R8B	68k	100k	120k	130 k	
+VAA	R117A* R117B*	1 k, 1 W	2.2 k, 1 W	3.3 k, 1 W	5.1 k, 1 W	
-VSS	R118A* R118B*	1 k, 1 W	2.2 k, 1 W	3.3 k, 1 W	5.1 k, 1 W	
	R114A* R114B*	100,1 W	220, 1 W	1 k, 1 W	2.2 k 1 W	
VCC	R115A R115B	4.7 k	10 k	15 k	20 k	
OCSET	R12A R12B	1.3 k (20 A)	3.9 k (23 A)	7.5 k (30 A)	5.1 k (23 A)	(Trip level)
CSH	R18A R18B	0.0 (20A)	4.7 k (23A)	9.1 k (29A)	8.2 k (23 A)	(Trip level)
Oscillation Frequency	R11A R11B	270	270	300	360	400kHz
VB	R17A R17B	20 k	33 k	47 k	75k	
OVP	Z100	24 V 1N5252BDICT- ND	47 V 1N5261BDICT- ND	68 V 1N5266B-TPCT- ND	91 V 1N5270B- TPCT-ND	Zener Digikey P/N
UVP	Z101	12 V 1N5242B-TPCT- ND	30 V 1N5256BDICT- ND	39 V 1N5259BDICT- ND	51 V 1N5262B- TPCT-ND	Zener Digikey P/N
Clamping Diode	D5A D5B D6A D6B	IN4002	IN4002	IN4002	N/A	
	* Marked	l components ar	e axial, ±5 %, ¼	w, and flame pro	oof type.	



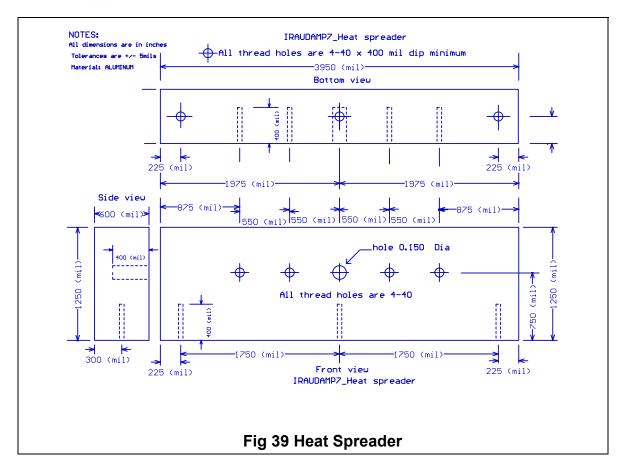
## **IRAUDAMP7D** Hardware

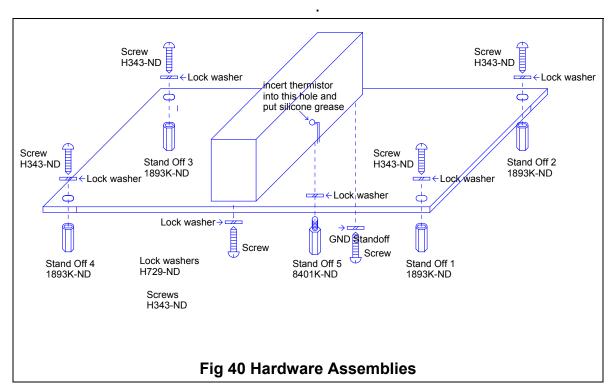














# **IRAUDAMP7D PCB Specifications**

#### PCB:

- 1. Single Layers SMT PCB with through holes
- 2. 1/16 thickness
- 3. 2/0 OZ Cu
- 4. FR4 material
- 5. 10 mil lines and spaces
- 6. Solder Mask to be Green enamel EMP110 DBG (CARAPACE) or Enthone Endplate DSR-3241or equivalent.
- 7. Top Silk Screen to be white epoxy non conductive per IPC-RB 276 Standard.
- 8. All exposed copper must finished with TIN-LEAD Sn 60 or 63 for 100u inches thick.
- 9. Tolerance of PCB size shall be 0.010 -0.000 inches
- 10. Tolerance of all Holes is -.000 + 0.003"
- 11. PCB acceptance criteria as defined for class II PCB'S standards.

#### Gerber Files Apertures Description:

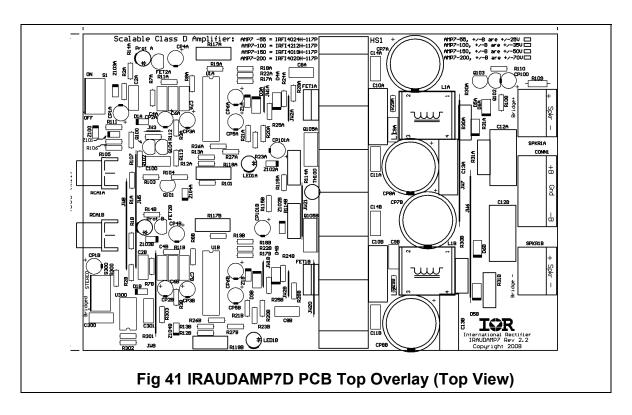
All Gerber files stored in the attached CD-ROM were generated from Protel Altium Designer Altium Designer 6. Each file name extension means the following:

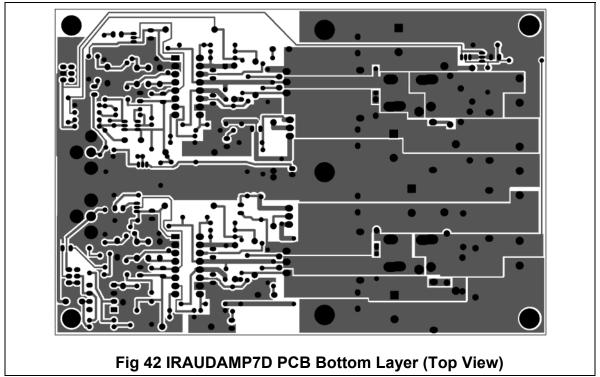
- 1. .gbl Bottom copper, bottom side
- 2. .gto Top silk screen
- 3. .gbs Bottom Solder Mask
- 4. .gko Keep Out,
- 5. .gm1 Mechanical
- 6. .gd1 Drill Drawing
- 7. .gg1 Drill locations
- 8. .txt CNC data
- 9. .apr Apertures data

Additional files for assembly that may not be related with Gerber files:

- 10. .pcb PCB file
- 11. .bom Bill of materials
- 12. .cpl Components locations
- 13. .sch Schematic
- 14. .csv Pick and Place Components
- 15. .net Net List
- 16. .bak Back up files
- 17. .lib PCB libraries











# **Revision changes descriptions**

Revision	Changes description	Date	
Rev 2.8	Released	September, 03 2008	
Rev 2.9	BOM append R21B; Schematic: CH2 R21A→R21B	October,24,2013	



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