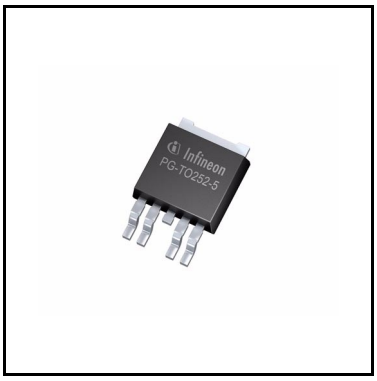
HITFET™ - BTS3011TE

Smart Low-Side Power Switch



1 Overview

Features

- Single channel device
- Digital Feedback
- Current limitation trigger concept
- 3.3 and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for inductive loads as well as loads with inrush currents

Description

The BTS3011TE is a 11 mΩ single channel Smart Low-Side Power Switch with in a PG-TO252-5 package providing embedded protective functions. The power transistor is built by an N-channel vertical power MOSFET.
The device is monolithically integrated. The BTS3011TE is automotive qualified and is optimized for 12 V automotive and industrial applications.

Type	Package	Marking
BTS3011TE	PG-TO252-5	S3011TE

Table 1 Product Summary

Operating voltage range	V_{OUT}	3 .. 28 V
Maximum battery voltage	$V_{BAT(LD)}$	40 V
Operating supply voltage range	V_{DD}	3.0 .. 5.5 V
Maximum input voltage	V_{IN}	5.5 V
Maximum On-State resistance at T_j = 150 °C, V_{DD} = 5 V, V_{IN} = 5 V	$R_{DS(ON)\_150}$	22 mΩ
Nominal load current	$I_{L(NOM)}$	10 A
Minimum current limitation trigger level	$I_{L(LIM)\_TRIGGER}$	70 A

Overview

Table 1 Product Summary (cont'd)

Minimum current limitation level	$I_{L(LIM)}$	35 A
Maximum OFF state load current at $T_J \leq 85$ °C	$I_{L(OFF)\_85}$	3 µA
Maximum stand-by supply current at $T_J \leq 85$ °C	$I_{DD(OFF)\_85}$	6 µA

Diagnostic Functions

- Short circuit to battery
- Over temperature
- Stable latching diagnostic signal

Protection Functions

- Over temperature shutdown with delayed auto restart
- Active clamp over voltage protection of the OUTput
- Current limitation with current limitation trigger
- Enhanced short circuit protection

Detailed Description

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by maximum clamping energy and maximum current capabilities.

The BTS3011TE offers dedicated ESD protection on the IN, VDD and STATUS pin referring to the Ground pin, as well as an over voltage clamping of the Drain/OUT to Source/GND.

The over voltage protection gets activated during inductive turn off conditions or other over voltage events (such as load dump). The power MOSFET is limiting the drain-source voltage, if it rises above the $V_{OUT(CLAMP)}$.

The over temperature protection prevents the device from overheating due to overload and/or bad cooling conditions.

The BTS3011TE has a delayed auto restart thermal shut-down function. The device will turn on again, If the input pin is still high after a delayed time $t_{D(RESTART)}$ considering the junction temperature has dropped below the thermal hysteresis.

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2 Block Diagram

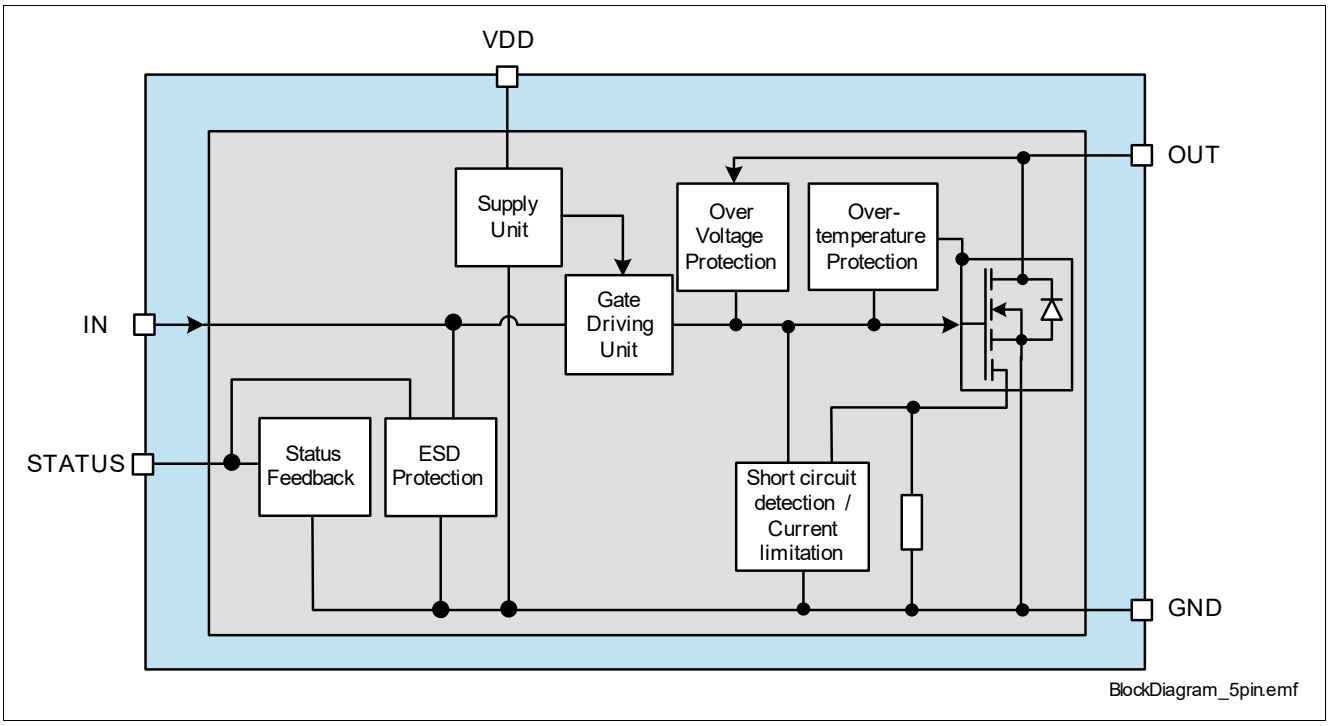

Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment BTS3011TE

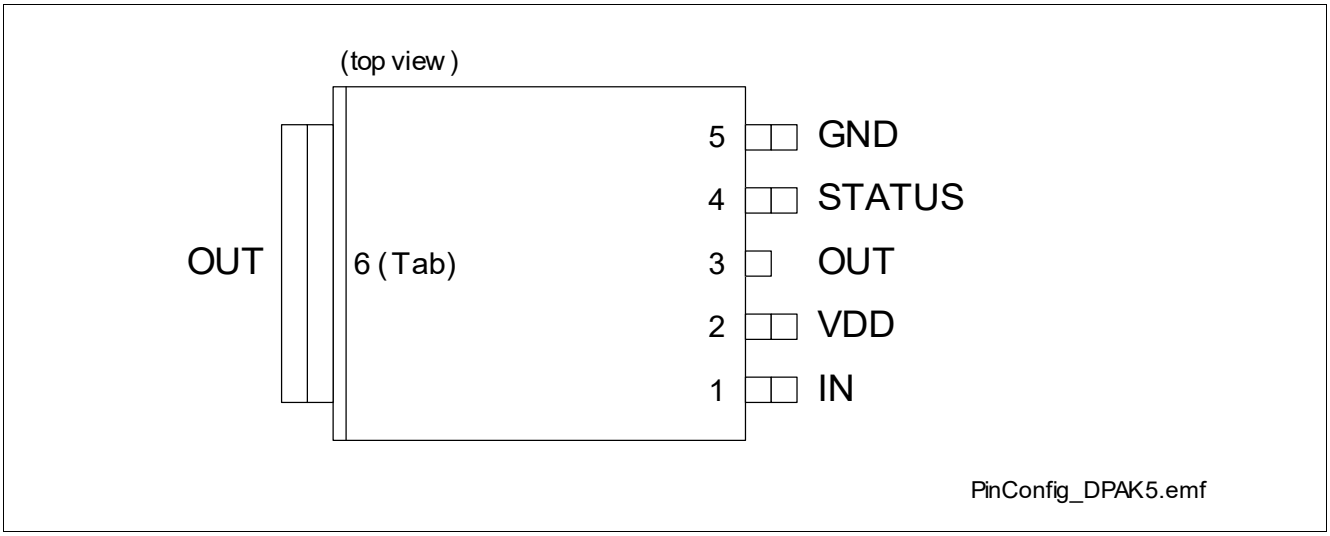

Figure 2 Pin Configuration DPAK5

3.2 Pin Definitions and Functions

Table 2

Pin	Symbol	Function
1	IN	Input pin
2	VDD	5 V supply pin
3,6	OUT	Drain, Load connection for power DMOS
4	STATUS	Open-drain status feedback (low active)
5	GND	Ground, Source of power DMOS

3.3 Voltage and Current Definition

Figure 3 shows all external terms used in this data sheet, with associated convention for positive values.

Pin Configuration

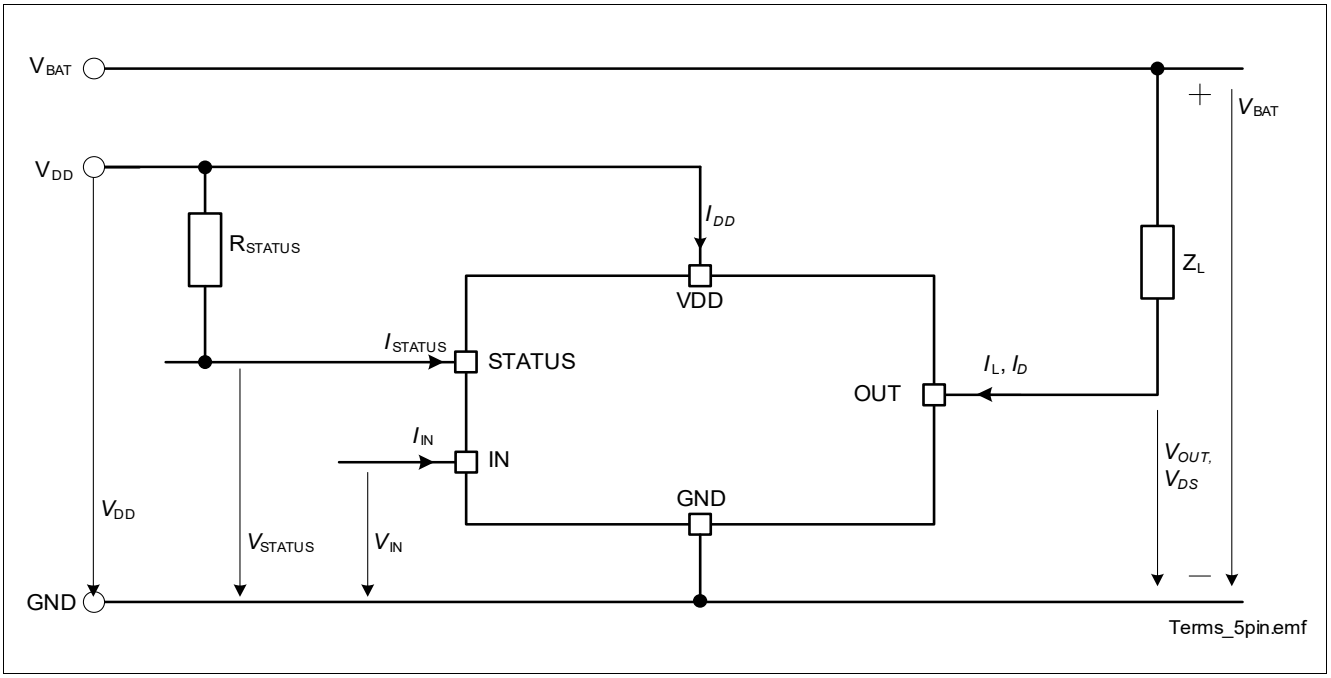

Figure 3 Naming Definition of electrical parameters

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_{DD}	-0.3	–	5.5	V	–	P_4.1.1
Output voltage	V_{OUT}	–	–	40	V	internally clamped	P_4.1.2
Battery voltage for short circuit protection	$V_{BAT(SC)}$	–	–	32	V	[1)] l = 0 or 5 m R_{SC} = 30 mΩ + R_{Cable} R_{Cable} = l * 16 mΩ/m L_{SC} = 5 µH + L_{Cable} L_{Cable} = l * 1 µH/m	P_4.1.3
Battery voltage for load dump protection ($V_{BAT(LD)}$ = V_A + V_S with V_A=13.5 V)	$V_{BAT(LD)}$	–	–	40	V	[2)] R_i = 2 Ω; R_{Load} = 2.2 Ω; t_d=400 ms; suppressed pulse	P_4.1.4
Input Pin							
Input voltage	V_{IN}	-0.3	–	5.5	V	–	P_4.1.8
Status Pin							
Status voltage	V_{STATUS}	-0.3	–	5.5	V	–	P_4.1.9
Power Stage							
Load current	$\|I_L\|$	–	–	$I_{L(LIM)\_TRIGGER}$	A	–	P_4.1.12
Energies							
Unclamped single inductive energy single pulse	E_{AS}	–	–	390	mJ	$I_{L(0)}$ = $I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{J(0)}$ = 150°C	P_4.1.13
Unclamped repetitive inductive energy pulse with 100k cycles	$E_{AR(100k)}$	–	–	290	mJ	$I_{L(0)}$ = $I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{j(0)}$ = 105°C	P_4.1.15
Temperatures							
Operating temperature	T_j	-40	–	+150	°C	–	P_4.1.17
Storage temperature	T_{stg}	-55	–	+150	°C	–	P_4.1.18
ESD Susceptibility							

Table 3 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	HBM[3)]	P_4.1.19
ESD susceptibility OUT pin vs. GND	V_{ESD}	-4	–	4	kV	HBM[3)]	P_4.1.20
ESD susceptibility	V_{ESD}	-750	–	750	V	CDM[4)]	P_4.1.21

1) Not subject to production test, specified by design.

2) $V_{BAT(LD)}$ is setup without the DUT connected to the generator per ISO7637-1;
R_i is the internal resistance of the load dump test pulse generator;
t_d is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)

4) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation*

4.2 Functional Range

Table 4 Functional Range[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Nominal Operation	$V_{DD(NOM)}$	3.0	5.0	5.5	V		P_4.2.1
Supply current continuous ON operation	$I_{DD(ON)}$	–	–	1	mA	–	P_4.2.2
Standby supply current (ambient)	$I_{DD(OFF)}$	–	1.5	6	µA	$T_j \leq 85°C$	P_4.2.4
Battery Voltage Range for Nominal Operation	$V_{BAT(NOR)}$	6	13.5	18	V	–	P_4.2.5
Extended Battery Voltage Range for Operation	$V_{BAT(EXT)}$	0	–	32	V	parameter deviations possible	P_4.2.6

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 5 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Solder Point	R_{thJSP}	–	2	–	K/W	1) 2)	P_4.3.1
Junction to Ambient (2s2p)	$R_{thJA(2s2p)}$	–	25	–	K/W	1) 3)	P_4.3.2
Junction to Ambient (1s0p+600mm^2 Cu)	$R_{thJA(1s0p)}$	–	38	–	K/W	1) 4)	P_4.3.3

1) Not subject to production test, specified by design.

2) Specified RthJSP value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). Tc = 85°C. Device is loaded with 1 W power.

3) Specified RthJA value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip and Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Ta = 85°C. Device is loaded with 1 W power.

4) Specified RthJA value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip and Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm2 and 70 µm thickness. Ta = 85°C. Device is loaded with 1 W power

4.3.1 PCB set up (from THB report)

The following PCB set up was implemented to determine the transient thermal impedance.

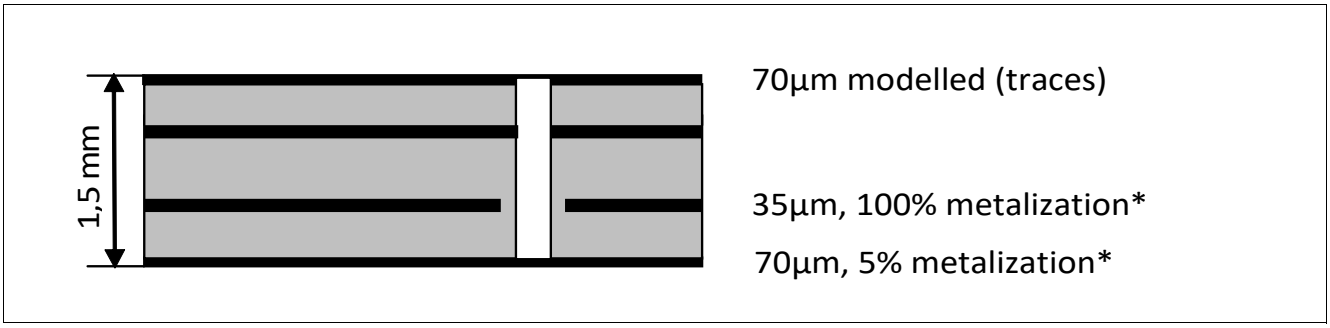

Figure 4 Cross section JEDEC 2s2p.

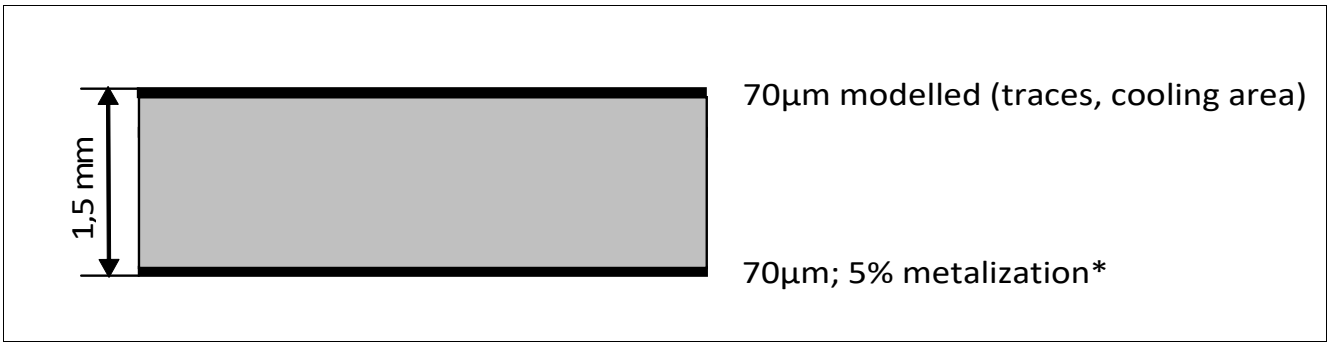

Figure 5 Cross section JEDEC 1s0p.

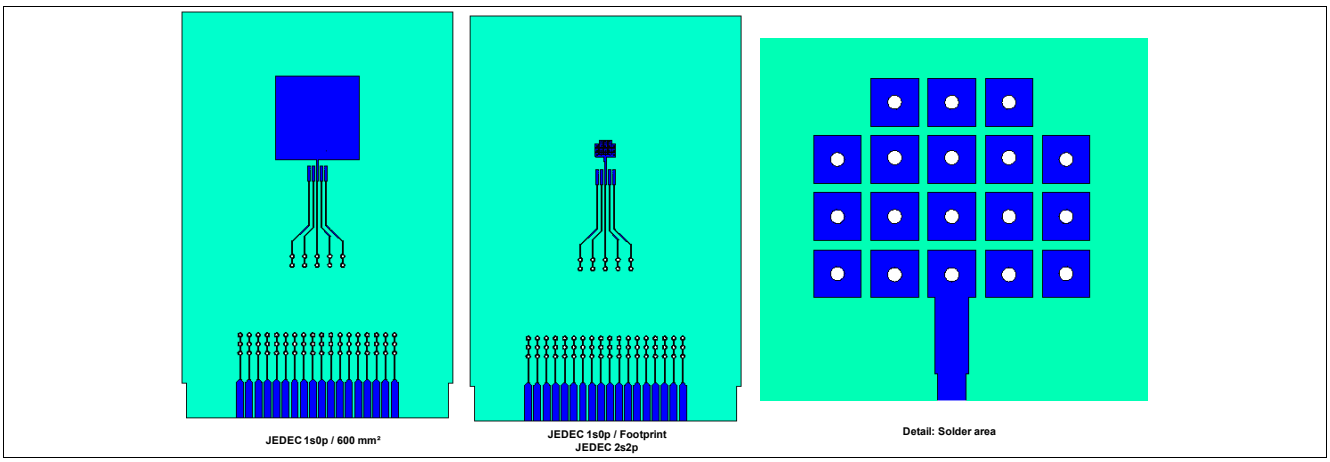

Figure 6 PCB layout.

4.3.2 Transient Thermal Impedance

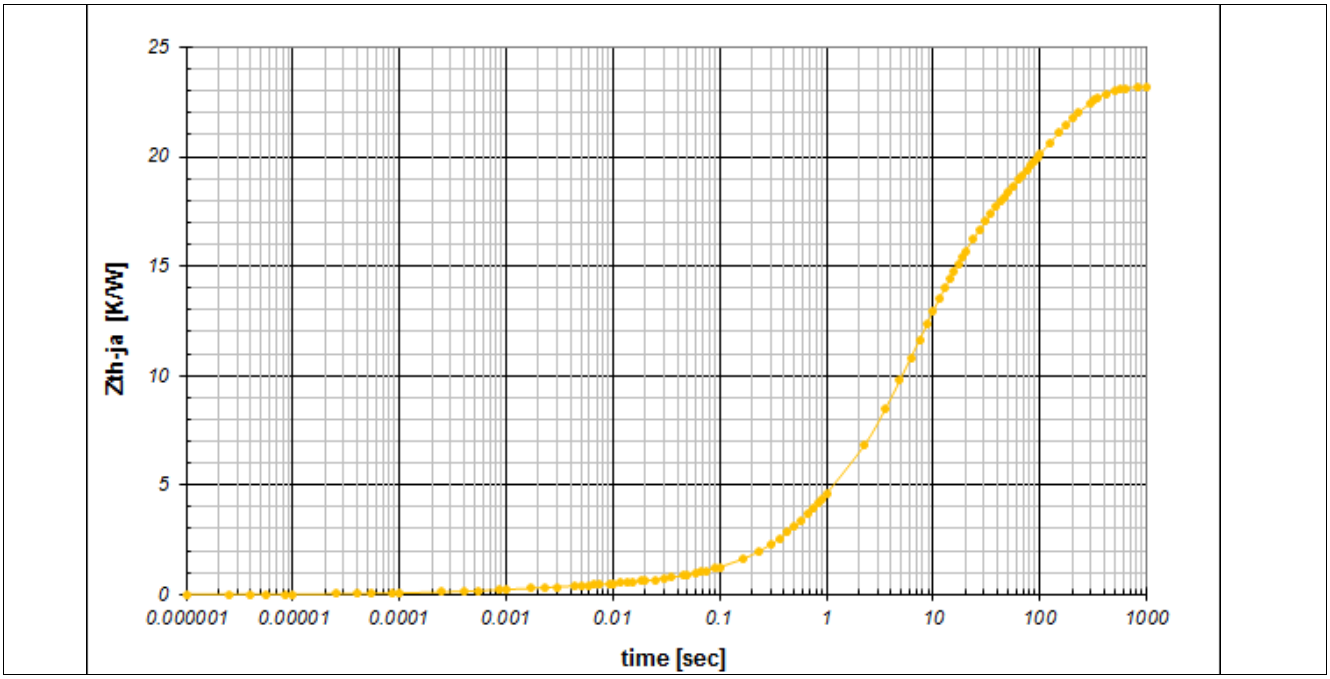

Figure 7 **Typical transient thermal impedance $Z_{thJA} = f(t_p)$, $T_a = 85$ °C**
Value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip and Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70 um Cu, 2 x 35 um Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Device is dissipating 1 W power.

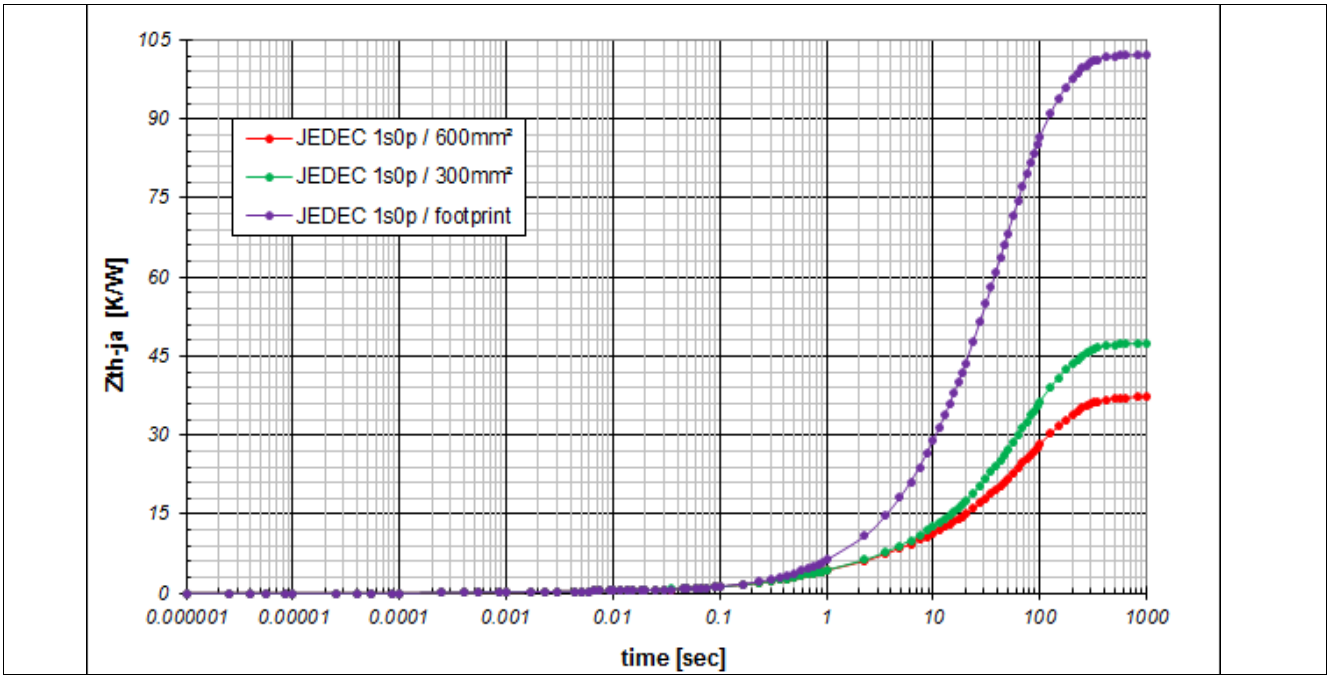

Figure 8 **Typical transient thermal impedance $Z_{thJA} = f(t_p)$, $T_a = 85$°C**
Value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. Device is dissipating 1 W power.

5 Power Stage

5.1 Output On-state Resistance

The on-state resistance depends on the supply voltage as well as on the junction temperature T_J. **Figure 9** shows this dependencies in terms of temperature and voltage for the typical on-state resistance $R_{DS(ON)}$. The behavior in reverse polarity is described in chapter**"Reverse Current Capability" on Page 16**.

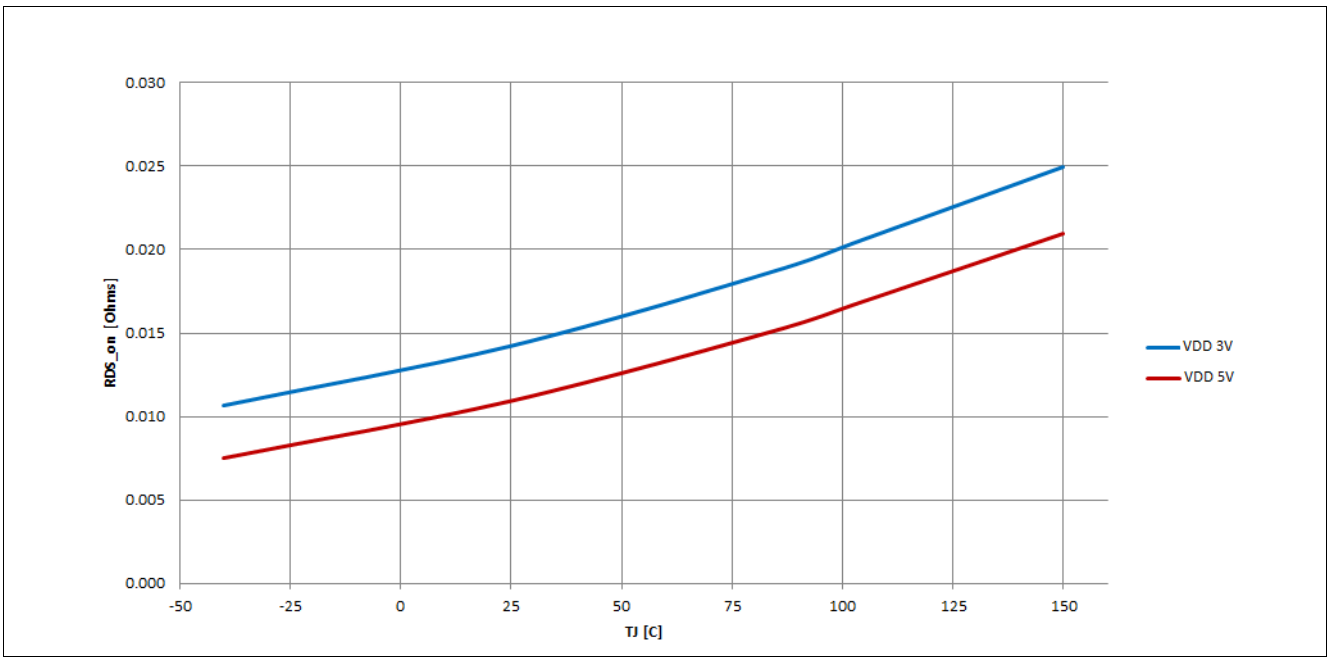

Figure 9 Typical On-State Resistance, $R_{DS(ON)} = f(T_J)$; V_{DD} = 5 V, 3 V; V_{IN} = high

A high signal at the input pin causes the power DMOS to switch ON with a dedicated slope.

To achieve the specified $R_{DS(ON)}$ and switching speed, a 5 V supply is required.

5.2 Resistive Load Output Timing

Figure 10 shows the typical timing when switching a resistive load.

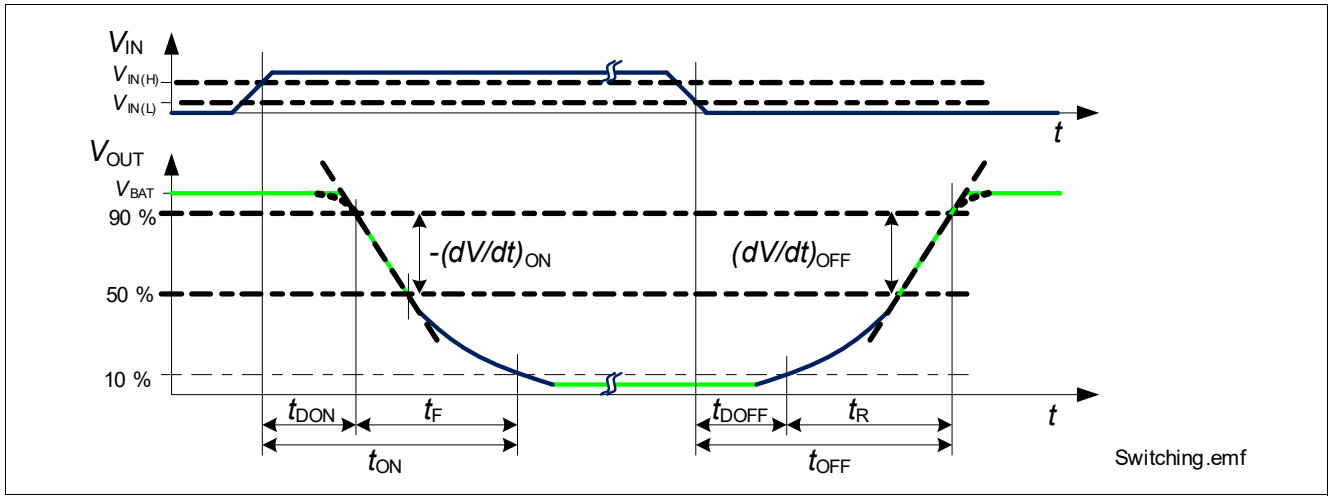

Figure 10 Definition of Power Output Timing for Resistive Load

5.3 Inductive Load

5.3.1 Output Clamping

When switching off inductive loads with low side switches, the drain-source voltage V_{OUT} rises above battery potential, because the inductance intends to continue driving the current. To prevent unwanted high voltages the device has a voltage clamping mechanism to keep the voltage at $V_{OUT(CLAMP)}$. During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See **Figure 11** and **Figure 12** for more details.

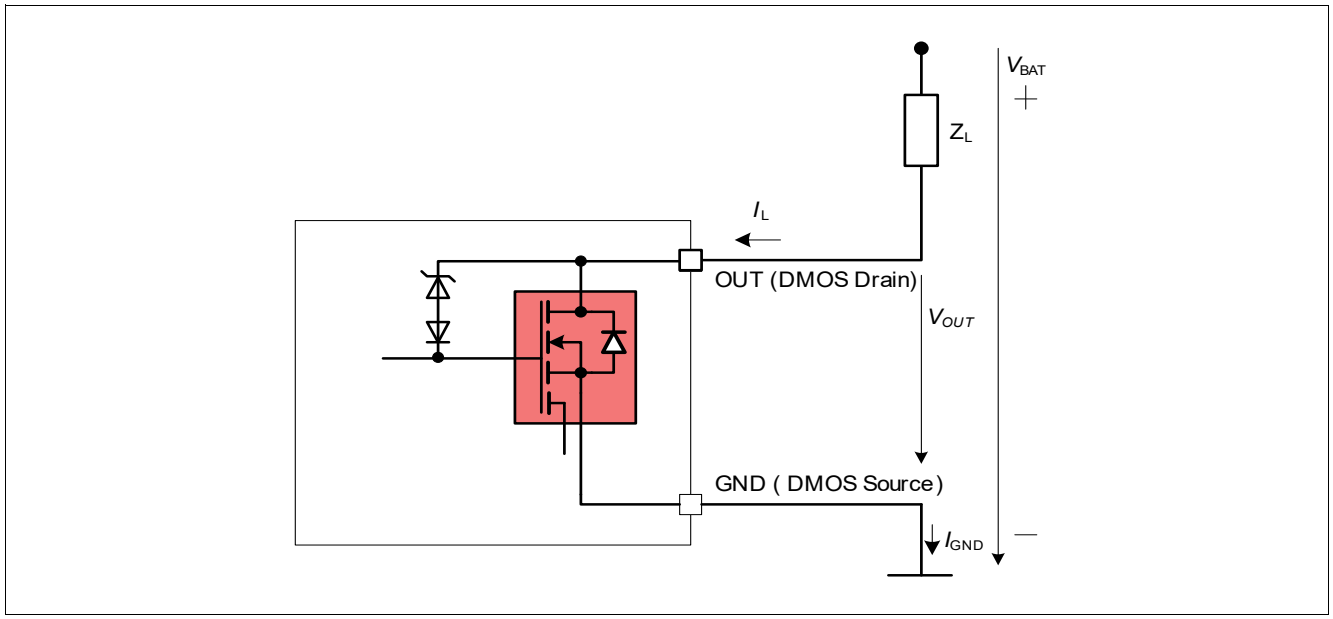

Figure 11 Output Clamp Circuitry

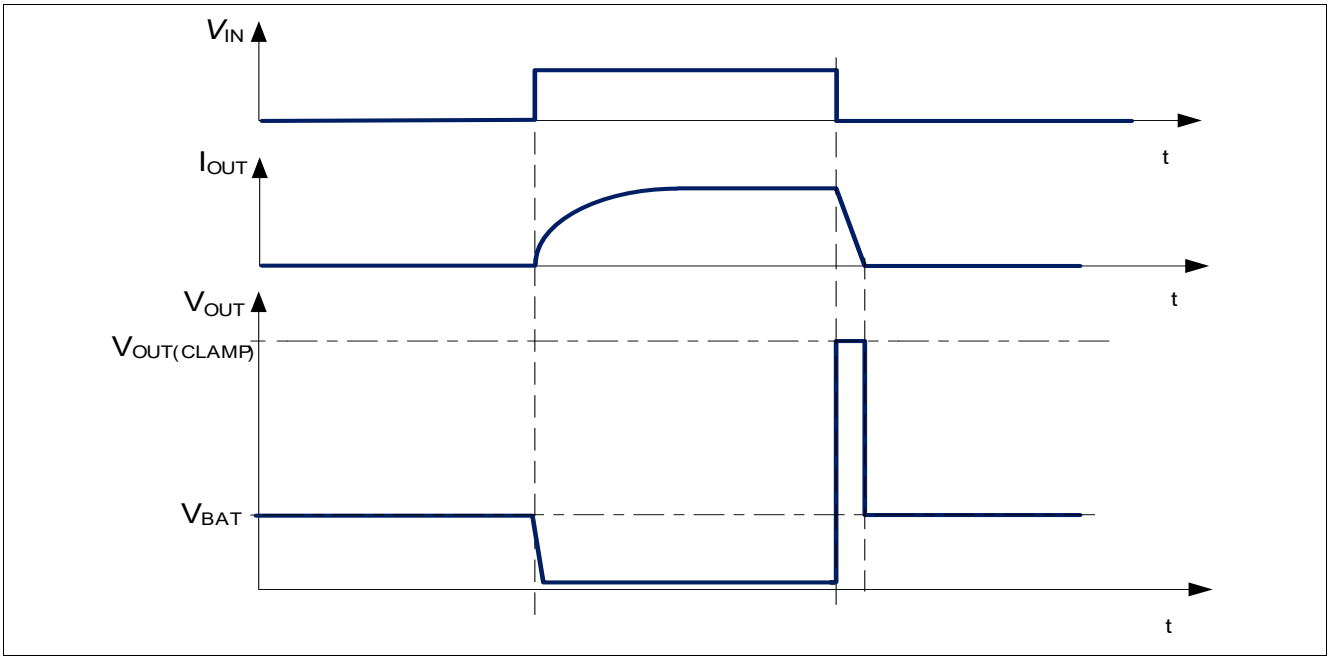

Figure 12 Switching an Inductive Load

Note: Repetitive switching of inductive load by VDD instead of using the input is a not recommended operation and may affect the device reliability and reduce the lifetime.

5.3.2 Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTS3011TE.
This energy can be calculated by the following equation:

$$E = V_{OUT(CLAMP)} \times \left[\frac{V_{BAT} - V_{OUT(CLAMP)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_{BAT} - V_{OUT(CLAMP)}}\right) + I_L \right] \times \frac{L}{R_L} \quad (5.1)$$

Following equation simplifies under assumption of $R_L = 0$

$$E = \frac{1}{2} L I_L^{\,2} \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CLAMP)}}\right) \quad (5.2)$$

Figure 13 shows the inductance / current combination the BTS3011TE can handle.
For maximum single avalanche energy please also refer to E_{AS} parameter in **Page 8**

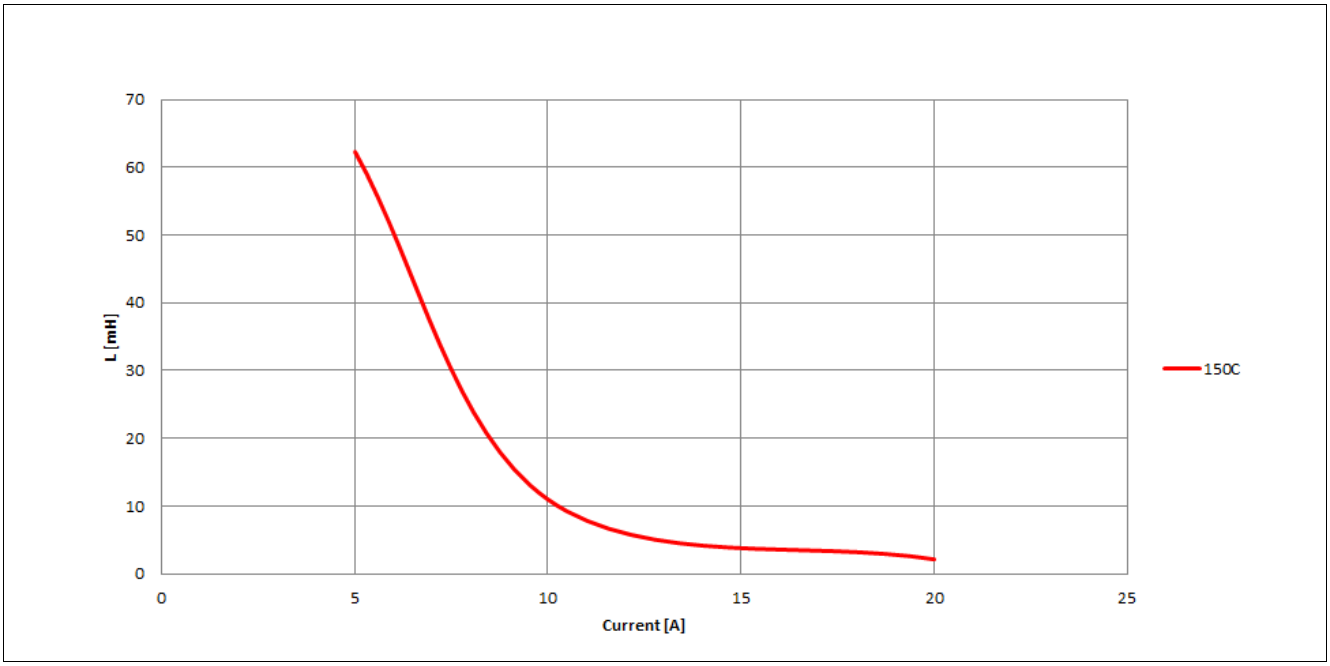

Figure 13 Maximum load inductance for single pulse
$L = f(I_L)$;
$T_{J(0)} = 150°C$; $V_{BAT} = 13.5$ V

5.4 Reverse Current Capability

A reverse battery situation means the OUT pin is pulled below GND potential to $-V_{BAT}$ via the load Z_L.

In this situation the load is driven by a current through the intrinsic body diode of the BTS3011TE and all protection, such as current limitation, over temperature or over voltage clamping, are not active.

OT is active in inverse current if DMOS is ON

In certain application case (for example in a bridge or half-bridge configuration) the intrinsic reverse body diode is used for freewheeling of an inductive load. In this case the device is still supplied but an inverse current is flowing from GND to OUT(drain) and the OUT will be pulled below GND.

In inverse or reverse operation via the reverse body diode, the device is dissipating a power loss which is defined by the driven current and the voltage drop on the body diode -VDS.

The BTS3011TE is capable of switching ON during inverse current by setting the IN high. In this condition, the over temperature is active.

5.5 Characteristics

Please see **“Power Stage” on Page 24** for electrical characteristic table.

6 Protection Functions

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operation. Protection functions are not to be used for continuous or repetitive operation.

6.1 Over Voltage Clamping on OUTput

The BTS3011TE is equipped with a voltage clamp circuitry that keeps the drain-source voltage V_{DS} at a certain level $V_{OUT(CLAMP)}$. The over voltage clamping is overruling the other protection functions. Power dissipation has to be limited to not exceed the maximum allowed junction temperature.

This function is also used in terms of inductive clamping. Please see also **“Output Clamping” on Page 14** for more details.

6.2 Thermal Protection

The device is protected against over temperature due to overload and/or bad cooling conditions by an integrated temperature sensor. The thermal protection is available if the device is active. .

The device incorporates an absolute ($T_{J(SD)}$) and a dynamic temperature limitation ($\Delta T_{J(SW)}$). Triggering one of them will cause the output to switch off.

The BTS3011TE has a delayed thermal-restart function. If the input (IN) is still high the device will turn on again after a delayed time $t_{D(RESTART)}$ considering the junction temperature has dropped below the thermal hysteresis.

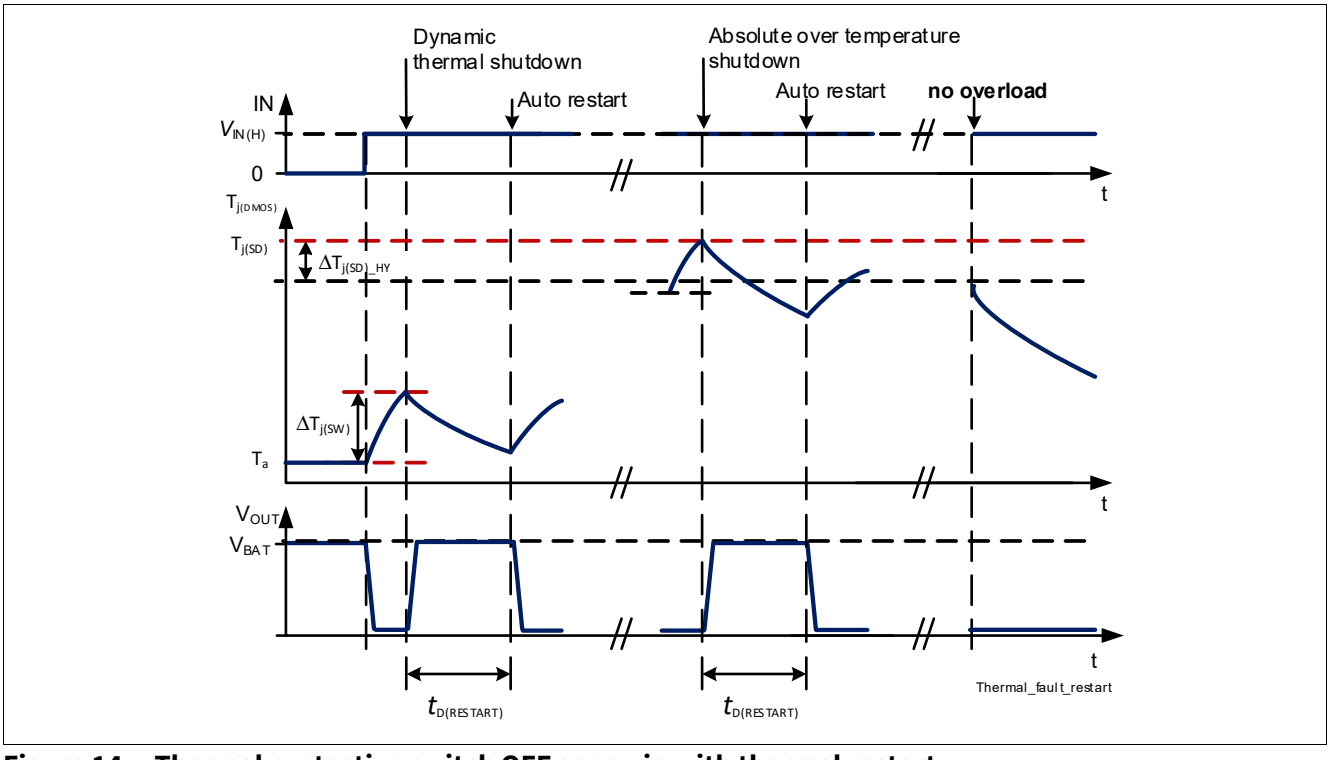

Figure 14 Thermal protective switch OFF scenario with thermal restart

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

6.3 Overcurrent Limitation / Short Circuit Behavior

This device is providing a smart overcurrent limitation intended to provide protection against short circuit conditions while allowing also load inrush currents higher than the current limitation level. To achieve this, the device has a current limitation level $I_{L(LIM)}$ which is triggered by a higher trigger level $I_{L(LIM)\_TRIGGER}$.

The condition short circuit is an overload condition on the device.

If the load current I_L reaches the current limitation trigger level $I_{L(LIM)\_TRIGGER}$ the internal current limitation will be activated and the device limits the current to a lower value $I_{L(LIM)}$. The device then starts heating up. When the thermal shutdown temperature $T_{J(SD)}$ is reached, the device turns off. The time from the beginning of current limitation until the over temperature switch off depends strongly on the cooling conditions.

If input is still high, the device will turn on again after a delayed time $t_{D(RESTART)}$ considering the junction temperature has dropped below the thermal hysteresis. The current limitation trigger is a latched signal. It will be only reset by input (IN) pin low and resetting the latch fault signal (STATUS pin = high. See **Chapter 7** Diagnostics) at the same time. This means if the input stays high all the time during short circuit, the current will be limited to $I_{L(LIM)}$ during the following pulses (while on thermal restart). It also means that the output current remains limited to the current limitation level $I_{L(LIM)}$ as long as the current limitation trigger is not reset.

Figure 15 shows this behavior.

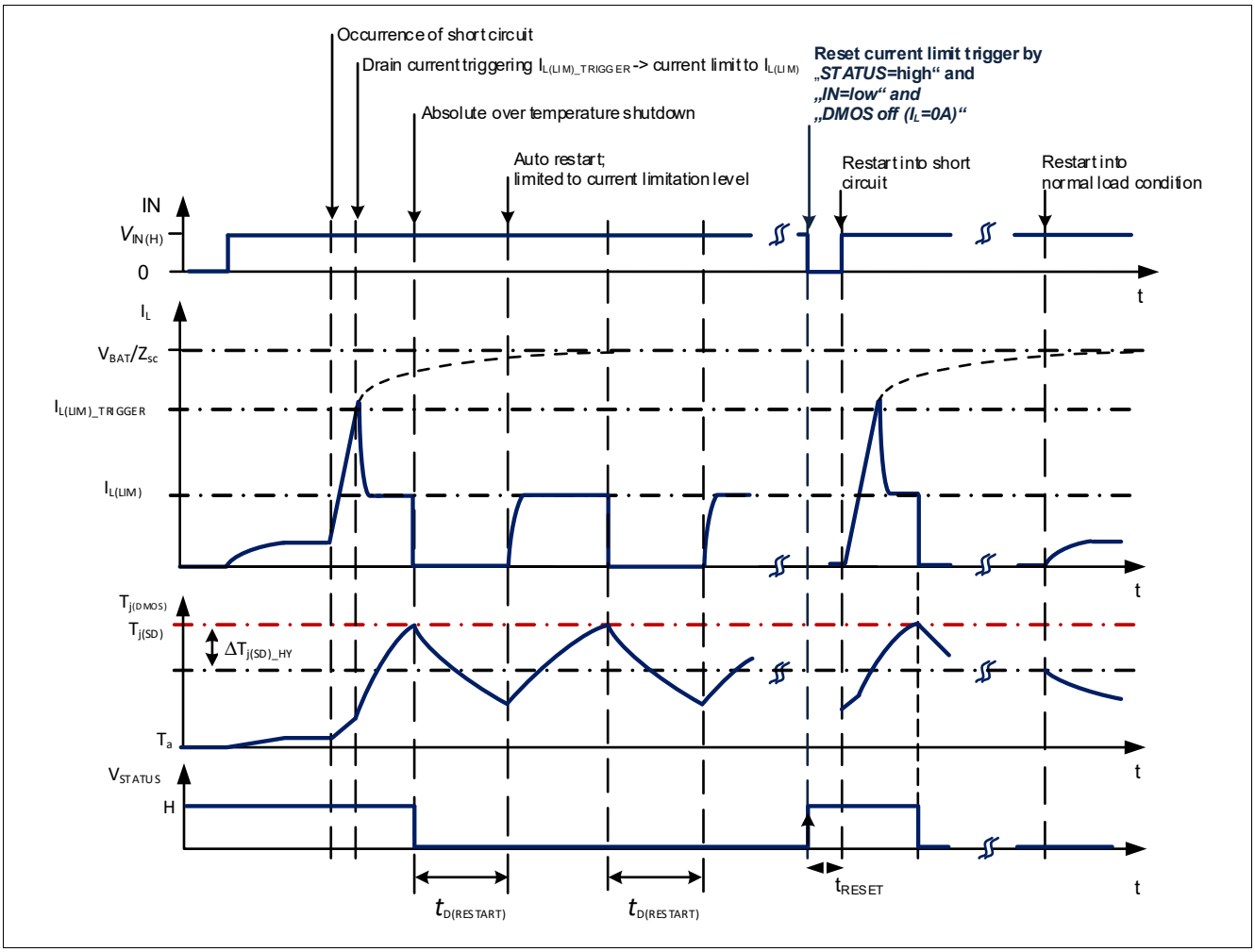

Figure 15 Short circuit protection via current limitation and thermal switch off, with latched fault signal on STATUS-pin

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

Behavior with overload current below current limitation trigger level

The lower current limitation level $I_{L(LIM)}$ will be also triggered by a thermal shutdown. This could be the case in terms of overload with a current still below the current limitation trigger level ($I_L < I_{L(LIM)TRIGGER}$).

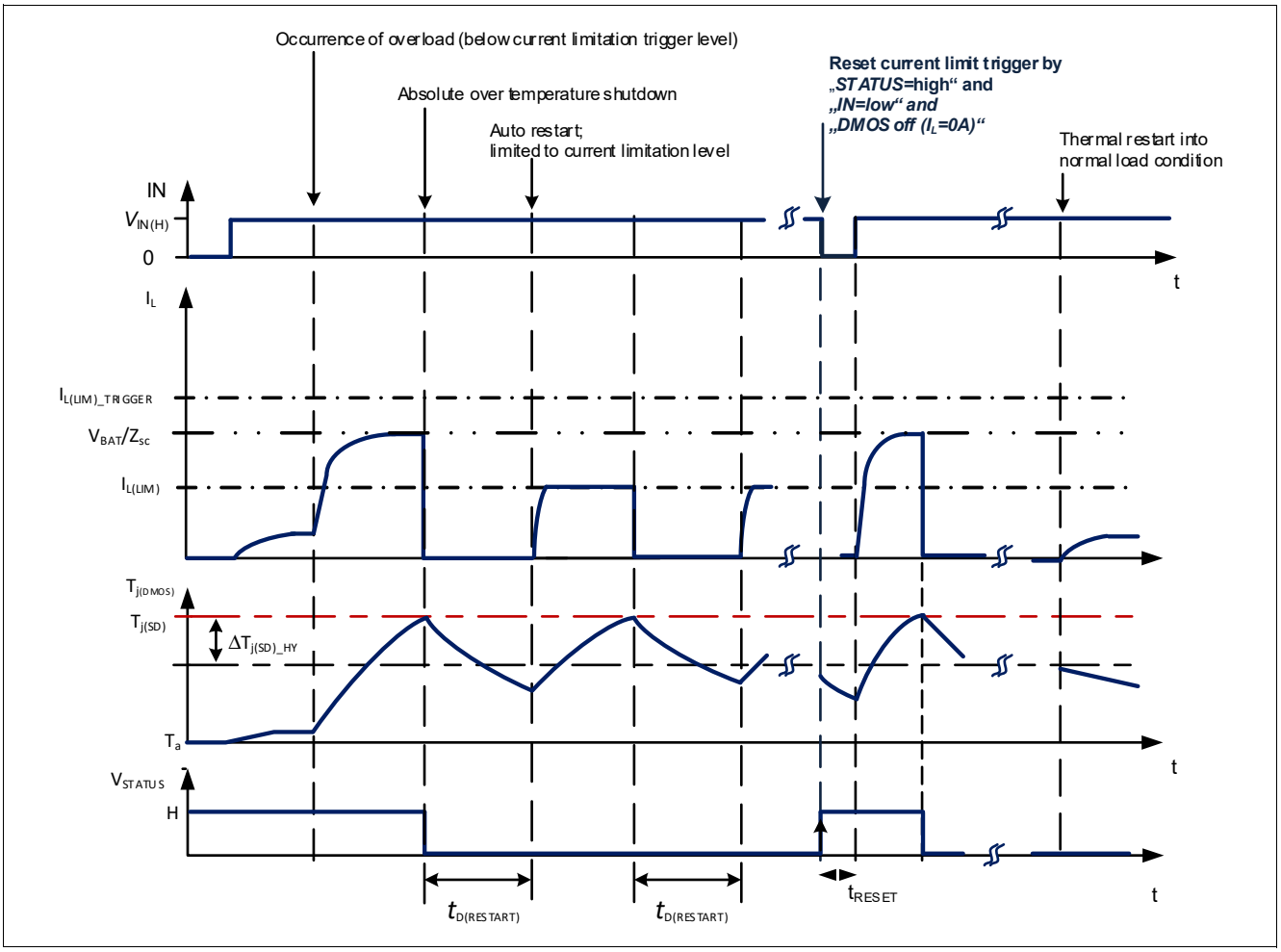

Figure 16 Example of overload behavior with thermal shutdown

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

6.4 Characteristics

Please see **“Protection” on Page 26** for electrical characteristic table.

7 Diagnostics

The BTS3011TE provides a latching digital fault feedback signal on the STATUS pin triggered by an over temperature shutdown.

7.1 Functional Description of the STATUS Pin

The BTS3011TE provides digital status information via the STATUS pin to give an alarm feedback to a connected microcontroller. Please see **Figure 17 “Feedback and control of STATUS pin” on Page 20**

Normal operation mode

In normal operation (no fault is detected) the STATUS pin’s logic is set ”high”. It is pulled up via an external Resistor (R_{STATUS}). Internally it is connected to an open drain MOSFET through an internal resistor.

Fault operation

In case of a thermal shutdown (fault), an internal MOSFET connected to the STATUS pin, pulls its voltage down to GND, providing a “low” level signal to the microcontroller. Fault mode operation remains active independent from the input pin state or internal restarts until it is reset.

Reset latch fault signal (external pull up)

To reset the latch fault signal of the BTS3011TE, the STATUS pin has to be pulled up to 5 V (recommended V_{DD}). Resetting the fault signal will not reset the current limitation trigger signal. To do so, the INPUT pin has to be set in logic “low” at the same time the STATUS pin is set “high”. In this case, the fault latch signal and the current limitation trigger will be reset (assuming the temperature has dropped below ΔT_{J_HYS}). Please refer to **Figure 15** and **Figure 16**.

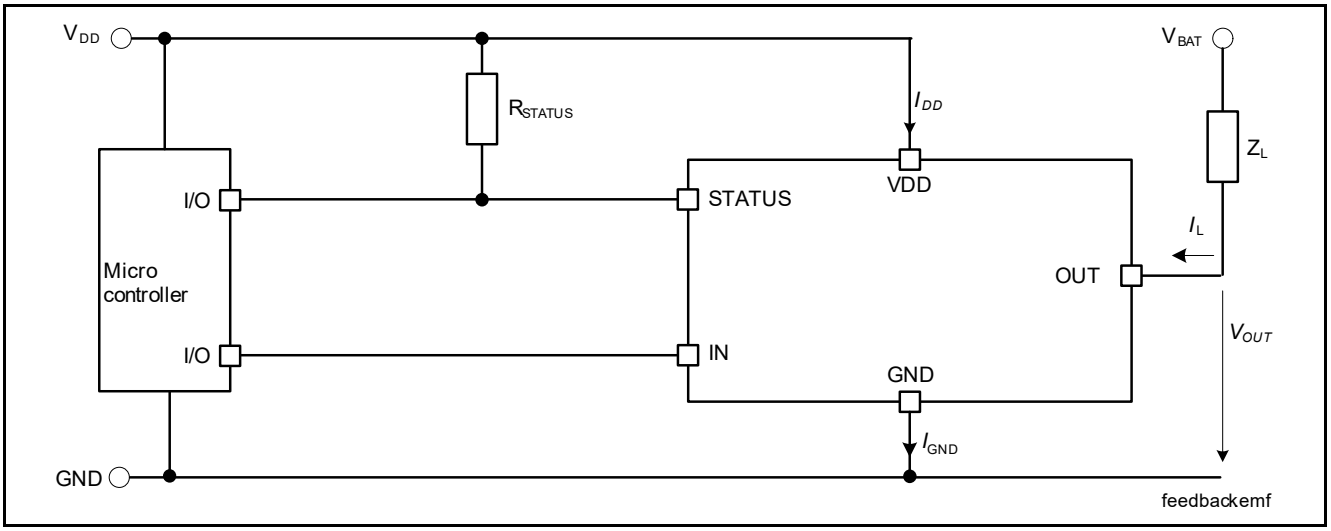

Figure 17 Feedback and control of STATUS pin

For recommended values of external components please see **“Application Information” on Page 40**

7.2 Characteristics

Please see **“Diagnostics” on Page 27** for electrical characteristic table.

8 Supply and Input Stage

8.1 Supply Circuit

The supply pin V_{DD} is protected against ESD pulses as shown in **Figure 18**.

The device supply is not internal regulated but directly taken from a external supply. Therefore a reverse polarity protected and buffered 5 V (or 3.3 V) voltage supply is required. To achieve the specified $R_{DS(ON)}$ and switching speed a 5 V supply is required.

The device shall be supplied via the V_{DD} pin before applying an input signal V_{IN} to ensure the correct functionality of the device.

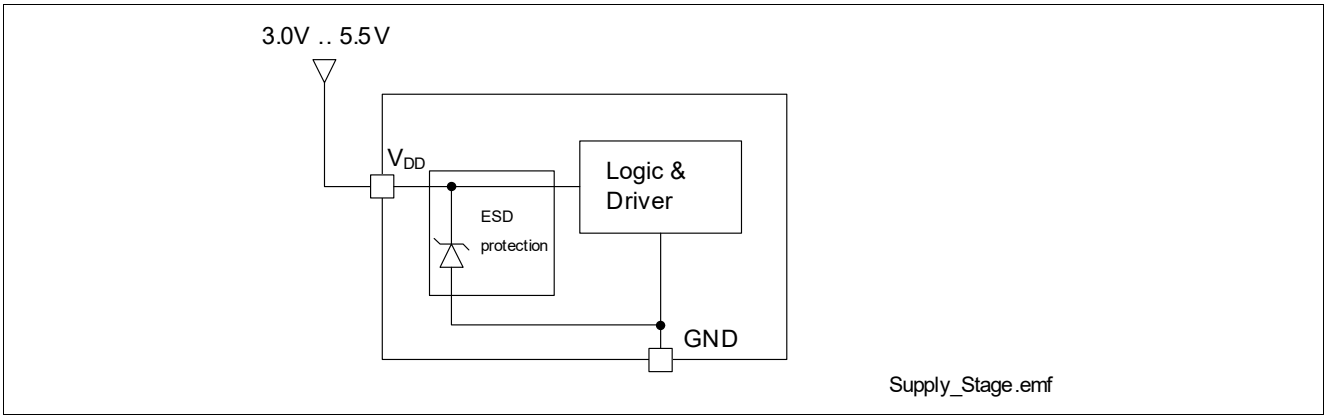

Figure 18 Supply Circuit

8.1.1 Undervoltage Shutdown

In order to ensure a stable and defined device behavior under all allowed conditions the supply voltage V_{DD} is monitored.

The output switches off, if the supply voltage V_{DD} drops below the switch-off threshold $V_{DD(TH)}$. In this case also all latches will be reset. The device functions are only given for supply voltages above the supply voltage threshold $V_{DD(SD)MAX}$. There is no failure feedback ensured for $V_{DD} < V_{DD(SD)}$.

8.2 Input Circuit

Figure 19 shows the input circuit of the BTS3011TE. Due to an internal pull-down it is ensured that the device switches off in case of open input pin. A Zener structure protects the input circuit against ESD pulses. As the BTS3011TE has a supply pin, the $R_{DS(ON)}$ of the power MOS is independent of the voltage on the IN pin (assumed V_{DD} is sufficient).

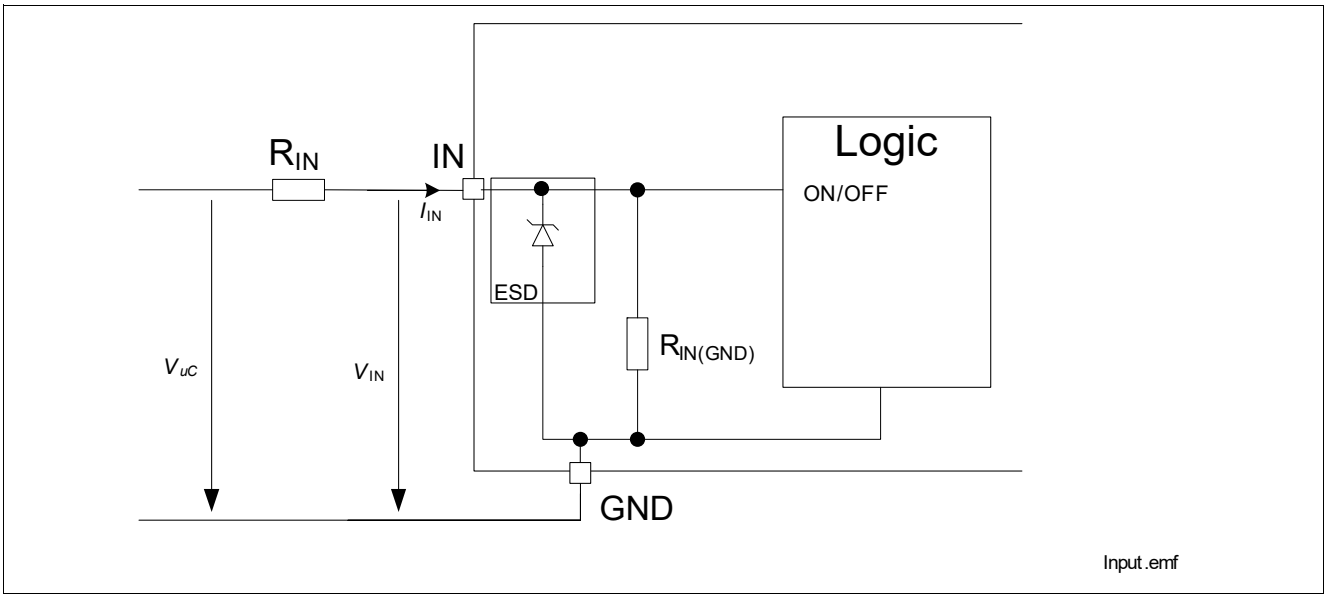

Figure 19 Simplified INput circuitry

8.3 Characteristics

Please see **“Supply and Input Stage” on Page 28** for electrical characteristic table.

9 Electrical Characteristics

Note: Characteristics show the deviation of parameter at given input voltage and junction temperature. Typical values show the typical parameters expected from manufacturing and in typical application condition.
All voltages and currents naming and polarity in accordance to
Figure 3 "Naming Definition of electrical parameters" on Page 7

9.1 Power Stage

Please see Chapter **"Power Stage" on Page 13** for parameter description and further details.

Table 6 Electrical Characteristics: Power Stage

T_j = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Stage - Static Characteristics							
On-State resistance at 25°C	$R_{DS(ON)\_25}$	–	10.7	–	mΩ	I_L = $I_{L(NOM)}$; V_{DD} = 5 V; T_J = 25°C	P_9.1.1
On-State resistance at 150°C	$R_{DS(ON)\_150}$	–	19	22	mΩ	I_L = $I_{L(NOM)}$; V_{DD} = 5 V; T_j = 150°C	P_9.1.2
Nominal load current	$I_{L(NOM)}$	–	10	–	A	1) T_J < 150°C; V_{DD} = 5 V;	P_9.1.7
OFF state load current, Output leakage current	$I_{L(OFF)\_85}$	–	–	3	µA	2) V_{OUT} = V_{BAT}; V_{IN} = 0 V; V_{DD} = 5 V; T_J ≤ 85°C	P_9.1.8
OFF state load current, Output leakage current at 150°C	$I_{L(OFF)\_150}$	–	6	14	µA	V_{OUT} = V_{BAT}; V_{IN} = 0 V; V_{DD} = 5 V; T_J = 150°C	P_9.1.9
Reverse Diode							
Reverse diode forward voltage	$-V_{DS}$	–	0.8	1.5	V	I_L = - $I_{L(NOM)}$; V_{IN} = 0 V	P_9.1.11
Power Stage - Dynamic characteristics - switching time V_{BAT} = 13.5 V;V_{DD} = 5 V; resistive load: R_L = 2.2 Ω see Figure 10 "Definition of Power Output Timing for Resistive Load" on Page 14 for definition details							
Turn-on time	t_{ON}	35	75	115	µs	-	P_9.1.12
Turn-off time	t_{OFF}	70	135	210	µs	-	P_9.1.13
Turn-on delay time	t_{DON}	5	15	25	µs	-	P_9.1.14

Table 6 Electrical Characteristics: Power Stage (cont'd)

T_j = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn-off delay time	t_{DOFF}	40	75	120	µs	-	P_9.1.15
Turn-on output fall time	t_F	30	60	90	µs	-	P_9.1.16
Turn-off output rise time	t_R	30	60	90	µs	-	P_9.1.17
Turn-on Slew rate [3]	$(DV/Dt)_{ON}$	0.22	0.4	0.65	V/µs	-	P_9.1.18
Turn-off Slew rate [4]	$(DV/Dt)_{OFF}$	0.22	0.4	0.65	V/µs	-	P_9.1.19

1) Not subject to production test, calculated by R_{thJA} and $R_{DS(ON)}$
2) Not subject to production test, specified by design
3) Not subject to production test, calculated slew rate between 90% and 50%; $dV/dt = (V_{OUT(90\%)} - V_{OUT(50\%)}) / |(t_{90\%} - t_{50\%})|$
4) Not subject to production test, calculated slew rate between 50% and 90%; $dV/dt = (V_{OUT(50\%)} - V_{OUT(90\%)}) / |(t_{50\%} - t_{90\%})|$

9.2 Protection

Please see Chapter **"Protection Functions" on Page 17** for parameter description and further details.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation

Table 7 Electrical characteristics: Protection

T_j = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V; V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal shut down [1)]							
Thermal shut down junction temperature	$T_{J(SD)}$	150	170	200	°C	1)	P_9.2.1
Thermal hysteresis	ΔT_{J_HYS}	–	20	–	K	1)	P_9.2.4
Dynamic temperature limitation	$\Delta T_{J(SW)}$	–	70	–	K	1)	P_9.2.5
Auto-restart delay time	$t_{D(RESTART)}$	10	30	40	ms	1) 2) V_{DD} = 5.0 V	P_9.2.8
Over Voltage Protection / Clamping							
Drain clamp voltage	$V_{OUT(CLAMP)}$	40	–	–	V	V_{IN} = 0 V; I_D = 50 mA;	P_9.2.9
Current limitation							
Current limitation trigger level	$I_{L(LIM)\_TRIGGER}$	70	–	140	A	V_{IN} = 5 V; V_{DD} = 5 V; V_{DS} = V_{BAT}	P_9.2.10
Current limitation level	$I_{L(LIM)}$	35	–	70	A	V_{IN} = 5 V; V_{DD} = 5 V; V_{DS} = V_{BAT}	P_9.2.11

1) Not subject to production test, specified by design.

2) Auto restart delay time after temperature protection shutdown. Thermal hysteresis must be also considered.

9.3 Diagnostics

Please see Chapter **"Diagnostics" on Page 20** for description and further details.

Table 8 Electrical Characteristics: Diagnostics

T_j = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Feedback pin							
Status pin voltage drop	$V_{STATUS(ON)}$	–	0.5	0.8	V	I_{STATUS} = 0.5 mA; 3 V ≤ V_{IN} ≤ 5.5 V latched fault;	P_9.3.1
Status pin leakage current	$I_{STATUS(OFF)\_85}$	–	1.5	6	µA	1) V_{STATUS} ≤ 5.5 V; T_J ≤ 85°C; 0 V ≤ V_{IN} ≤ 5.5 V	P_9.3.2
Status pin leakage current at 150°C	$I_{STATUS(OFF)\_150}$	–	6	12	µA	V_{STATUS} ≤ 5.5 V; T_J ≤ 150°C; 0 V ≤ V_{IN} ≤ 5.5 V	P_9.3.3
Status pin reset threshold	$V_{STATUS(RESET)}$	0.9	1.8	2.7	V	–	P_9.3.4
Status pin reset current	$I_{STATUS(RESET)}$	3	–	7	mA	–	P_9.3.5
Fault feedback reset time	$t_{STATUS(RESET)}$	100	–	–	µs	V_{STATUS} > $V_{STATUS(RESET)}$; no over temperature	P_9.3.6

1) Not subject to production test, specified by design.

9.4 Supply and Input Stage

Please see Chapter **"Supply and Input Stage" on Page 21** for description and further details.

Table 9 Electrical Characteristics: Supply and Input

T_j = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply							
Nominal supply voltage	$V_{DD(NOM)}$	3.0	5.0	5.5	V	–	P_9.4.1
Supply Undervoltage Shutdown Switch-on/off threshold voltage	$V_{DD(TH)}$	1.3	2.2	3.0	V	V_{IN} = 5.0 V	P_9.4.2
Supply current, continuos ON operation	$I_{DD(ON)}$	–	–	1	mA	device on-state V_{DD} = 5.0 V $I_{L(0)} = I_{L(NOM)}$	P_9.4.3
Supply current, inverse condition on OUT to GND	$I_{DD(-VOUT)}$	–	–	1	mA	1) V_{OUT} < -0.3 V V_{IN} = 5.0 V	P_9.4.5
Standby supply current	$I_{DD(OFF)\_85}$	–	1.5	6	µA	1) V_{IN} = 0 V V_{DD} = 5.0 V T_J < 85°C no fault signal	P_9.4.6
Standby supply current at 150°C	$I_{DD(OFF)\_150}$	–	6	14	µA	V_{IN} = 0 V V_{DD} = 5.0 V T_J < 150°C no fault signal	P_9.4.7
Standby supply current, inverse condition on OUT to GND	$I_{DD(OFF)(-VOUT)}$	–	–	200	µA	I_L=-$I_{L(NOM)}$ V_{IN} = 0 V	P_9.4.8
Input							
Low level input voltage	$V_{IN(L)}$	-0.3	–	0.8	V	–	P_9.4.9
High level input voltage	$V_{IN(H)}$	2.0	–	5.5	V	–	P_9.4.10
Input voltage hysteresis	$V_{IN(HYS)}$	–	200	–	mV	1)	P_9.4.11
Input pull down current	I_{IN}	–	–	160	µA	2.7 V < V_{IN} < 5.5 V -0.3 V < V_{DD} < 5.5V	P_9.4.12
Internal Input pull down resistor	$R_{IN(GND)}$	25	50	100	kΩ	–	P_9.4.13

1) Not subject to production test, specified by design.

10 Characterisation Results

Typical performance characteristics

10.1 Power Stage

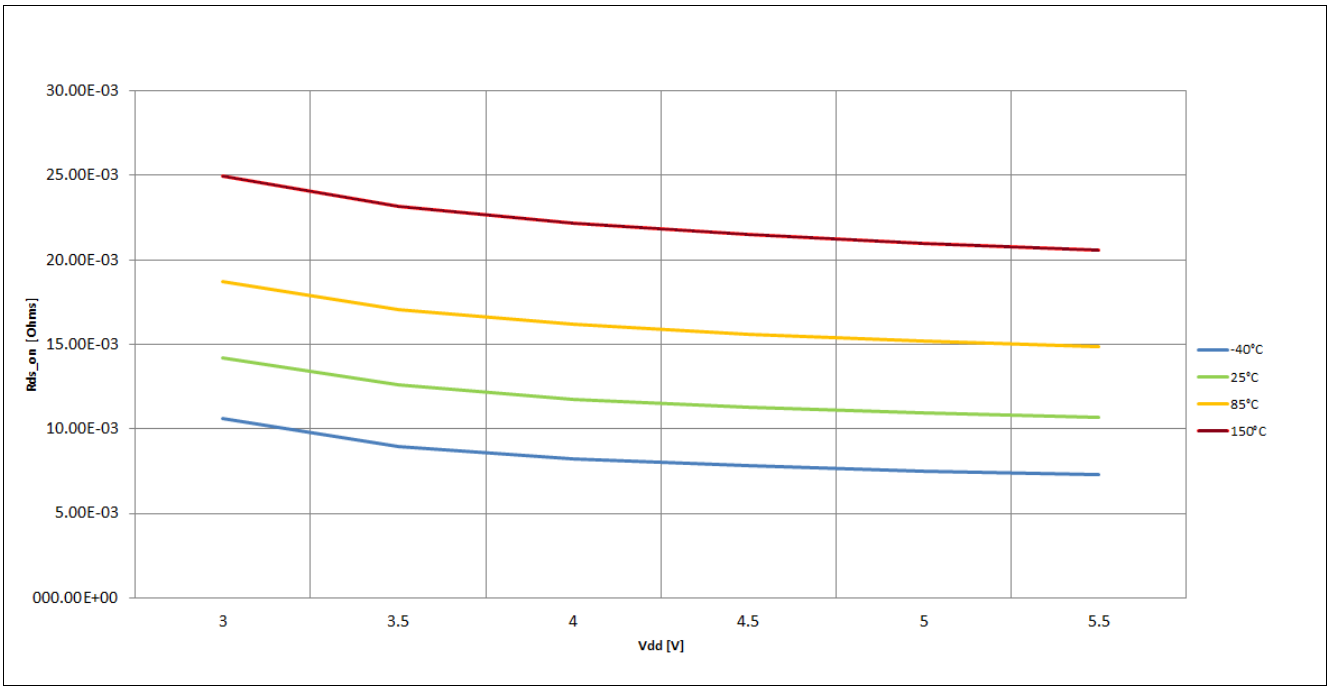

Figure 20 Typical $R_{DS(ON)}$ vs. V_{DD} (3..5.5 V) @ T_j=-40, 25, 85, 150°C; $I_{L(NOM)}$

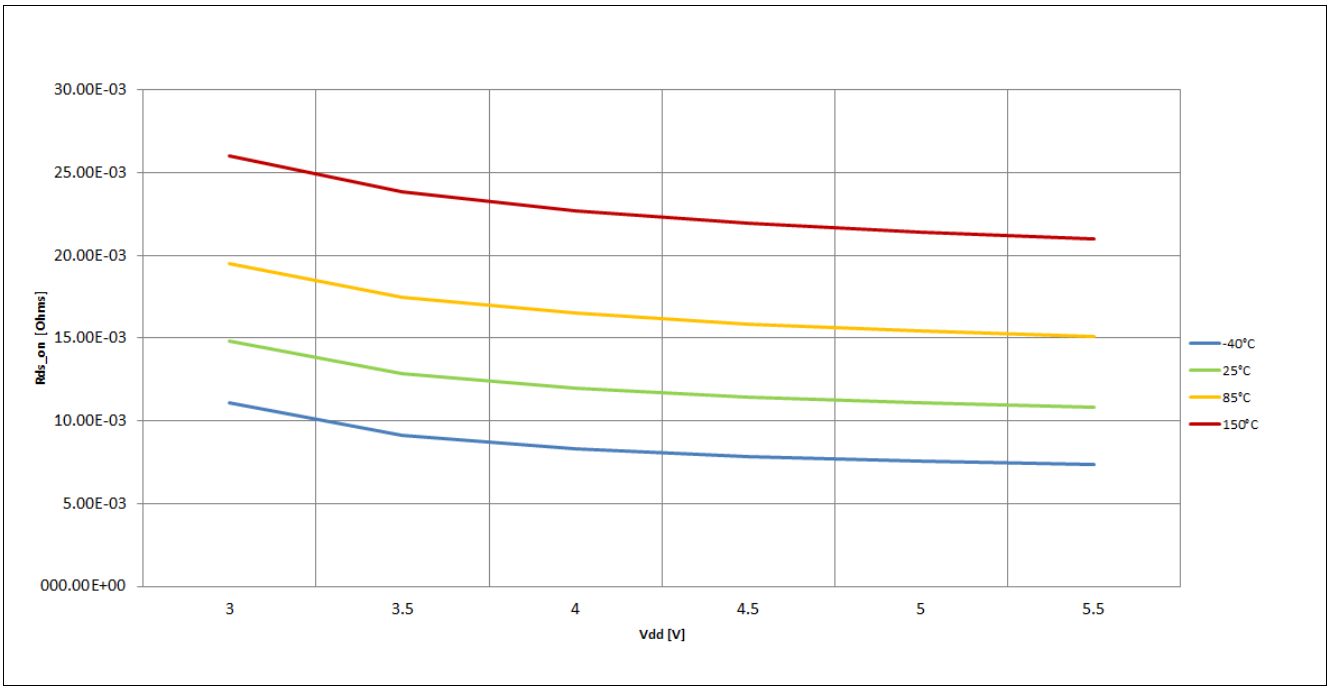

Figure 21 Typical $R_{DS(ON)}$ vs. V_{DD} (3..5.5 V) @ T_j=-40, 25, 85, 150°C; I_L=2*$I_{L(NOM)}$

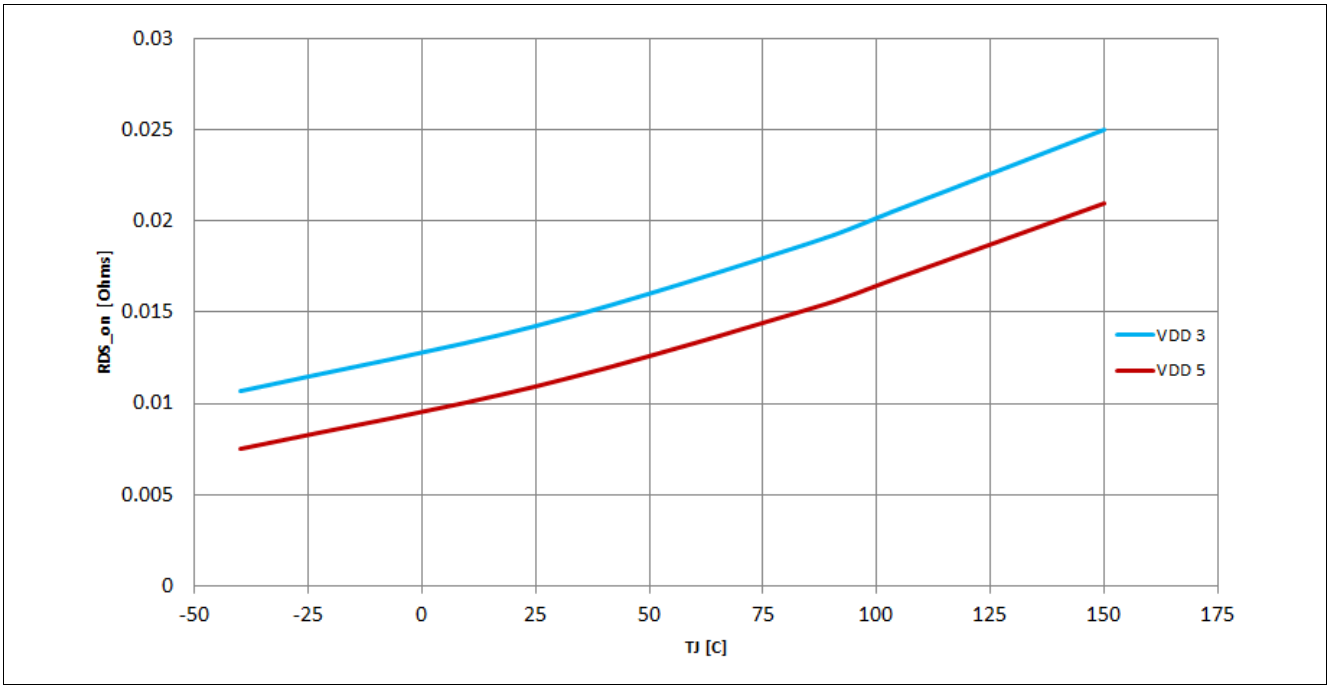

Figure 22 Typical $R_{DS(ON)}$ vs. T_j (-40..150°C) @ V_{DD}=5 V, 3 V; $I_{L(NOM)}$

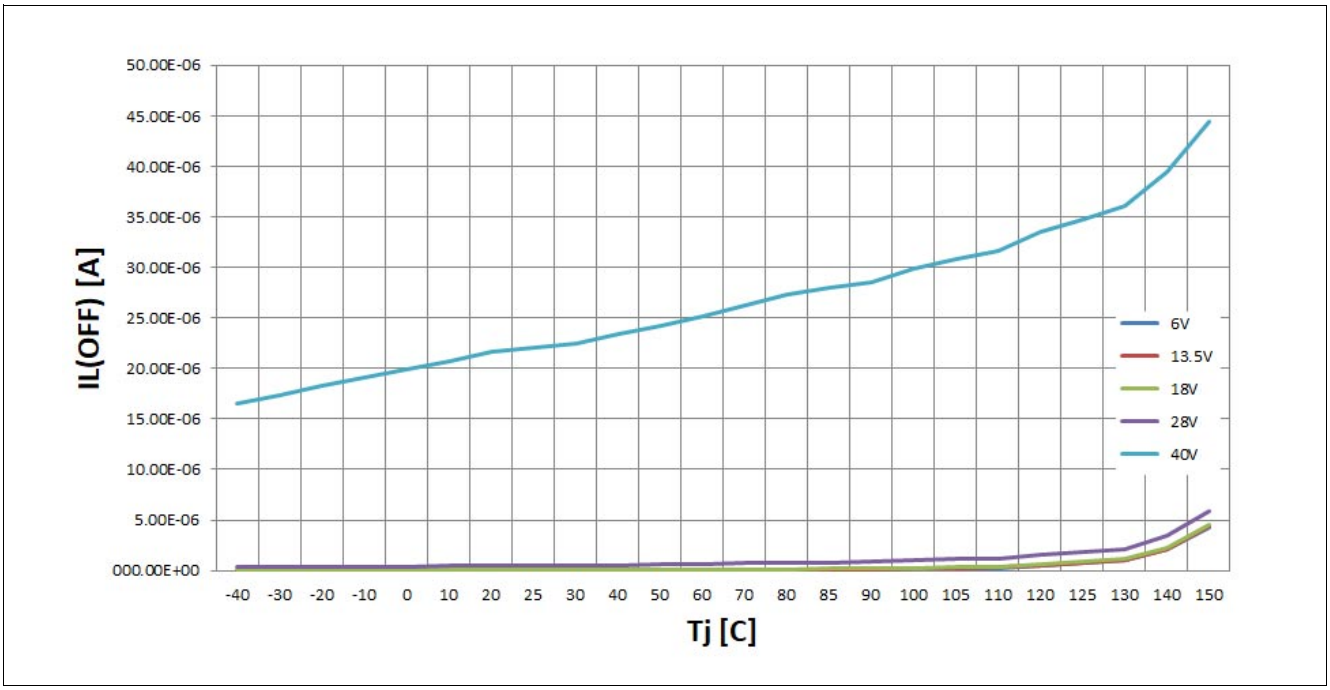

Figure 23 Typical $I_{L(OFF)}$ vs. T_j (-40..150°C) @ V_{BAT}=6 V, 13.5 V, 18 V, $V_{BAT(SC)}$V, 40 V; V_{IN}=0V;

Characterisation Results

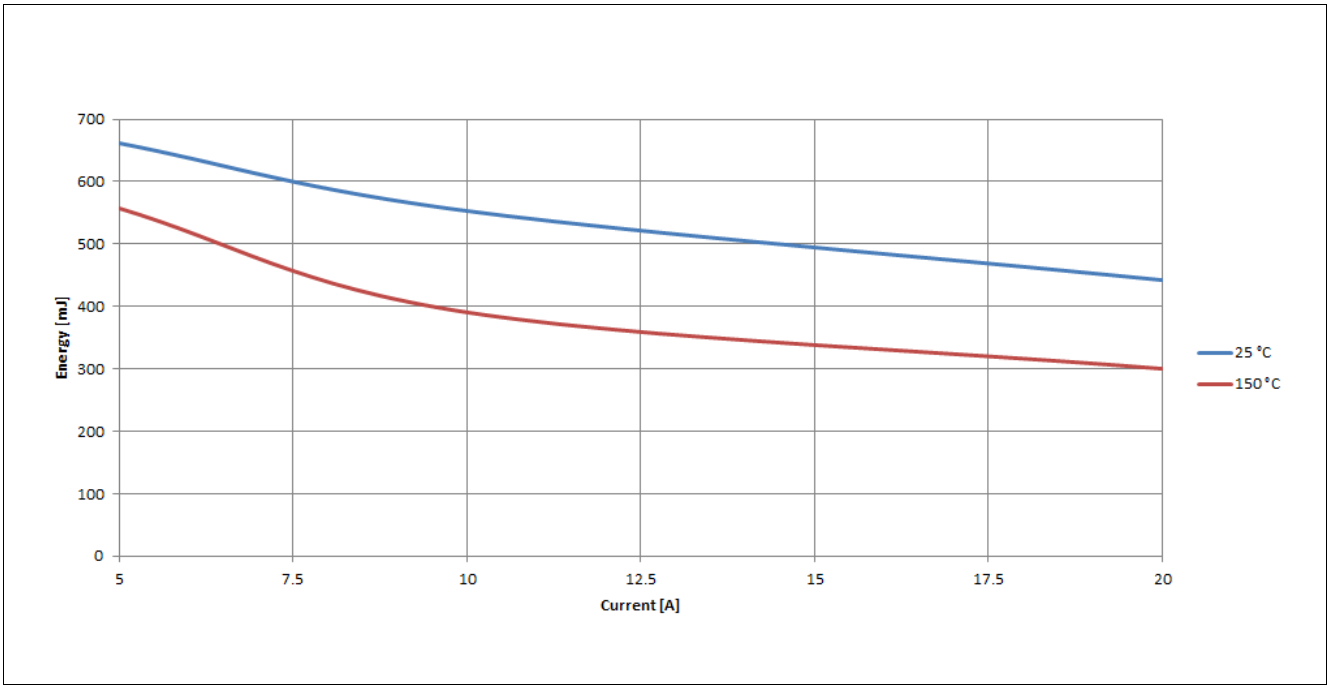

Figure 24 E_{AS} [J] vs. I_L ($0.5*I_{L(NOM)}$, $I_{L(NOM)}$, $2*I_{L(NOM)}$) @ $T_{J(0)}$ = 25°C and 150°C

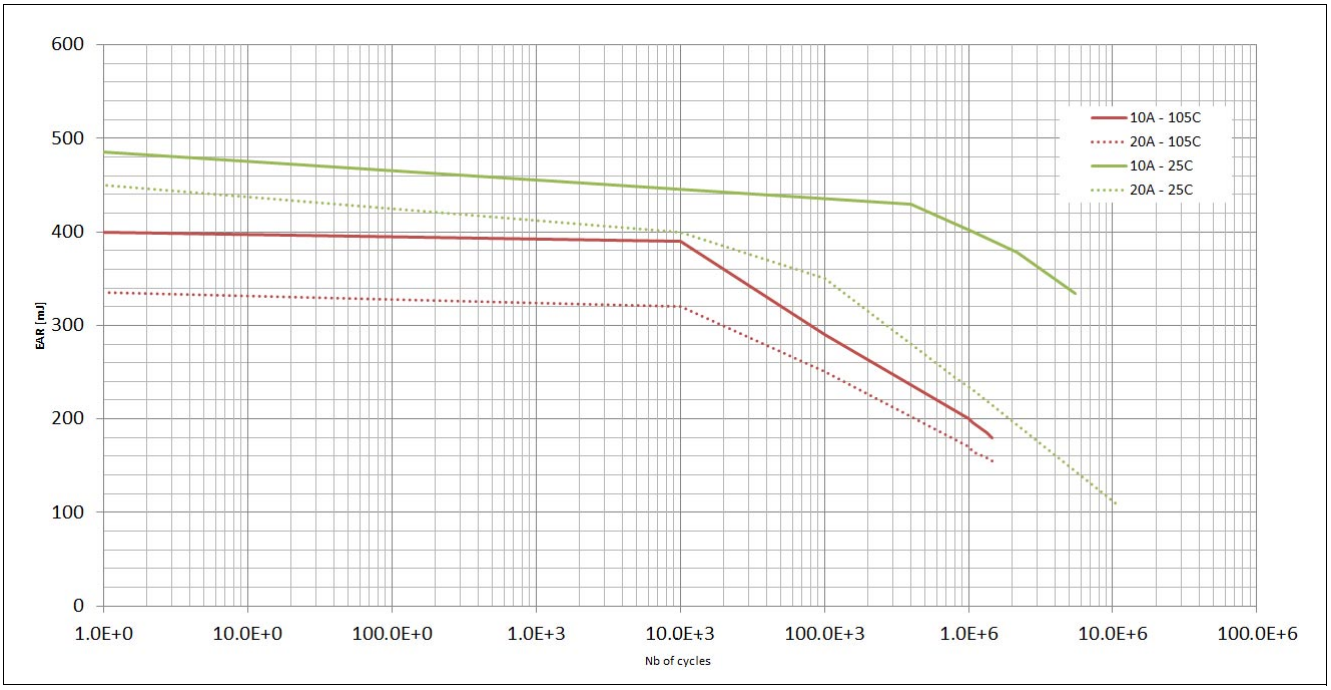

Figure 25 E_{AR} [J] vs. No. cycles; @ $I_{L(NOM)}$, $2*I_{L(NOM)}$; $T_{J(0)}$ = 25, 105°C;

10.2 Dynamic characteristics

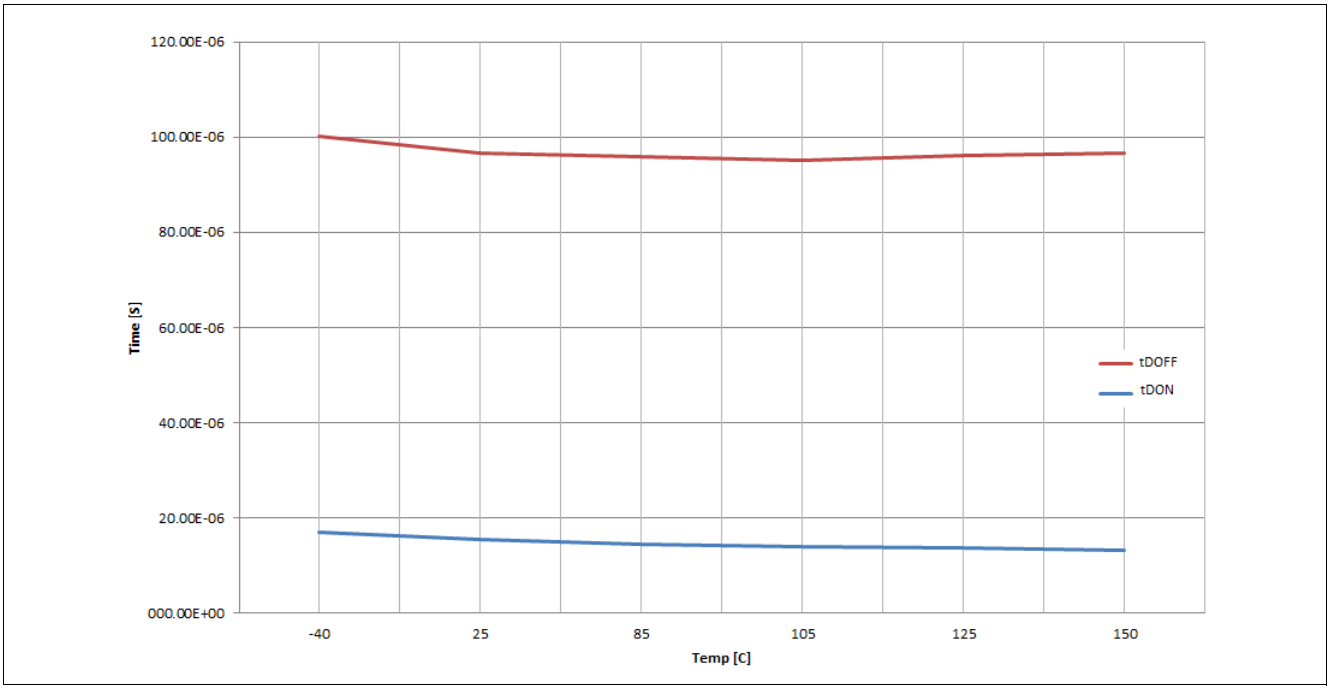

Figure 26 *Typical delay on time, delay off time vs. T (-40..150°C) @* $_J$ V_{DD}=5 V; V_{BAT}=13.5 V

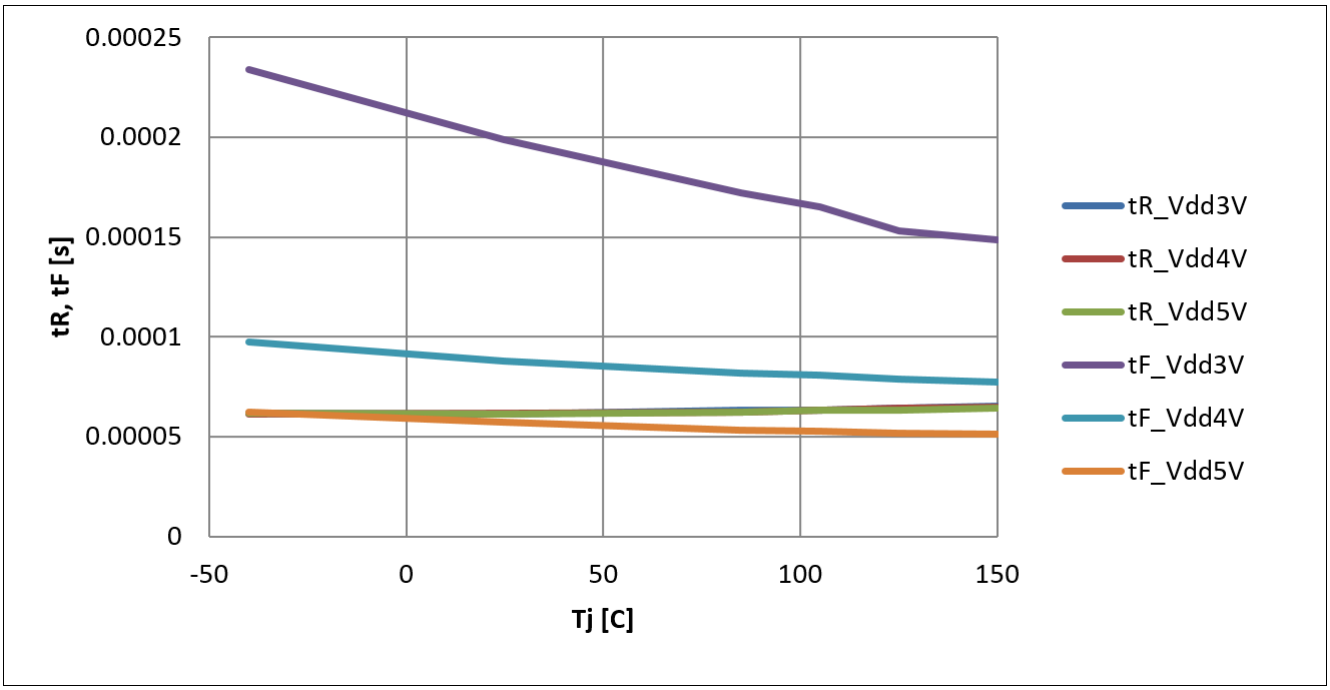

Figure 27 *Typical fall time, rise time vs.* T_J (-40..150°C) @ V_{DD}=5 V; V_{BAT}=13.5 V

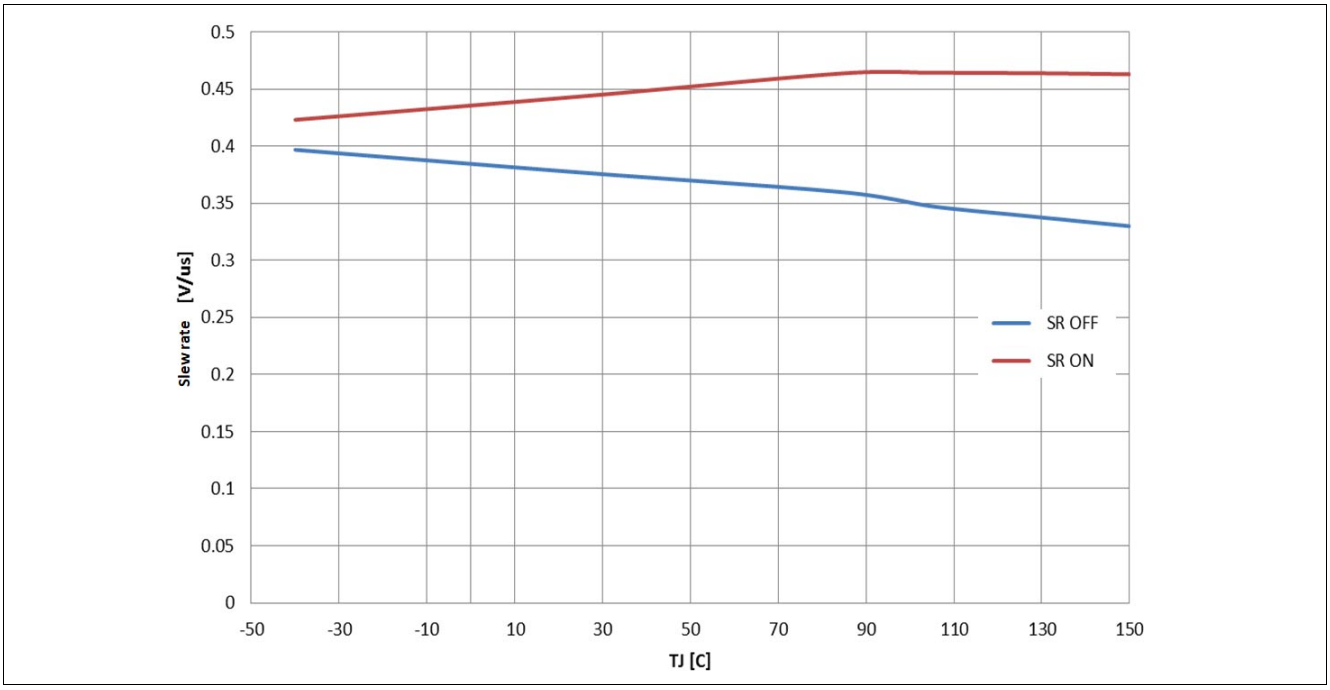

Figure 28 *Typical slew rate (ON&OFF) vs. T_J* (-40..150°C) @ V_{DD}=5 V; V_{BAT}=13.5 V

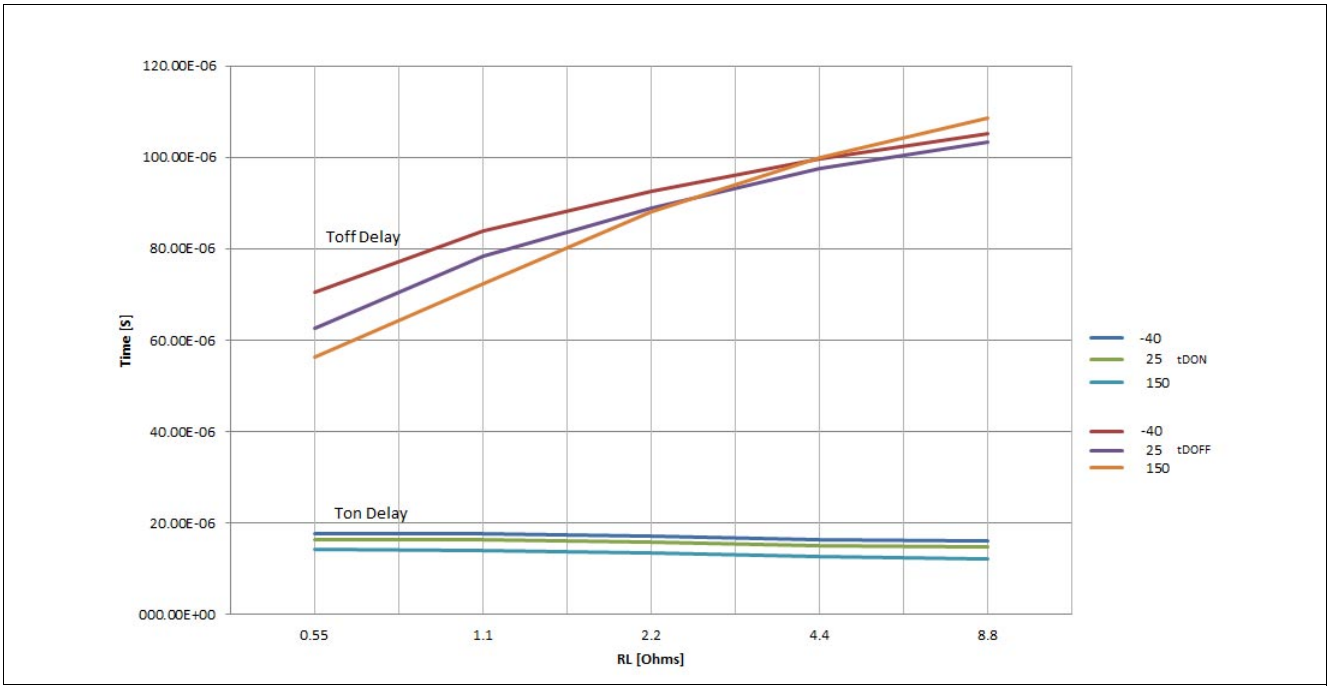

Figure 29 *Typical delay on time, delay off time vs. R_L* @ T_J(-40..150°C); V_{DD}=5 V; V_{BAT}=13.5 V

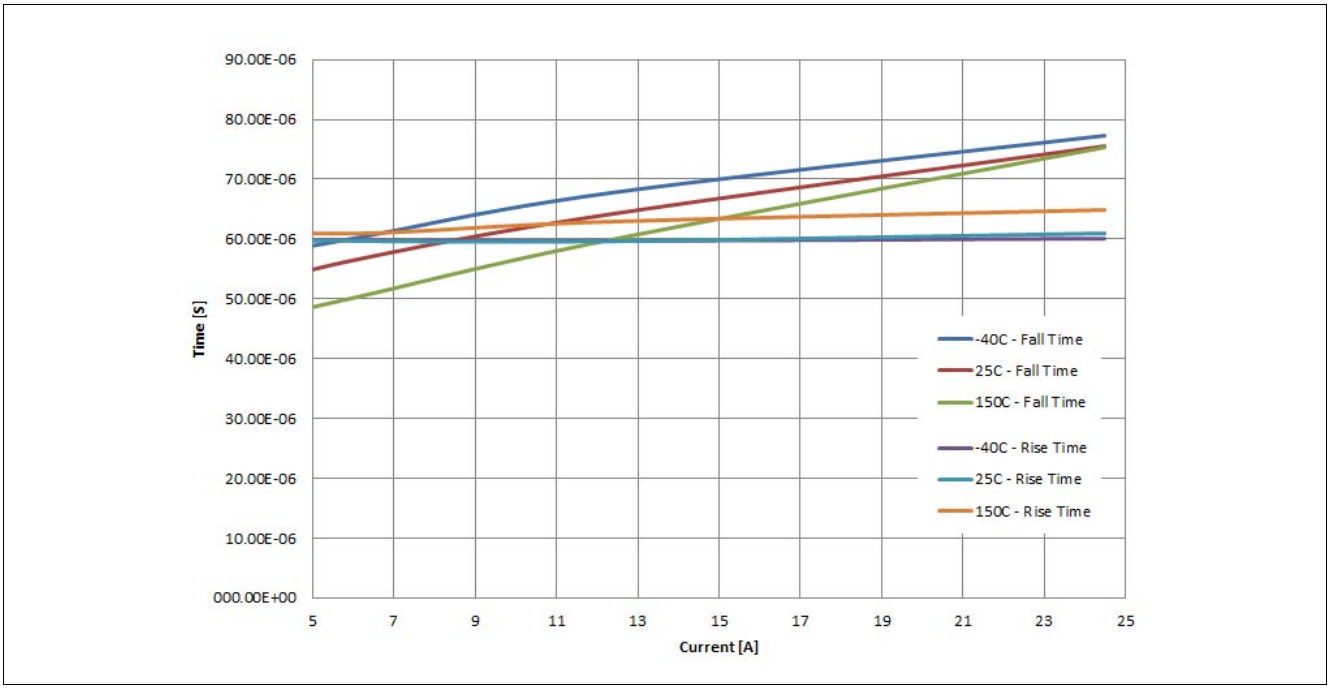

Figure 30 *Typical fall time, rise time vs.* I_L **(0.5A..**$I_{L(LIM)\_MIN}$**) @** T_J **(-40, 25, 150°C);** V_J**=5 V;** V_{BAT}**=13.5 V**

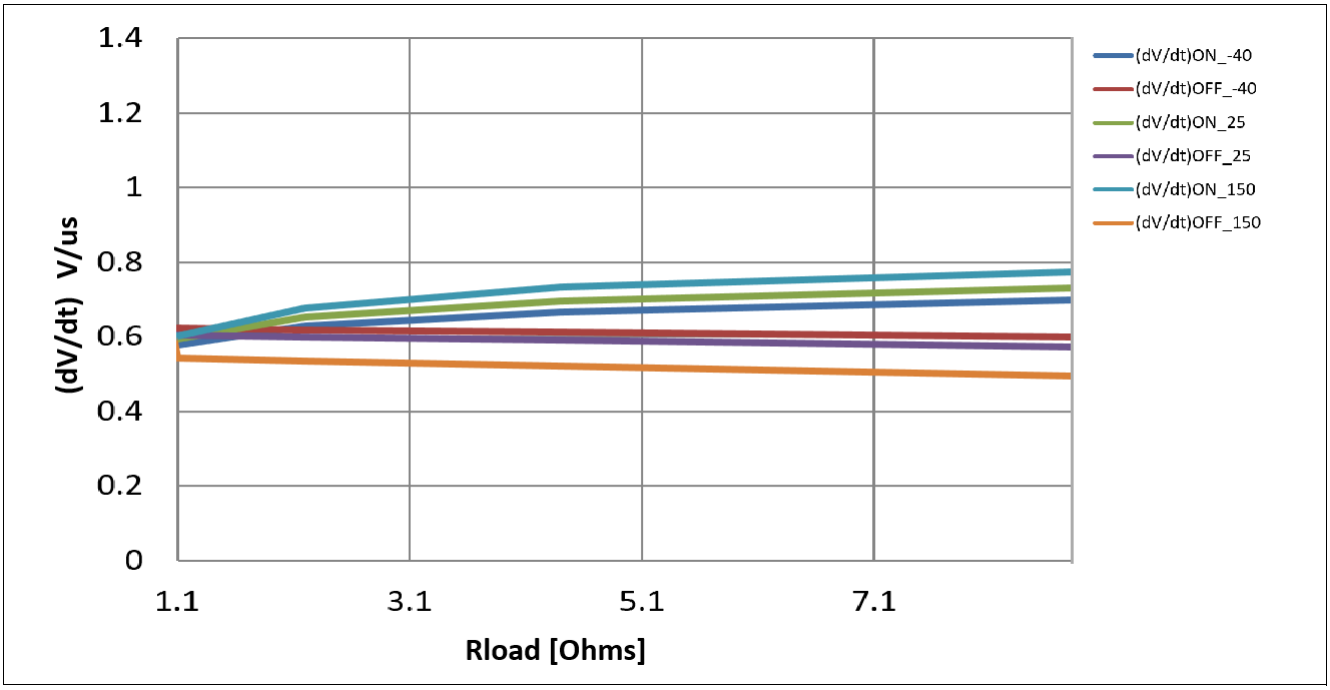

Figure 31 *Typical slew rate (ON&OFF) vs.* R_L **@** T_J**(-40, 25, 150°C);** V_{DD}**=5 V;** V_{BAT}**=13.5 V**

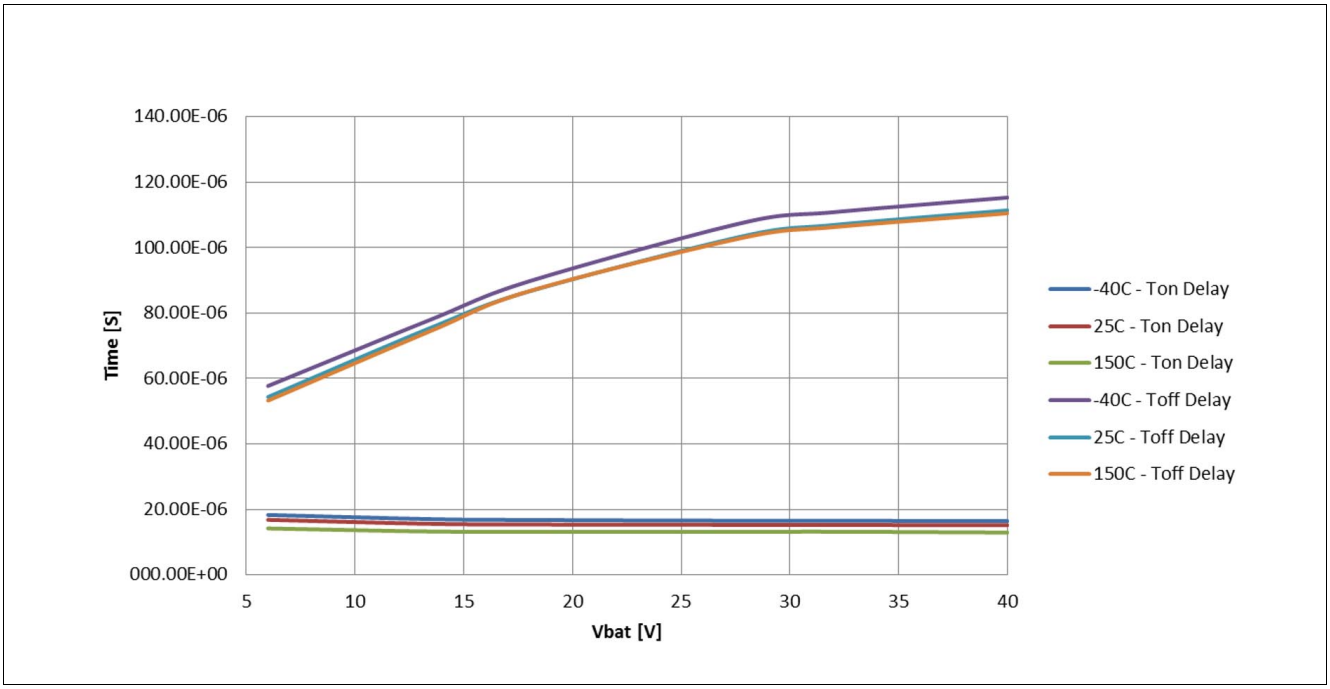

Figure 32 *Typical delay on time, delay off time vs.* V_{BAT} (0..40V) @ T_J (-40, 25, 150°C); V_{DD}=5 V; I_L=$I_{L(NOM)}$

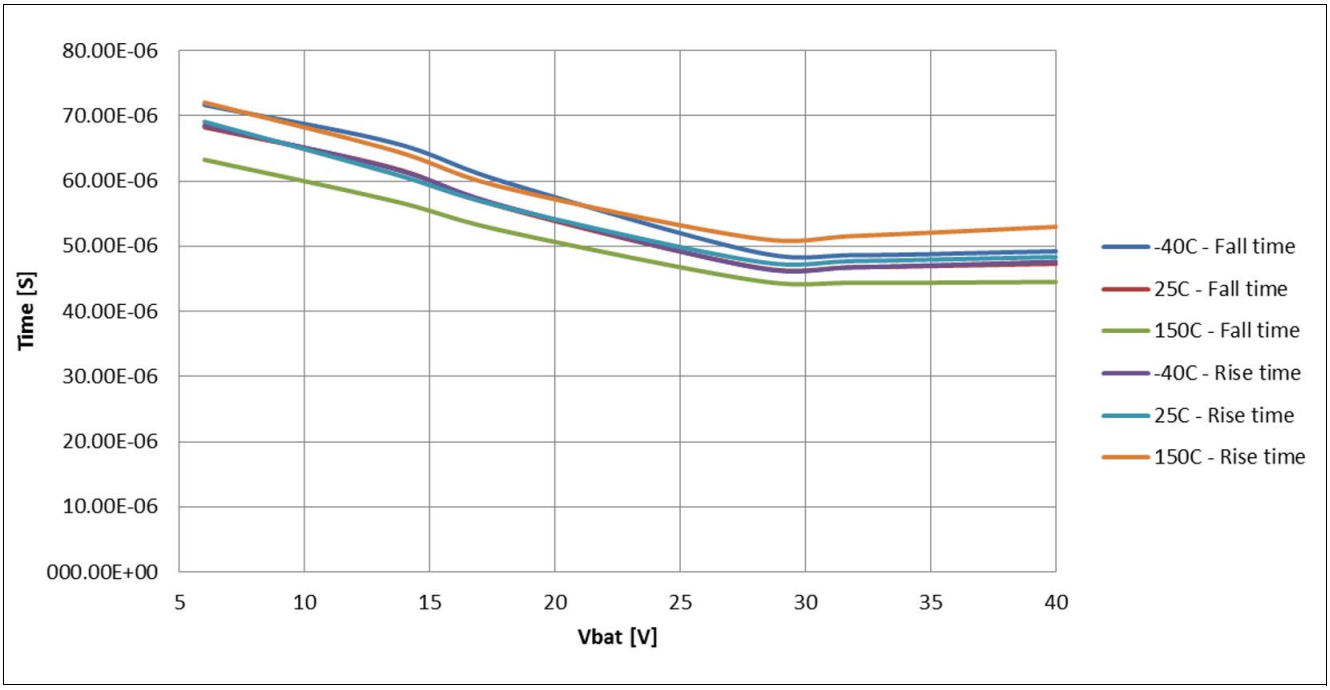

Figure 33 *Typical fall time, rise time vs.* V_{BAT} (0..40V) @ T_J (-40, 25, 150°C); V_{DD}=5 V; I_L=$I_{L(NOM)}$

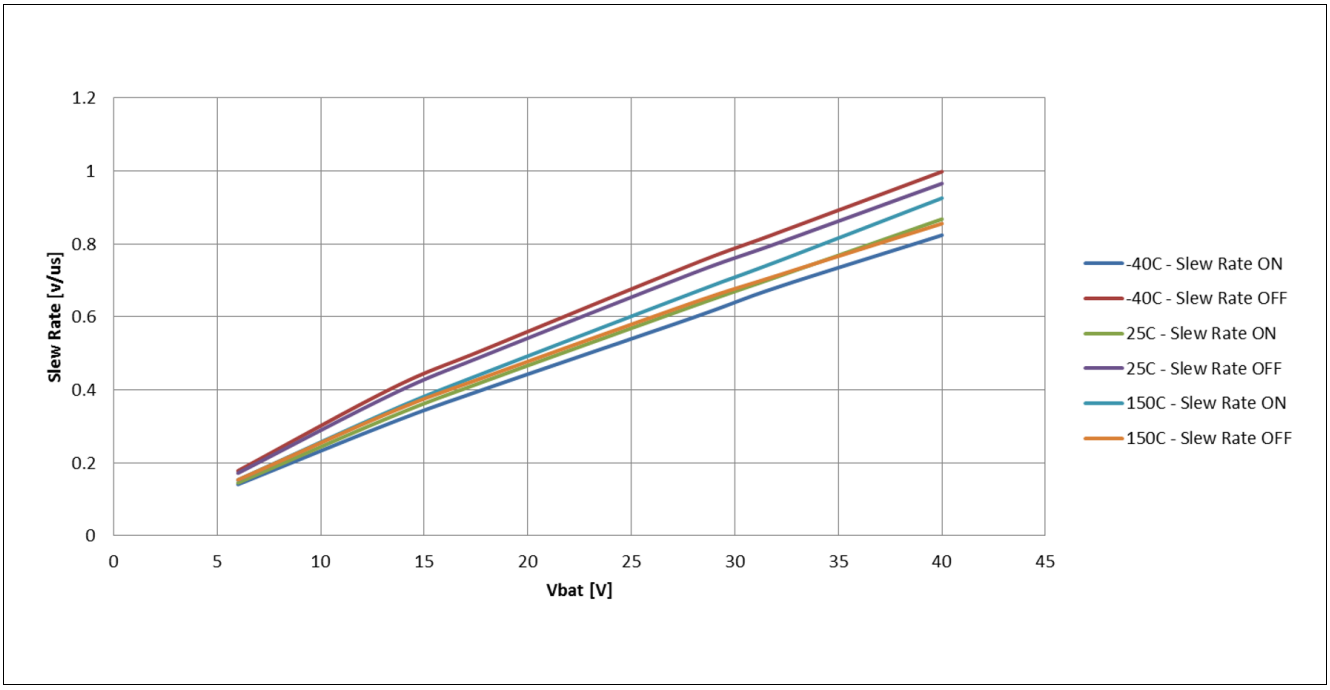

Figure 34 *Typical slew rate (ON&OFF) vs.* V_{BAT} (0..40V) @ T_J (-40, 25, 150°C); V_{DD}=5 V; I_L=$I_{L(NOM)}$

10.3 Supply and Input Stage

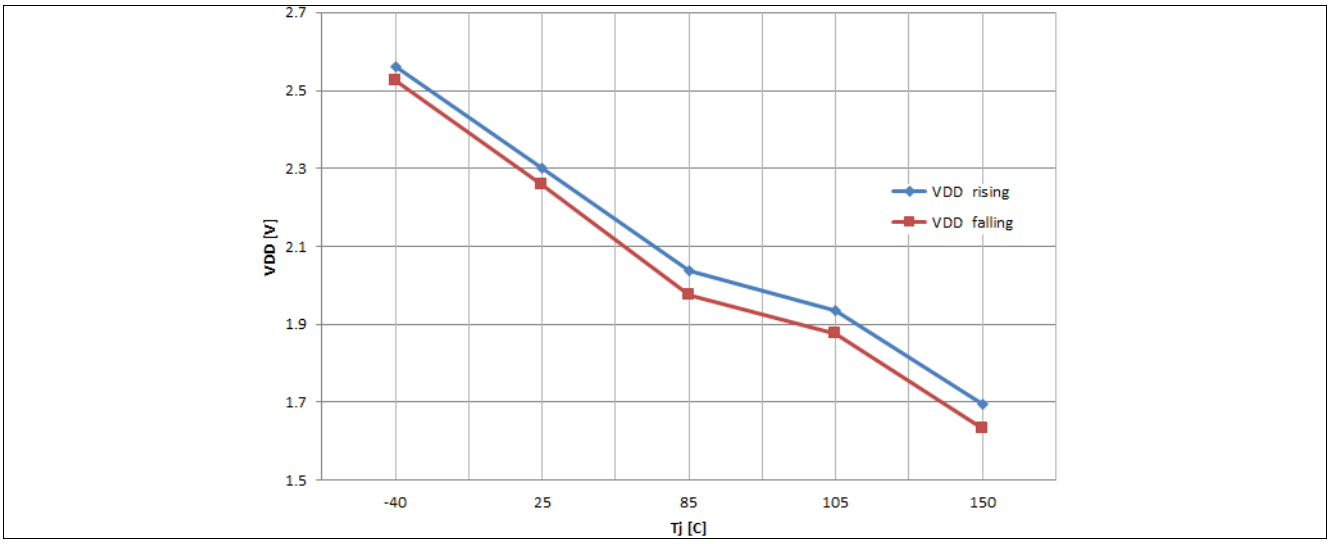

Figure 35 $V_{DD}(U_{V\_on})$, $V_{DD}(U_{V\_off})$ vs. T_J

Characterisation Results

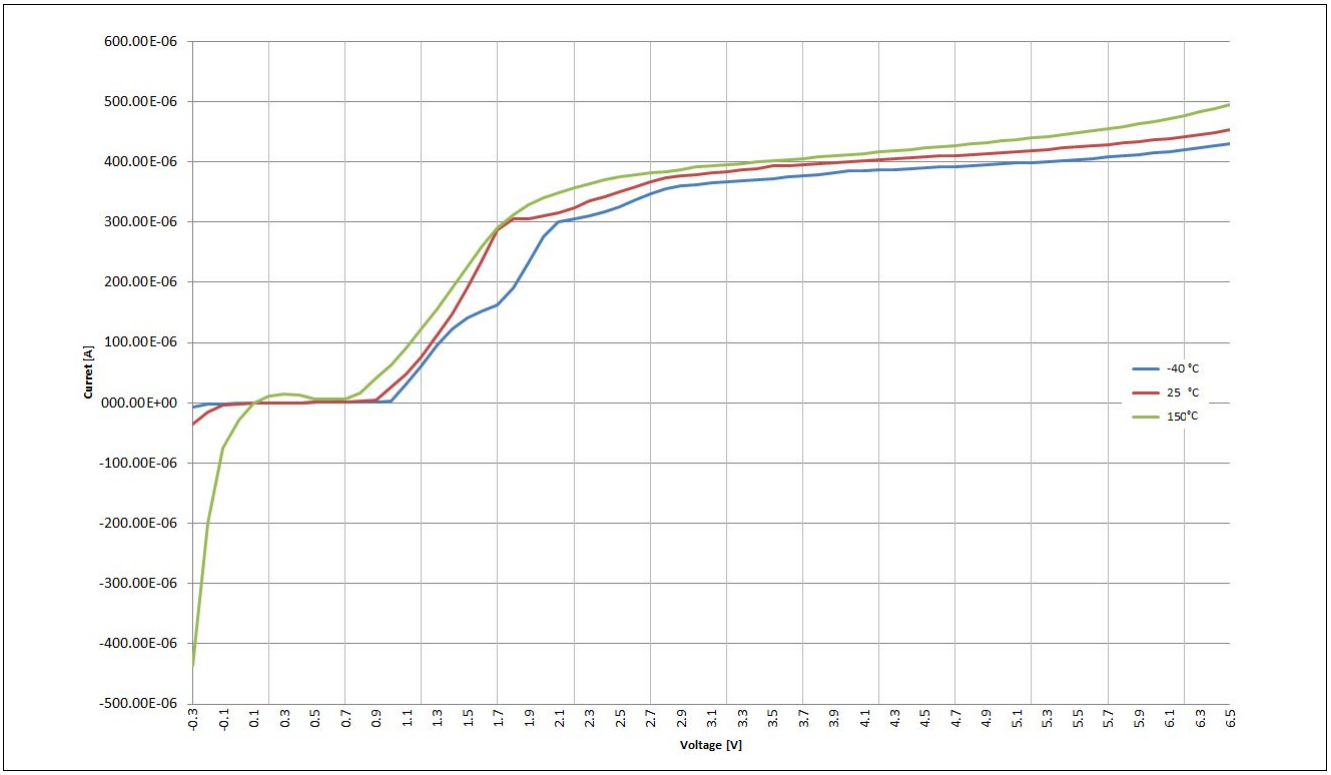

Figure 36 $I_{DD(on)}$ vs. V_{DD} @ T_j = -40, 25, 150°C

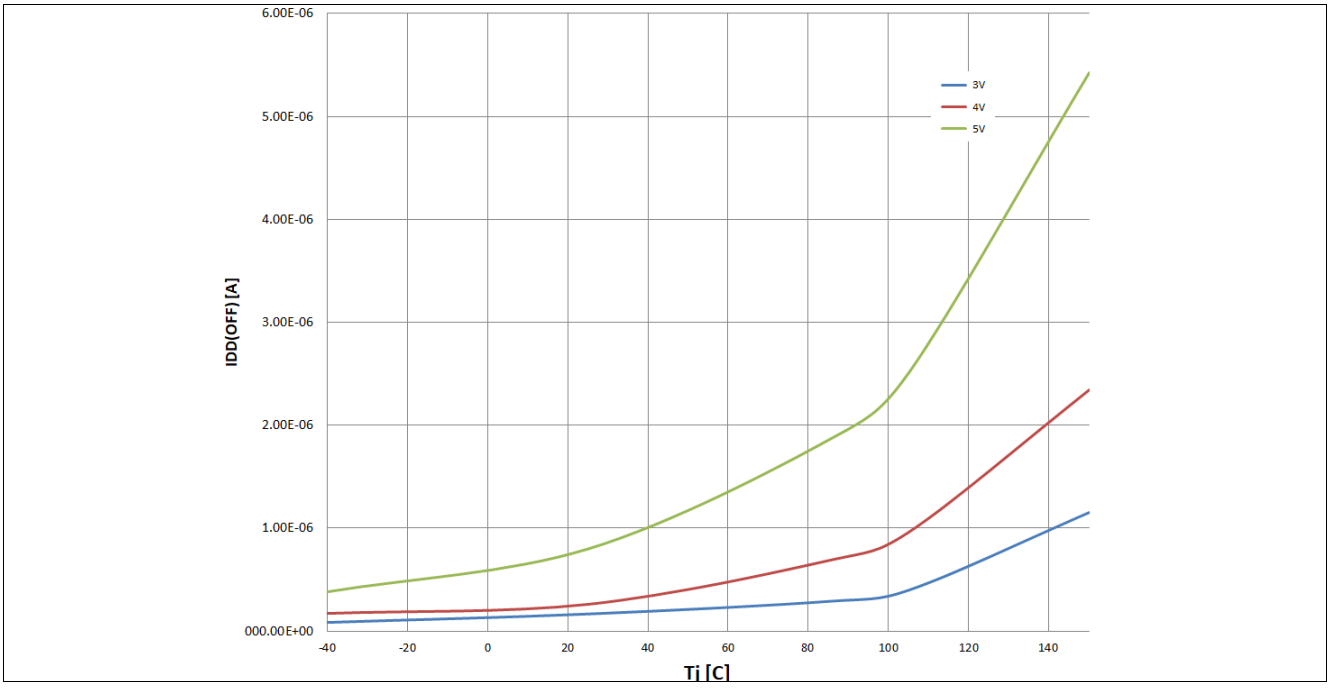

Figure 37 $I_{DD(off)}$ vs. T_j @ V_{DD} = 3, 4, 5 V

Characterisation Results

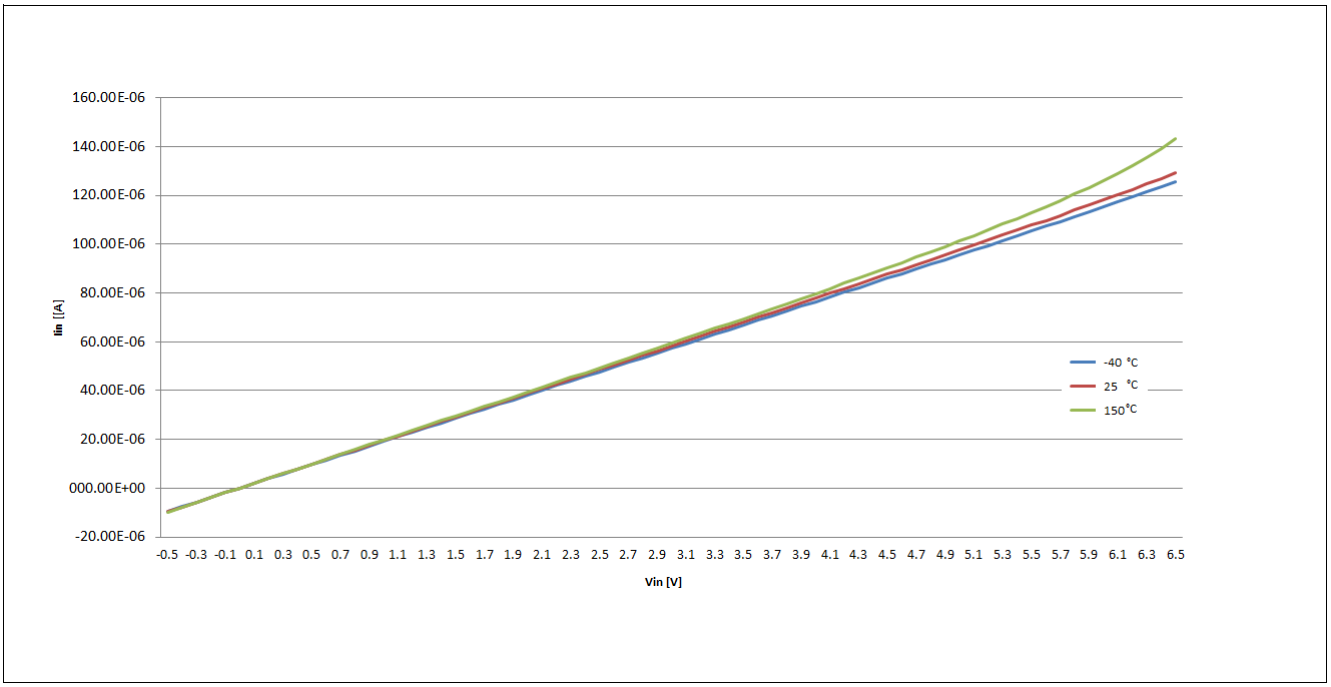

Figure 38 I_{IN} vs. V_{in} @ T_j = -40, 25, 150°C

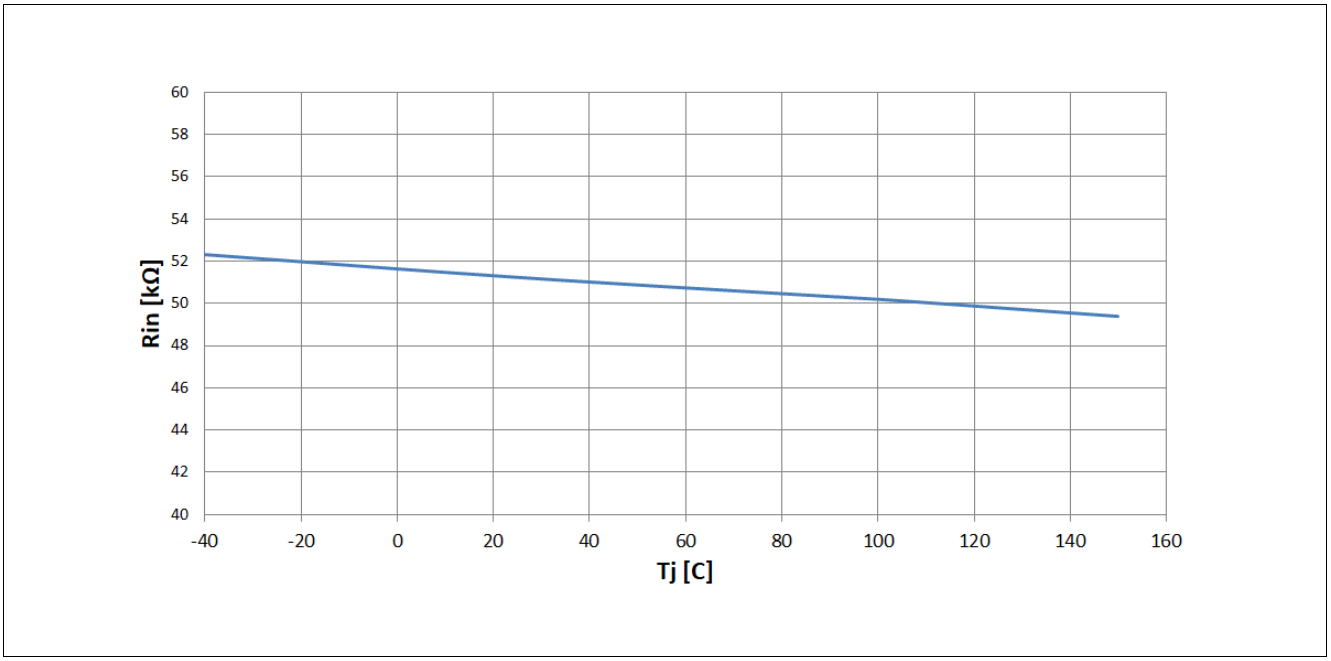

Figure 39 $R_{IN(GND)}$ vs. T_j

Characterisation Results

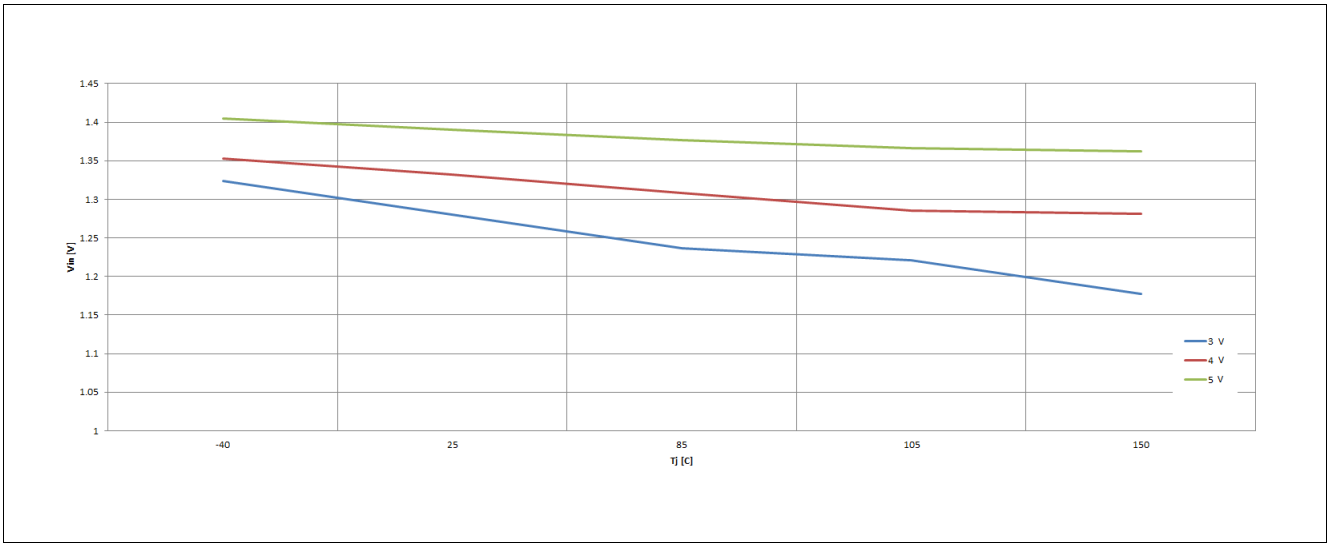

Figure 40 $V_{IN(L)}$ vs. T_j @ V_{DD} = 3, 4, 5 V

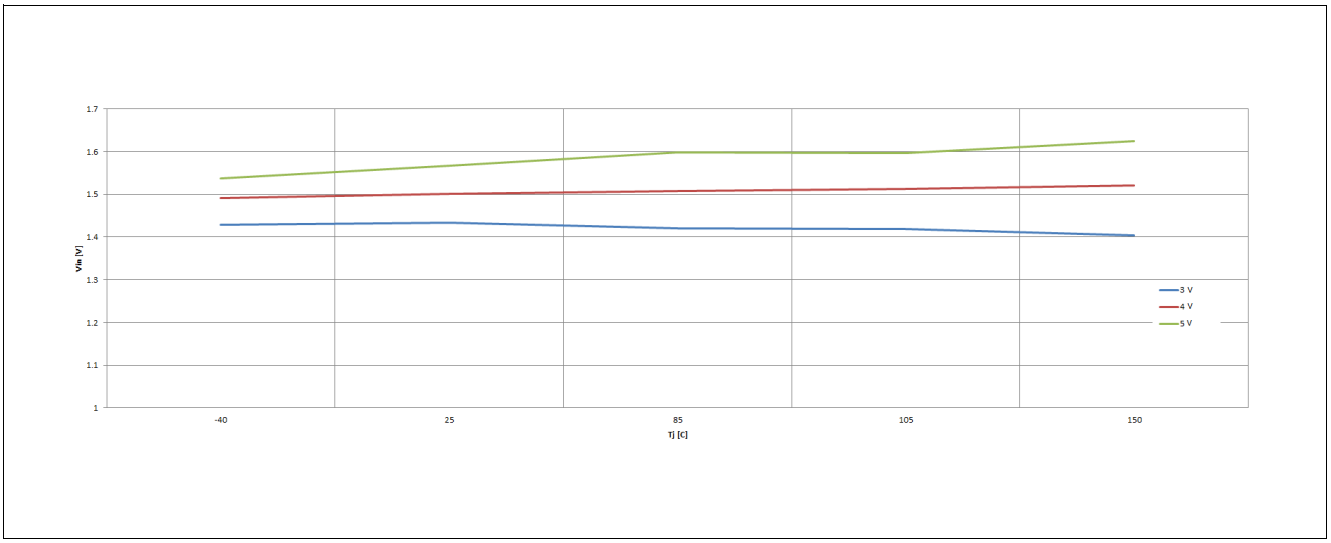

Figure 41 $V_{IN(H)}$ vs. T_j @ V_{DD} = 3, 4, 5 V

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Application Diagram

An application example with the BTS3011TE is shown below.

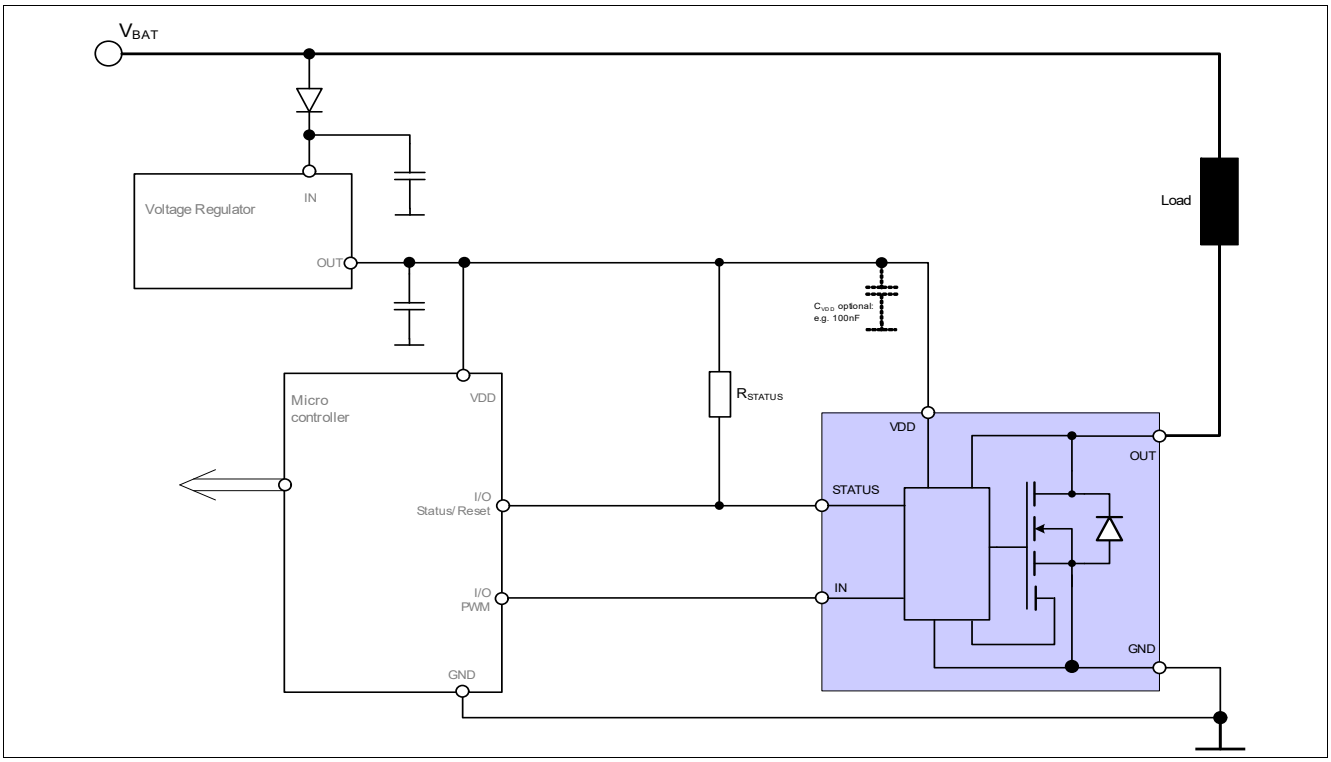

Figure 42 Simplified application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 10 Recommended external components

Reference	Value	Description
R_{STATUS}	10 kΩ	Pull-up resistor for STATUS pin
C_{VDD}	100 nF	Supply pin capacitor for fast supply current transients

11.1 Design and Layout Recommendations/Considerations

As consequence of the fast switching times for high currents, special care has to be taken with the PCB layout. Stray inductances have to be minimized.

12 Package Outlines BTS3011TE

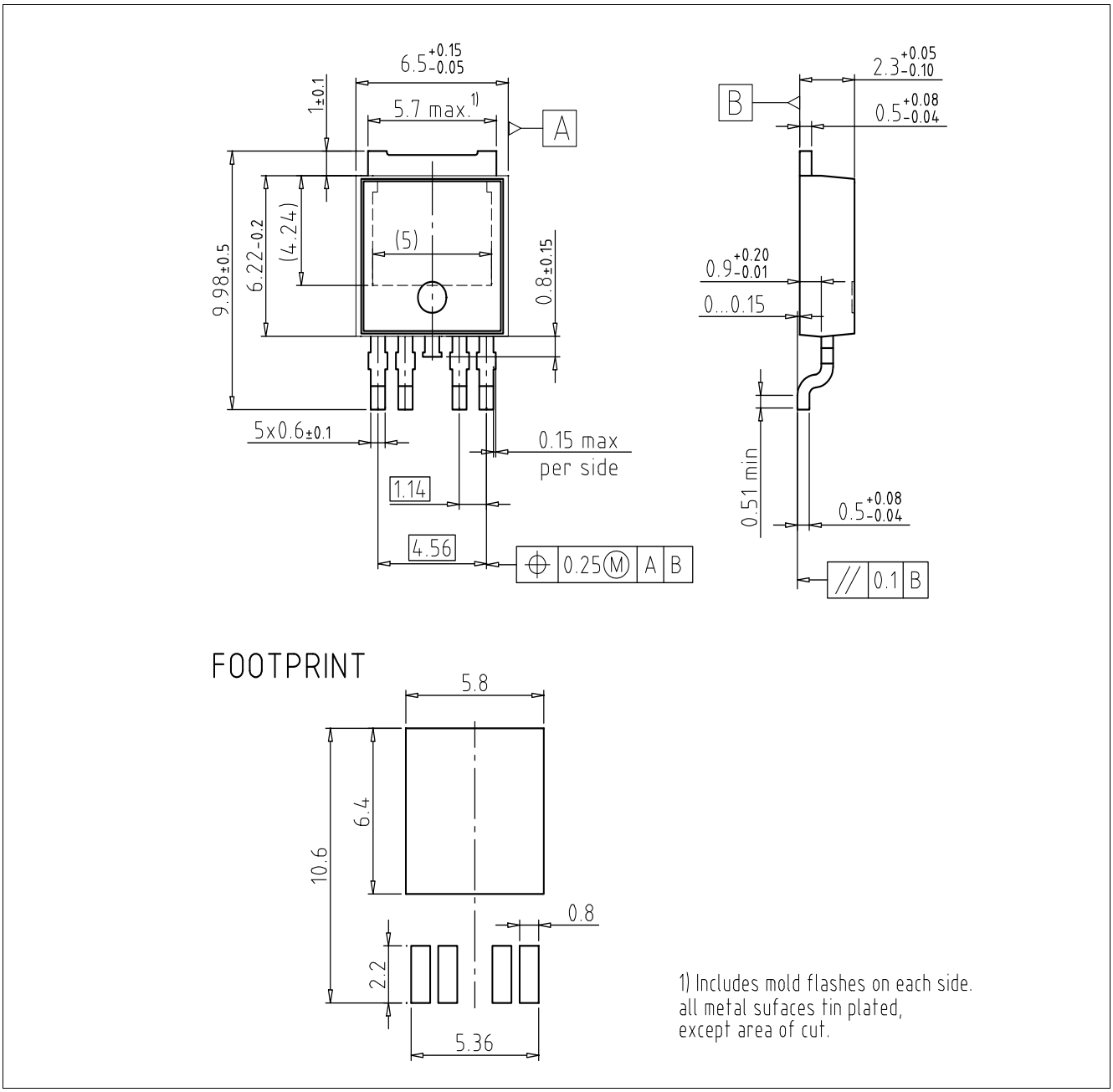

Figure 43 PG-TO252-5

Transistor Outline Package

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

13 Revision History

Revision	Date	Changes
Rev. 1.0	2018-07-19	Datasheet released

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Edition 2018-07-19
Published by
Infineon Technologies AG
81726 Munich, Germany

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