

## HIGH SIDE & DUAL LOW SIDE DRIVER IC

### Features

- 2 low side output channels sharing common ground
- 1 high side output channel
- CMOS Schmitt trigger inputs with pull down resistor
- Under voltage lockout on all channels
- 5 V compatible logic level Inputs
- Immune to  $-V_s$  spike and tolerant to  $dV_s/dt$  &  $dV_{ss}/dt$
- Shoot through prevention logic

### Descriptions

The IRS21953 contains 2 low side outputs sharing common ground and 1 high side output. Low side drivers can tolerate up to -600 V below input signal (VSS: input supply return). High side driver can tolerate up to 600 V above low side ground (COM: low side supply return). The IRS21953 has better propagation delay and thermal characteristics compared to a photo-coupler driver. The logic inputs are compatible with standard CMOS or LSTTL output. Proprietary HVIC and latch-up immune CMOS technologies enable ruggedized monolithic construction.

### Product Summary

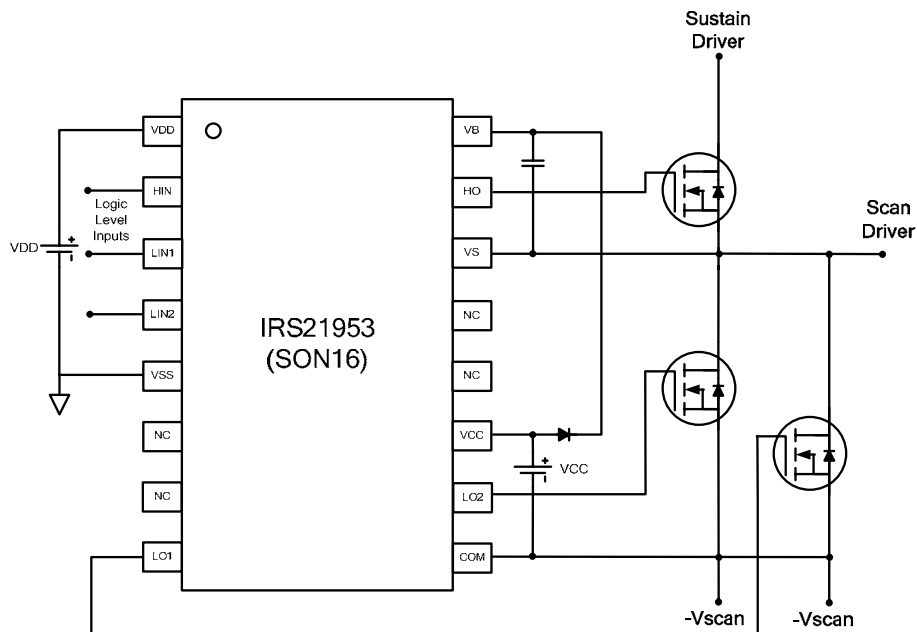
|                                      |               |
|--------------------------------------|---------------|
| $V_{\text{OFFSET}}$ (low side)       | -600 V (VSS)  |
| $V_{\text{OFFSET}}$ (high side)      | 600 V (COM)   |
| $V_{\text{OUT}}$                     | 10 V to 20 V  |
| $t_{\text{on}}/t_{\text{off}}$ (typ) | 380 ns/380 ns |
| $I_{\text{O+/-}}$                    | 0.5 A/0.5 A   |

### Package



16-Lead SOIC (narrow body)

### Typical Connection Diagram



**Absolute Maximum Ratings**

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

| Symbol              | Definition                                              | Min     | Max     | Units |
|---------------------|---------------------------------------------------------|---------|---------|-------|
| HIN<br>LIN1<br>LIN2 | Floating logic level Input voltage                      | VSS-0.3 | VDD+0.3 | V     |
| VDD                 | Floating logic input supply voltage                     | -0.3    | 625     |       |
| VSS                 | Floating logic input supply return voltage              | VDD-25  | VDD+0.3 |       |
| VB                  | High side floating well supply voltage                  | -0.3    | 625     |       |
| VS                  | High side floating well supply return voltage           | VB-25   | VB+0.3  |       |
| HO                  | High side floating gate drive output voltage            | VS-0.3  | VB+0.3  |       |
| VCC                 | Low side supply voltage                                 | -0.3    | 25      |       |
| LO1<br>LO2          | Low side output voltage                                 | -0.3    | VCC+0.3 |       |
| dVS/dt              | Allowable VS offset transient relative to earth ground  | -       | 50      | V/ns  |
| dVSS/dt             | Allowable VSS offset transient relative to earth ground | -       | 50      |       |
| P <sub>D</sub>      | Package power dissipation @ T <sub>A</sub> ≤ +25 °C     | -       | 1       | W     |
| R <sub>θJA</sub>    | Thermal resistance, junction to ambient                 | -       | 100     | °C/W  |
| T <sub>J</sub>      | Junction temperature                                    | -55     | 150     | °C    |
| T <sub>S</sub>      | Storage temperature                                     | -55     | 150     |       |
| T <sub>L</sub>      | Lead temperature (soldering, 10 seconds)                | -       | 300     |       |

**Recommended Operating Conditions**

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM.

| Symbol              | Definition                                    | Min    | Max    | Units |
|---------------------|-----------------------------------------------|--------|--------|-------|
| HIN<br>LIN1<br>LIN2 | Floating logic level input voltage            | VSS    | VDD    | V     |
| VDD                 | Floating logic input supply voltage           | VSS+10 | VSS+20 |       |
| VSS                 | Floating logic input supply return voltage    | -5     | 600    |       |
| VB                  | High side floating well supply voltage        | VS+10  | VS+20  |       |
| VS                  | High side floating well supply return voltage | -5     | 600    |       |
| HO                  | High side floating gate drive output voltage  | VS     | VB     |       |
| VCC                 | Low side supply voltage                       | 10     | 20     |       |
| LO1<br>LO2          | Low side output voltage                       | 0      | VCC    |       |
| T <sub>A</sub>      | Ambient temperature                           | -40    | 125    | °C    |

Note 1: Logic operation for V<sub>S</sub> of -5 V to 600 V. Logic state held for V<sub>S</sub> of -5 V to -V<sub>BS</sub>. (Please refer to Design Tip DT97-3 for more details).

**Static Electrical Characteristics**

(VB-VS)=15 V. The  $V_{IN}$ ,  $V_{IN,TH}$ ,  $V_{BSUV}$ ,  $V_O$ ,  $I_O$  and  $I_{IN}$  parameters are referenced to  $V_S$ .  $T_A = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

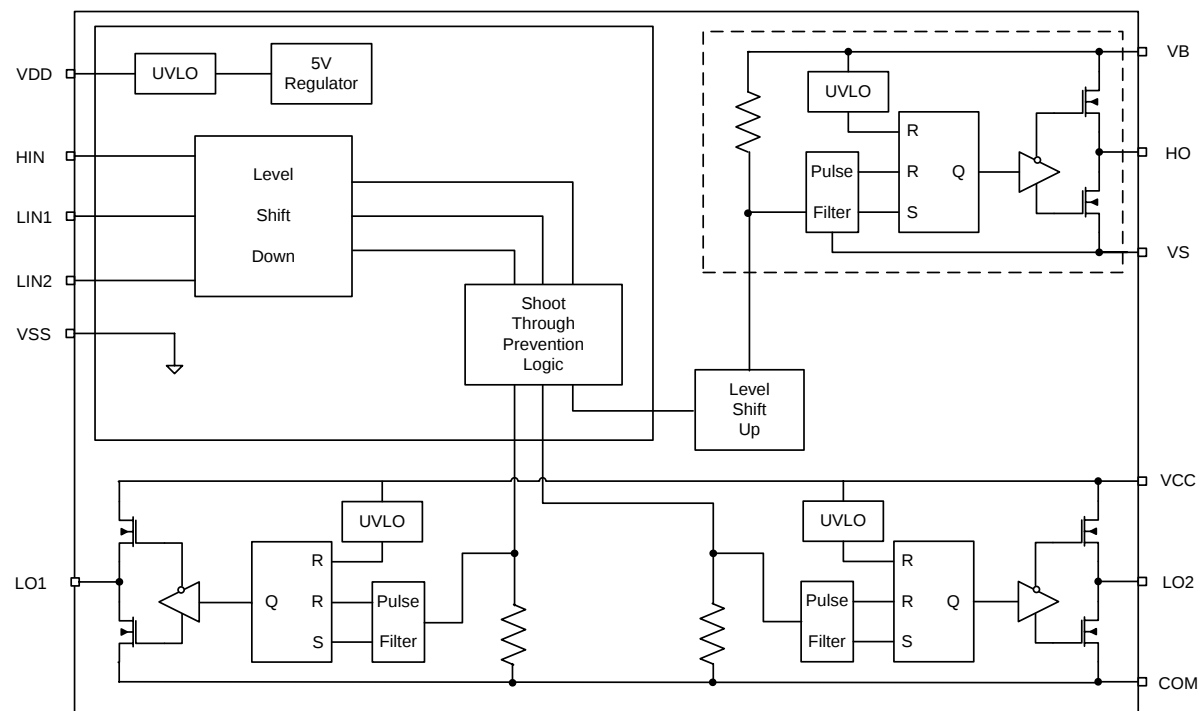
| Symbol                     | Definition                                                      | Min | Typ | Max | Units         | Test Conditions                                                              |
|----------------------------|-----------------------------------------------------------------|-----|-----|-----|---------------|------------------------------------------------------------------------------|
| $V_{CCUV+}$                | $V_{CC}$ supply undervoltage positive going threshold           | 7.5 | 8.6 | 9.7 | V             |                                                                              |
| $V_{CCUV-}$                | $V_{CC}$ supply undervoltage negative going threshold           | 7.0 | 8.2 | 9.4 |               |                                                                              |
| $V_{BSUV+}$                | $V_{BS}$ supply undervoltage positive going threshold           | 7.5 | 8.6 | 9.7 |               |                                                                              |
| $V_{BSUV-}$                | $V_{BS}$ supply undervoltage negative going threshold           | 7.0 | 8.2 | 9.4 |               |                                                                              |
| $V_{DDUV+}$                | $V_{DD}$ supply undervoltage positive going threshold           | 7.5 | 8.6 | 9.7 |               |                                                                              |
| $V_{DDUV-}$                | $V_{DD}$ supply undervoltage negative going threshold           | 7.0 | 8.2 | 9.4 |               |                                                                              |
| $I_{LKVCC}$<br>$I_{LKVBS}$ | Offset supply leakage current – both input well and output well | --- | --- | 50  | $\mu\text{A}$ | $V_B = V_S = 600\text{ V}$<br>$V_{CC} = V_{COM} = 600\text{ V}$              |
| $I_{QBS}$                  | Quiescent $V_{BS}$ supply current                               | --- | 70  | 140 |               | $V_{IN} = 0\text{ V or } 5\text{ V}$                                         |
| $I_{QDD}$                  | Quiescent $V_{DD}$ supply current                               | --- | 100 | 200 |               |                                                                              |
| $I_{QCC}$                  | Quiescent $V_{CC}$ supply current                               | --- | 130 | 260 |               |                                                                              |
| $V_{IH}$                   | Logic “1” input voltage                                         | 3.5 | --- | --- | V             |                                                                              |
| $V_{IL}$                   | Logic “0” input voltage                                         | --- | --- | 0.6 |               |                                                                              |
| $V_{OH}$                   | High level output voltage, $V_{BIAS}-V_O$                       | --- | --- | 0.1 |               | $I_O = 0\text{ A}$                                                           |
| $V_{OL}$                   | Low level output voltage, $V_O$                                 | --- | --- | 0.1 |               | $I_O = 0\text{ A}$                                                           |
| $I_{IN+}$                  | Logic “1” input bias current                                    | --- | 2   | 10  | $\mu\text{A}$ | $V_{IN} = 5\text{ V}$                                                        |
| $I_{IN-}$                  | Logic “0” input bias current                                    | --- | --- | 5   |               | $V_{IN} = 0\text{ V}$                                                        |
| $I_{O+}$                   | Output high short circuit pulsed current                        | --- | 0.5 | --- | A             | $V_O = 0\text{ V}, V_{IN} = 0\text{ V},$<br>$PW \leq 10\text{ }\mu\text{s}$  |
| $I_{O-}$                   | Output low short circuit pulsed current                         | --- | 0.5 | --- |               | $V_O = 15\text{ V}, V_{IN} = 5\text{ V},$<br>$PW \leq 10\text{ }\mu\text{s}$ |

**Dynamic Electrical Characteristics (All values are target data)**

(VB-VS)= 15 V.  $C_L = 1000$  pF unless otherwise specified. All parameters are reference to COM.  $T_A = 25$  °C unless otherwise specified.

| Symbol    | Definition                                      | Min | Typ | Max | Units | Test Conditions             |
|-----------|-------------------------------------------------|-----|-----|-----|-------|-----------------------------|
| $t_{on}$  | Turn-on propagation delay of high and low side  | --- | 380 | --- | ns    | $V_{SS}=200$ V, $V_S=0$ V   |
| $t_{off}$ | Turn-off propagation delay of high and low side | --- | 380 | --- |       | $V_{SS}=200$ V, $V_S=400$ V |
| $t_r$     | Turn-on rise time of high and low side          | --- | 25  | 70  |       | $V_{SS}=200$ V, $V_S=0$ V   |
| $t_f$     | Turn-off fall time of high and low side         | --- | 25  | 70  |       | $V_{SS}=200$ V, $V_S=400$ V |
| MT_on     | Turn on propagation delay matching              | --- | --- | 50  |       | $V_{SS}=200$ V, $V_S=0$ V   |
| MT_off    | Turn off propagation delay matching             | --- | --- | 50  |       | $V_{SS}=200$ V, $V_S=400$ V |

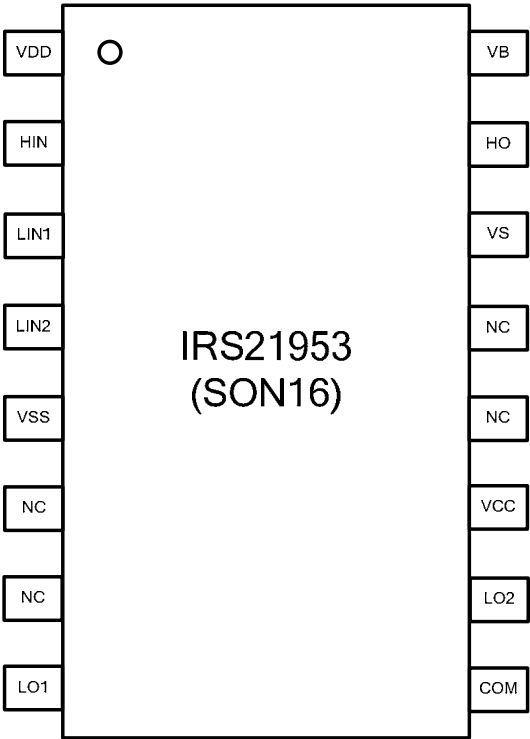
## Functional Block Diagram



**Lead Definitions**

| Symbol     | Description                           |
|------------|---------------------------------------|
| VDD        | Input logic supply voltage            |
| HIN        | Logic input for high side gate driver |
| LIN1, LIN2 | Logic inputs for low side gate driver |
| VSS        | Input logic supply return             |
| LO1, LO2   | Low side outputs                      |
| VCC        | Low side supply voltage               |
| COM        | Low side supply return                |
| HO         | High side output                      |
| VB         | High side floating supply voltage     |
| VS         | High side floating supply return      |

**Lead Assignments**



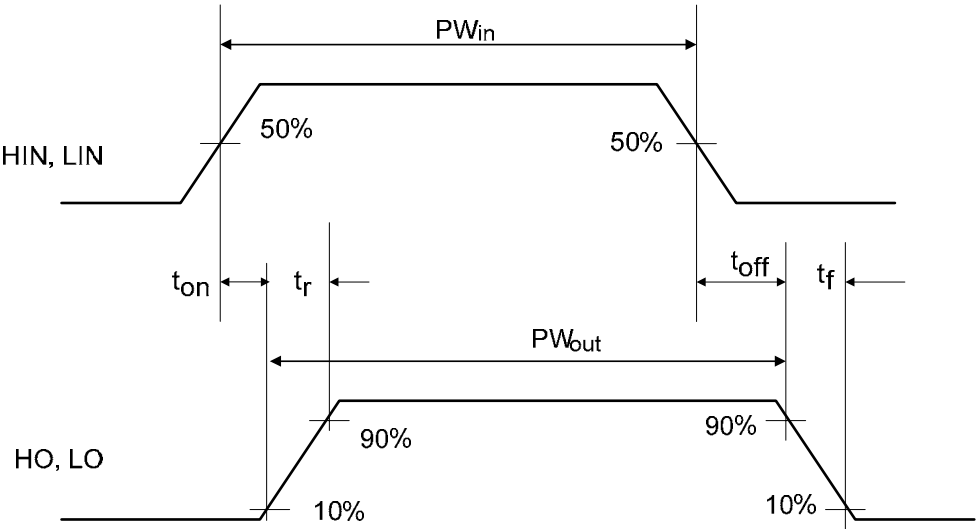
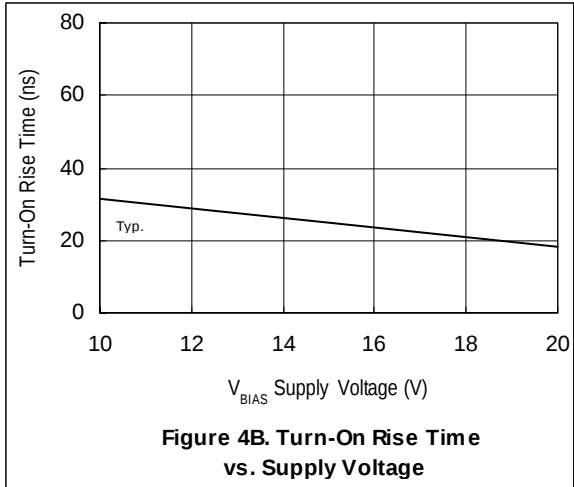
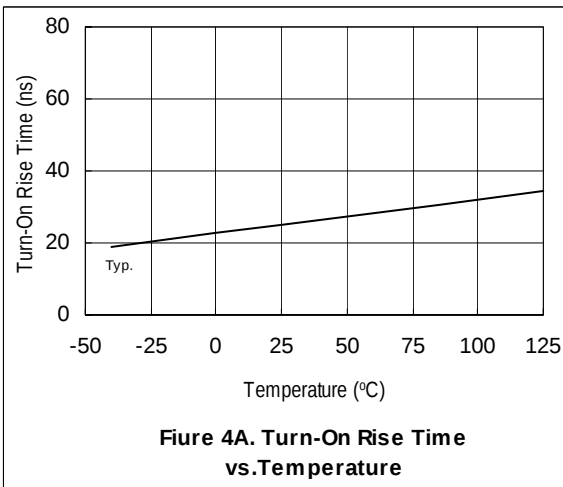
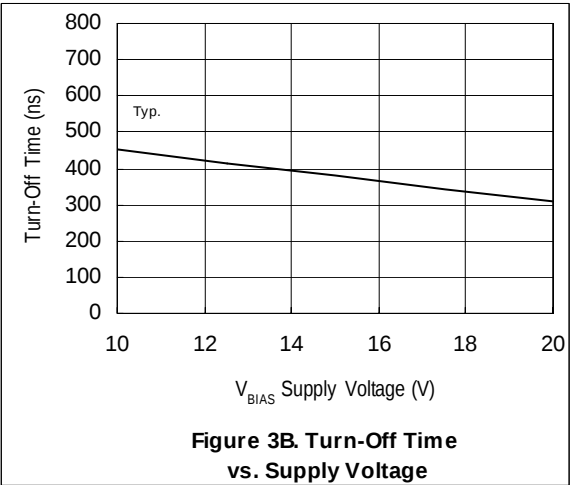
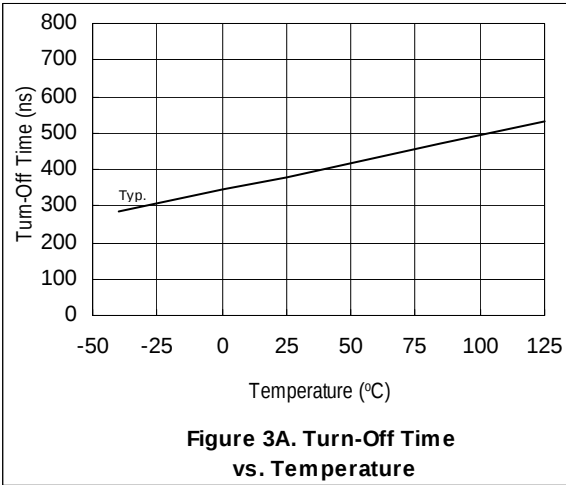
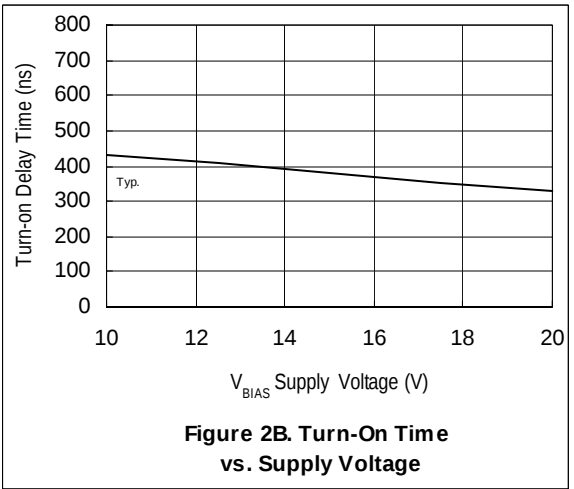
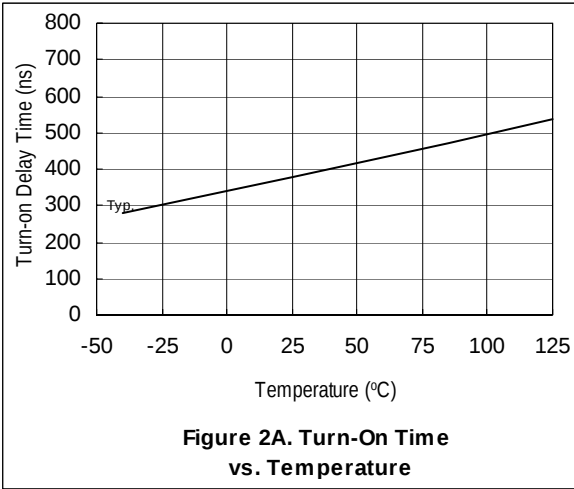
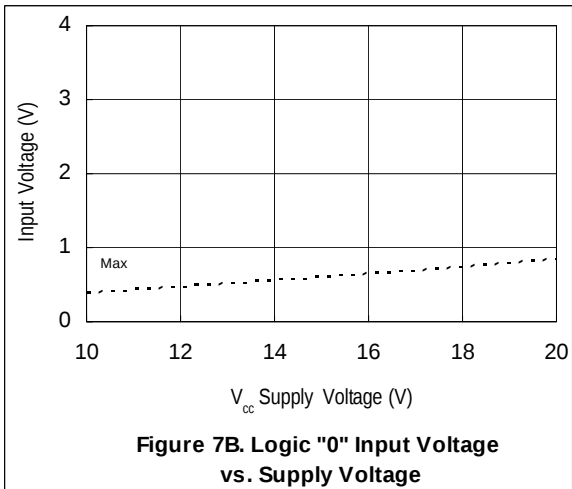
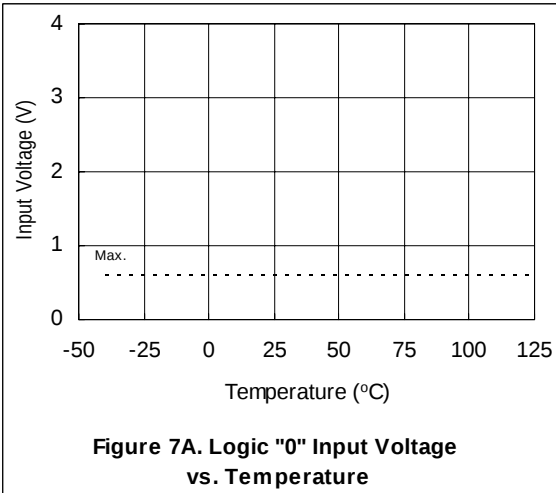
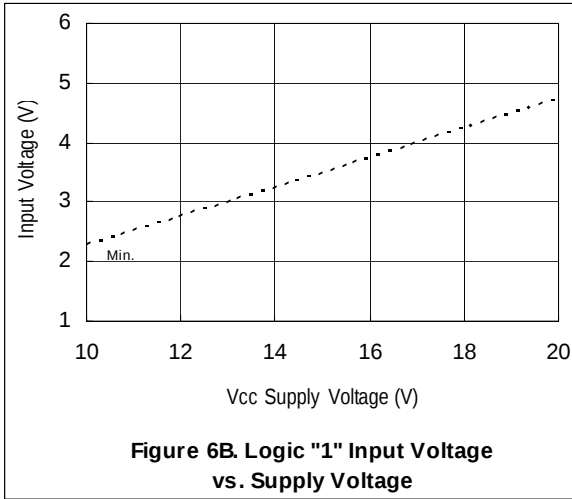
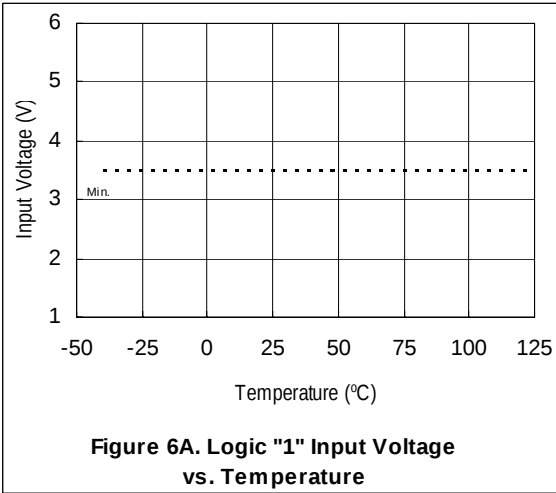
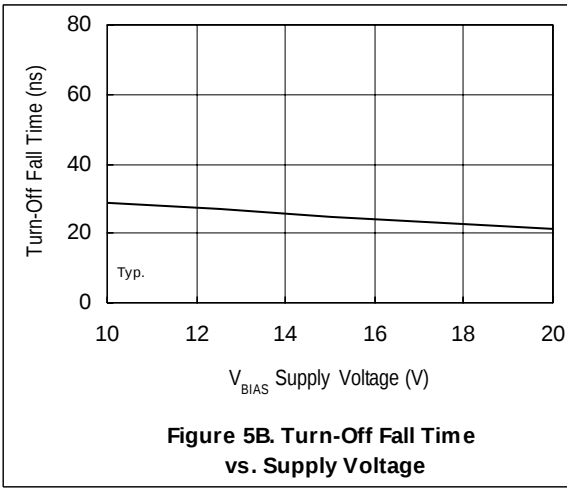
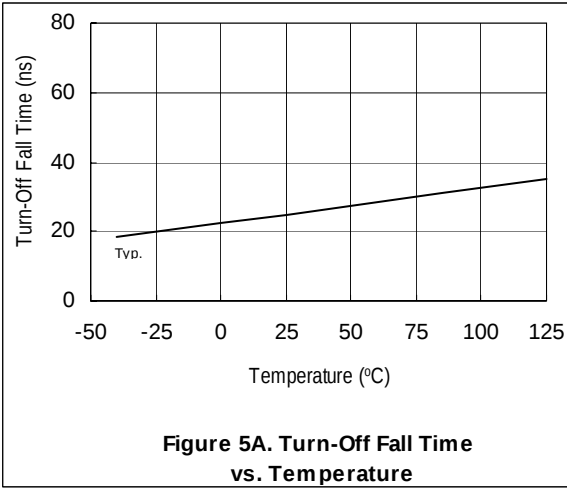


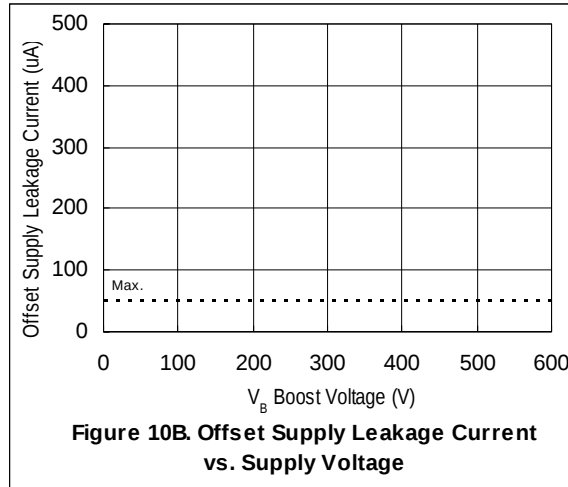
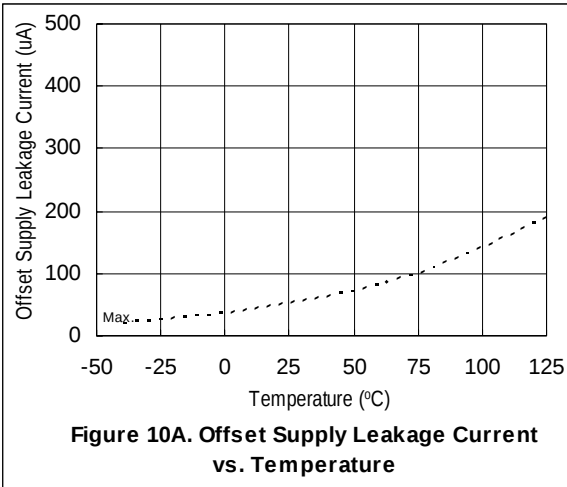
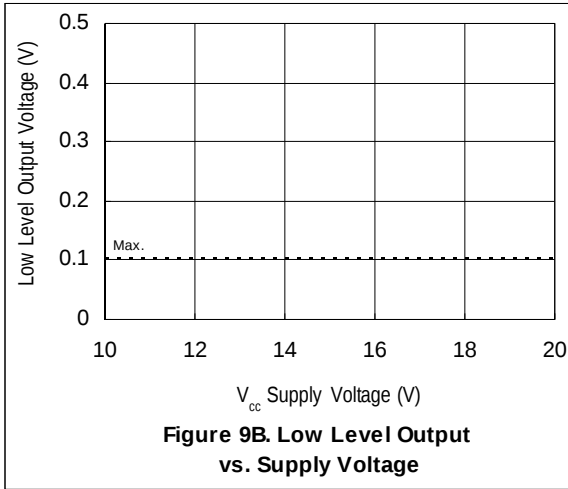
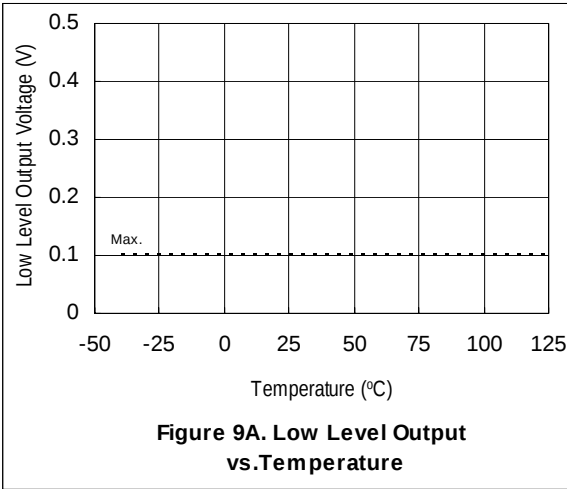
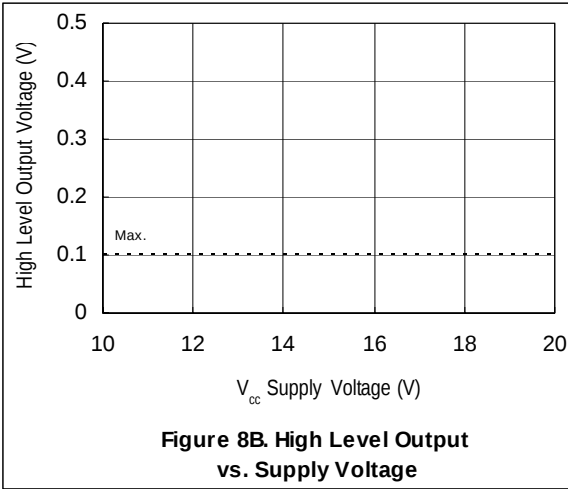
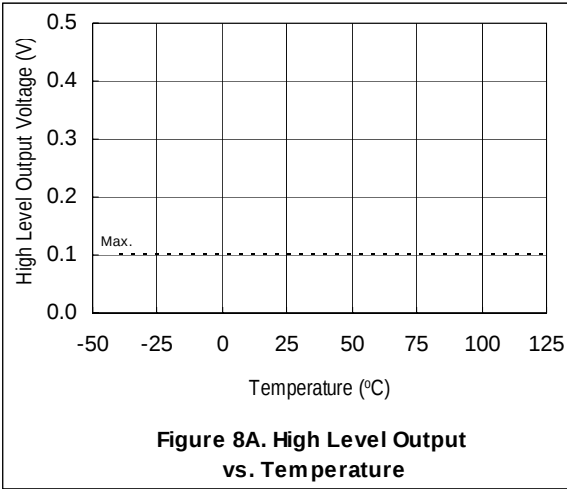
Figure 1: Switching Time Waveforms

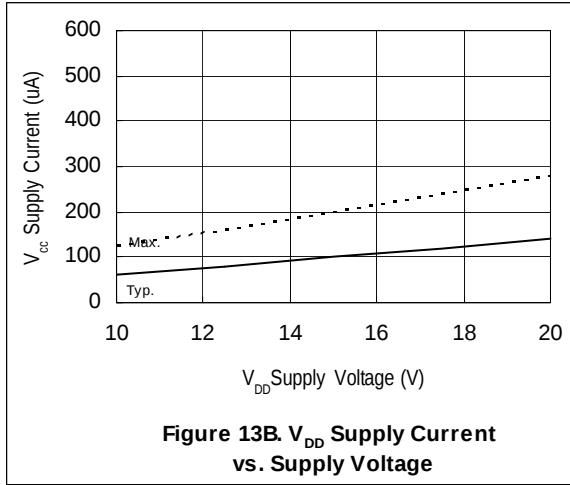
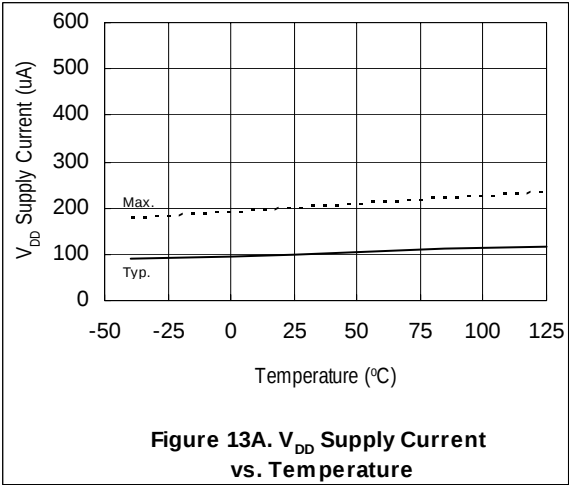
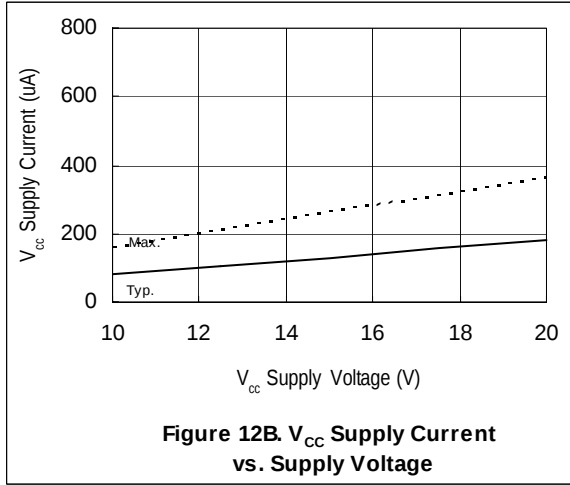
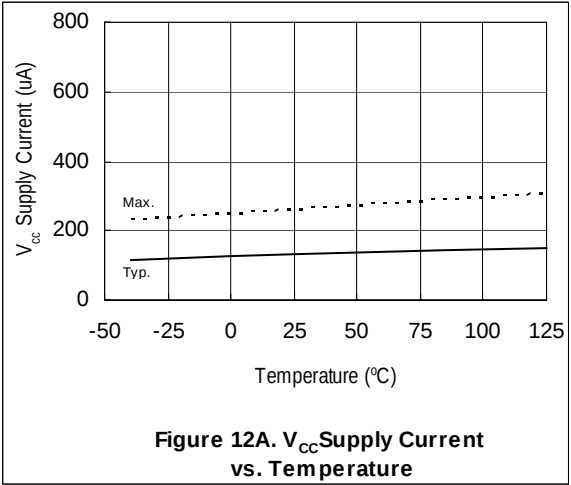
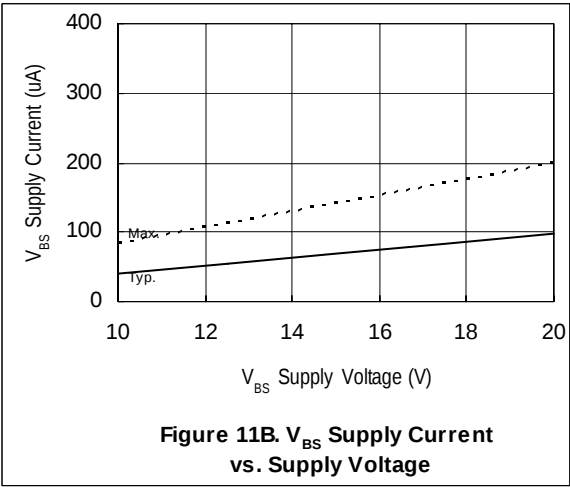
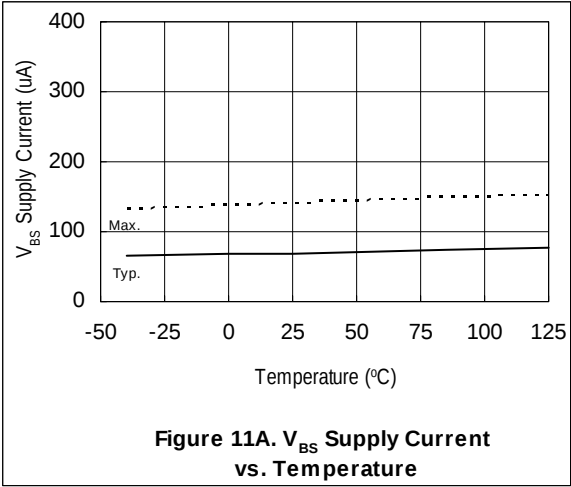
Shoot Through Prevention Logic

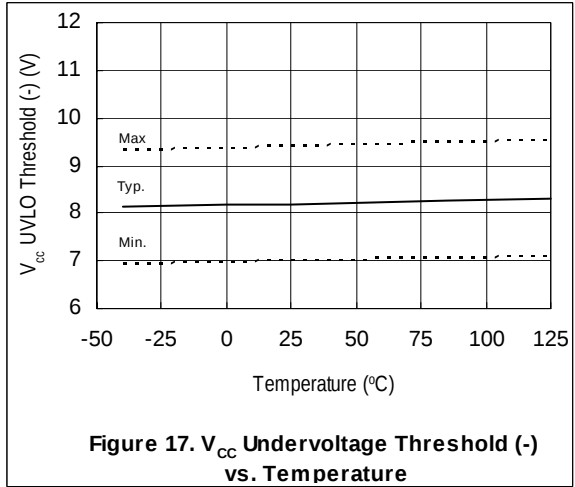
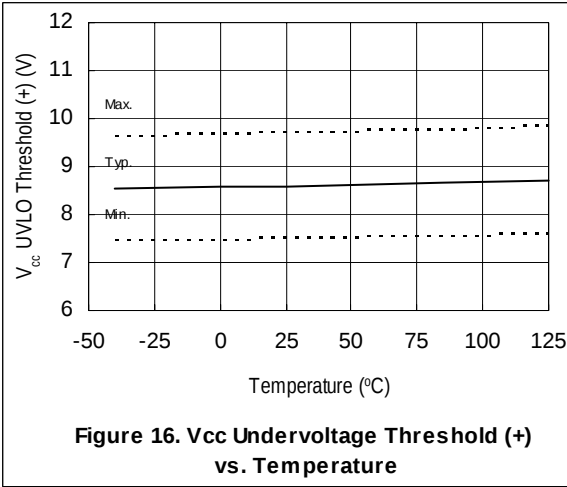
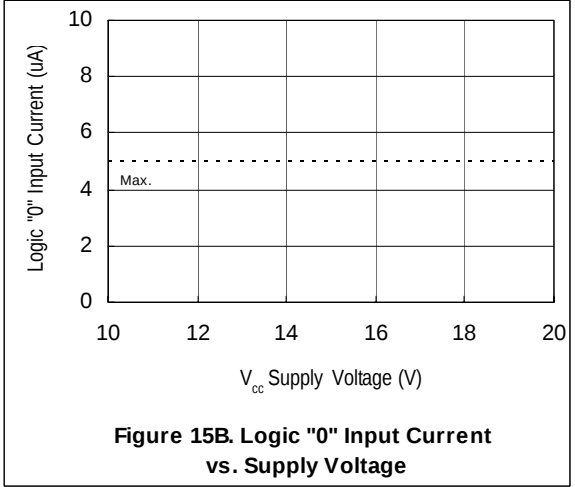
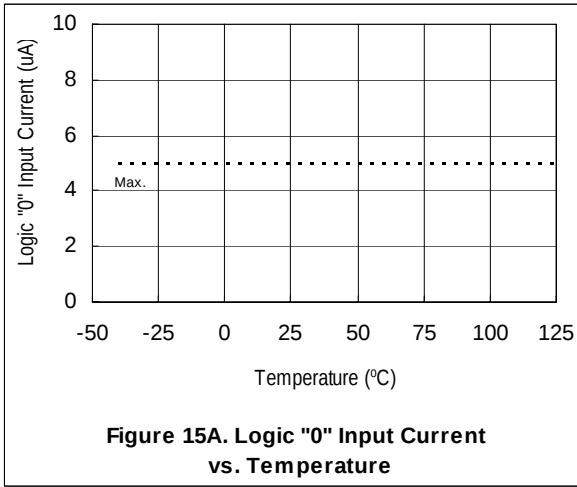
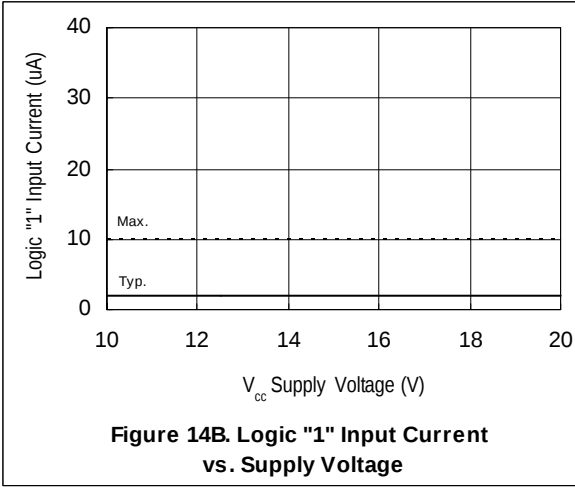
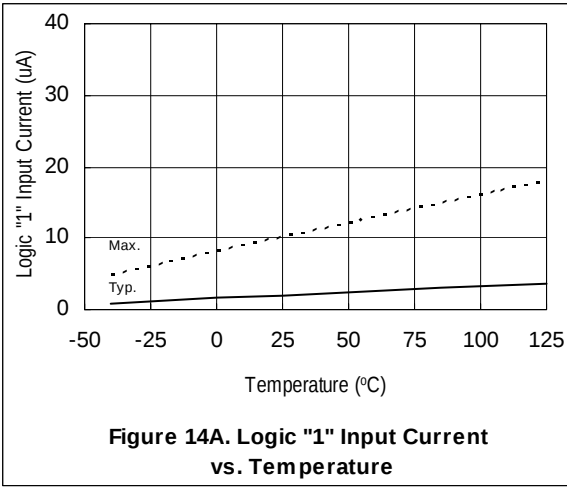
| HIN1 | LIN1 | LIN2 | HO1 | LO1 | LO2 |
|------|------|------|-----|-----|-----|
| 1    | 0    | 0    | 1   | 0   | 0   |
| 0    | 1    | 0    | 0   | 1   | 0   |
| 0    | 0    | 1    | 0   | 0   | 1   |
| 1    | 1    | 0    | 0   | 0   | 0   |
| 1    | 0    | 1    | 0   | 0   | 0   |
| 0    | 1    | 1    | 0   | 1   | 1   |
| 1    | 1    | 1    | 0   | 0   | 0   |
| 0    | 0    | 0    | 0   | 0   | 0   |

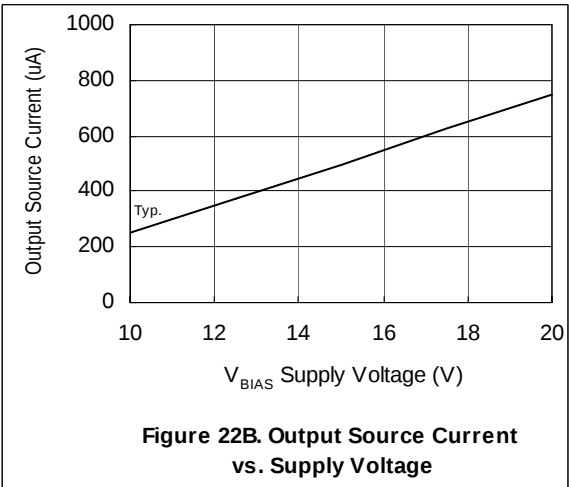
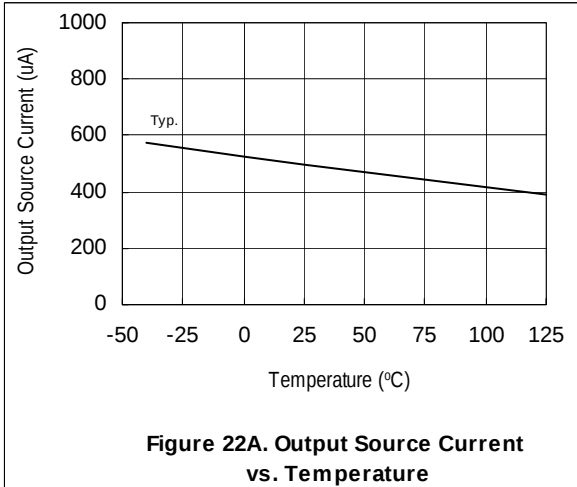
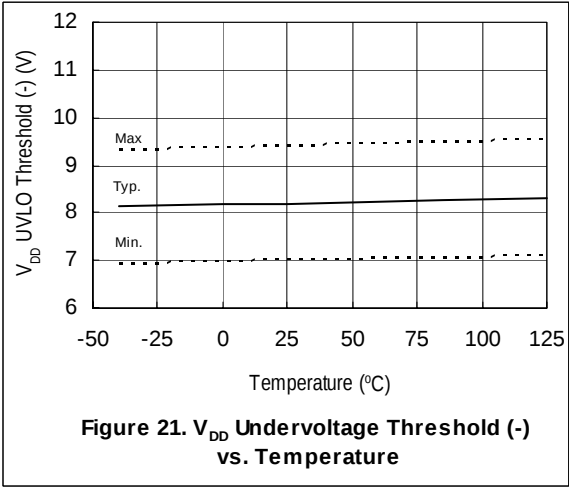
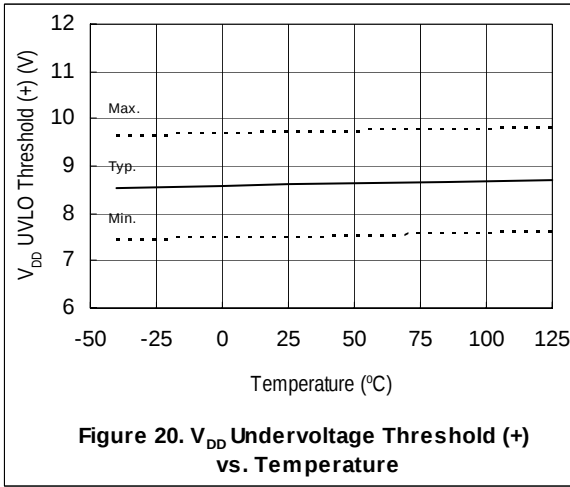
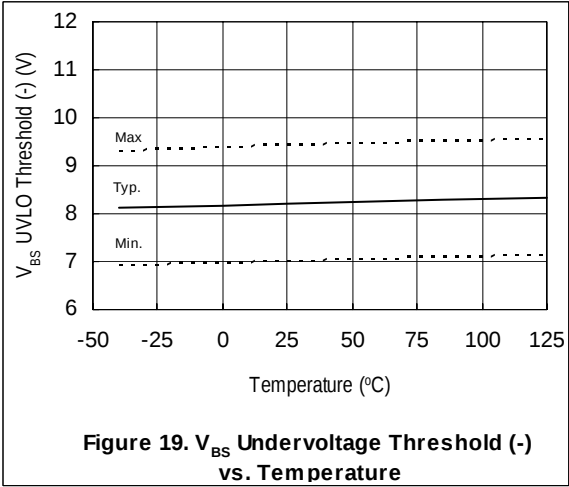
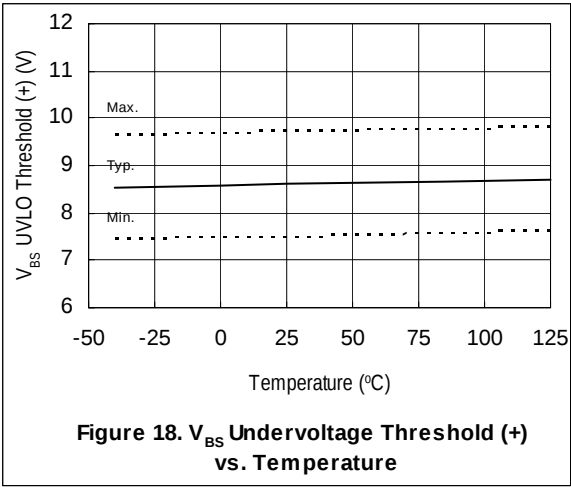


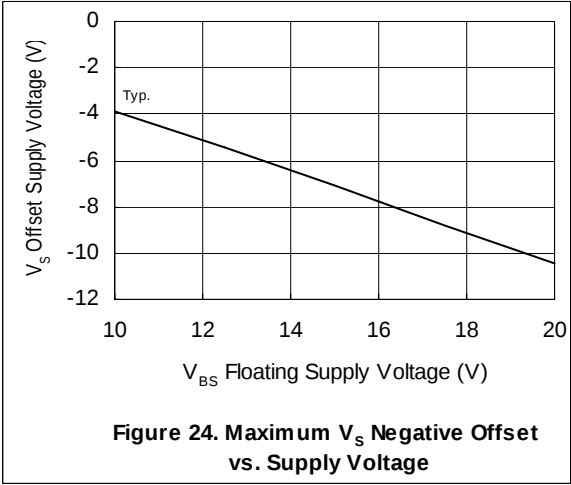
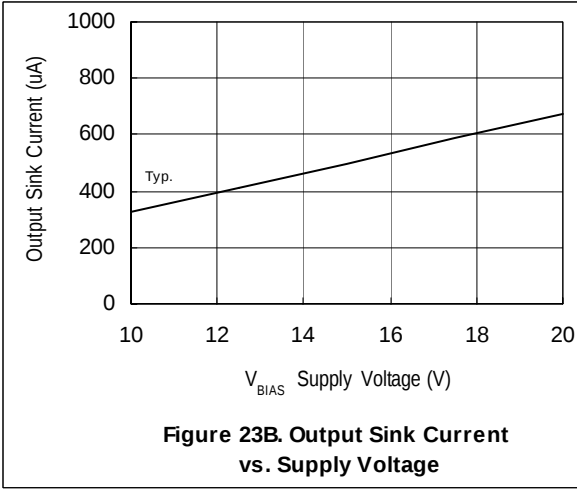
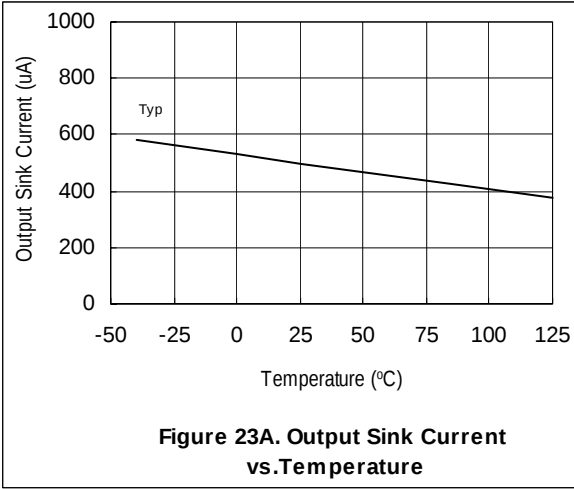


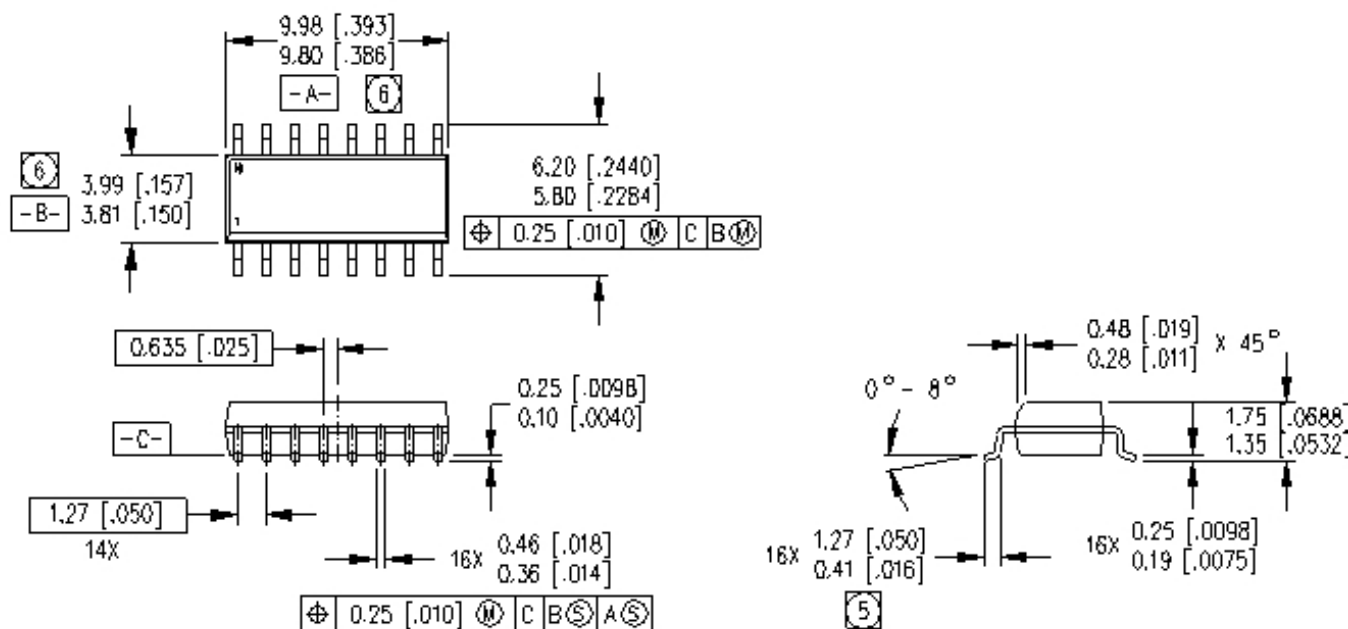








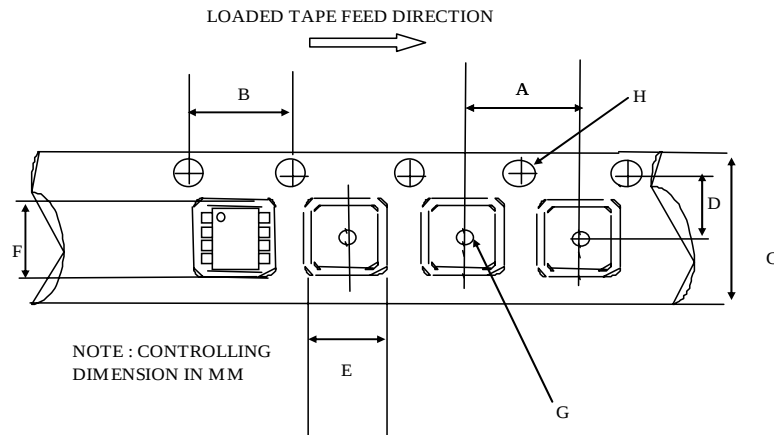




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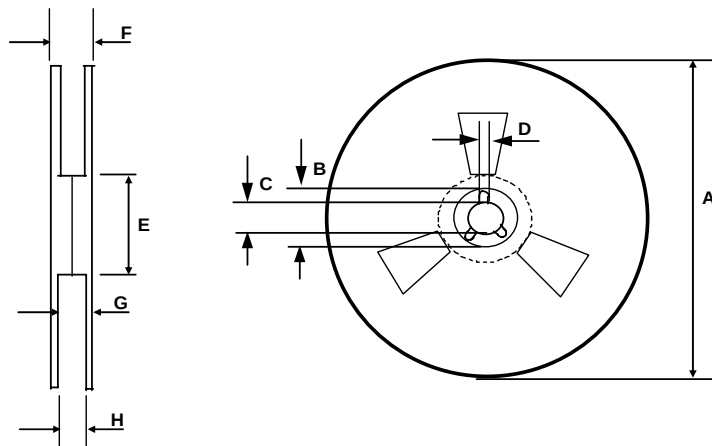
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5W-1982
2. CONTROLLING DIMENSION. MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETER [INCHES]
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [0.006]

**16-Lead SOIC (narrow body)**



CARRIER TAPE DIMENSION FOR 16SOICN

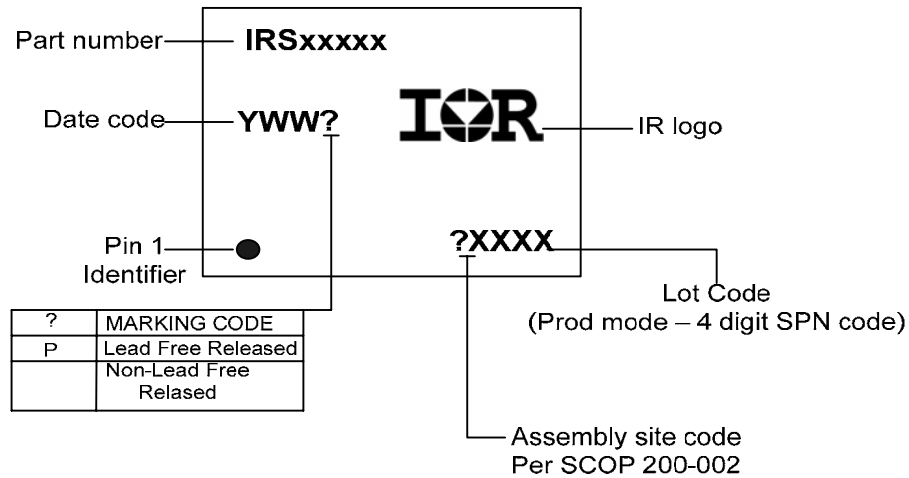
| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 7.90   | 8.10  | 0.311    | 0.318 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 15.70  | 16.30 | 0.618    | 0.641 |
| D    | 7.40   | 7.60  | 0.291    | 0.299 |
| E    | 6.40   | 6.60  | 0.252    | 0.260 |
| F    | 10.20  | 10.40 | 0.402    | 0.409 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |



REEL DIMENSIONS FOR 16SOICN

| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 22.40  | n/a      | 0.881  |
| G    | 18.50  | 21.10  | 0.728    | 0.830  |
| H    | 16.40  | 18.40  | 0.645    | 0.724  |

### LEAD-FREE PART MARKING INFORMATION



### ORDER INFORMATION

16-Lead SOIC IRS21953SPBF

16-Lead SOIC Tape & Reel IRS21953STRPBF

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