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FR60 MB91460A Series 32-bit Microcontroller Datasheet

MB91460A series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family* of CPUs.

This series contains the LIN-USART and CAN controllers.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
Signed 32-bit multiplication: 5 cycles
Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal peripheral resources

- General-purpose ports : Maximum 73 ports
- DMAC (DMA Controller)
 - Maximum of 5 channels able to operate simultaneously.
 - 2 transfer sources (internal peripheral/software)
 - Activation source can be selected using software.
 - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
 - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
 - Transfer data size selectable from 8/16/32-bit
 - Multi-byte transfer enabled (by software)
 - DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
 - 10-bit resolution: 21 channels
 - Conversion time: minimum 1 μ s
- External interrupt inputs : 10 channels
 - Shares the CAN RX pin and the I²C SDA pin
- Bit search module (for REALOS)

Function to search from the MSB (most significant bit) for the position of the first "0", "1", or changed bit in a word

- LIN-USART (full duplex double buffer): 5 channels
 - Clock synchronous/asynchronous selectable
 - Sync-break detection
 - Internal dedicated baud rate generator
- I²C bus interface (supports 400 kbps): 1 channel
 - Master/slave transmission and reception
 - Arbitration function, clock synchronisation function
- CAN controller (C-CAN): 1 channel
 - Maximum transfer speed: 1 Mbps
 - 32 transmission/reception message buffers
- 16-bit PPG timer : 10 channels
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 6 channels (operates in conjunction with the free-run timer)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Supply Supervisor: Low voltage detection circuit for external V_{DD5} and internal 1.8V core voltage
- Clock supervisor
Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
Sub-clock calibration
Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
Main oscillator stabilisation timer
Generates an interrupt in sub-clock mode after the stabilisation wait time has elapsed on the 23-bit stabilisation wait time counter
Sub-oscillator stabilisation timer
Generates an interrupt in main clock mode after the stabilisation wait time has elapsed on the 15-bit stabilisation wait time counter

Package and technology

- Package : 100-pin plastic LQFP (LQFP-100)
- CMOS 0.18 μm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between -40°C and $+105^{\circ}\text{C}$

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1. Product Lineup

Feature	MB91V460A (Evaluation device)	MB91F464AA MB91F464AB
Max. core frequency (CLKB)	80MHz	80MHz
Max. resource frequency (CLKP)	40MHz	40MHz
Max. external bus freq. (CLKT)	40MHz	40MHz
Max. CAN frequency (CLKCAN)	20MHz	40MHz
Technology	0.35 μm	0.18 μm
Watchdog timer	yes	yes
Watchdog timer (RC osc. based)	yes (disengageable)	yes
Bit Search	yes	yes
Reset input (INITX)	yes	yes
Hardware Standby input (HSTX)	yes	-
Clock Modulator	yes	yes
Low Power Mode	yes	yes
DMA	5 ch	5 ch
MMU/MPU	MPU (16 ch) ¹⁾	MPU (2 ch) ¹⁾
Flash memory	Emulation SRAM 32bit read data	416 KByte
Satellite Flash memory	n.a.	-
Flash Protection	n.a.	yes
D-RAM	64 KByte	8 KByte
ID-RAM	64 KByte	8 KByte
Flash-cache (F-cache)	16 KByte	-
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte
RTC	1 ch	1 ch
Free Running Timer	8 ch	8 ch
ICU	8 ch	8 ch
OCU	8 ch	6 ch
Reload Timer	8 ch	8 ch
PPG 16-bit	16 ch	10 ch
PFM 16-bit	1 ch	-
Sound Generator	1 ch	-
Up/Down Counter (8/16-bit)	4 ch (8-bit) / 2 ch (16-bit)	-
C_CAN	6 ch (128msg)	1 ch (32msg)
LIN-USART	4 ch + 4 ch FIFO + 8 ch	4 ch + 1 ch FIFO
I2C (400k)	4 ch	1 ch

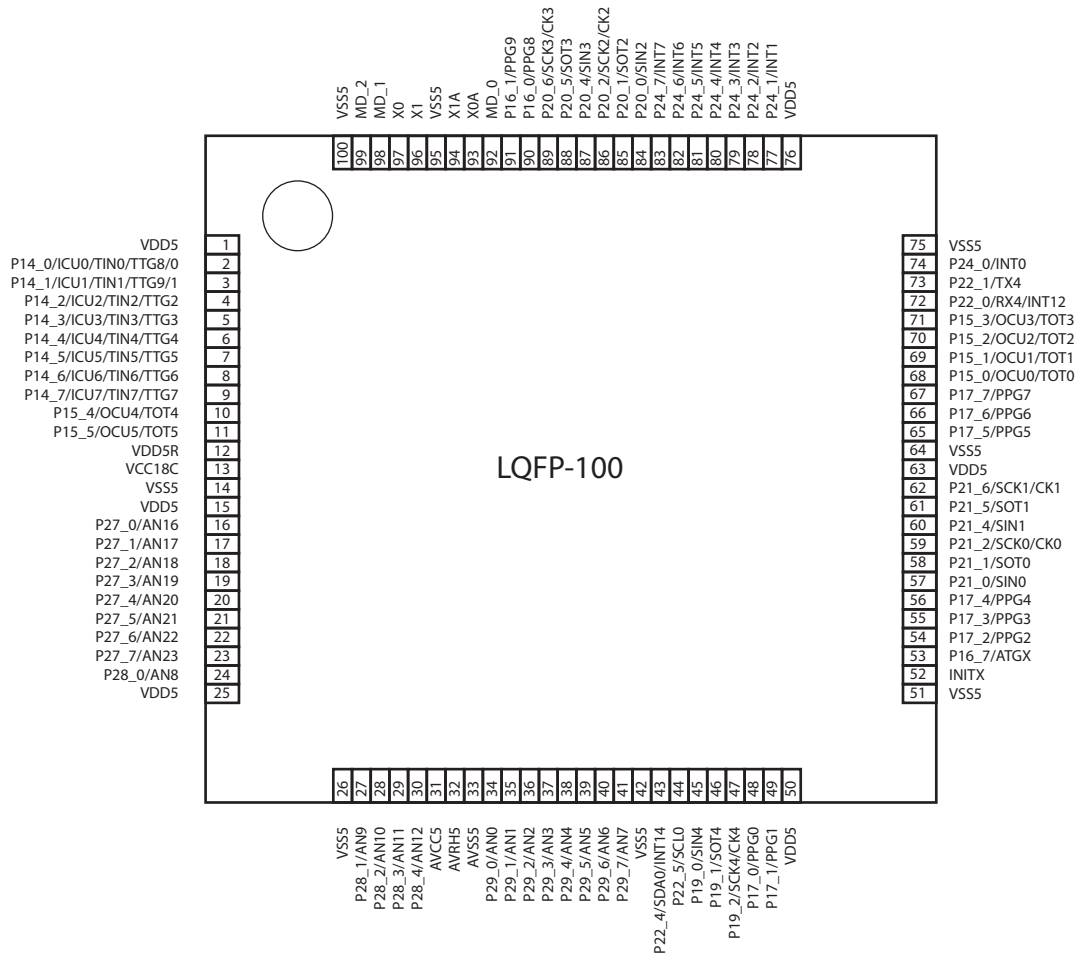
Feature	MB91V460A (Evaluation device)	MB91F464AA MB91F464AB
FR external bus	yes (32bit addr, 32bit data)	-
External Interrupts	16 ch	10 ch
NMI Interrupts	1 ch	-
SMC	6 ch	-
LCD controller (40x4)	1 ch	-
ADC (10 bit)	32 ch	21 ch
Alarm Comparator	2 ch	-
Supply Supervisor (low voltage detection)	yes	yes
Clock Supervisor	yes	yes
Main clock oscillator	4MHz	4MHz
Sub clock oscillator	32kHz	32kHz
RC Oscillator	100kHz	100kHz / 2MHz
PLL	x 20	x 20
DSU4	yes	-
EDSU	yes (32 BP) *1	yes (4 BP) *1
Supply Voltage	3V / 5V	3V / 5V
Regulator	yes	yes
Power Consumption	n.a.	< 800 mW
Temperature Range (T _A)	0..70 C	-40..105 C
Package	BGA660	LQFP100
Power on to PLL run	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 4 sec typical

*1 : MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

2. Pin Assignment

■ MB91F464Ax

(TOP VIEW)



FPT-100P-M20

3. Pin Description

■ MB91F464Ax

Pin no.	Pin name	I/O	I/O circuit type*	Description
2 to 9	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN0 to TIN7			External trigger input pins for reload timer
	TTG0/8, TTG1/9, TTG2 to TTG7			External trigger input pins for PPG timer
10, 11	P15_4, P15_5	I/O	A	General-purpose input/output ports
	OCU4, OCU5			Output compare output pins
	TOT4, TOT5			Reload timer output pins
16 to 23	P27_0 to P27_7	I/O	B	General-purpose input/output ports
	AN16 to AN23			Analog input pins for A/D converter
24, 27 to 30	P28_0 to P28_4	I/O	B	General-purpose input/output ports
	AN8 to AN12			Analog input pins for A/D converter
34 to 41	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins for A/D converter
43	P22_4	I/O	C	General-purpose input/output port
	SDA0			I ² C bus data input/output pin
	INT14			External interrupt input pin
44	P22_5	I/O	C	General-purpose input/output port
	SCL0			I ² C bus CLK input/output pin
45	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin for USART4
46	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin for USART4
47	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin for USART4
	CK4			External clock input pin for free-run timer 4
48, 49	P17_0, P17_1	I/O	A	General-purpose input/output ports
	PPG0, PPG1			PPG timer output pins
52	INITX	I	H	External reset input pin
53	P16_7	I/O	A	General-purpose input/output port
	ATGX			A/D converter external trigger input pin
54 to 56	P17_2 to P17_4	I/O	A	General-purpose input/output ports
	PPG2 to PPG4			PPG timer output pins

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Pin no.	Pin name	I/O	I/O circuit type*	Description
57	P21_0	I/O	A	General-purpose input/output port
	SIN0			Data input pin for USART0
58	P21_1	I/O	A	General-purpose input/output port
	SOT0			Data output pin for USART0
59	P21_2	I/O	A	General-purpose input/output port
	SCK0			Clock input/output pin for USART0
	CK0			External clock input pin for free-run timer 0
60	P21_4	I/O	A	General-purpose input/output port
	SIN1			Data input pin for USART1
61	P21_5	I/O	A	General-purpose input/output port
	SOT1			Data output pin for USART1
62	P21_6	I/O	A	General-purpose input/output port
	SCK1			Clock input/output pin for USART1
	CK1			External clock input pin for free-run timer 1
65 to 67	P17_5 to P17_7	I/O	A	General-purpose input/output ports
	PPG5 to PPG7			PPG timer output pins
68 to 71	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
72	P22_0	I/O	A	General-purpose input/output port
	RX4			RX input pin for CAN4
	INT12			External interrupt input pin
73	P22_1	I/O	A	General-purpose input/output port
	TX4			TX output pin for CAN4
74, 77 to 83	P24_0 to P24_7	I/O	A	General-purpose input/output ports
	INT0 to INT7			External interrupt input pins
84	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin for USART2
85	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin for USART2

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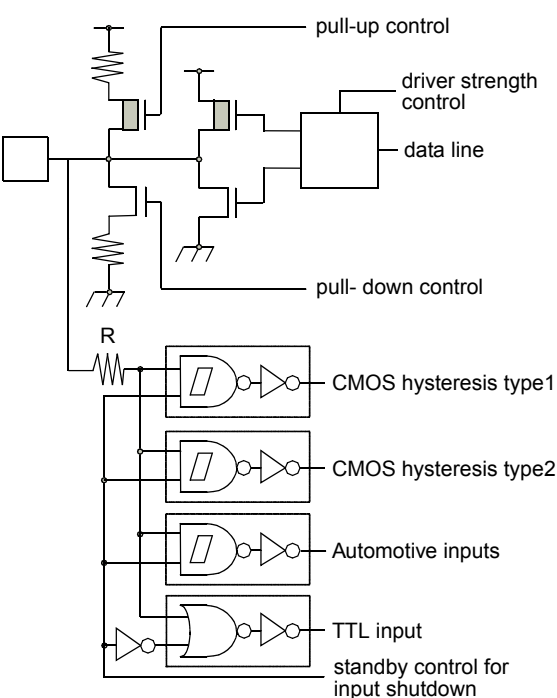
Pin no.	Pin name	I/O	I/O circuit type*	Description
86	P20_2	I/O	A	General-purpose input/output port
	SCK2			Clock input/output pin for USART2
	CK2			External clock input pin for free-run timer 2
87	P20_4	I/O	A	General-purpose input/output port
	SIN3			Data input pin for USART3
88	P20_5	I/O	A	General-purpose input/output port
	SOT3			Data output pin for USART3
89	P20_6	I/O	A	General-purpose input/output port
	SCK3			Clock input/output pin for USART3
	CK3			External clock input pin for free-run timer 3
90, 91	P16_0, P16_1	I/O	A	General-purpose input/output ports
	PPG8, PPG9			PPG timer output pins
92	MD_0	I	G	Mode setting pin
93	X0A	—	J2	Sub clock (oscillation) input
94	X1A	—	J2	Sub clock (oscillation) output
96	X1	—	J1	Clock (oscillation) output
97	X0	—	J1	Clock (oscillation) input
98	MD_1	I	G	Mode setting pins
99	MD_2	I	G	

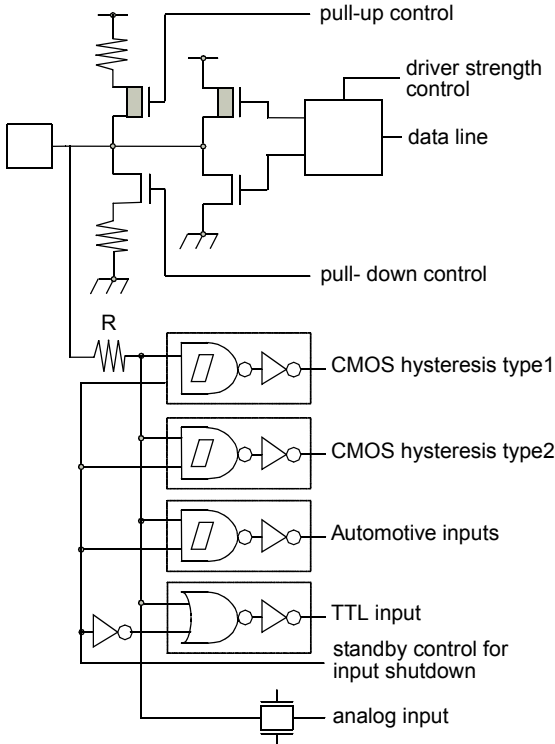
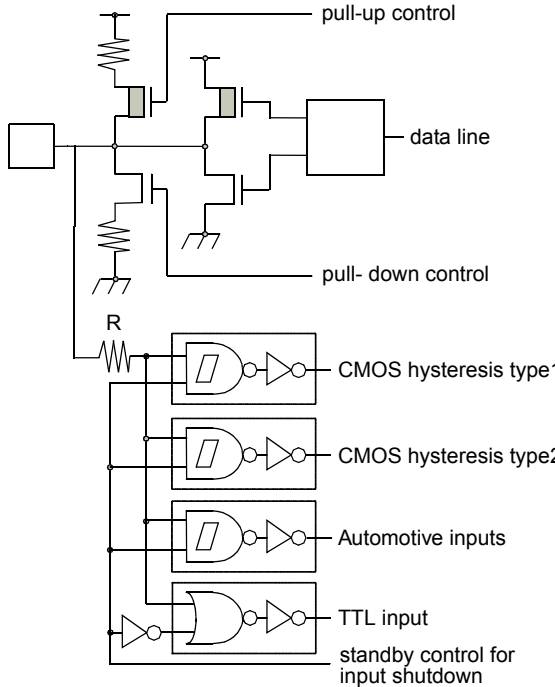
 * : For information about the I/O circuit type, refer to “[I/O Circuit Types](#)”.

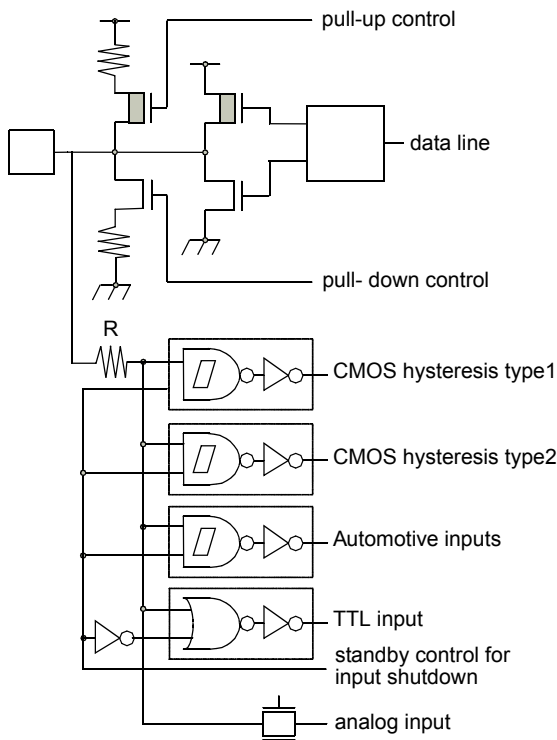
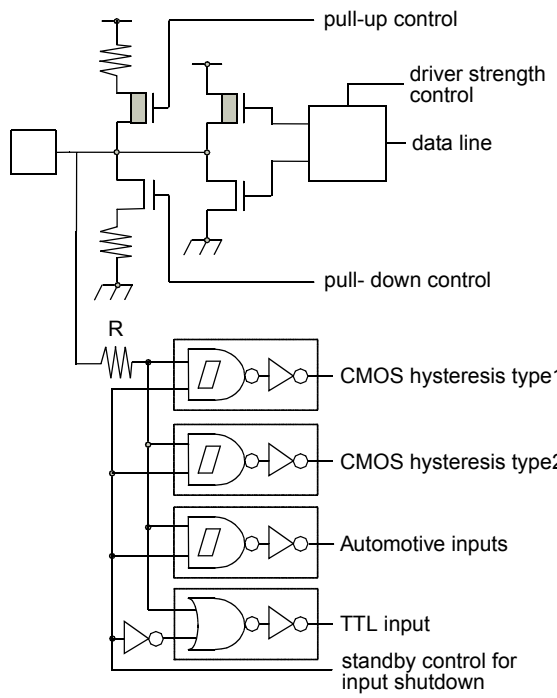
[Power supply/Ground pins]

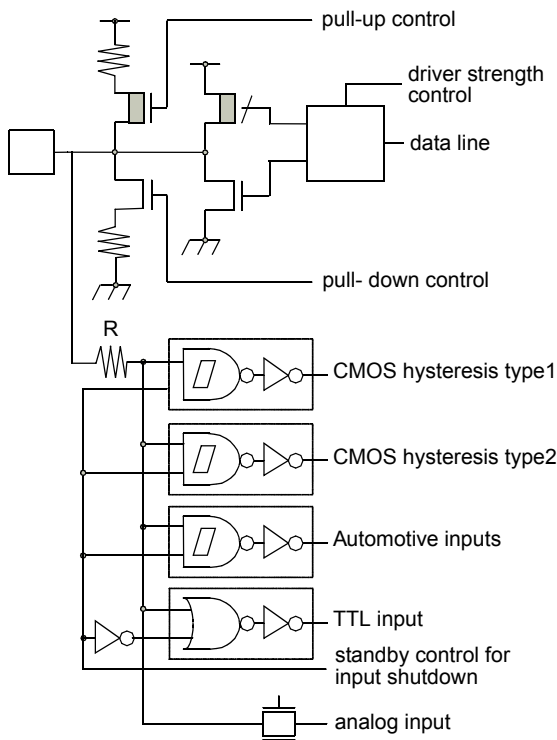
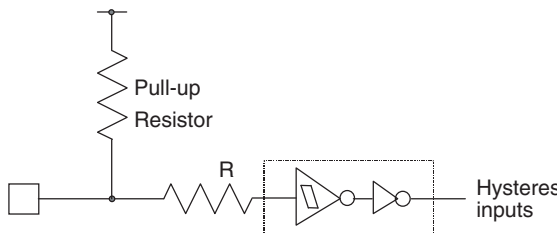
Pin no.	Pin name	Description
14, 26, 42, 51, 64, 75, 95, 100	VSS5	Ground pins
1, 15, 25, 50, 63, 76	VDD5	Power supply pins
12	VDD5R	Power supply pin for internal regulator
33	AVSS5	Analog ground pin for A/D converter
31	AVCC5	Power supply pin for A/D converter
32	AVRH5	Reference power supply pin for A/D converter
13	VCC18C	Capacitor connection pin for internal regulator

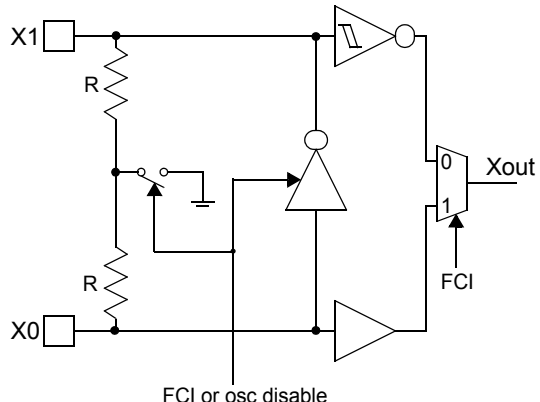
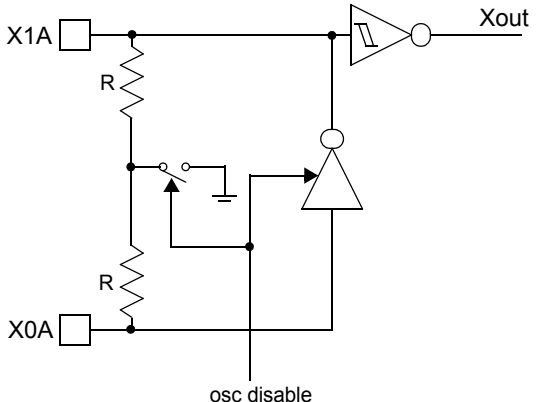
4. I/O Circuit Types

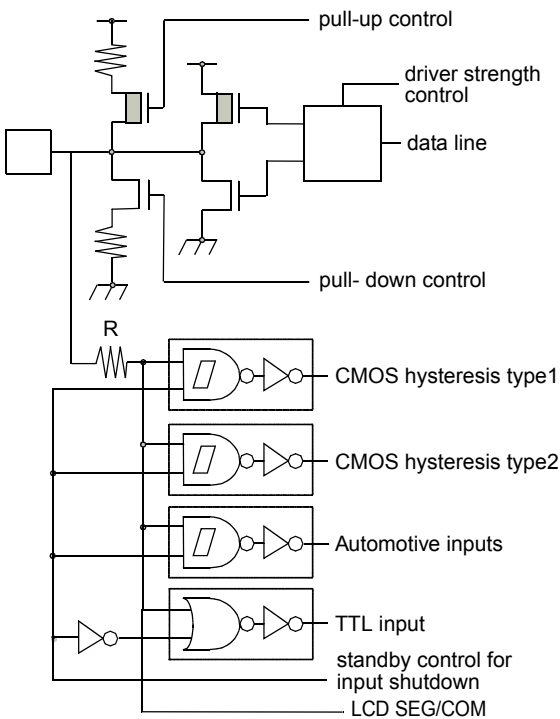
Type	Circuit	Remarks
A	 pull-up control driver strength control data line pull- down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown	CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx.

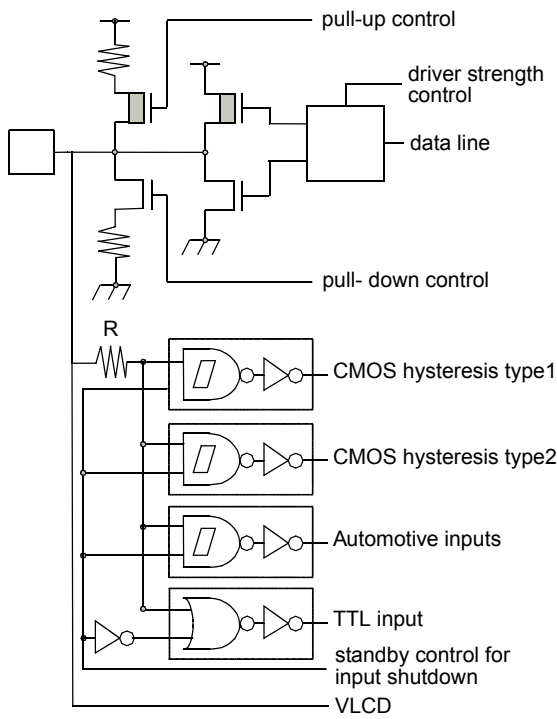
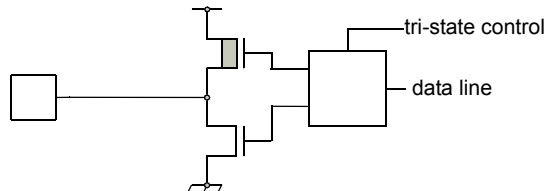
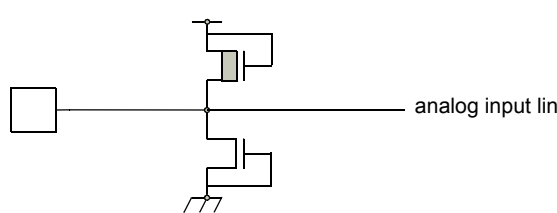
Type	Circuit	Remarks
B	 pull-up control driver strength control data line pull- down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown analog input	CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx. Analog input
C	 pull-up control data line pull- down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown	CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx.

Type	Circuit	Remarks
D	 The diagram for Type D shows a data line connected to a pull-up control and a pull-down control. A resistor R is connected to the data line. Below the data line, there are four input types: CMOS hysteresis type1, CMOS hysteresis type2, Automotive inputs, and TTL input. A standby control for input shutdown is also shown, connected to an analog input.	CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx. Analog input
E	 The diagram for Type E is similar to Type D, but includes a driver strength control connected to the data line. The input types and standby control are the same as in Type D.	CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$, and $I_{OL} = 30\text{mA}$, $I_{OH} = -30\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx.

Type	Circuit	Remarks
F		CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$, and $I_{OL} = 30\text{mA}$, $I_{OH} = -30\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.

Type	Circuit	Remarks
J1	 FCI or osc disable	High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. $2 * 0.5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2	 osc disable	Low-speed oscillation circuit: ■ Feedback resistor = approx. $2 * 5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K	 pull-up control driver strength control data line pull-down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown LCD SEG/COM	CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx. LCD SEG/COM output

Type	Circuit	Remarks
L		CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: $50\text{k}\Omega$ approx. Analog input LCD Voltage input
M		CMOS level tri-state output ($I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$)
N		Analog input pin with protection

5. Handling Devices

1. Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than (V_{DD5}) or less than (V_{SS5}) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

2. Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor ($2K\Omega$ to $10K\Omega$) or enable internal pullup or pulldown resistors (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to V_{SS5} or V_{DD5} directly. Unused ALARM input pins can be connected to AV_{SS5} directly.

3. Power supply pins

In MB91460A series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460A series must be connected to the current supply source via a low impedance.

It is also recommended to connect a ceramic capacitor of approximately $0.1\ \mu F$ as a bypass capacitor between power supply pin and ground pin near this device.

This series has a built-in step-down regulator. Connect a bypass capacitor of $4.7\ \mu F$ (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

4. Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.

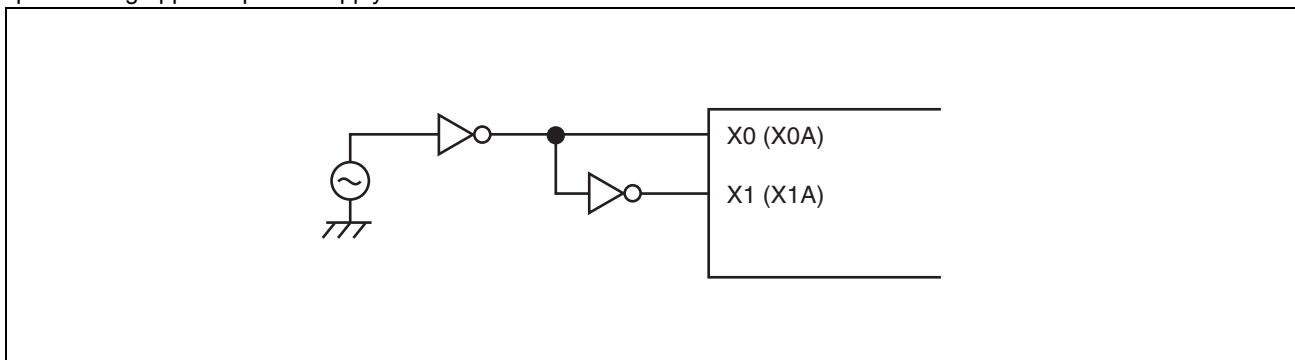
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.

Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5. Notes on using external clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Example of using opposite phase supply



6. Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

7. Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

8. Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

9. Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

■ The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

- a user interrupt or NMI is accepted;
- single-step execution is performed;
- execution breaks due to a data event or from the emulator menu.
 - D0 and D1 flags are updated in advance.
 - An EIT handling routine (user interrupt/NMI or emulator) is executed.
 - Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

■ The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.

- The PS register is updated in advance.
- An EIT handling routine (user interrupt/NMI or emulator) is executed.
- Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

6. Notes On Debugger

1. Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

2. Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

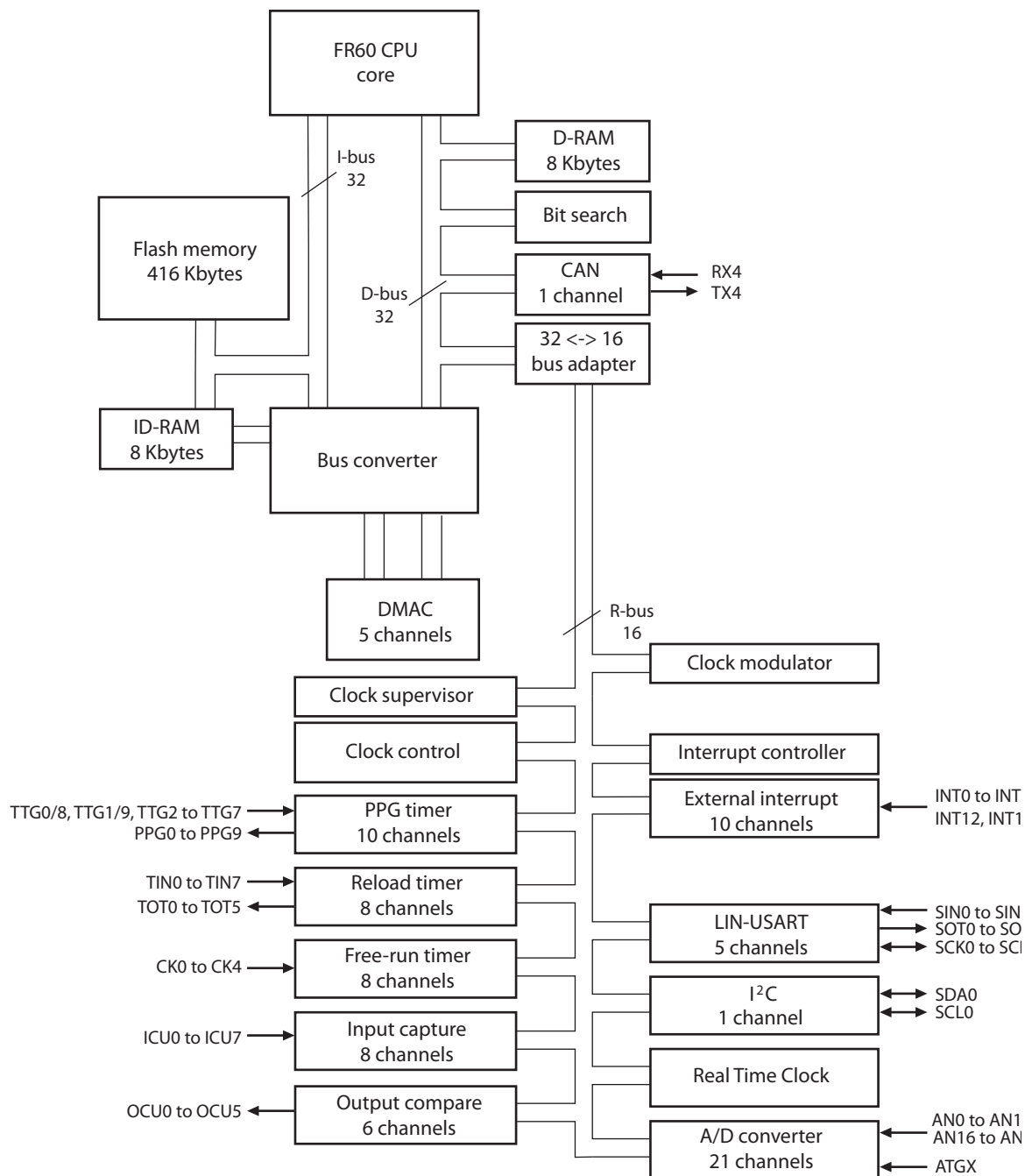
To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

3. Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

7. Block Diagram

■ MB91F464Ax



8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

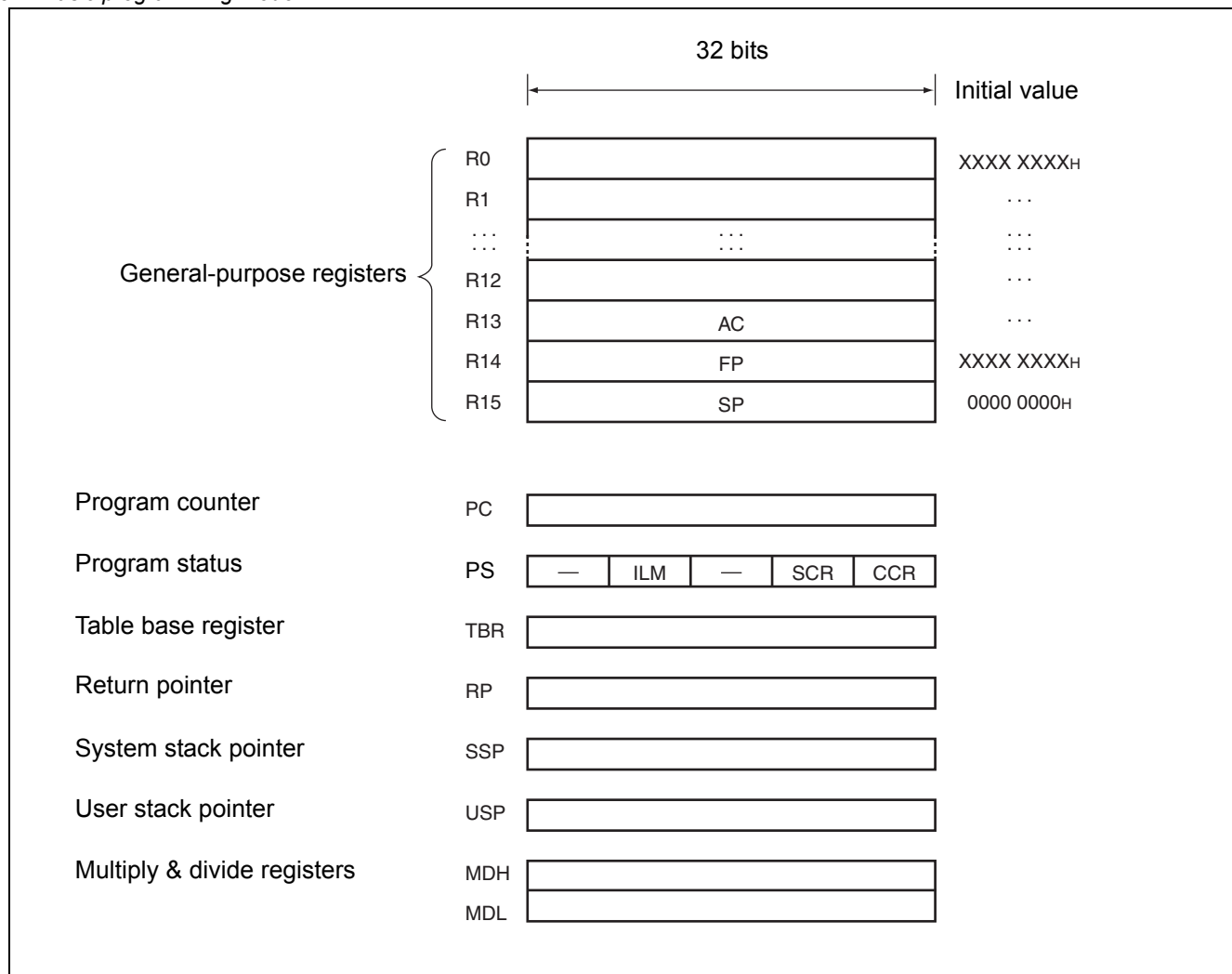
- Adoption of RISC architecture
Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
32-bit × 32-bit multiplication: 5 cycles
16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
Quick response speed (6 cycles)
Multiple-interrupt support
Level mask function (16 levels)
- Enhanced instructions for I/O operation
Memory-to-memory transfer instruction
Bit processing instruction
Basic instruction word length: 16 bits
- Low-power consumption
Sleep mode/stop mode

8.2 Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

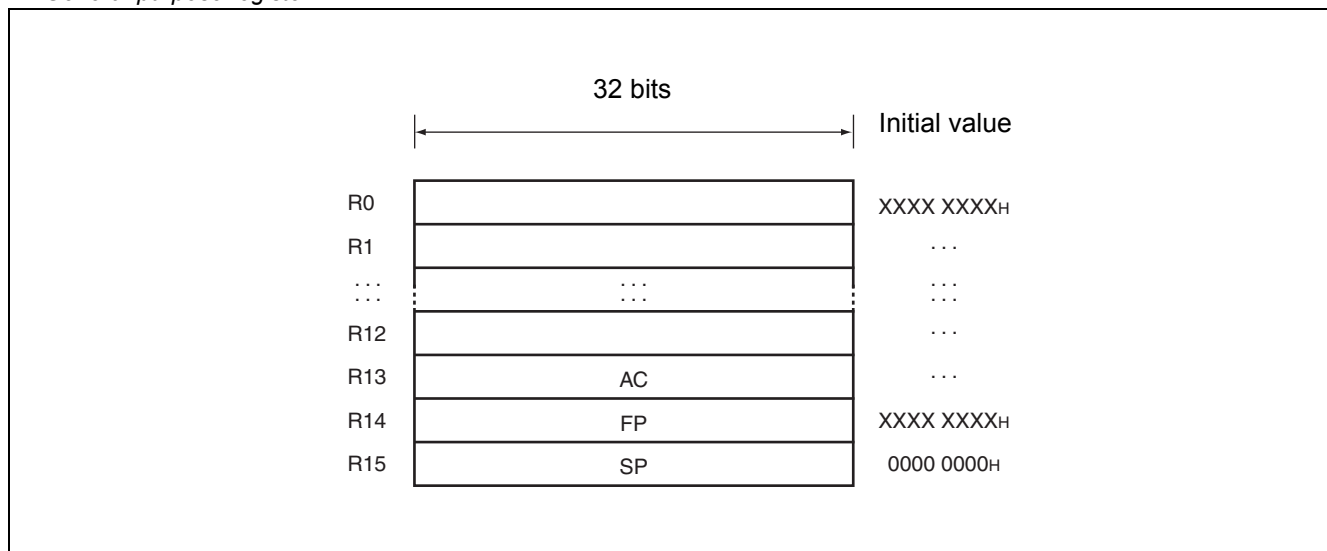
8.3 Programming model

8.3.1 Basic programming model



8.4 Registers

8.4.1 General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

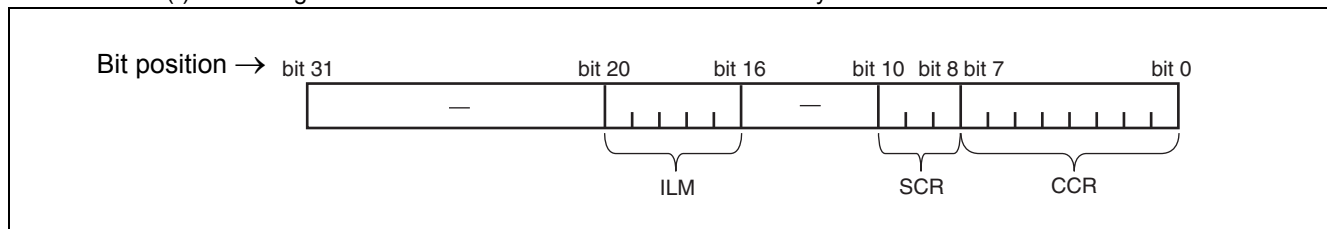
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

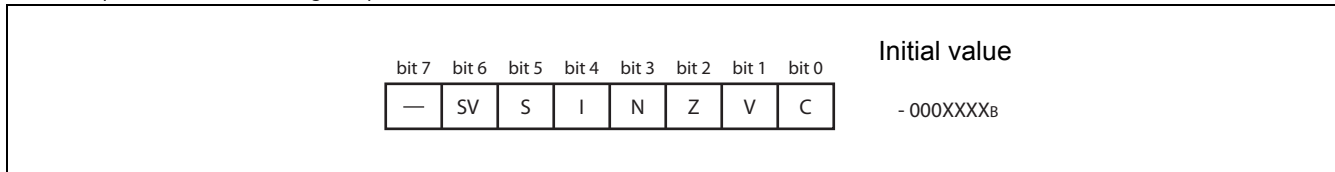
8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.

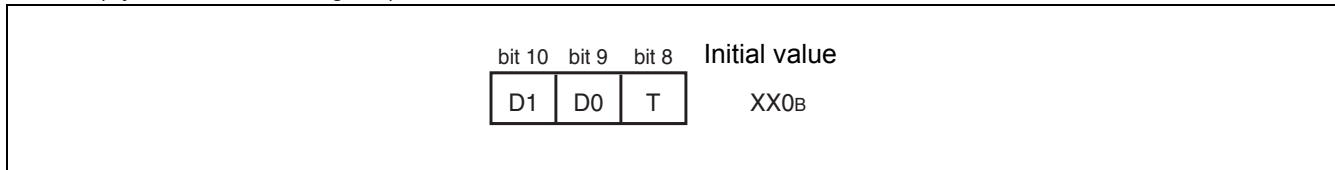


8.4.3 CCR (Condition Code Register)



SV : Supervisor flag
 S : Stack flag
 I : Interrupt enable flag
 N : Negative enable flag
 Z : Zero flag
 V : Overflow flag
 C : Carry flag

8.4.4 SCR (System Condition Register)



Flag for step division (D1, D0)

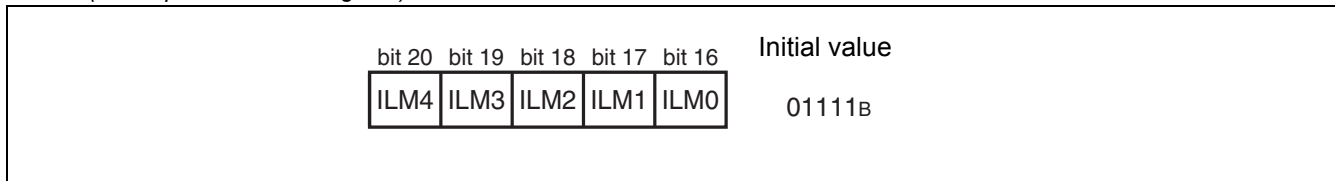
This flag stores interim data during execution of step division.

Step trace trap flag (T)

This flag indicates whether the step trace trap is enabled or disabled.

The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

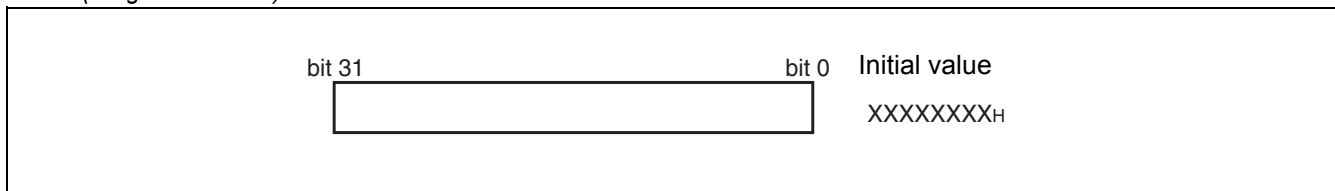
8.4.5 ILM (Interrupt Level Mask register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value "01111_B" at reset.

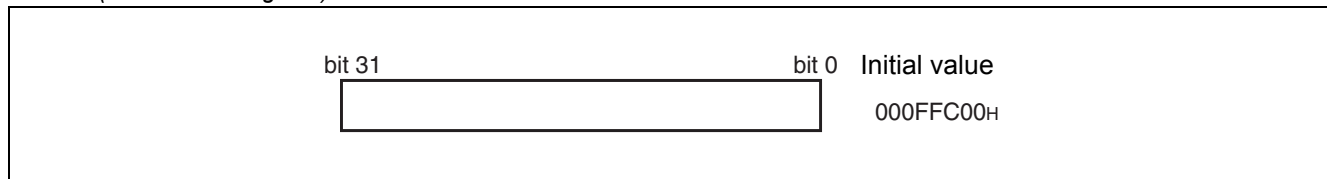
8.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

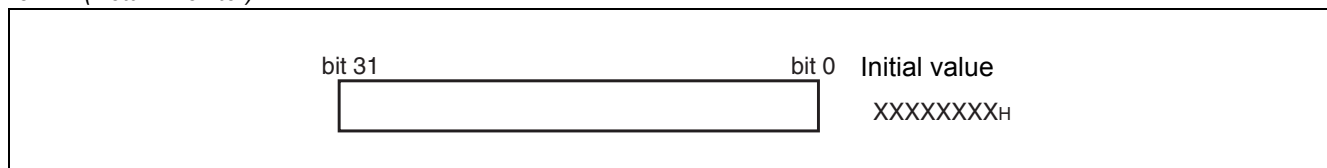
8.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is 000FFC00_H.

8.4.8 RP (Return Pointer)



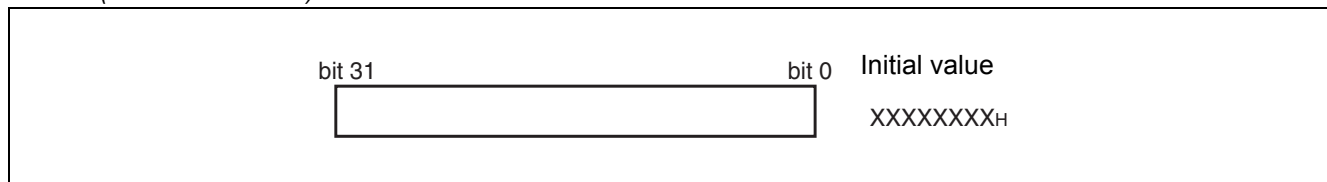
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

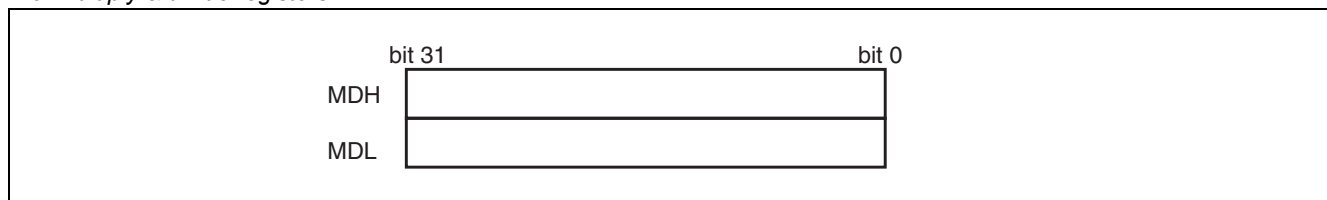
8.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

8.4.10 Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

9. Embedded Program/data Memory (Flash)

9.1 Flash features

- MB91F464Ax: 416 Kbytes ($6 \times 64 \text{ Kbytes} + 4 \times 8 \text{ Kbytes}$) = 3.25 Mbits
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

9.2 Operation modes

(1) 32-bit CPU mode :

- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

(2) 16-bit CPU mode :

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in half-word (16-bit) length units.

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

9.3 Flash access in CPU mode

9.3.1 Flash configuration

■ Flash memory map MB91F464Ax

Address										
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7	
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)					
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)					
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)					
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6	
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)					
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5	
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4	
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3	
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2	
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1	
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0	
16bit read/write 32bit read	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7		
	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]			
	dat[31:0]				dat[31:0]					
Legend	Memory not available in this area				Memory available in this area					

9.3.2 Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

■ Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 80 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on MB91F464Ax

■ Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	-	-	0	4	
to 48 MHz	1	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 80 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on MB91F464Ax

9.3.3 Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming:

■ Address mapping MB91F464Ax

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h + 00:2000h
0A:0000h to 0F:FFFFh	addr[2]==0	SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 00:0000h
0A:0000h to 0F:FFFFh	addr[2]==1	SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 00:0000h + 01:0000h

Note: FA result is without 10:0000h offset for parallel Flash programming .

Set offset by keeping FA[20] = 1 as described in section "Parallel Flash programming mode".

9.4 Parallel Flash programming mode

9.4.1 Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F464Ax

FA[20:0]	
001F:FFFFh 001F:0000h	SA19 (64KB)
001E:FFFFh 001E:0000h	SA18 (64KB)
001D:FFFFh 001D:0000h	SA17 (64KB)
001C:FFFFh 001C:0000h	SA16 (64KB)
001B:FFFFh 001B:0000h	SA15 (64KB)
001A:FFFFh 001A:0000h	SA14 (64KB)
	SA13 (64KB)
	SA12 (64KB)
	SA11 (64KB)
	SA10 (64KB)
	SA9 (64KB)
	SA8 (64KB)
0017:FFFFh 0017:E000h	SA7 (8KB)
0017:DFFFh 0017:C000h	SA6 (8KB)
0017:BFFFh 0017:A000h	SA5 (8KB)
0017:9FFFh 0017:8000h	SA4 (8KB)
	SA3 (8KB)
	SA2 (8KB)
	SA1 (8KB)
	SA0 (8KB)
16bit write mode	FA[1:0]=00
	FA[1:0]=10
	DQ[15:0]
	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend

Memory available in this area
Memory not available in this area

9.4.2 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F464Ax external pins			Comment
		Flash memory mode	Normal function	Pin number	
–	INITX	–	INITX	52	
RESET	–	FRSTX	P16_7	53	
–	–	MD_2	MD_2	99	Set to '1'
–	–	MD_1	MD_1	98	Set to '1'
–	–	MD_0	MD_0	92	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	P24_0	74	
BYTE	Internally fixed to 'H'	BYTEX	P24_2	78	
WE	Internal control signal + control via interface circuit	WEX	P28_3	29	
OE		OEX	P28_2	28	
CE		CEX	P28_1	27	
–		ATDIN	P22_1	73	Set to '0'
–		EQIN	P22_0	72	Set to '0'
–		TESTX	P24_3	79	Set to '1'
–		RDYI	P24_1	77	Set to '0'
A-1	Internal address bus	FA0	P19_2	47	Set to '0'
A0 to A7		FA1 to FA8	P27_0 to P27_7	16 to 23	
A8 to A15		FA9 to FA16	P15_0 to P15_5, P21_0, P21_1	68 to 71, 10, 11, 57, 58	
A16 to A18		FA17 to FA19	P21_2, P21_4, P21_5	59, 60, 61	
–		FA20,FA21	P21_6, P28_0	62, 24	Set to '1'
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P17_0 to P17_7	48, 49, 54, 55, 56, 65, 66, 67	
DQ8 to DQ15		DQ8 to DQ15	P14_0 to P14_7	2 to 9	

9.5 Power on Sequence in parallel programming mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

9.6 Flash Security

9.6.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

■ FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to "0"	set to "0"	set to "0"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "0"	set to "1"	set to "0"	Write Protection (all device modes, without exception)
set all to "0"	set to "0"	set to "1"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000") and Write Protection (all device modes)
set all to "0"	set to "1"	set to "0"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "1"	set to "1"	set to "0"	Write Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "1"	set to "1"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000") and Write Protection (all device modes except INTVEC mode MD[2:0] = "000")

■ FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1 [15:0]

MB91F464Ax

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	–	set to "0"	set to "1"	not available
FSV1[1]	–	set to "0"	set to "1"	not available
FSV1[2]	–	set to "0"	set to "1"	not available
FSV1[3]	–	set to "0"	set to "1"	not available
FSV1[4]	SA4	set to "0"	–	write protection is mandatory!
FSV1[5]	SA5	set to "0"	set to "1"	

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[6]	SA6	set to "0"	set to "1"	
FSV1[7]	SA7	set to "0"	set to "1"	
FSV1[8]	–	set to "0"	set to "1"	not available
FSV1[9]	–	set to "0"	set to "1"	not available
FSV1[10]	–	set to "0"	set to "1"	not available
FSV1[11]	–	set to "0"	set to "1"	not available
FSV1[12]	–	set to "0"	set to "1"	not available
FSV1[13]	–	set to "0"	set to "1"	not available
FSV1[14]	–	set to "0"	set to "1"	not available
FSV1[15]	–	set to "0"	set to "1"	not available

Note : It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.

See section "Flash access in CPU mode" for an overview about the sector organization of the Flash Memory.

9.6.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 Kbytes sectors. It is only evaluated if write protection bit FSV1 [17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

MB91F464Ax:

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[5:0]	–	set to “0”	set to “1”	not available
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[31:12]	–	set to “0”	set to “1”	not available

Note : See section “Flash access in CPU mode” for an overview about the sector organization of the Flash Memory.

10. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : 000_H to 0FF_H

Half word access : 000_H to 1FF_H

Word data access : 000_H to 3FF_H

11. Memory Maps

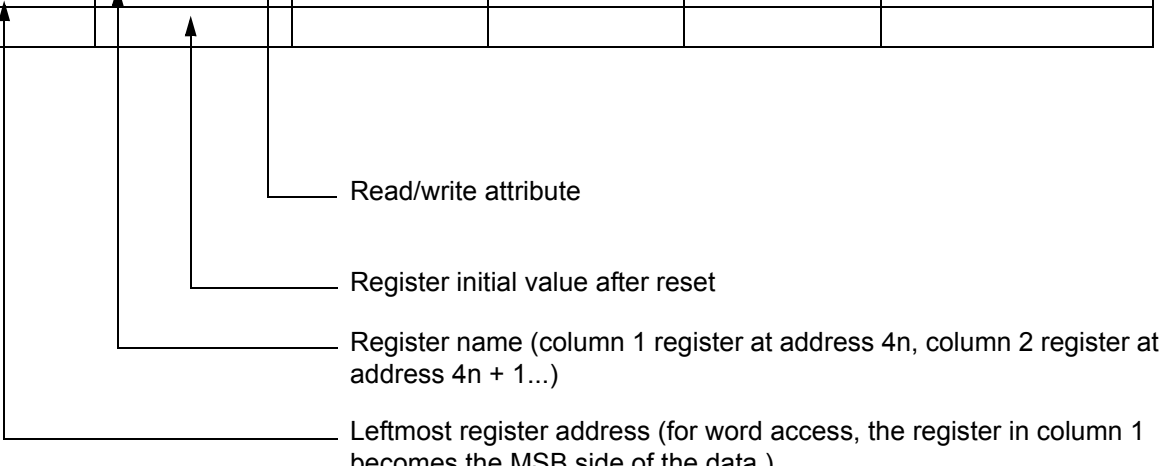
■ MB91F464Ax

MB91F464Ax	
00000000 _H	I/O (direct addressing area)
00000400 _H	I/O
00001000 _H	DMA
00002000 _H	
00007000 _H	Flash memory control
00008000 _H	
0000B000 _H	Boot ROM (4 Kbytes)
0000C000 _H	CAN
0000D000 _H	
0002E000 _H	D-RAM (0 wait, 8 Kbytes)
00030000 _H	ID-RAM (8 Kbytes)
00032000 _H	
00040000 _H	
00080000 _H	
000A0000 _H	Flash memory (384Kbytes)
00100000 _H	
00148000 _H	Flash memory (32 Kbytes)
00150000 _H	
FFFFFFF _H	
Note:	Access prohibited areas

12. I/O Map

■ MB91F464Ax

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Read/write attribute

Register initial value after reset

Register name (column 1 register at address 4n, column 2 register at address 4n + 1...)

Leftmost register address (for word access, the register in column 1 becomes the MSB side of the data.)

Note : Initial values of register bits are represented as follows:

“ 1 ” : Initial value “ 1 ”

“ 0 ” : Initial value “ 0 ”

“ X ” : Initial value “ undefined ”

“ - ” : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H to 000008 _H	Reserved				R-bus Port Data Register
00000C _H	Reserved		PDR14 [R/W] XXXXXXXX	PDR15 [R/W] -- XXXXXX	
000010 _H	PDR16 [R/W] X - - - - - XX	PDR17 [R/W] XXXXXXXXXX	Reserved	PDR19 [R/W] - - - - - XXX	
000014 _H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - XXX - XXX	PDR22 [R/W] - - XX - - XX	Reserved	
000018 _H	PDR24 [R/W] XXXXXXXXXX	Reserved		PDR27 [R/W] XXXXXXXXXX	
00001C _H	PDR28 [R/W] - - - XXXXX	PDR29 [R/W] XXXXXXXXXX	Reserved		
000020 _H to 00002C _H	Reserved				Reserved
000030 _H	EIRR0 [R/W] XXXXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External Interrupt (INT0 to INT7)
000034 _H	EIRR1 [R/W] XXXXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External Interrupt (INT8 to INT15)
000038 _H	DICR [R/W] - - - - - 0	HRCL [R/W] 0 - - 11111	Reserved		Delay Interrupt
00003C _H	Reserved				Reserved
000040 _H	SCR00 [R/W, W] 00000000	SMR00 [R/W, W] 00000000	SSR00 [R/W, R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044 _H	ESCR00 [R/W] 00000X00	ECCR00 [R/W, R, W] -00000XX	Reserved		
000048 _H	SCR01 [R/W, W] 00000000	SMR01 [R/W, W] 00000000	SSR01 [R/W, R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
00004C _H	ESCR01 [R/W] 00000X00	ECCR01 [R/W, R, W] -00000XX	Reserved		
000050 _H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054 _H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	Reserved		

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000058 _H	SCR03 [R/W, W] 00000000	SMR03 [R/W, W] 00000000	SSR03 [R/W, R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
00005C _H	ESCR03 [R/W] 00000X00	ECCR03 [R/W, R, W] -00000XX	Reserved		
000060 _H	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064 _H	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068 _H to 00007C _H	Reserved				Reserved
000080 _H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baudrate Generator LIN-USART 0 to 4
000084 _H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088 _H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	Reserved		
00008C _H to 0000CC _H	Reserved				Reserved
0000D0 _H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - 00	ITBAL0 [R/W] 00000000	I ² C 0
0000D4 _H	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8 _H	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] 00011111	Reserved	
0000DC _H to 0000FC _H	Reserved				Reserved
000100 _H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104 _H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108 _H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
00010C _H	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000110 _H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114 _H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118 _H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
00011C _H	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120 _H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124 _H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128 _H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
00012C _H	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130 _H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134 _H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138 _H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013C _H	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140 _H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144 _H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148 _H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014C _H	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150 _H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154 _H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158 _H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015C _H	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000160 _H to 00017C _H	Reserved				Reserved
000180 _H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184 _H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188 _H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
00018C _H	OCS01 [R/W] --- 0 -- 00 0000 -- 00		OCS23 [R/W] --- 0 -- 00 0000 -- 00		Output Compare 0 to 3
000190 _H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194 _H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198 _H , 00019C _H	Reserved				Reserved
0001A0 _H	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4 _H	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8 _H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] --- 00000	ADECH [R/W] --- 00000	
0001AC _H	Reserved				Reserved
0001B0 _H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
0001B4 _H	Reserved		TMCSRH0 [R/W] --- 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8 _H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
0001BC _H	Reserved		TMCSRH1 [R/W] --- 00000	TMCSRL1 [R/W] 0 - 000000	
0001C0 _H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
0001C4 _H	Reserved		TMCSRH2 [R/W] --- 00000	TMCSRL2 [R/W] 0 - 000000	

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001C8 _H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
0001CC _H	Reserved		TMCSRH3 [R/W] --- 00000	TMCSRL3 [R/W] 0 - 000000	
0001D0 _H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
0001D4 _H	Reserved		TMCSRH4 [R/W] --- 00000	TMCSRL4 [R/W] 0 - 000000	
0001D8 _H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
0001DC _H	Reserved		TMCSRH5 [R/W] --- 00000	TMCSRL5 [R/W] 0 - 000000	
0001E0 _H	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
0001E4 _H	Reserved		TMCSRH6 [R/W] --- 00000	TMCSRL6 [R/W] 0 - 000000	
0001E8 _H	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (ADC)
0001EC _H	Reserved		TMCSRH7 [R/W] --- 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0 _H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
0001F4 _H	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
0001F8 _H	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU1)
0001FC _H	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU3)

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000200 _H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208 _H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C _H	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210 _H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214 _H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 _H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220 _H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224 _H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228 _H to 00023C _H	Reserved				
000240 _H	DMACR [R/W] 00 - - 0000	Reserved			
000244 _H to 0002CC _H	Reserved				Reserved
0002D0 _H	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
0002D4 _H	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
0002D8 _H	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
0002DC _H	OCS45 [R/W] - - - 0 - - 00 0000 - - 00		Reserved		Output Compare 4, 5
0002E0 _H	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
0002E4 _H to 0002EC _H	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0002F0 _H	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU4, ICU5)
0002F4 _H	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU6, ICU7)
0002F8 _H	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU4, OCU5)
0002FC _H	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7
000300 _H to 00038C _H	Reserved				Reserved
000390 _H	ROMS [R] 11111111 01000011		Reserved		ROM Select Register
000394 _H to 0003EC _H	Reserved				Reserved
0003F0 _H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4 _H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H to 00043C _H	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440 _H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444 _H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448 _H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044C _H	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450 _H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454 _H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458 _H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045C _H	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460 _H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464 _H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468 _H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046C _H	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470 _H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474 _H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478 _H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
00047C _H	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480 _H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] X0000X00	CTBR [W] XXXXXXXX	Clock Control
000484 _H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488 _H	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00048C _H	PLLDIVM [R/W] --- 00000	PLLDIVN [R/W] -- 000000	PLLDIVG [R/W] ---- 0000	PLLMULG [W] 00000000	PLL Interface
000490 _H	PLLCTRL [R/W] ---- 0000	Reserved			
000494 _H	OSCC1 [R/W] ----- 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] ----- 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498 _H	PORTEN [R/W] ----- 00	Reserved			Port Input Enable Control
0004A0 _H	Reserved	WTCER [R/W] ----- 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4 _H	Reserved	WTBR [R/W] --- XXXXX XXXXXXXX XXXXXXXX			
0004A8 _H	WTHR [R/W] --- 00000	WTMR [R/W] -- 000000	WTSR [R/W] -- 000000	Reserved	
0004AC _H	CSVTR [R/W] --- 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	Reserved	Clock Supervisor / Selector
0004B0 _H	CUCR [R/W] ----- 0 -- 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
0004B4 _H	CUTR1 [R] ----- 00000000		CUTR2 [R] 00000000 00000000		
0004B8 _H	CMPR [R/W] -- 000010 11111101		Reserved	CMCR [R/W] - 001 -- 00	Clock Modulator
0004BC _H	CMT1 [R/W] 00000000 1 --- 0000		CMT2 [R/W] -- 000000 -- 000000		
0004C0 _H	CANPRE [R/W] 0 --- 0000	CANCKD [R/W] --- 0 ----	Reserved		CAN Clock Control
0004C4 _H	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] ----- 00	HWWD [R/W, W] 00011000	Low Voltage Detection / Hardware Watchdog
0004C8 _H	OSCRH [R/W] 000 -- 001	OSCRL [R/W] ----- 000	WPCRH [R/W] 00 --- 000	WPCRL [R/W] ----- 00	Main/Sub Oscillation Stabilisation Timer
0004CC _H	OSCCR [R/W] ----- 0	Reserved	REGSEL [R/W] -- 000110	REGCTR [R/W] --- 0 -- 00	Main Oscillation Standby Control / Main/Sub Regulator Control
0004D0 _H to 000D08 _H	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D0C _H	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] -- XXXXXX	R-bus Port Data Direct Read Register
000D10 _H	PDRD16 [R] X - - - - XX	PDRD17 [R] XXXXXXXX	Reserved	PDRD19 [R] - - - - - XXX	
000D14 _H	PDRD20 [R] - XXX - XXX	PDRD21 [R] - XXX - XXX	PDRD22 [R] - - XX - - XX	Reserved	
000D18 _H	PDRD24 [R] XXXXXXXX	Reserved		PDRD27 [R] XXXXXXXX	
000D1C _H	PDRD28 [R] - - - XXXXX	PDRD29 [R] XXXXXXXX	Reserved		
000D20 _H to 000D48 _H	Reserved				Reserved
000D4C _H	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] - - 000000	R-bus Port Direction Register
000D50 _H	DDR16 [R/W] 0 - - - - 00	DDR17 [R/W] 00000000	Reserved	DDR19 [R/W] - - - - - 000	
000D54 _H	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - 000 - 000	DDR22 [R/W] - - 00 - - 00	Reserved	
000D58 _H	DDR24 [R/W] 00000000	Reserved		DDR27 [R/W] 00000000	
000D5C _H	DDR28 [R/W] - - - 00000	DDR29 [R/W] 00000000	Reserved		
000D60 _H to 000D88 _H	Reserved				Reserved
000D8C _H	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] - - 000000	R-bus Port Function Register
000D90 _H	PFR16 [R/W] 0 - - - - 00	PFR17 [R/W] 00000000	Reserved	PFR19 [R/W] - - - - - 000	
000D94 _H	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - 000 - 000	PFR22 [R/W] - - 00 - - 00	Reserved	
000D98 _H	PFR24 [R/W] 00000000	Reserved		PFR27 [R/W] 00000000	
000D9C _H	PFR28 [R/W] - - - 00000	PFR29 [R/W] 00000000	Reserved		
000DA0 _H to 000DC8 _H	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000DCC _H	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] -- 000000	R-bus Expansion Port Function Register
000DD0 _H	EPFR16 [R/W] 0 -----	EPFR17 [R/W] -----	Reserved	EPFR19 [R/W] ----- 0 --	
000DD4 _H	EPFR20 [R/W] - 0 - - 0 - -	EPFR21 [R/W] - 0 - - 0 - -	EPFR22 [R/W] -----	Reserved	
000DD8 _H	EPFR24 [R/W] -----	Reserved		EPFR27 [R/W] 00000000	
000DDC _H	Reserved	EPFR29 [R/W] -----	Reserved		
000DE0 _H to 000E08 _H	Reserved				Reserved
000E0C _H	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] -- 000000	R-bus Port Output Drive Select Register
000E10 _H	PODR16 [R/W] 0 - - - - 00	PODR17 [R/W] 00000000	Reserved	PODR19 [R/W] - - - - 000	
000E14 _H	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - 000 - 000	PODR22 [R/W] - - 00 - - 00	Reserved	
000E18 _H	PODR24 [R/W] 00000000	Reserved		PODR27 [R/W] 00000000	
000E1C _H	PODR28 [R/W] - - - 00000	PODR29 [R/W] 00000000	Reserved		
000E20 _H to 000E48 _H	Reserved				Reserved
000E4C _H	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] -- 000000	R-bus Pin Input Level Select Register
000E50 _H	PILR16 [R/W] 0 - - - - 00	PILR17 [R/W] 00000000	Reserved	PILR19 [R/W] - - - - 000	
000E54 _H	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - 000 - 000	PILR22 [R/W] - - 00 - - 00	Reserved	
000E58 _H	PILR24 [R/W] 00000000	Reserved		PILR27 [R/W] 00000000	
000E5C _H	PILR28 [R/W] - - - 00000	PILR29 [R/W] 00000000	Reserved		
000E60 _H to 000E88 _H	Reserved				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E8C _H	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] - - 000000	R-bus Expansion Port Input Level Select Register
000E90 _H	EPILR16 [R/W] 0 - - - - 00	EPILR17 [R/W] 00000000	Reserved	EPILR19 [R/W] - - - - 000	
000E94 _H	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - 000 - 000	EPILR22 [R/W] - - 00 - - 00	Reserved	
000E98 _H	EPILR24 [R/W] 00000000	Reserved		EPILR27 [R/W] 00000000	
000E9C _H	EPILR28 [R/W] - - - 00000	EPILR29 [R/W] 00000000	Reserved		
000EA0 _H to 000EC8 _H	Reserved				Reserved
000ECC _H	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] - - 000000	R-bus Port Pull-Up/Down Enable Register
000ED0 _H	PPER16 [R/W] 0 - - - - 00	PPER17 [R/W] 00000000	Reserved	PPER19 [R/W] - - - - 000	
000ED4 _H	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - 000 - 000	PPER22 [R/W] - - 00 - - 00	Reserved	
000ED8 _H	PPER24 [R/W] 00000000	Reserved		PPER27 [R/W] 00000000	
000EDC _H	PPER28 [R/W] - - - 00000	PPER29 [R/W] 00000000	Reserved		
000EE0 _H to 000F08 _H	Reserved				Reserved
000F0C _H	Reserved		PPCR14 [R/W] 11111111	PPCR15 [R/W] - - 111111	R-bus Port Pull-Up/Down Control Register
000F10 _H	PPCR16 [R/W] 1- - - - 11	PPCR17 [R/W] 11111111	Reserved	PPCR19 [R/W] - 1- - 111	
000F14 _H	PPCR20 [R/W] - 111 - 111	PPCR21 [R/W] - 111 - 111	PPCR22 [R/W] - - 11 - - 11	Reserved	
000F18 _H	PPCR24 [R/W] 11111111	Reserved		PPCR27 [R/W] 11111111	
000F1C _H	PPCR28 [R/W] - - - 11111	PPCR29 [R/W] 11111111	Reserved		
000F20 _H to 000F3C _H	Reserved				Reserved

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001000 _H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004 _H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008 _H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100C _H	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010 _H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014 _H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018 _H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101C _H	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020 _H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024 _H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028 _H to 006FFC _H	Reserved				Reserved
007000 _H	FMCS [R/W] 01101000	FMCR [R] --- 00000	FCHCR [R/W] ----- 00 10000011		Flash Memory/ Control Register
007004 _H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 ----	FMPS [R/W] ----- 000	
007008 _H	FMAC [R] 00000000 00000000 00000000 00000000				
00700C _H to 007FFC _H	Reserved				Reserved
008000 _H to 00BFFC _H	MB91F464Ax Boot-ROM size is 4 Kbytes : 00B000 _H to 00BFFC _H (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
00C000 _H to 00C3FC _H	Reserved				Reserved

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C400 _H	CTRLR4 [R/W] 00000000 00000001		STATR4 [R/W] 00000000 00000000		CAN 4 Control Register
00C404 _H	ERRCNT4 [R] 00000000 00000000		BTR4 [R/W] 00100011 00000001		
00C408 _H	INTR4 [R] 00000000 00000000		TESTR4 [R/W] 00000000 X0000000		
00C40C _H	BRPE4 [R/W] 00000000 00000000		Reserved		
00C410 _H	IF1CREQ4 [R/W] 00000000 00000001		IF1CMSK4 [R/W] 00000000 00000000		CAN 4 IF 1 Register
00C414 _H	IF1MSK24 [R/W] 11111111 11111111		IF1MSK14 [R/W] 11111111 11111111		
00C418 _H	IF1ARB24 [R/W] 00000000 00000000		IF1ARB14 [R/W] 00000000 00000000		
00C41C _H	IF1MCTR4 [R/W] 00000000 00000000		Reserved		
00C420 _H	IF1DTA14 [R/W] 00000000 00000000		IF1DTA24 [R/W] 00000000 00000000		
00C424 _H	IF1DTB14 [R/W] 00000000 00000000		IF1DTB24 [R/W] 00000000 00000000		
00C428 _H to 00C42C _H	Reserved				
00C430 _H	IF1DTA24 [R/W] 00000000 00000000		IF1DTA14 [R/W] 00000000 00000000		
00C434 _H	IF1DTB24 [R/W] 00000000 00000000		IF1DTB14 [R/W] 00000000 00000000		
00C438 _H , 00C43C _H	Reserved				

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C440 _H	IF2CREQ4 [R/W] 00000000 00000001		IF2CMSK4 [R/W] 00000000 00000000		CAN 4 IF 2 Register
00C444 _H	IF2MSK24 [R/W] 11111111 11111111		IF2MSK14 [R/W] 11111111 11111111		
00C448 _H	IF2ARB24 [R/W] 00000000 00000000		IF2ARB14 [R/W] 00000000 00000000		
00C44C _H	IF2MCTR4 [R/W] 00000000 00000000		Reserved		
00C450 _H	IF2DTA14 [R/W] 00000000 00000000		IF2DTA24 [R/W] 00000000 00000000		
00C454 _H	IF2DTB14 [R/W] 00000000 00000000		IF2DTB24 [R/W] 00000000 00000000		
00C458 _H , 00C45C _H	Reserved				
00C460 _H	IF2DTA24 [R/W] 00000000 00000000		IF2DTA14 [R/W] 00000000 00000000		
00C464 _H	IF2DTB24 [R/W] 00000000 00000000		IF2DTB14 [R/W] 00000000 00000000		
00C468 _H to 00C47C _H	Reserved				
00C480 _H	TREQR24 [R] 00000000 00000000		TREQR14 [R] 00000000 00000000		CAN 4 Status Flags
00C484 _H to 00C48C _H	Reserved				
00C490 _H	NEWDT24 [R] 00000000 00000000		NEWDT14 [R] 00000000 00000000		
00C494 _H to 00C49C _H	Reserved				
00C4A0 _H	INTPND24 [R] 00000000 00000000		INTPND14 [R] 00000000 00000000		
00C4A4 _H to 00C4AC _H	Reserved				
00C4B0 _H	MSGVAL24 [R] 00000000 00000000		MSGVAL14 [R] 00000000 00000000		
00C4B4 _H to 00EFC _H	Reserved				Reserved

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00F00 _H	BCTRL [R/W] ----- 11111100 00000000				EDSU / MPU
00F004 _H	BSTAT [R/W] ----- 000 00000000 10 -- 0000				
00F008 _H	BIAC [R] ----- 00000000				
00F00C _H	BOAC [R] ----- 00000000				
00F010 _H	BIRQ [R/W] ----- 00000000				
00F014 _H to 00F01C _H	Reserved				
00F020 _H	BCR0 [R/W] ----- 00000000 00000000 00000000				
00F024 _H	BCR1 [R/W] ----- 00000000 00000000 00000000				
00F028 _H to 00F07C _H	Reserved				Reserved
00F080 _H	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F084 _H	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F088 _H	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F08C _H	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F090 _H	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F094 _H	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F098 _H	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F09C _H	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A0 _H to 01FFFC _H	Reserved				Reserved

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
020000 _H to 02FFFC _H	MB91F464Ax D-RAM size is 8 Kbytes : 02E000 _H to 02FFFC _H (data access is 0 wait cycles)				D-RAM area
030000 _H to 03FFFC _H	MB91F464Ax ID-RAM size is 8 Kbytes : 030000 _H to 031FFC _H (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

*1 : depends on the number of available CAN channels

*2 : ACR0 [11 : 10] depends on bus width setting in Mode vector fetch information

*3 : TCR [3 : 0] INIT value = 0000, keeps value after RST

12.1 Flash memory and external bus area

12.1.1 MB91F464Ax

32bit read mode	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000 _H to 05FFF8 _H	reserved				reserved				ROMS0
060000 _H to 07FFF8 _H	reserved				reserved				ROMS1
080000 _H to 09FFF8 _H	reserved				reserved				ROMS2
0A0000 _H to 0BFFF8 _H	SA14 (64KB)				SA15 (64KB)				ROMS3
0C0000 _H to 0DFFF8 _H	SA16 (64KB)				SA17 (64KB)				ROMS4
0E0000 _H to 0FFFF0 _H	SA18 (64KB)				SA19 (64KB)				ROMS5
0FFFF8 _H	FMV [R] 06 00 00 00 _H				FRV [R] 00 00 BF F8 _H				
100000 _H to 11FFF8 _H	reserved				reserved				ROMS6
120000 _H to 13FFF8 _H	reserved				reserved				
140000 _H to 143FF8 _H	reserved				reserved				ROMS7
144000 _H to 17FF8 _H	reserved				reserved				
148000 _H to 14BFF8 _H	SA4 (8KB)				SA5 (8KB)				
14C000 _H to 14FFF8 _H	SA6 (8KB)				SA7 (8KB)				
150000 _H to 17FFF8 _H	Reserved								

32bit read mode	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000 _H to 1BFFF8 _H	Reserved								ROMS8
1C0000 _H to 1FFFF8 _H									ROMS9
200000 _H to 27FFF8 _H									ROMS10
280000 _H to 2FFFF8 _H									ROMS11
300000 _H to 37FFF8 _H									ROMS12
380000 _H to 3FFFF8 _H									ROMS13
400000 _H to 47FFF8 _H									ROMS14
480000 _H to 4FFFF8 _H									ROMS15

Note: Write operations to address 0FFFF8_H and 0FFFC_H are not possible. When reading these addresses, the values shown above will be read.

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	—	—	3FC _H	000FFFFC _H	—
Mode vector	1	01	—	—	3F8 _H	000FFFF8 _H	—
System reserved	2	02	—	—	3F4 _H	000FFFF4 _H	—
System reserved	3	03	—	—	3F0 _H	000FFFF0 _H	—
System reserved	4	04	—	—	3EC _H	000FFFE _C	—
CPU supervisor mode (INT #5 instruction) *5	5	05	—	—	3E8 _H	000FFFE8 _H	—
Memory Protection exception *5	6	06	—	—	3E4 _H	000FFFE4 _H	—
System reserved	7	07	—	—	3E0 _H	000FFFE0 _H	—
System reserved	8	08	—	—	3DC _H	000FFFD _C	—
System reserved	9	09	—	—	3D8 _H	000FFFD8 _H	—
System reserved	10	0A	—	—	3D4 _H	000FFFD4 _H	—
System reserved	11	0B	—	—	3D0 _H	000FFFD0 _H	—
System reserved	12	0C	—	—	3CC _H	000FFFC _C	—
System reserved	13	0D	—	—	3C8 _H	000FFFC8 _H	—
Undefined instruction exception	14	0E	—	—	3C4 _H	000FFFC4 _H	—
NMI request	15	0F	F _H fixed		3C0 _H	000FFFC0 _H	—
External Interrupt 0	16	10	ICR00	440 _H	3BC _H	000FFFB _C	0, 16
External Interrupt 1	17	11			3B8 _H	000FFFB8 _H	1, 17
External Interrupt 2	18	12	ICR01	441 _H	3B4 _H	000FFFB4 _H	2, 18
External Interrupt 3	19	13			3B0 _H	000FFFB0 _H	3, 19
External Interrupt 4	20	14	ICR02	442 _H	3AC _H	000FFFA _C	20
External Interrupt 5	21	15			3A8 _H	000FFFA8 _H	21
External Interrupt 6	22	16	ICR03	443 _H	3A4 _H	000FFFA4 _H	22
External Interrupt 7	23	17			3A0 _H	000FFFA0 _H	23
Reserved	24	18	ICR04	444 _H	39C _H	000FFF9 _C	—
Reserved	25	19			398 _H	000FFF98 _H	—
Reserved	26	1A	ICR05	445 _H	394 _H	000FFF94 _H	—
Reserved	27	1B			390 _H	000FFF90 _H	—
External Interrupt 12	28	1C	ICR06	446 _H	38C _H	000FFF8 _C	—
Reserved	29	1D			388 _H	000FFF88 _H	—
External Interrupt 14	30	1E	ICR07	447 _H	384 _H	000FFF84 _H	—
Reserved	31	1F			380 _H	000FFF80 _H	—

(Continued)

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 0	32	20	ICR08	448 _H	37C _H	000FFF7C _H	4, 32
Reload Timer 1	33	21			378 _H	000FFF78 _H	5, 33
Reload Timer 2	34	22	ICR09	449 _H	374 _H	000FFF74 _H	34
Reload Timer 3	35	23			370 _H	000FFF70 _H	35
Reload Timer 4	36	24	ICR10	44A _H	36C _H	000FFF6C _H	36
Reload Timer 5	37	25			368 _H	000FFF68 _H	37
Reload Timer 6	38	26	ICR11	44B _H	364 _H	000FFF64 _H	38
Reload Timer 7	39	27			360 _H	000FFF60 _H	39
Free Run Timer 0	40	28	ICR12	44C _H	35C _H	000FFF5C _H	40
Free Run Timer 1	41	29			358 _H	000FFF58 _H	41
Free Run Timer 2	42	2A	ICR13	44D _H	354 _H	000FFF54 _H	42
Free Run Timer 3	43	2B			350 _H	000FFF50 _H	43
Free Run Timer 4	44	2C	ICR14	44E _H	34C _H	000FFF4C _H	44
Free Run Timer 5	45	2D			348 _H	000FFF48 _H	45
Free Run Timer 6	46	2E	ICR15	44F _H	344 _H	000FFF44 _H	46
Free Run Timer 7	47	2F			340 _H	000FFF40 _H	47
Reserved	48	30	ICR16	450 _H	33C _H	000FFF3C _H	–
Reserved	49	31			338 _H	000FFF38 _H	–
Reserved	50	32	ICR17	451 _H	334 _H	000FFF34 _H	–
Reserved	51	33			330 _H	000FFF30 _H	–
CAN 4	52	34	ICR18	452 _H	32C _H	000FFF2C _H	–
Reserved	53	35			328 _H	000FFF28 _H	–
LIN-USART 0 RX	54	36	ICR19	453 _H	324 _H	000FFF24 _H	6, 48
LIN-USART 0 TX	55	37			320 _H	000FFF20 _H	7, 49
LIN-USART 1 RX	56	38	ICR20	454 _H	31C _H	000FFF1C _H	8, 50
LIN-USART 1 TX	57	39			318 _H	000FFF18 _H	9, 51
LIN-USART 2 RX	58	3A	ICR21	455 _H	314 _H	000FFF14 _H	52
LIN-USART 2 TX	59	3B			310 _H	000FFF10 _H	53
LIN-USART 3 RX	60	3C	ICR22	456 _H	30C _H	000FFF0C _H	54
LIN-USART 3 TX	61	3D			308 _H	000FFF08 _H	55
System reserved	62	3E	ICR23 *3	457 _H	304 _H	000FFF04 _H	–
Delayed Interrupt	63	3F			300 _H	000FFF00 _H	–

(Continued)

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved *4	64	40	(ICR24)	(458 _H)	2FC _H	000FFEFC _H	–
System reserved *4	65	41			2F8 _H	000FFE8 _H	–
LIN-USART (FIFO) 4 RX	66	42	ICR25	459 _H	2F4 _H	000FFE4 _H	10, 56
LIN-USART (FIFO) 4 TX	67	43			2F0 _H	000FEE0 _H	11, 57
Reserved	68	44	ICR26	45A _H	2EC _H	000FEEC _H	12, 58
Reserved	69	45			2E8 _H	000FEE8 _H	13, 59
Reserved	70	46	ICR27	45B _H	2E4 _H	000FEE4 _H	60
Reserved	71	47			2E0 _H	000FEE0 _H	61
Reserved	72	48	ICR28	45C _H	2DC _H	000FFEDC _H	62
Reserved	73	49			2D8 _H	000FFED8 _H	63
I ² C 0	74	4A	ICR29	45D _H	2D4 _H	000FFED4 _H	–
Reserved	75	4B			2D0 _H	000FFED0 _H	–
Reserved	76	4C	ICR30	45E _H	2CC _H	000FFEC _H	64
Reserved	77	4D			2C8 _H	000FFEC8 _H	65
Reserved	78	4E	ICR31	45F _H	2C4 _H	000FFEC4 _H	66
Reserved	79	4F			2C0 _H	000FFEC0 _H	67
Reserved	80	50	ICR32	460 _H	2BC _H	000FFEC _H	68
Reserved	81	51			2B8 _H	000FFEB8 _H	69
Reserved	82	52	ICR33	461 _H	2B4 _H	000FFEB4 _H	70
Reserved	83	53			2B0 _H	000FFEB0 _H	71
Reserved	84	54	ICR34	462 _H	2AC _H	000FFEA _H	72
Reserved	85	55			2A8 _H	000FFEA8 _H	73
Reserved	86	56	ICR35	463 _H	2A4 _H	000FFEA4 _H	74
Reserved	87	57			2A0 _H	000FFEA0 _H	75
Reserved	88	58	ICR36	464 _H	29C _H	000FFE9C _H	76
Reserved	89	59			298 _H	000FFE98 _H	77
Reserved	90	5A	ICR37	465 _H	294 _H	000FFE94 _H	78
Reserved	91	5B			290 _H	000FFE90 _H	79
Input Capture 0	92	5C	ICR38	466 _H	28C _H	000FFE8C _H	80
Input Capture 1	93	5D			288 _H	000FFE88 _H	81
Input Capture 2	94	5E	ICR39	467 _H	284 _H	000FFE84 _H	82
Input Capture 3	95	5F			280 _H	000FFE80 _H	83

(Continued)

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Input Capture 4	96	60	ICR40	468 _H	27C _H	000FFE7C _H	84
Input Capture 5	97	61			278 _H	000FFE78 _H	85
Input Capture 6	98	62	ICR41	469 _H	274 _H	000FFE74 _H	86
Input Capture 7	99	63			270 _H	000FFE70 _H	87
Output Compare 0	100	64	ICR42	46A _H	26C _H	000FFE6C _H	88
Output Compare 1	101	65			268 _H	000FFE68 _H	89
Output Compare 2	102	66	ICR43	46B _H	264 _H	000FFE64 _H	90
Output Compare 3	103	67			260 _H	000FFE60 _H	91
Output Compare 4	104	68	ICR44	46C _H	25C _H	000FFE5C _H	92
Output Compare 5	105	69			258 _H	000FFE58 _H	93
Reserved	106	6A	ICR45	46D _H	254 _H	000FFE54 _H	94
Reserved	107	6B			250 _H	000FFE50 _H	95
Reserved	108	6C	ICR46	46E _H	24C _H	000FFE4C _H	–
Reserved	109	6D			248 _H	000FFE48 _H	–
System reserved	110	6E	ICR47 *3	46F _H	244 _H	000FFE44 _H	–
System reserved	111	6F			240 _H	000FFE40 _H	–
PPG0	112	70	ICR48	470 _H	23C _H	000FFE3C _H	15, 96
PPG1	113	71			238 _H	000FFE38 _H	97
PPG2	114	72	ICR49	471 _H	234 _H	000FFE34 _H	98
PPG3	115	73			230 _H	000FFE30 _H	99
PPG4	116	74	ICR50	472 _H	22C _H	000FFE2C _H	100
PPG5	117	75			228 _H	000FFE28 _H	101
PPG6	118	76	ICR51	473 _H	224 _H	000FFE24 _H	102
PPG7	119	77			220 _H	000FFE20 _H	103
PPG8	120	78	ICR52	474 _H	21C _H	000FFE1C _H	104
PPG9	121	79			218 _H	000FFE18 _H	105
Reserved	122	7A	ICR53	475 _H	214 _H	000FFE14 _H	106
Reserved	123	7B			210 _H	000FFE10 _H	107
Reserved	124	7C	ICR54	476 _H	20C _H	000FFE0C _H	108
Reserved	125	7D			208 _H	000FFE08 _H	109
Reserved	126	7E	ICR55	477 _H	204 _H	000FFE04 _H	110
Reserved	127	7F			200 _H	000FFE00 _H	111

(Continued)

(Continued)

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	128	80	ICR56	478 _H	1FC _H	000FFDFC _H	–
Reserved	129	81			1F8 _H	000FFDF8 _H	–
Reserved	130	82	ICR57	479 _H	1F4 _H	000FFDF4 _H	–
Reserved	131	83			1F0 _H	000FFDF0 _H	–
Real Time Clock	132	84	ICR58	47A _H	1EC _H	000FFDEC _H	–
Calibration Unit	133	85			1E8 _H	000FFDE8 _H	–
A/D Converter 0	134	86	ICR59	47B _H	1E4 _H	000FFDE4 _H	14, 112
Reserved	135	87			1E0 _H	000FFDE0 _H	–
Reserved	136	88	ICR60	47C _H	1DC _H	000FFDDC _H	–
Reserved	137	89			1D8 _H	000FFDD8 _H	–
Low Voltage Detection	138	8A	ICR61	47D _H	1D4 _H	000FFDD4 _H	–
Reserved	139	8B			1D0 _H	000FFDD0 _H	–
Timebase Overflow	140	8C	ICR62	47E _H	1CC _H	000FFDCC _H	–
PLL Clock Gear	141	8D			1C8 _H	000FFDC8 _H	–
DMA Controller	142	8E	ICR63	47F _H	1C4 _H	000FFDC4 _H	–
Main/Sub OSC stability wait	143	8F			1C0 _H	000FFDC0 _H	–
Security vector	144	90	–	–	1BC _H	000FFDBC _H	–
Used by the INT instruction.	145 to 255	91 to FF	–	–	1B8 _H to 000 _H	000FFDB8 _H to 000FFC00 _H	–

*1 : The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (000FFC00_H) . The TBR is initialized to this value by a reset. The TBR is set to 000FFC00_H after the internal boot ROM is executed.

*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0C03_H : IOS[0])

*4 : Used by REALOS

*5 : Memory Protection Unit (MPU) support

14. Recommended Settings

14.1 PLL and Clockgear settings

Please note that for MB91F464Ax the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	*1
4	2	24	16	24	192	96	*1
4	2	23	16	24	184	92	*1
4	2	22	16	24	176	88	*1
4	2	21	16	20	168	84	*1
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

*1 This setting is not possible at MB91F464Ax

14.2 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 48MHz. Base clock frequencies above 48 MHz are not allowed on MB91F465Kx.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	*1
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	*1
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	*1
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	*1

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	*1
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	*1
8	3	1068	44	28.9	92.1	*1
1	3	026F	40	37	43.6	
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	*1
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	*1
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	*1
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	*1
9	3	1267	40	25.3	95.8	*1
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	
1	11	036B	36	27.1	53.8	
1	13	03AA	36	25.8	59.3	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	*1
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	*1
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	*1
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	
5	5	0AA6	32	19.5	89.1	*1
6	3	0C6A	32	23	52.5	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	*1

*1 These settings are not possible at MB91F464Ax

15. Electrical Characteristics

15.1 Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	–	–	50	V/ms	
Power supply voltage 1*1	V _{DD5R}	– 0.3	+ 6.0	V	
Power supply voltage 2*1	V _{DD5}	– 0.3	+ 6.0	V	
Relationship of the supply voltages	AV _{CC5}	V _{DD5} -0.3	V _{DD5} +0.3	V	At least one pin of the Ports 25 to 29 (ANn) is used as digital input or output
		V _{SS5} -0.3	V _{DD5} +0.3	V	All pins of the Ports 25 to 29 (ANn) follow the condition of V _{IA}
Analog power supply voltage*1	AV _{CC5}	– 0.3	+ 6.0	V	*2
Analog reference power supply voltage*1	AVRH5	– 0.3	+ 6.0	V	*2
Input voltage 1*1	V _{I1}	V _{SS5} – 0.3	V _{DD5} + 0.3	V	
Analog pin input voltage*1	V _{IA}	AV _{SS5} – 0.3	AV _{CC5} + 0.3	V	
Output voltage 1*1	V _{O1}	V _{SS5} – 0.3	V _{DD5} + 0.3	V	
Maximum clamp current	I _{CLAMP}	– 4.0	+ 4.0	mA	*3
Total maximum clamp current	Σ I _{CLAMP}	–	20	mA	*3
"L" level maximum output current*4	I _{OL}	–	10	mA	
"L" level average output current*5	I _{OLAV}	–	8	mA	
"L" level total maximum output current	ΣI _{OL}	–	100	mA	
"L" level total average output current*6	ΣI _{OLAV}	–	50	mA	
"H" level maximum output current*4	I _{OH}	–	– 10	mA	
"H" level average output current*5	I _{OHAV}	–	– 4	mA	
"H" level total maximum output current	ΣI _{OH}	–	– 100	mA	
"H" level total average output current*6	ΣI _{OHAV}	–	– 25	mA	
Power consumption	P _D	–	600	mW	at T _A = 105 °C
Operating temperature	T _A	– 40	+ 105	°C	
Storage temperature	T _{stg}	– 55	+ 150	°C	

*1 : The parameter is based on V_{SS5} = HV_{SS5} = AV_{SS5} = 0.0 V.

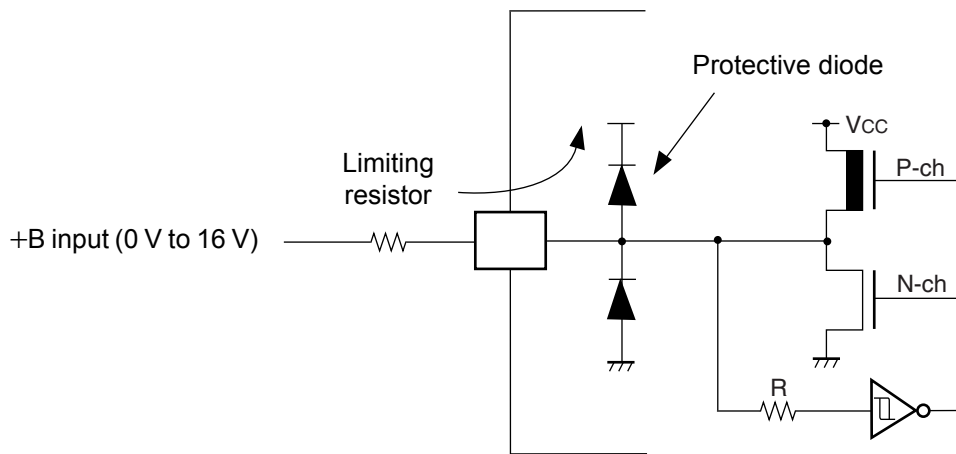
*2 : AV_{CC5} and AVRH5 must not exceed V_{DD5} + 0.3 V.

- *3 :
- Use within recommended operating conditions.
 - Use with DC voltage (current).
 - +B signals are input signals that exceed the V_{DD5} voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
 - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time , either instantaneously or for an extended period, when the +B signal

is input.

- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit :

• Input/output equivalent circuit



- *4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
- *5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.
- *6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

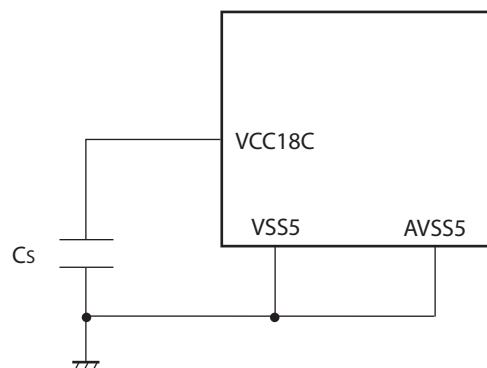
15.2 Recommended operating conditions

($V_{SS5} = AV_{SS5} = 0.0\text{ V}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{DD5}	3.0	–	5.5	V	
	V_{DD5R}	3.0	–	5.5	V	Internal regulator
	AV_{CC5}	3.0	–	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	–	4.7	–	μF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		–	–	50	V/ms	
Operating temperature	T_A	– 40	–	+ 105	$^{\circ}\text{C}$	
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz → 16 ... 100MHz)				0.6	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{\text{discharge}} = 1.5\text{k}\Omega$ $C_{\text{discharge}} = 100\text{pF}$
RC Oscillator	f_{RC100kHz}	50	100	200	kHz	$V_{DD\text{CORE}} \geq 1.65\text{V}$
	f_{RC2MHz}	1	2	4	MHz	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



15.3 DC characteristics

Note: In the following tables, “V_{DD}” means V_{DD5} for all pins.

In the following tables, “V_{SS}” means V_{SS5} for all pins.

(V_{DD5} = AV_{CC5} = 3.0 V to 5.5 V, V_{SS5} = AV_{SS5} = 0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H” voltage	V _{IH}	–	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V _{DD}	–	V _{DD} + 0.3	V	CMOS hysteresis input
		–	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V _{DD}	–	V _{DD} + 0.3	V	4.5 V ≤ V _{DD} ≤ 5.5 V
		–		0.74 × V _{DD}	–	V _{DD} + 0.3	V	3 V ≤ V _{DD} < 4.5 V
		–	AUTOMOTIVE Hysteresis input is selected	0.8 × V _{DD}	–	V _{DD} + 0.3	V	
	V _{IHR}	INITX	–	0.8 × V _{DD}	–	V _{DD} + 0.3	V	INITX input pin (CMOS Hysteresis)
		MD_2 to MD_0	–	V _{DD} – 0.3	–	V _{DD} + 0.3	V	Mode input pins
		X0, X0A	–	2.5	–	V _{DD} + 0.3	V	External clock in “Oscillation mode”
		X0	–	0.8 × V _{DD}	–	V _{DD} + 0.3	V	External clock in “Fast Clock Input mode”
Input “L” voltage	V _{IL}	–	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V _{SS} – 0.3	–	0.2 × V _{DD}	V	
		–	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V _{SS} – 0.3	–	0.3 × V _{DD}	V	
		–	Port inputs if AUTOMOTIVE Hysteresis input is selected	V _{SS} – 0.3	–	0.5 × V _{DD}	V	4.5 V ≤ V _{DD} ≤ 5.5 V
		–		V _{SS} – 0.3	–	0.46 × V _{DD}	V	3 V ≤ V _{DD} < 4.5 V
	V _{ILR}	INITX	–	V _{SS} – 0.3	–	0.2 × V _{DD}	V	INITX input pin (CMOS Hysteresis)
		MD_2 to MD_0	–	V _{SS} – 0.3	–	V _{SS} + 0.3	V	Mode input pins
		X0, X0A	–	V _{SS} – 0.3	–	0.5	V	External clock in “Oscillation mode”

(Continued)

($V_{DD5} = AV_{CC5} = 3.0\text{ V to }5.5\text{ V}$, $V_{SS5} = AV_{SS5} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 2 mA
			$3.0\text{ V} \leq V_{DD} \leq 4.5\text{ V}$, $I_{OH} = -1.6\text{ mA}$					
	V_{OH5}	Normal outputs	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH} = -5\text{ mA}$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 5 mA
			$3.0\text{ V} \leq V_{DD} \leq 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$					
	V_{OH3}	I ² C outputs	$3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
Output “L” voltage	V_{OL2}	Normal outputs	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL} = +2\text{ mA}$	—	—	0.4	V	Driving strength set to 2 mA
			$3.0\text{ V} \leq V_{DD} \leq 4.5\text{ V}$, $I_{OL} = +1.6\text{ mA}$					
	V_{OL5}	Normal outputs	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL} = +5\text{ mA}$	—	—	0.4	V	Driving strength set to 5 mA
			$3.0\text{ V} \leq V_{DD} \leq 4.5\text{ V}$, $I_{OL} = +3\text{ mA}$					
	V_{OL3}	I ² C outputs	$3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL} = +3\text{ mA}$	—	—	0.4	V	
Input leakage current	I_{IL}	Pnn_m *1	$3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ $T_A = 25\text{ }^{\circ}\text{C}$	— 1	—	+ 1	μA	$V_{SS5} < V_I < V_{DD}$
			$3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ $T_A = 105\text{ }^{\circ}\text{C}$	— 3	—	+ 3	μA	
Analog input leakage current	I_{AIN}	ANn *2	$3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ $T_A = 25\text{ }^{\circ}\text{C}$	— 1	—	+ 1	μA	$AV_{SS5} < V_I < AV_{CC5}$, AVRH5
			$3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ $T_A = 105\text{ }^{\circ}\text{C}$	— 3	—	+ 3	μA	

1. Pnn_m includes all GPIO pins. Analog (AN) channels and Pull Up/Pull Down are disabled.

2. ANn includes all pins where AN channels are enabled.

$(V_{DD5} = AV_{CC5} = 3.0 \text{ V to } 5.5 \text{ V}, V_{SS5} = AV_{SS5} = 0 \text{ V}, T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C})$

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance	R_{UP}	Pnn_m *1 INITX	$3.0\text{V} \leq V_{DD} \leq 3.6\text{V}$	40	100	160	k Ω	
			$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m *2	$3.0\text{V} \leq V_{DD} \leq 3.6\text{V}$	40	100	180	k Ω	
			$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$	25	50	100		
Input capacitance	C_{IN}	All except V_{DD5} , V_{DD5R} , V_{SS5} , AV_{CC5} , AV_{SS5} , $AVRH5$	$f = 1 \text{ MHz}$	-	5	15	pF	
Power supply current MB91-F464Ax	I_{CC}	V_{DD5R}	CLKB: 80 MHz CLKP: 40 MHz CLKT: 40 MHz CLKCAN: 40 MHz	-	75	85	mA	Code fetch from Flash
	I_{CCH}	V_{DD5R}	$T_A = +25 \text{ }^{\circ}\text{C}$	-	30	150	μA	At stop mode *3
			$T_A = +105 \text{ }^{\circ}\text{C}$	-	400	2000	μA	
			$T_A = +25 \text{ }^{\circ}\text{C}$	-	100	500	μA	RTC : 4 MHz mode *3
			$T_A = +105 \text{ }^{\circ}\text{C}$	-	500	2400	μA	
			$T_A = +25 \text{ }^{\circ}\text{C}$	-	50	250	μA	RTC : 100 kHz mode *3 32 kHz mode *4
			$T_A = +105 \text{ }^{\circ}\text{C}$	-	450	2200	μA	
	I_{LVE}	V_{DD5}	-	-	70	150	μA	External low voltage detection
	I_{LVI}	V_{DD5R}	-	-	50	100	μA	Internal low voltage detection
	I_{OSC}	V_{DD5}	-	-	250	500	μA	Main clock (4 MHz)
			-	-	20	40	μA	Sub clock (32 kHz)

1. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
2. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
3. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.
4. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled, RC oscillator enabled. Additional current consumption of Sub oscillator I_{OSC} has to be taken into account.

15.4 A/D converter characteristics
 $(V_{DD5} = AV_{CC5} = 3.0 \text{ V to } 5.5 \text{ V}, V_{SS5} = AV_{SS5} = 0 \text{ V}, T_A = -40^\circ\text{C to } +105^\circ\text{C})$

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	– 3	–	+ 3	LSB	
Nonlinearity error	–	–	– 2.5	–	+ 2.5	LSB	
Differential nonlinearity error	–	–	– 1.9	–	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL–1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH–3.5 LSB	AVRH–1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	–	0.6	–	16,500	μs	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			2.0	–	–	μs	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Sampling time	T_{samp}	–	0.4	–	–	μs	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$, $R_{EXT} < 2 \text{ k}\Omega$
			1.0	–	–	μs	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$, $R_{EXT} < 1 \text{ k}\Omega$
Conversion time	T_{conv}	–	1.0	–	–	μs	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			3.0	–	–	μs	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Input capacitance	C_{IN}	ANn	–	–	11	pF	
Input resistance	R_{IN}	ANn	–	–	2.6	kΩ	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			–	–	12.1	kΩ	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Analog input leakage current	I_{AIN}	ANn	– 1	–	+ 1	μA	$T_A = +25^\circ\text{C}$
			– 3	–	+ 3	μA	$T_A = +105^\circ\text{C}$
Analog input voltage range	V_{AIN}	ANn	AVRL	–	AVRH	V	
Offset between input channels	–	ANn	–	–	4	LSB	

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	$0.75 \times AV_{CC5}$	–	AV_{CC5}	V	
	AVRL	AV _{SS} 5	AV_{SS5}	–	$AV_{CC5} \times 0.25$	V	
Power supply current	I _A	AV _{CC} 5	–	2.5	5	mA	A/D Converter active
	I _{AH}	AV _{CC} 5	–	–	5	μA	A/D Converter not operated *1
Reference voltage current	I _R	AVRH5	–	0.7	1	mA	A/D Converter active
	I _{RH}	AVRH5	–	–	5	μA	A/D Converter not operated *2

*1 : Supply current at AV_{CC}5, if the A/D converter is not operating,
(V_{DD}5 = AV_{CC}5 = AVRH = 5.0 V)

*2 : Input current at AVRH5, if A/D converter is not operating, (V_{DD}5 = AV_{CC}5 = AVRH = 5.0 V)

Sampling Time Calculation

$$T_{\text{samp}} = (2.6 \text{ k}\Omega + R_{\text{EXT}}) \times 11\text{pF} \times 7; \text{ for } 4.5\text{V} \leq AV_{CC5} \leq 5.5\text{V}$$

$$T_{\text{samp}} = (12.1 \text{ k}\Omega + R_{\text{EXT}}) \times 11\text{pF} \times 7; \text{ for } 3.0\text{V} \leq AV_{CC5} \leq 4.5\text{V}$$

Conversion Time Calculation

$$T_{\text{conv}} = T_{\text{samp}} + T_{\text{comp}}$$

Definition of A/D converter terms

■ Resolution

Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error

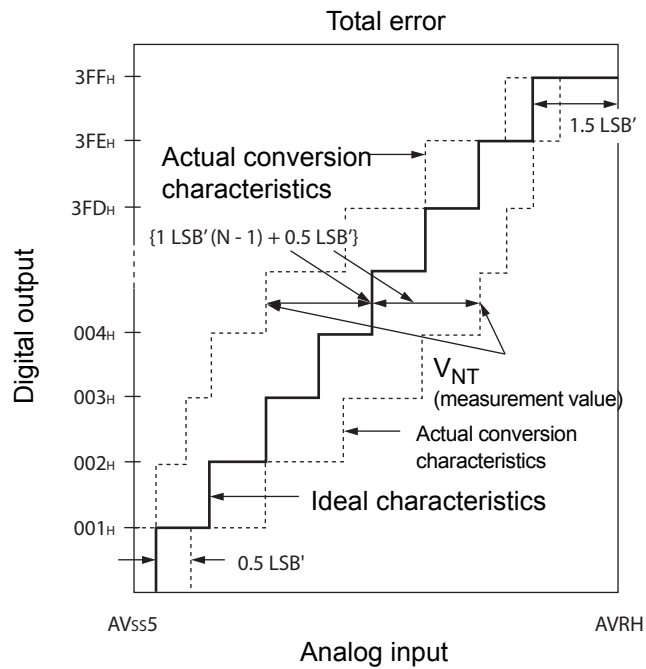
Deviation between actual conversion characteristics and a straight line connecting the zero transition point (00 0000 0000_B ↔ 00 0000 0001_B) and the full scale transition point (11 1111 1110_B ↔ 11 1111 1111_B).

■ Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



$$1\text{LSB}' \text{ (ideal value)} = \frac{\text{AVRH} - \text{AV}_{\text{SS5}}}{1024} \text{ [V]}$$

$$\text{Total error of digital output } N = \frac{V_{\text{NT}} - \{1\text{LSB}' \times (N - 1) + 0.5\text{LSB}'\}}{1\text{LSB}'}$$

N : A/D converter digital output value

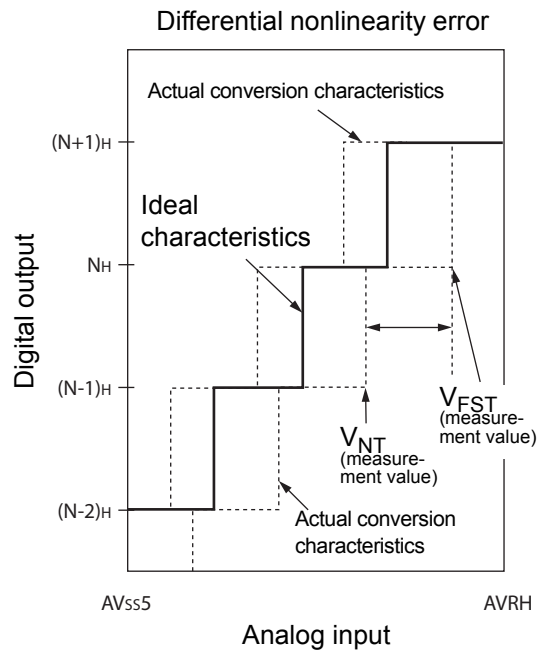
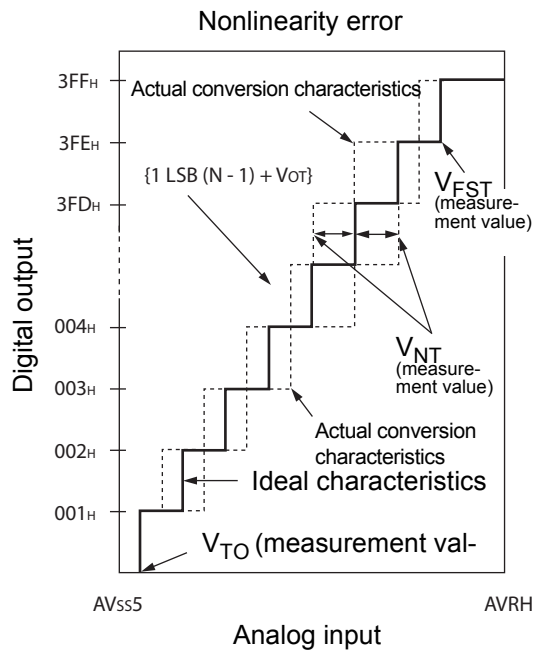
V_{OT}' (ideal value) = AV_{SS5} + 0.5 LSB' [V]

V_{FST}' (ideal value) = AV_{RH} - 1.5 LSB' [V]

V_{NT} : Voltage at which the digital output changes from (N + 1)_H to N_H

(Continued)

(Continued)



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{EST} - V_{OT}}{1022} [\text{V}]$$

N : A/D converter digital output value

V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.

V_{EST} : Voltage at which the digital output changes from 3FE_H to 3FF_H.

15.5 FLASH memory program/erase characteristics

15.5.1 MB91F464Ax

(T_A = 25°C, V_{CC} = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erase programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	μs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

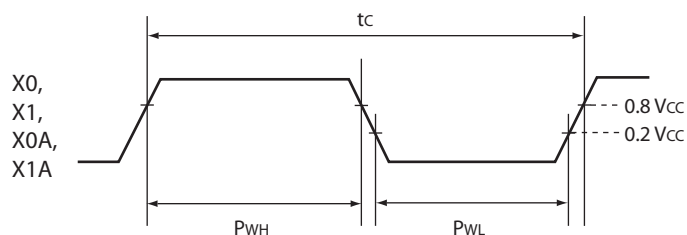
15.6 AC characteristics

15.6.1 Clock timing

($V_{DD5} = 3.0 \text{ V to } 5.5 \text{ V}$, $V_{SS5} = AV_{SS5} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

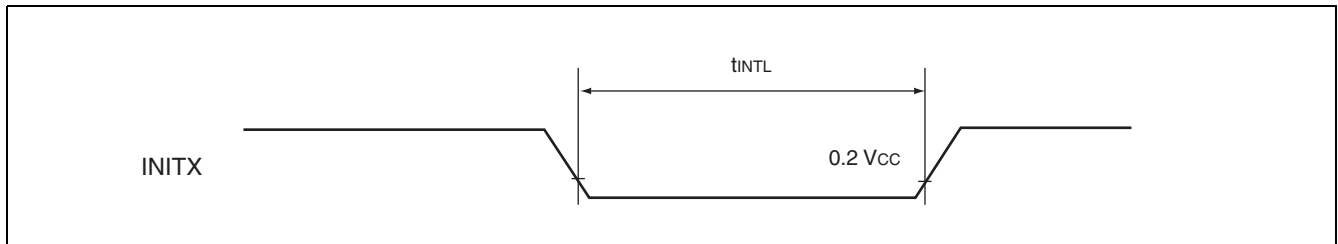
• Clock timing conditions



15.6.2 Reset input ratings

($V_{DD5} = 3.0 \text{ V to } 5.5 \text{ V}$, $V_{SS5} = AV_{SS5} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	–	10	–	ms
INITX input time (other than the above)				20	–	μs



15.6.3 LIN-USART Timings at $V_{DD5} = 3.0$ to 5.5 V

■ Conditions during AC measurements

■ All AC tests were measured under the following conditions:

- $I_{Odrive} = 5$ mA
- $V_{DD5} = 3.0$ V to 5.5 V, $I_{load} = 3$ mA
- $V_{SS5} = 0$ V
- $T_A = -40$ °C to $+105$ °C
- $C_l = 50$ pF (load capacity value of pins when testing)
- $VOL = 0.2 \times V_{DD5}$
- $VOH = 0.8 \times V_{DD5}$
- EPILR = 0, PILR = 1 (Automotive Level == worst case)

($V_{DD5} = 3.0$ V to 5.5 V, $V_{SS5} = AV_{SS5} = 0$ V, $T_A = -40$ °C to $+105$ °C)

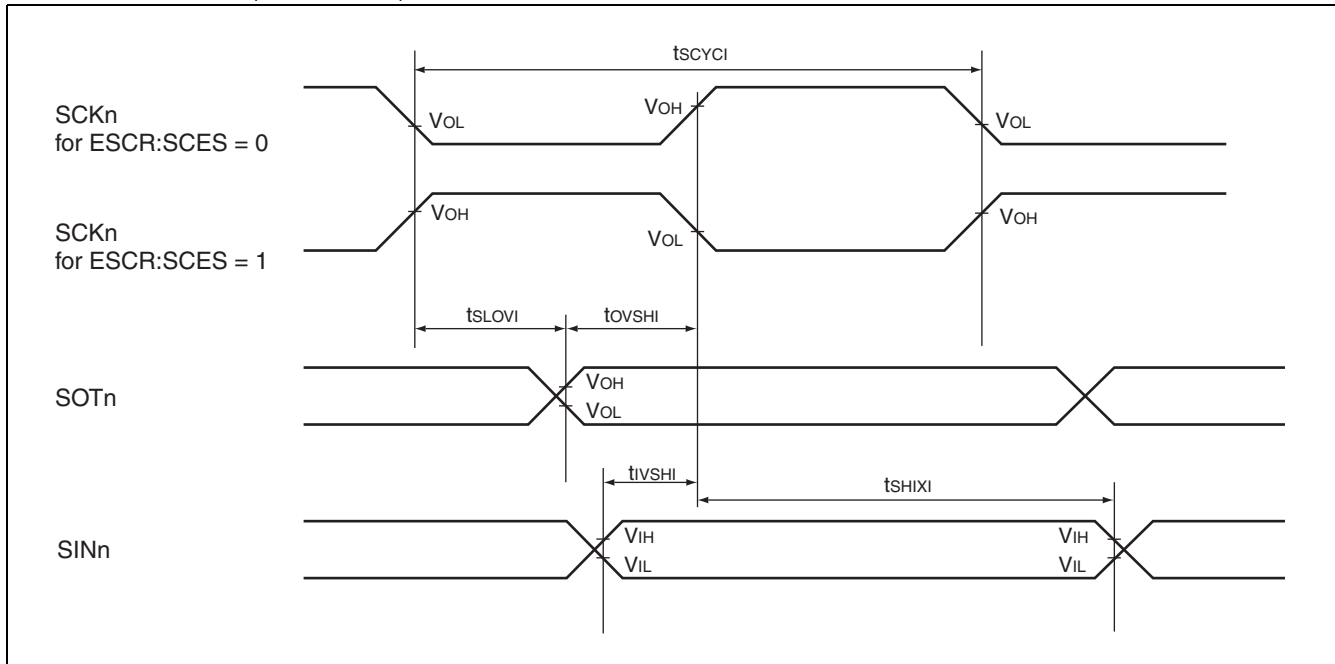
Parameter	Symbol	Pin name	Condition	$V_{DD5} = 3.0$ V to 4.5 V		$V_{DD5} = 4.5$ V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	$4 t_{CLKP}$	–	$4 t_{CLKP}$	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		– 30	30	– 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		$m \times t_{CLKP} - 30^*$	–	$m \times t_{CLKP} - 20^*$	–	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		$t_{CLKP} + 55$	–	$t_{CLKP} + 45$	–	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	–	0	–	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	$t_{CLKP} + 10$	–	$t_{CLKP} + 10$	–	ns
Serial clock “L” pulse width	t_{LSHE}	SCKn		$t_{CLKP} + 10$	–	$t_{CLKP} + 10$	–	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		–	$2 t_{CLKP} + 55$	–	$2 t_{CLKP} + 45$	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	–	10	–	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		$t_{CLKP} + 10$	–	$t_{CLKP} + 10$	–	ns
SCK rising time	t_{FE}	SCKn		–	20	–	20	ns
SCK falling time	t_{RE}	SCKn		–	20	–	20	ns

* : Parameter m depends on t_{SCYCI} and can be calculated as :

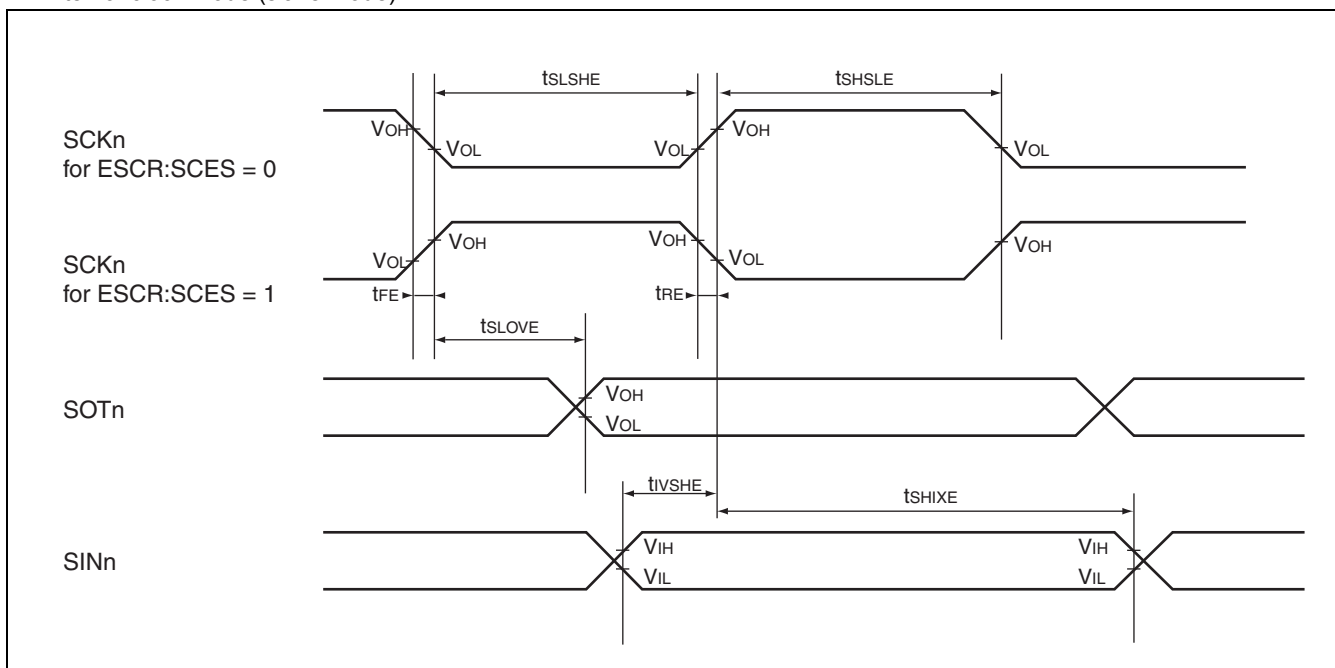
- if $t_{SCYCI} = 2^k \times t_{CLKP}$, then $m = k$, where k is an integer > 2
- if $t_{SCYCI} = (2^k + 1) \times t_{CLKP}$, then $m = k + 1$, where k is an integer > 1

Notes : • The above values are AC characteristics for CLK synchronous mode.
• t_{CLKP} is the cycle time of the peripheral clock.

• Internal clock mode (master mode)



• External clock mode (slave mode)



15.6.4 I²C AC Timings at V_{DD5} = 3.0 to 5.5 V

- Conditions during AC measurements

All AC tests were measured under the following conditions:

- IO_{drive} = 3 mA
- V_{DD5} = 3.0 V to 5.5 V, I_{load} = 3 mA
- V_{SS5} = 0 V
- T_A = -40 °C to +105 °C
- C_I = 50 pF
- VOL = 0.3 × V_{DD5}
- VOH = 0.7 × V_{DD5}
- EPILR = 0, PILR = 0 (CMOS Hysteresis V_{IL}/V_{IH} = 0.3 × V_{DD5}/0.7 × V_{DD5})

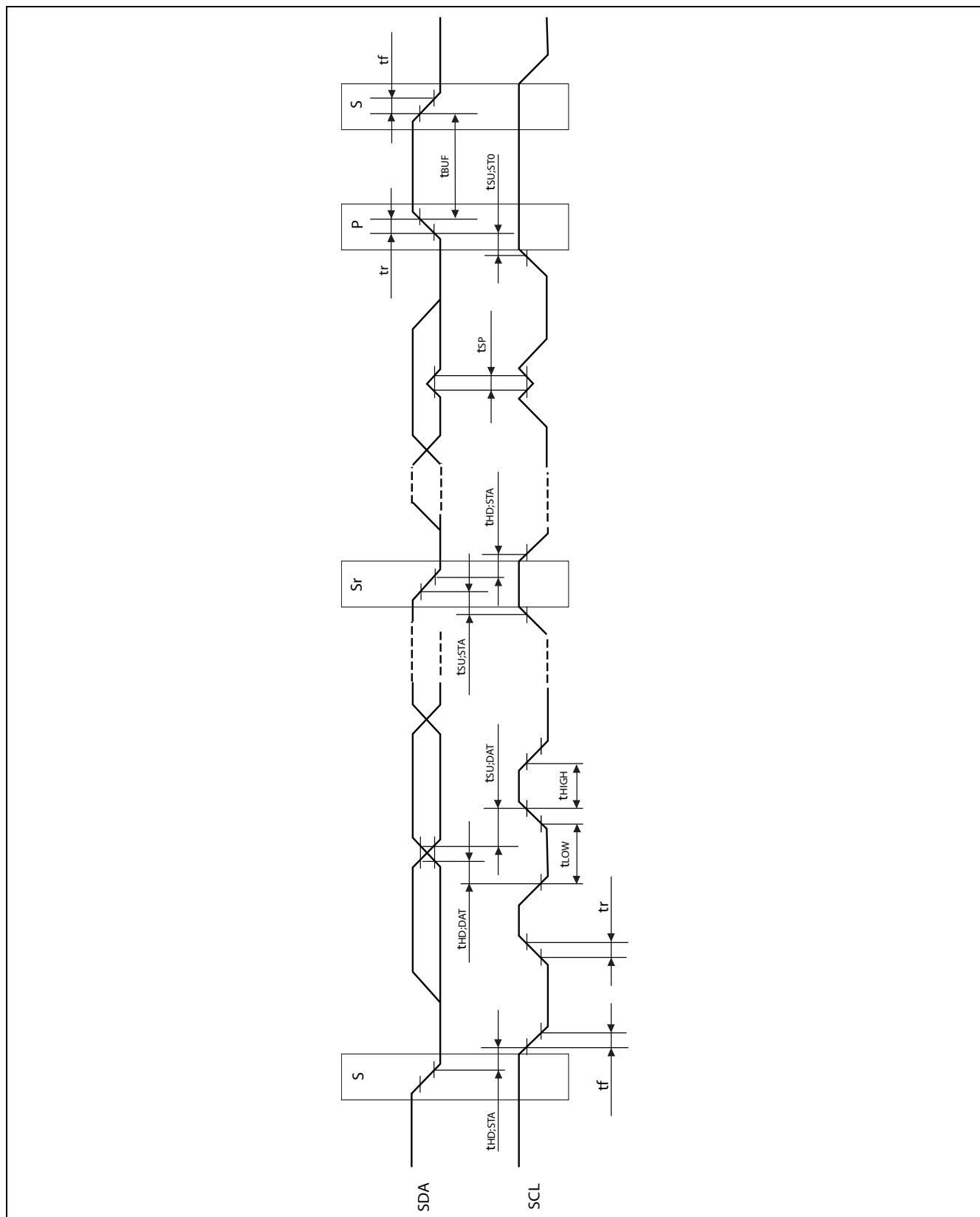
Fast mode:

(V_{DD5} = 3.5 V to 5.5 V, V_{SS5} = AV_{SS5} = 0 V, T_A = -40 °C to +105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f _{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t _{HD;STA}	SCLn, SDAn	0.6	–	μs	
LOW period of the SCL clock	t _{LOW}	SCLn	1.3	–	μs	
HIGH period of the SCL clock	t _{HIGH}	SCLn	0.6	–	μs	
Setup time for a repeated START condition	t _{SU;STA}	SCLn, SDAn	0.6	–	μs	
Data hold time for I ² C-bus devices	t _{HD;DAT}	SCLn, SDAn	0	0.9	μs	
Data setup time	t _{SU;DAT}	SCLn, SDAn	100	–	ns	
Rise time of both SDA and SCL signals	t _r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t _f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	t _{SU;STO}	SCLn, SDAn	0.6	–	μs	
Bus free time between a STOP and START condition	t _{BUF}	SCLn, SDAn	1.3	–	μs	
Capacitive load for each bus line	C _b	SCLn, SDAn	–	400	pF	
Pulse width of spike suppressed by input filter	t _{SP}	SCLn, SDAn	0	(1..1.5) × t _{CLKP}	ns	*1

*1 The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I2C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

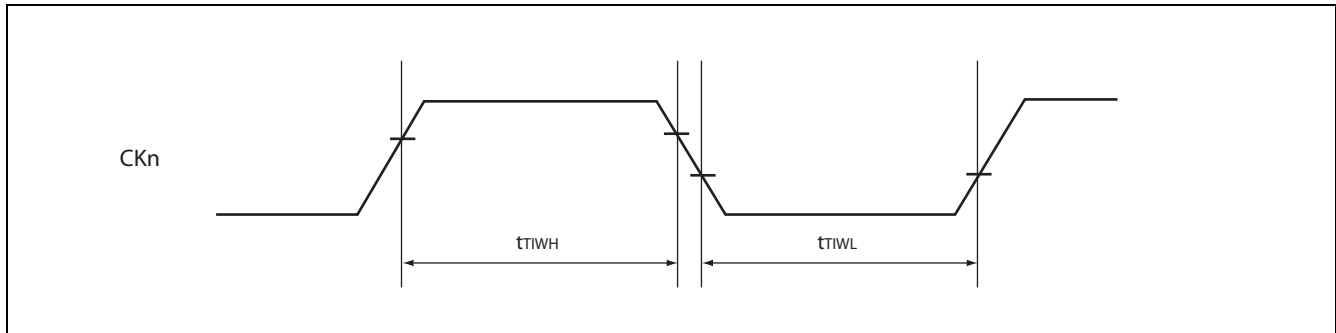


15.6.5 Free-run timer clock

($V_{DD5} = 3.0\text{ V to } 5.5\text{ V}$, $V_{SS5} = AV_{SS5} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to } +105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	–	$4t_{CLKP}$	–	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.

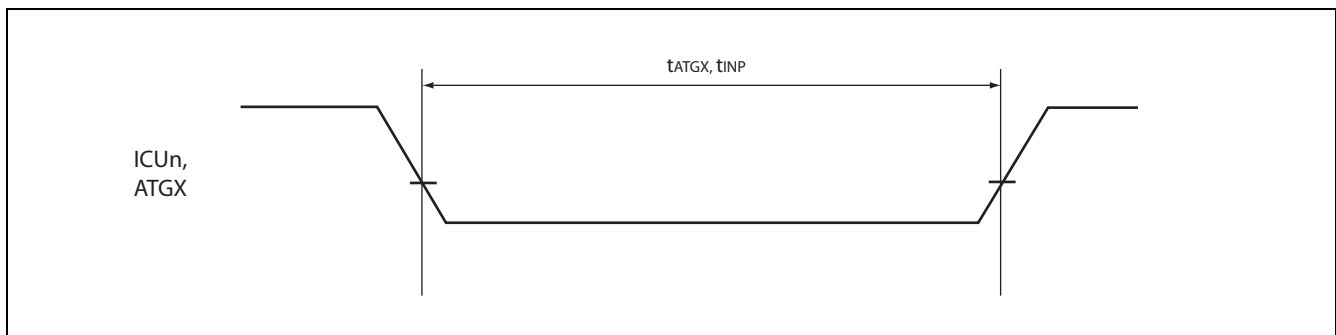


15.6.6 Trigger input timing

($V_{DD5} = 3.0\text{ V to } 5.5\text{ V}$, $V_{SS5} = AV_{SS5} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to } +105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	–	$5t_{CLKP}$	–	ns
A/D converter trigger	t_{ATGX}	ATGX	–	$5t_{CLKP}$	–	ns

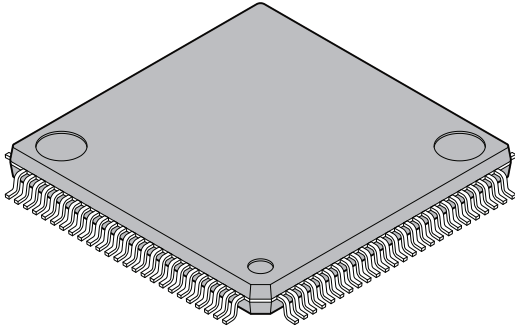
Note : t_{CLKP} is the cycle time of the peripheral clock.

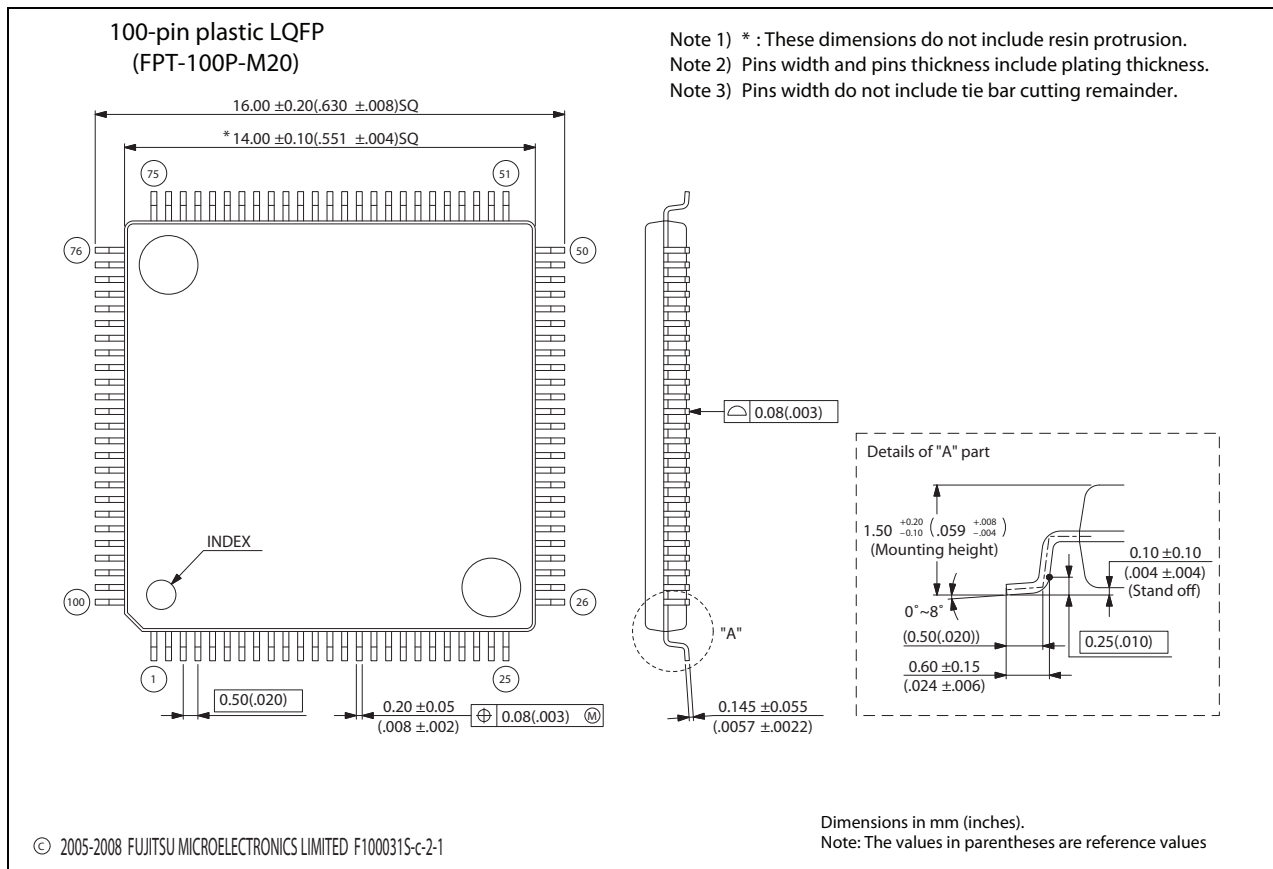


16. Ordering Information

Part number	Package	Remarks
MB91F464AAPMC-GSE2	100-pin plastic LQFP (FPT-100P-M20)	not recommended
MB91F464ABPMC-GSE2		Lead-free package

17. Package Dimension

100-pin plastic LQFP  (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14 ×14-0.50



18. Major Changes

Spanion Publication Number: DS07-16605-4E

Page	Section	Change Results
1	Top page	Information about Fujitsu MCU support page updated
4	Product lineup	Technology in μm instead of um
4	Product lineup	Temperatur --> Temperature
6	Pin Assignment	Removed the quadratic index mark on upper left corner
10	Pin Description; Power supply/Ground pins	Renamed "GND" into "ground"
17	Handling devices; Power supply pins	Corrected "capacitator" into "capacitor"
21	Block diagram	Renamed "RTC" into "Real Time Clock"
23	Programming model	Renamed Program status register into "PS" (instead of RS)
40	I/O Map address 00010CH	Added address 00010CH (Reserved)
47	I/O Map address 0004C0H	Changed "CAN (Clock Control)" into "CAN Clock Control"
56	I/O Map; Flash memory and external bus area	Corrected table header (Added "+0 +1 +2 +3")
64	Recommended Settings; Clock Modulator settings	Removed all settings for Baseclk > 48 MHz
70	Recommended operating conditions	Corrected "Look-up time PLL" into "Lock-up time PLL"
72	DC Characteristics; Output "L" voltage	Corrected condition I_{OH} into I_{OL}
72	DC Characteristics; Table foot note	Changed "PullUp/PullDown" into "Pull-Up/Pull-Down"
73	DC Characteristics; I_{ccH}	I_{ccH} (RTC mode) at 32kHz is similar to 100kHz, footnote added
74	A/D converter characteristics; Zero reading voltage, Full scale reading voltage	Corrected Values into "value +- n LSB " and Unit into "V" (Volt)
80	AC Characteristics; Reset input ratings	INITX at power-on min. 10ms (according to the Main Oscillation Stabilisation Time)
5,81,83	Ambient temperature	Changed the symbol of ambient temperature from T_a into T_A
81,83	AC Characteristics; LIN AC Timings I2C AC Timings	Corrected condition VOL into V_{OL} , VOH into V_{OH}
83	AC Characteristics; I2C AC Timings	Corrected EPILR,PILR condition into "CMOS Hysteresis VIL/VIH =..."
87	Package Dimension	Corrected the link to package web page

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB91F464AA, MB91F464AB FR60 MB91460A Series 32-bit Microcontroller Datasheet Document Number: 002-04600				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	10/30/2009	Migrated to Cypress and assigned document number 002-04600. No change to document contents or format.
*A	5226606	AKIH	04/18/2016	Updated to Cypress template

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