International
IOR Rectifier

AUIRS2181(4)S

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability (typical) 1.9 A /2.3 A
- Leadfree, RoHS compliant
- Automotive qualified*

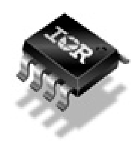
Typical Applications

- Piezo/ common rail Injection
- Starter/Alternator
- Electric Power Steering
- Fan and compressor

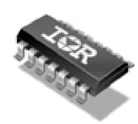
Product Summary

Topology	High and Low Side Driver
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typical)	1.9 A &2.3 A
t_{ON} & t_{OFF} (typical)	160 ns & 200 ns

Package Options

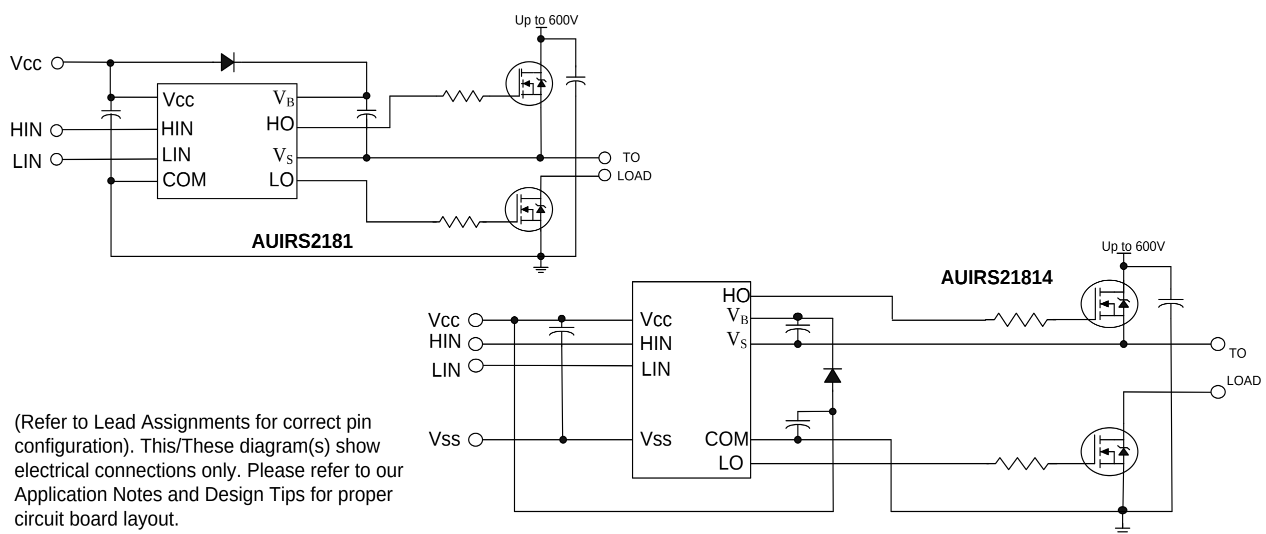


8-Lead SOIC
AUIRS2181S



14-Lead SOIC
Narrow Body
AUIRS21814S

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2181S	SOIC8	Tube/Bulk	95	AUIRS2181S
		Tape and Reel	2500	AUIRS2181STR
AUIRS21814S	SOIC14N	Tube/Bulk	55	AUIRS21814S
		Tape and Reel	2500	AUIRS21814STR

Description

The AUIRS2181(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Feature Comparison: AUIRS2181/AUIRS2183/AUIRS2184

Part	Input Logic	Cross-Conduction Prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	160/200 ns
21814				V_{SS}/COM	
2183	HIN/LIN	yes	Internal 500ns	COM	160/200 ns
21834			Programmable 0.4 – 5 us	V_{SS}/COM	
2184	IN/SD	yes	Internal 500ns	COM	600/230 ns
21844			Programmable 0.4 – 5 us	V_{SS}/COM	

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Definition		Min	Max	Units
V_B	High-side floating absolute voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	20 (†)	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN &LIN)		V_{SS} -0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (AUIRS21814(S) only)		V_{CC} - 20	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	(8 lead SOIC)	—	0.625	W
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead SOIC)	—	200	°C/W
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min	Max	Units
V_B	High-side floating supply absolute voltage	V_S +10	V_S +20	V
V_S	High-side floating supply offset voltage	(††)	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	V_{CC}	
DT	Programmable deadtime pin voltage	V_{SS}	V_{CC}	
V_{SS}	Logic ground	-5	5	
T_A	Ambient temperature	-40	125	°C

†† Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	160	270		V_S = 0 V
t_{off}	Turn-off propagation delay	—	200	330		V_S = 0 V or 600 V
MT	Delay matching, HS & LS turn-on/off	—	—	35	ns	
t_r	Turn-on rise time	—	15	60		V_S = 0 V
t_f	Turn-off fall time	—	15	35		

Static Electrical Characteristics

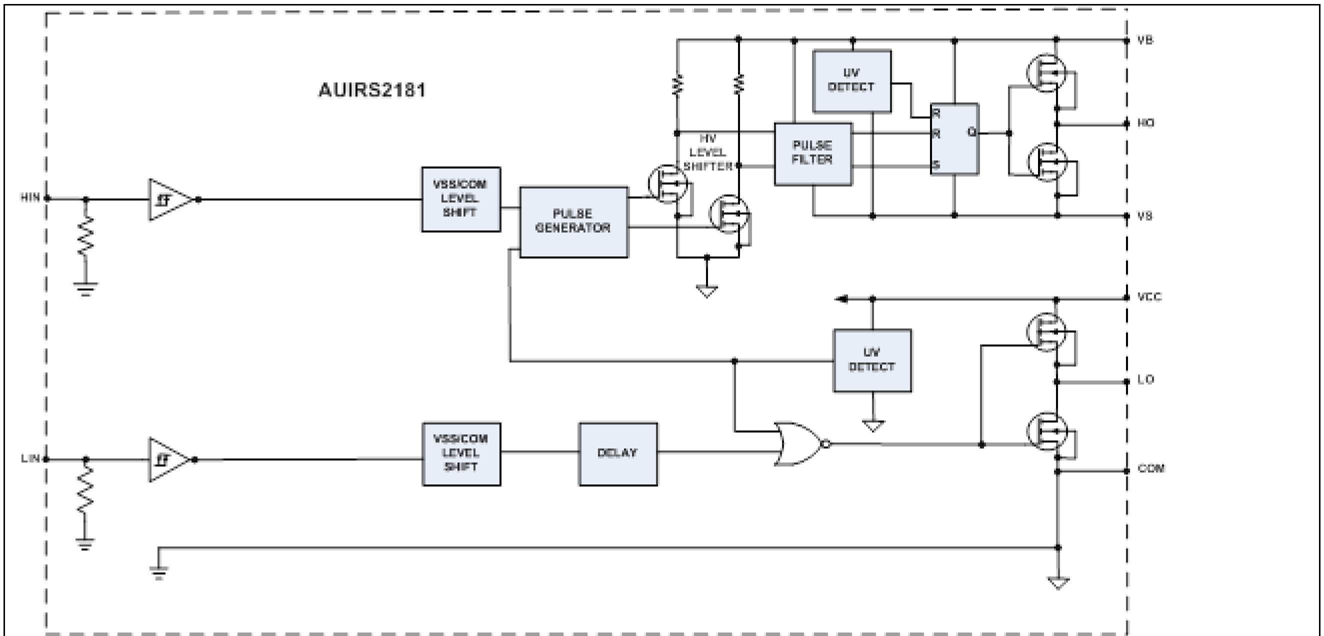
Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and LIN. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

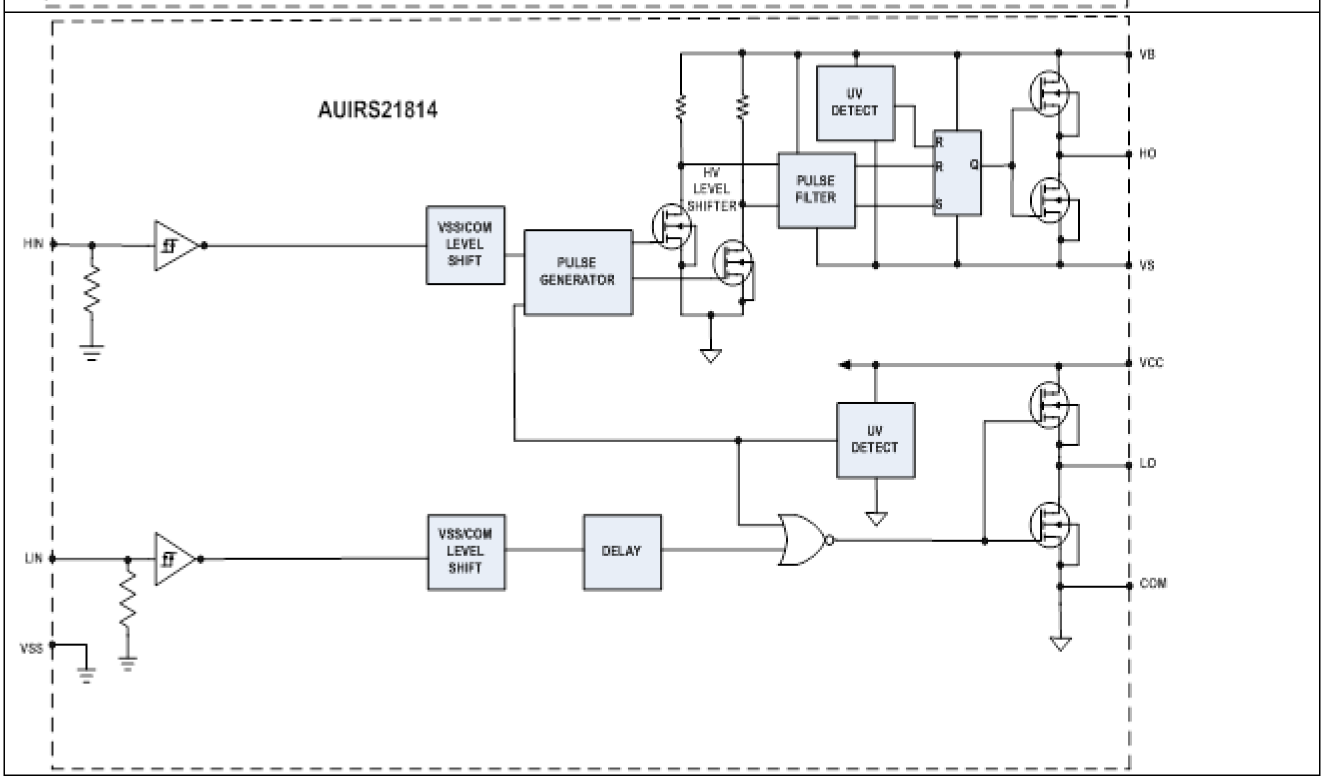
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—		V_{CC} = 10 V to 20 V
V_{IL}	Logic "0" input voltage	—	—	0.8	V	V_{CC} = 10 V to 20 V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.4		I_O = 0 mA
V_{OL}	Low level output voltage, V_O	—	—	0.2		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50		V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	15	60	150		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	15	120	240	µA	
I_{IN+}	Logic "1" input bias current	—	25	60		V_{IN} = 5 V
I_{IN-}	Logic "0" input bias current	—	—	5.0		V_{IN} = 0 V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0	V	
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage Hysteresis	0.3	0.7	—		
I_{O25+} (†)	Output high short circuit pulsed current	1.4	1.9	—		V_O = 0V, PW ≤ 10us, T_J = 25°C
I_{O25-} (†)	Output low short circuit pulsed current	1.8	2.3	—	A	V_O = 15V, PW ≤ 10us, T_J = 25°C
I_{O+} (†)(††)	Output high short circuit pulsed current	1.2	—	—		V_O = 0 V, PW ≤ 10 us
I_{O-} (†)(††)	Output low short circuit pulsed current	1.5	—	—		V_O = 15 V, PW ≤ 10 us

(†) Guaranteed by design

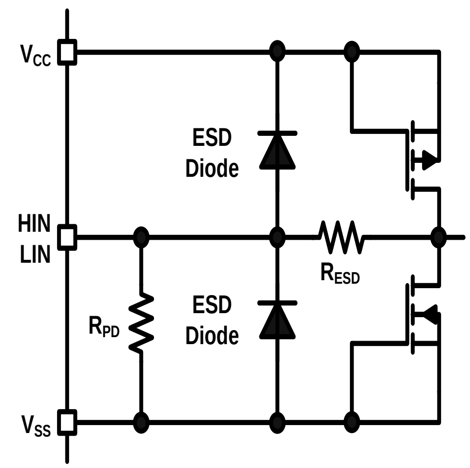
(††) I_{O+} and I_{O-} decrease with rising temperature

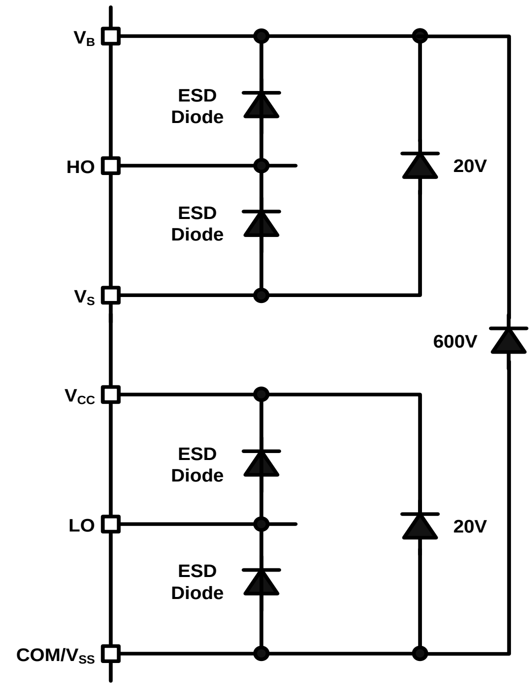
Functional Block Diagrams: AUIRS2181, AUIRS21814



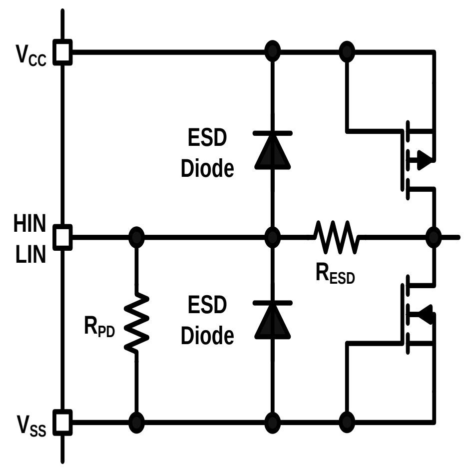


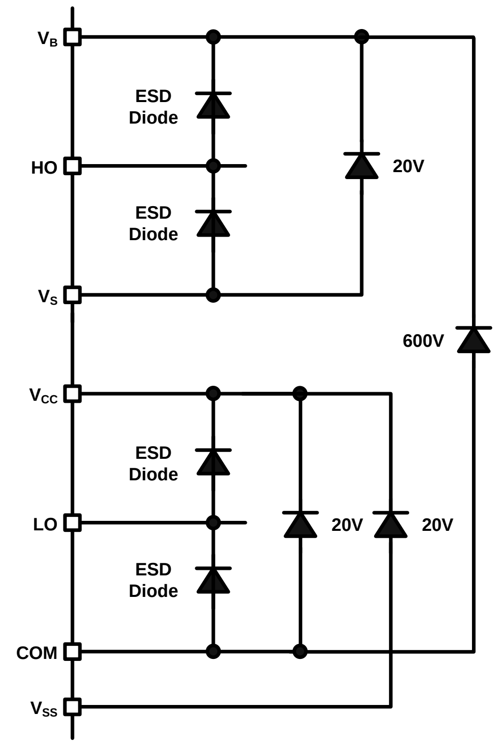
Input/Output Pin Equivalent Circuit Diagrams: AUIRS2181S





Input/Output Pin Equivalent Circuit Diagrams: AUIRS21814S

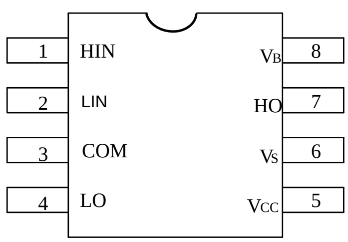




Lead Definitions: AUIRS2181(4)S

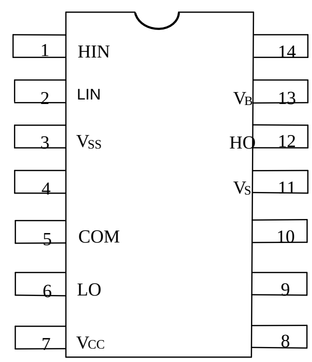
Symbol	Description
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side driver output (LO), in phase
V_{SS}	Logic ground (AUIRS21814 only)
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return

Lead Assignments: AUIRS2181(4)S



8 Lead SOIC

AUIRS2181S



14 Lead SOIC
Narrow Body

AUIRS21814S

Application Information and Additional Details

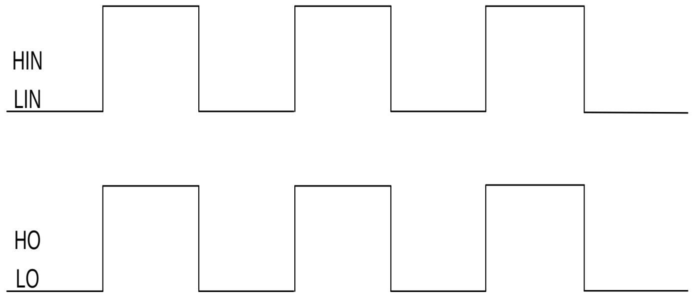


Figure 1. Input/Output Timing Diagram

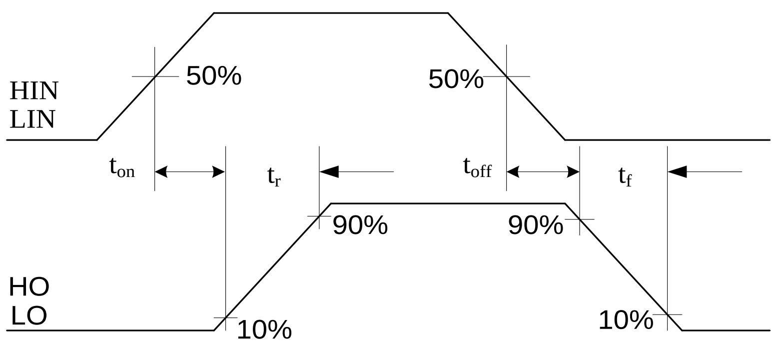


Figure 2. Switching Time Waveform Definitions

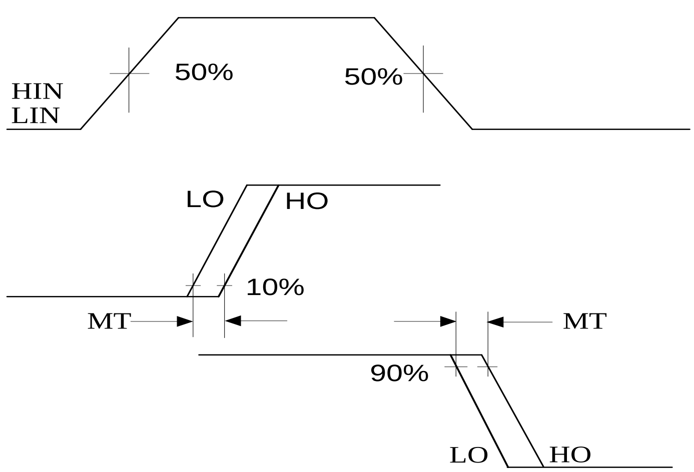


Figure 3. Delay Matching Waveform Definitions

Parameter Trends vs. Temperature and vs. Supply Voltage

Figures of this chapter provide information on the experimental performance of the AUIRS2181(4)S HVIC. The line plotted in each figure is generated from actual lab data.

A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

A different set of individual samples was used to generate curves of parameter trends vs. supply voltage.

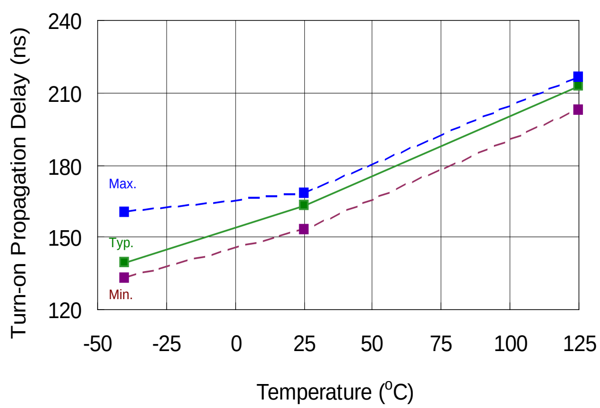


Figure 1A. Turn-On Propagation Delay vs. Temperature

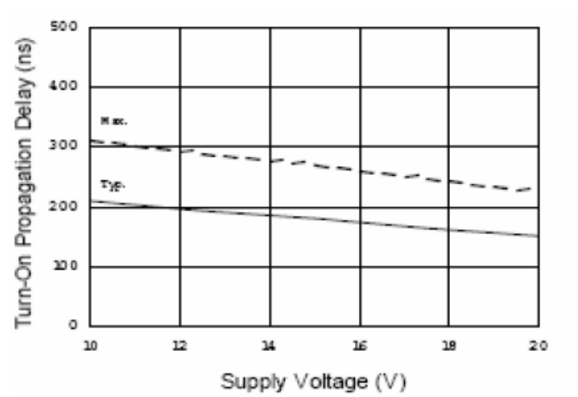


Figure 1B. Turn-On Propagation Delay vs. Supply Voltage

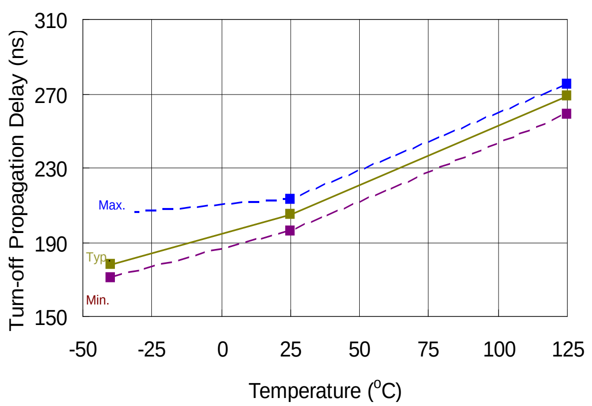


Figure 2A. Turn-Off Propagation Delay vs. Temperature

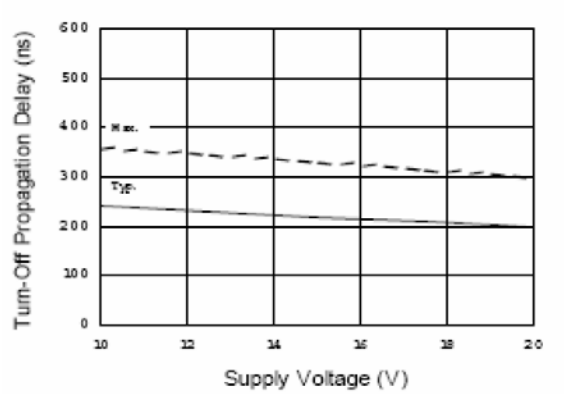


Figure 2B. Turn-Off Propagation Delay vs. Supply Voltage

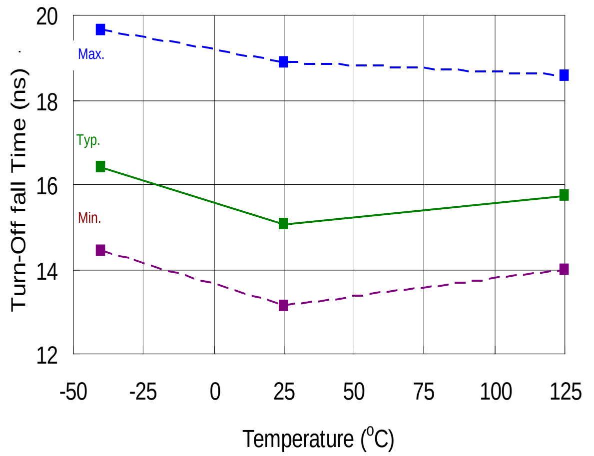


Figure 3A. Turn-Off Fall Time vs. Temperature

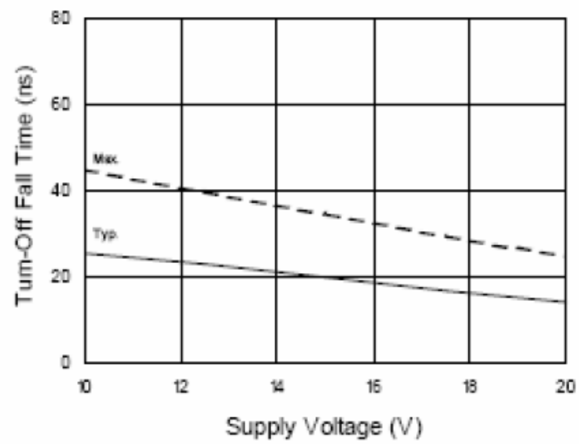


Figure 3B. Turn-Off Fall Time vs. Supply Voltage

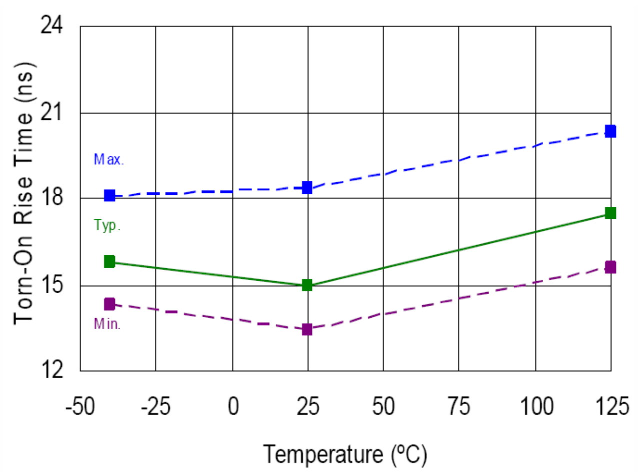


Figure 4. Turn-On Rise Time vs. Temperature

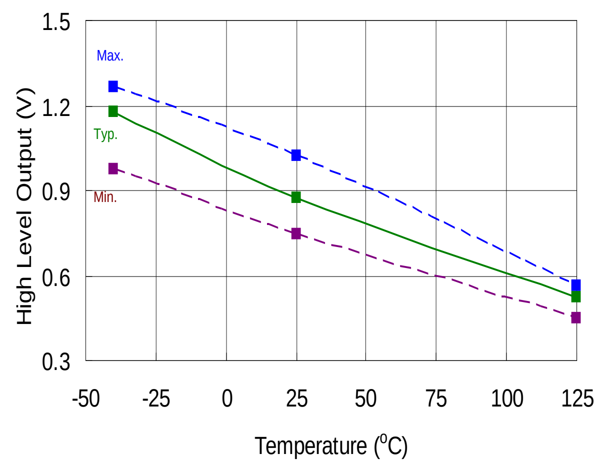


Figure 5. High Level Output Voltage vs. Temperature (Io = 0mA)

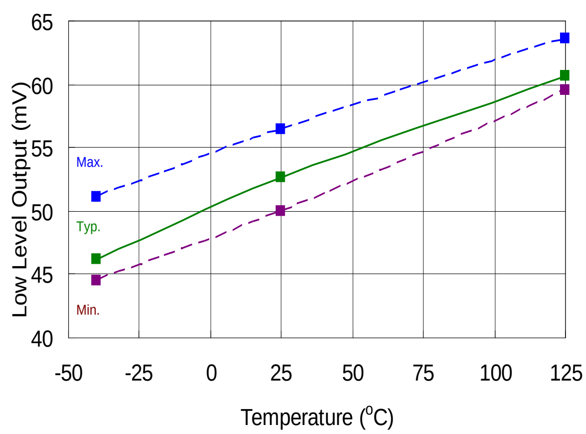


Figure 6. Low Level Output vs. Temperature

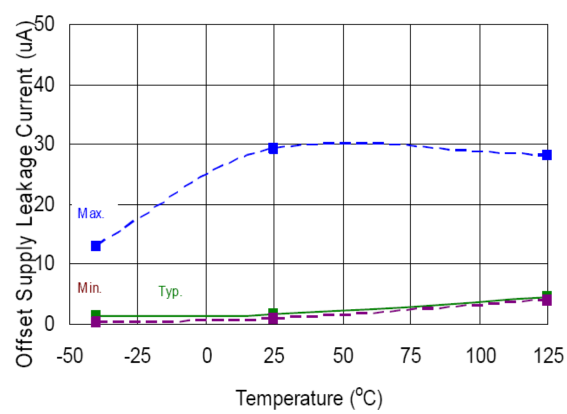


Figure 7. Offset Supply Leakage Current vs. Temperature

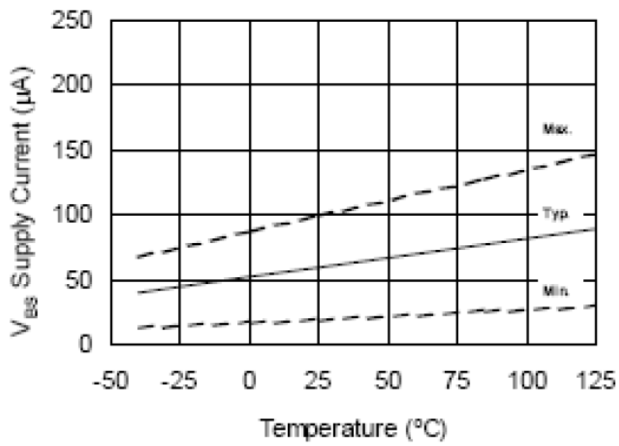


Figure 8A V_{BS} Supply Current vs. Temperature

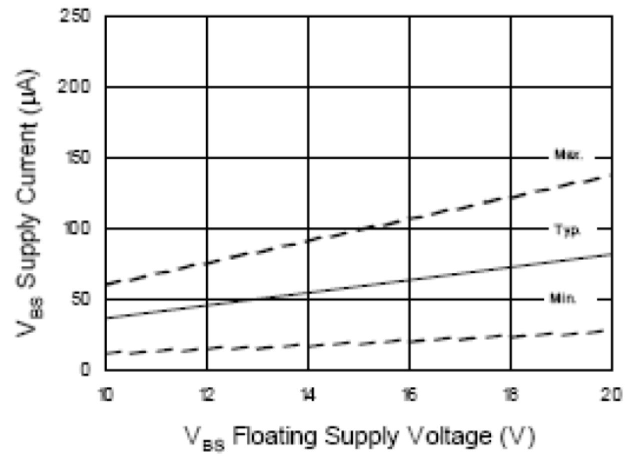


Figure 8B V_{BS} Supply Current vs. V_{BS} Floating Supply Voltage

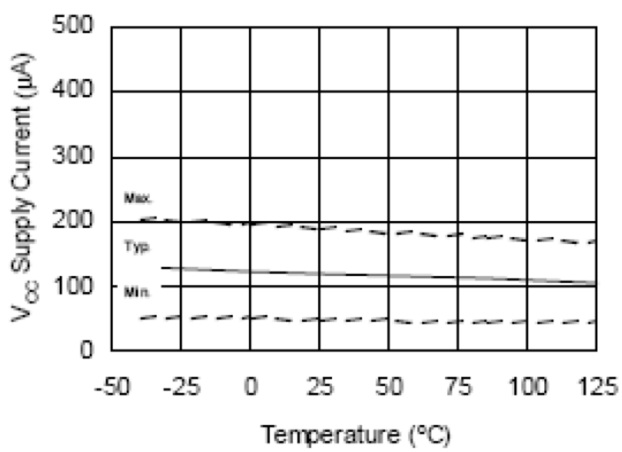


Figure 9A V_{CC} Supply Current vs Temperature

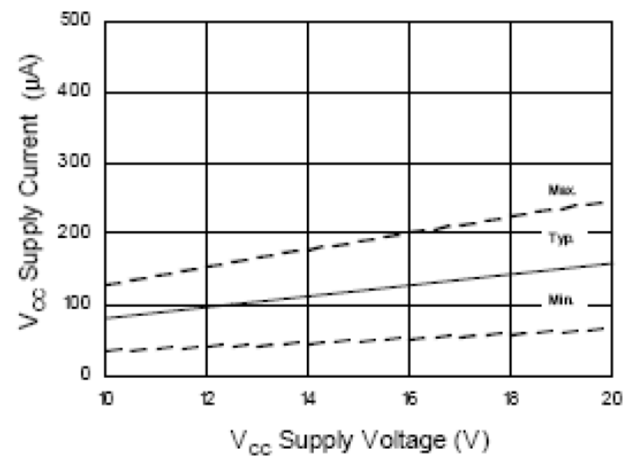


Figure 9B V_{CC} Supply Current vs. V_{CC} Supply Voltage

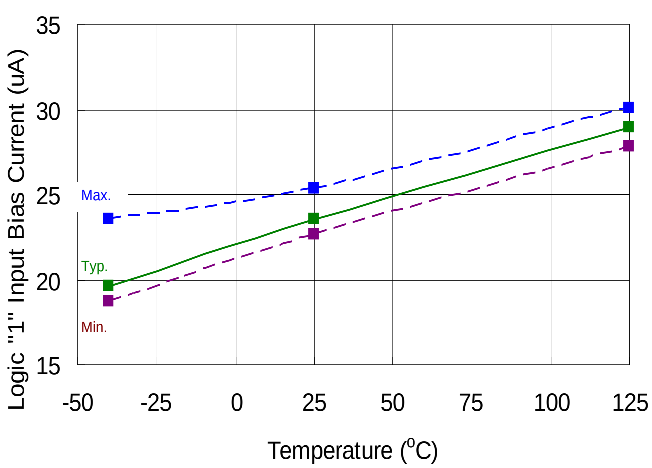


Figure 10. Logic “1” Input Bias vs Temperature

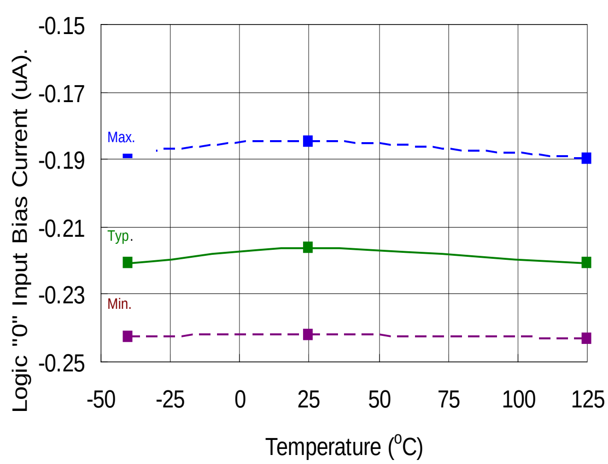


Figure 11. Logic “0” Input Bias vs Temperature

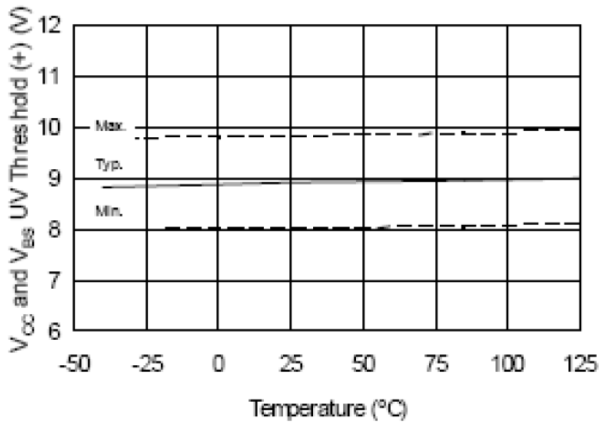


Figure 12. V_{CC} and V_{BS} Undervoltage Threshold(+) vs Temperature

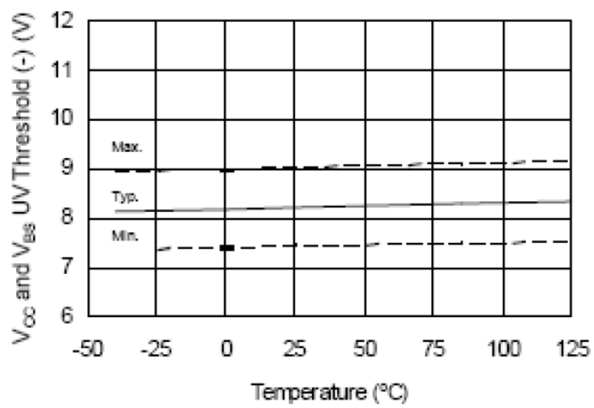


Figure 13. V_{CC} and V_{BS} Undervoltage Threshold(-) vs Temperature

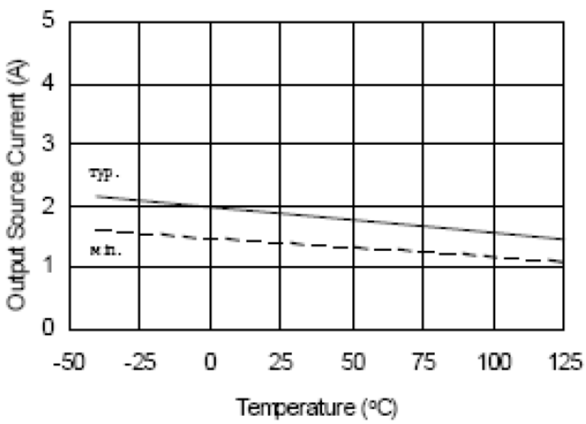


Figure 14A. Output Source Current vs Temperature

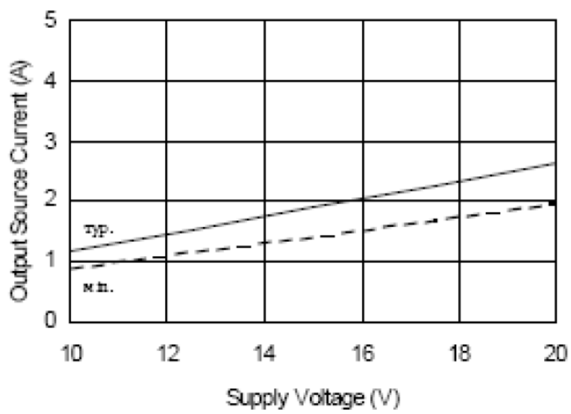


Figure 14B. Output Source Current vs Supply Voltage

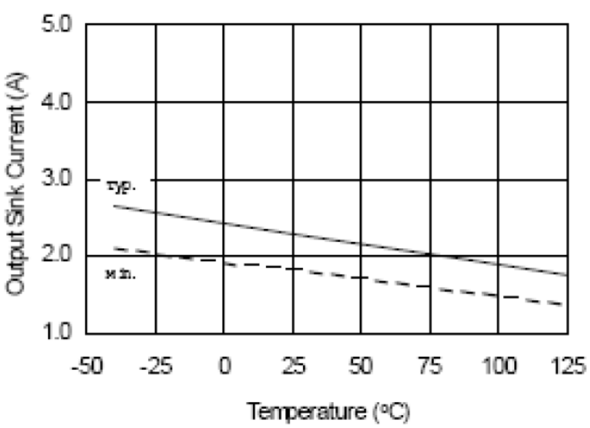


Figure 15A. Output Sink Current vs Temperature

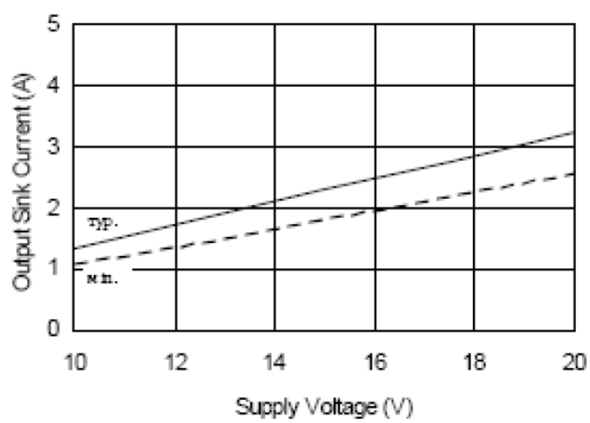


Figure 15B. Output Sink Current vs Supply Voltage

Negative Vs Safety Operating Area (negVs SOA)

There could be conditions in which Vs node falls below (i.e. negative) VSS/COM nodes (e.g. because of wrong system layout). This condition should be avoided because it could bring to uncontrolled behavior of the driver.
The negVs SOA identifies the energy of negative Vs pulses at which the driver can withstand; pulse energy is identified as the product of pulse duration by its amplitude. Fig. 16 shows the negVs SOA of AUIRS2181(4)S at both ambient and over temperature conditions. Test conditions were VCC=VBS=15V referenced to VSS=COM.
Even though the AUIRS2181(4)S has been designed and tested to handle these negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

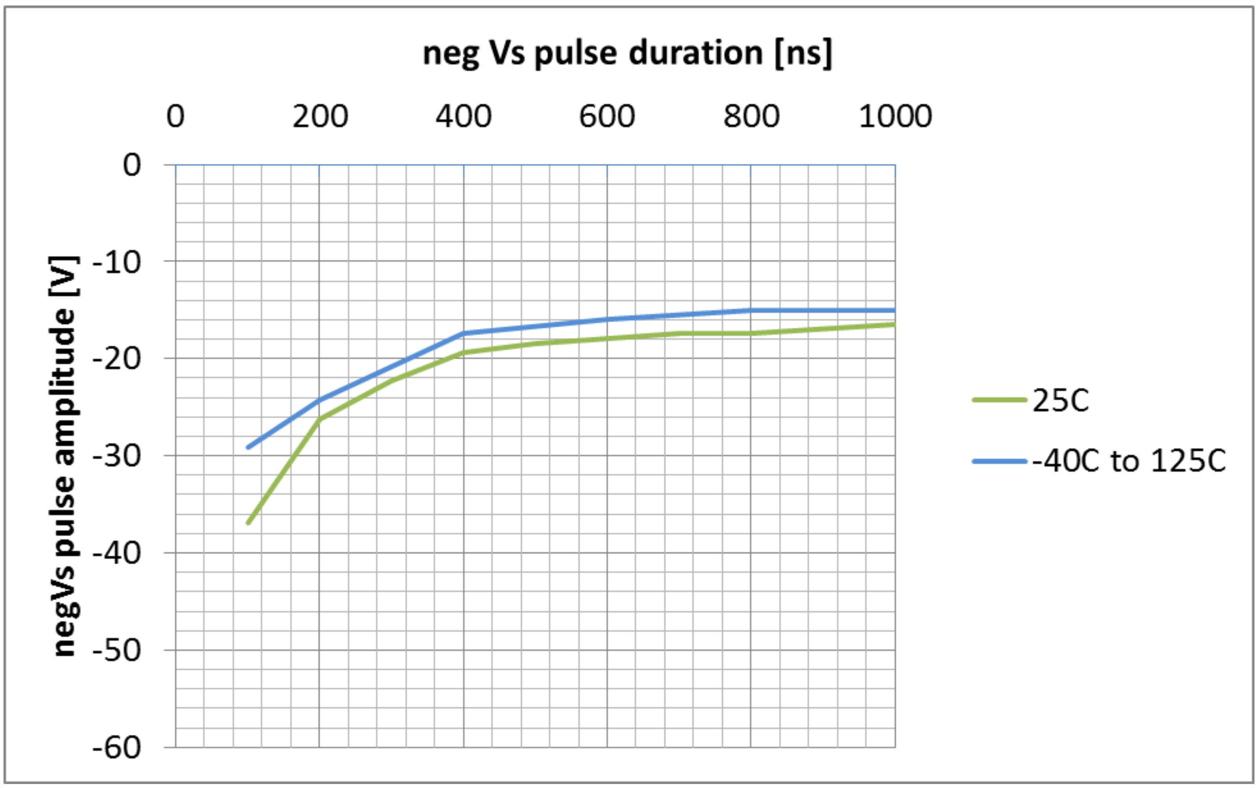
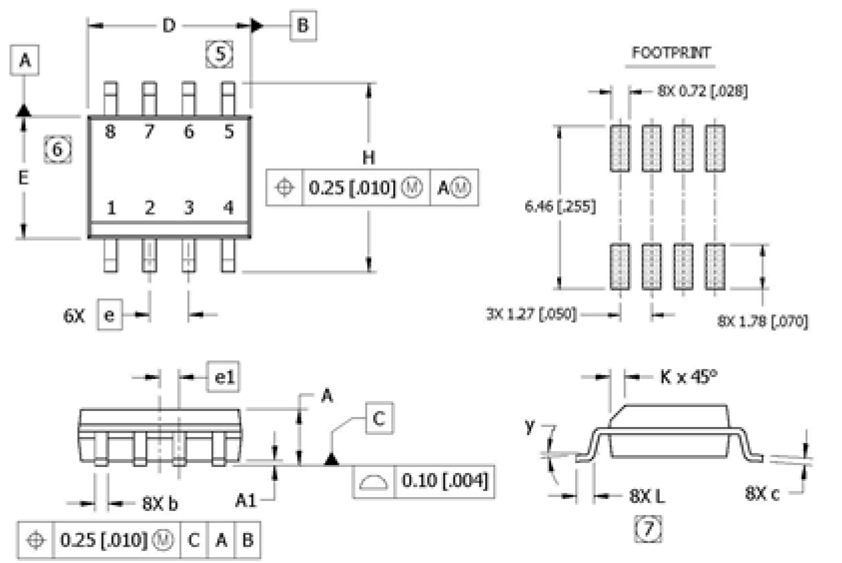


Fig. 16 Negative Vs SOA of AUIRS2181(4)S.

Package Details: SOIC8



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

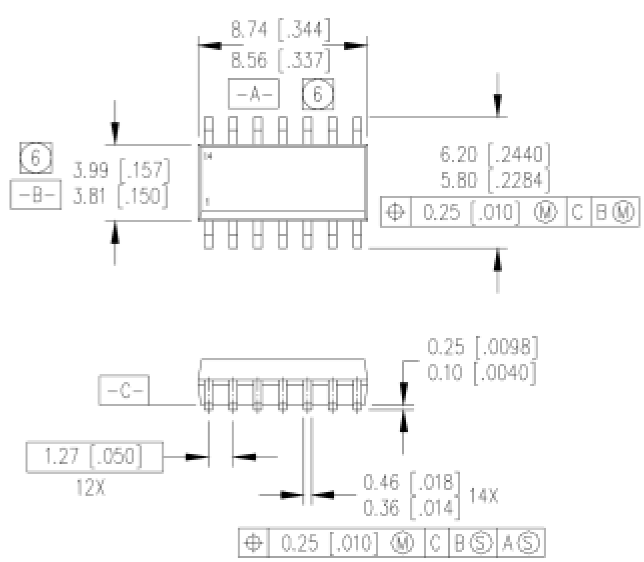
5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

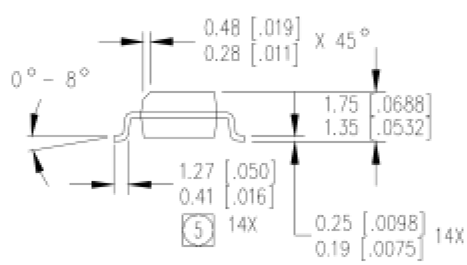
8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

Package Details: SOIC14N

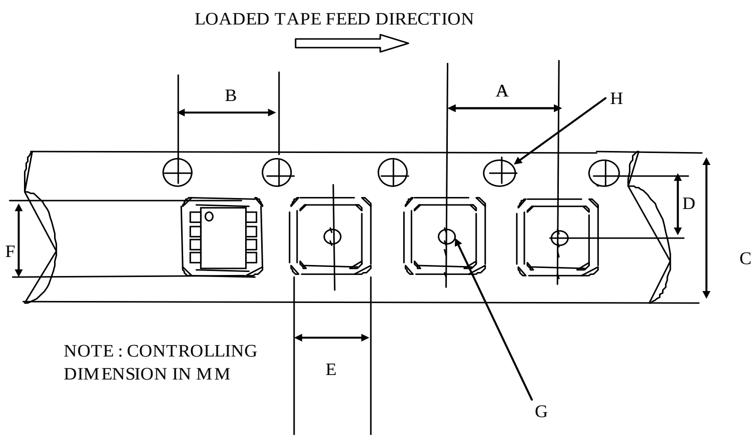
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006]





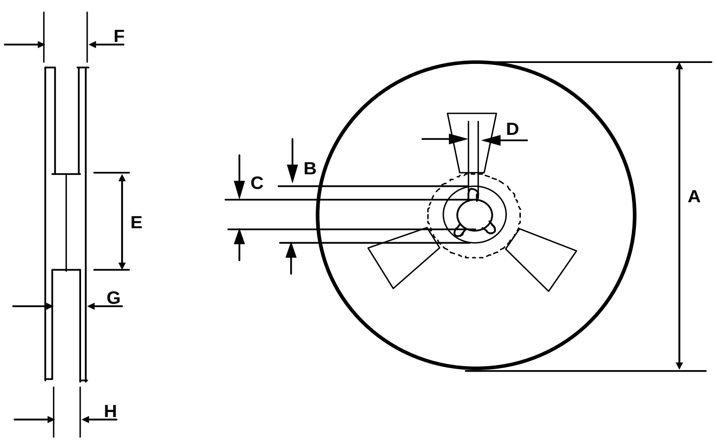
14 Lead SOIC (narrow body)

Tape and Reel Details: SOIC8



CARRIER TAPE DIMENSION FOR 8SOICN

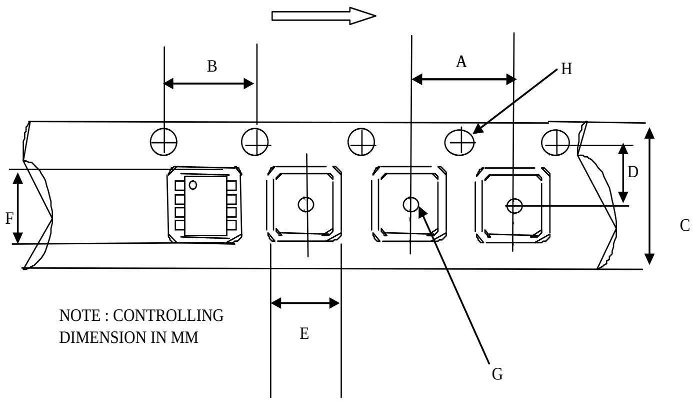
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

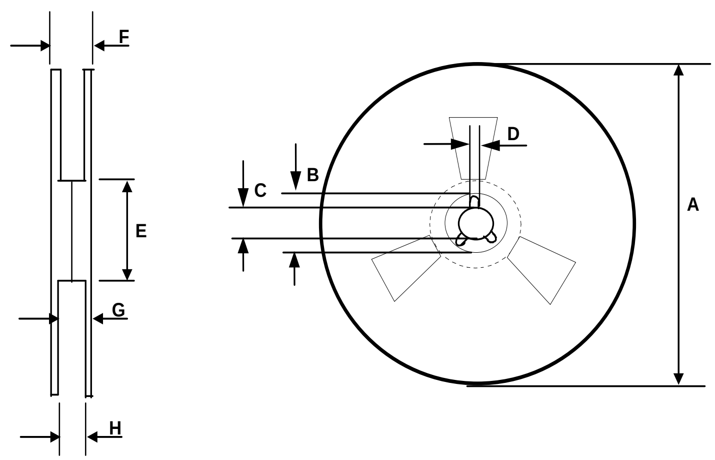
Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Tape and Reel Details: SOIC14N



CARRIER TAPE DIMENSION FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

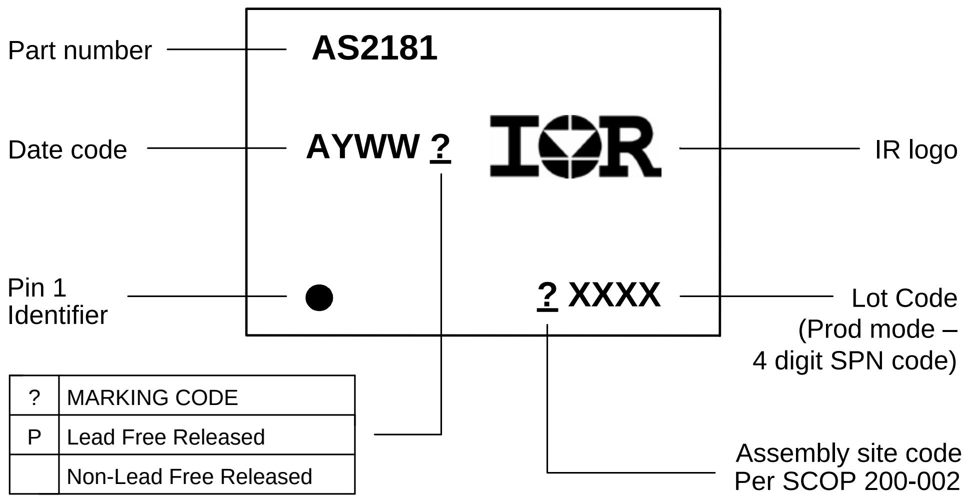


REEL DIMENSIONS FOR 14SOICN

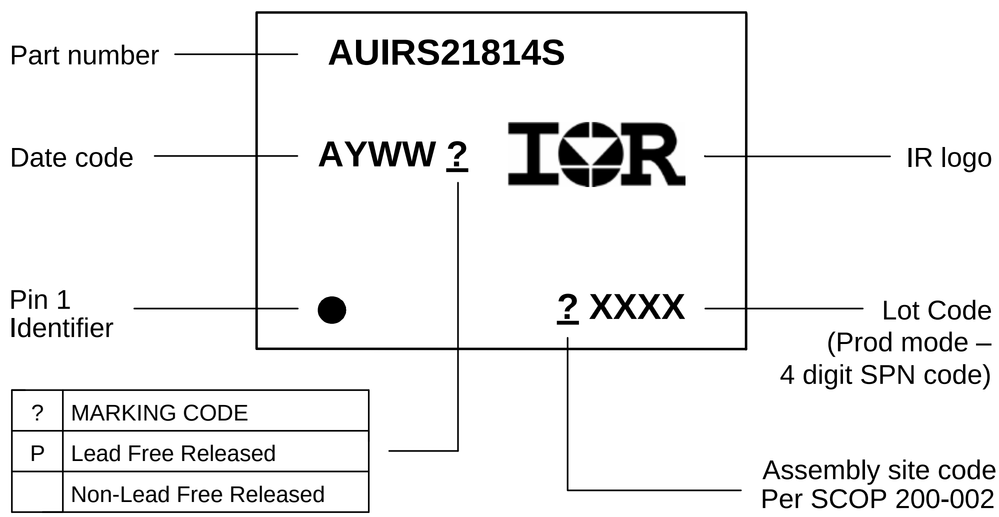
	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information

SOIC8:



SOIC14N:



Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
		SOIC14N	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	*Machine Model*	Class M2 (Pass +/-150V) (per AEC-Q100-003)	
	Human Body Model	Class H1B (Pass +/-1000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A†††† (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† HIN, LIN Class II Level B at 80mA per JESD78.

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Revision History

Date	Comment
04/29/08	Draft
5/6/08	Converted to new automotive format
9/30/08	Reviewed and updated various missing information
10/01/08	Inserted Input/Output Pin Equivalent Circuit Diagram
Feb, 10th, 2009	Typ application list and other minor changes
Feb. 11, 2009	Removed PDIP package versions from datasheet
Aug. 4, 2009	Updated qualification information, characterization curves
Aug. 11, 2009	Updated plot, removed characterization graphs, changes package type info
Aug. 13, 2009	Updated VIH/VIL graphs
Sep 23rd, 2009	Typ appl. Section update; Rearranged graphs with temperature and supply characteristic, updated marking detail with p/n; added ESD passing voltage; update LU test passing current from 40mA to 80mA.
Dec. 16, 09	Changed Iqcc/Iqbs min to 15uA; added Important Notice page; changed ton typ=160ns; toff typ=200ns; tr typ=15ns; tf typ=15ns
Feb. 24, 2010	Page 6: Added I_{O25+} and I_{O25-} specification and the notes
Jul. 27, 2010	clamp diode values changed from 25V into 20V (in-out pin eq. circ. diagrams)
Mar 07, 2012	Input zener clamp note deleted in recommended op cond
Sept. 30th, 2013	Added negVs SOA
Oct. 04th, 2013	Adapted to new format
Jan. 10, 2014	Updated datasheet to display respective page number on bottom left corner of every page

