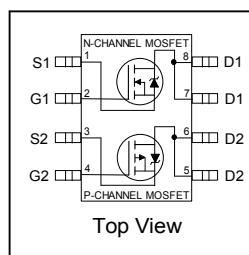


Features

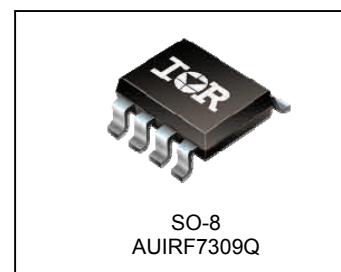
- Advanced Planar Technology
- Low On-Resistance
- Logic Level Gate Drive
- Dual N and P Channel MOSFET
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Lead-Free, RoHS Compliant
- Automotive Qualified *



	N-CH	P-CH
V_{DS}	30V	-30V
$R_{DS(on)}$ max.	0.05Ω	0.10Ω
I_D	4.7A	-3.5A

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF7309Q	SO-8	Tape and Reel	4000	AUIRF7309QTR

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ $T_A = 25^\circ\text{C}$	10 Sec. Pulsed Drain Current, V_{GS} @ 10V	4.7	-3.5	A
I_D @ $T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	4.0	-3.0	
I_D @ $T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	3.2	-2.4	
I_{DM}	Pulsed Drain Current ①	16	-12	
P_D @ $T_A = 25^\circ\text{C}$	Maximum Power Dissipation ④	1.4		W
	Linear Derating Factor④	0.011		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	6.9	-6.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ④	—	90	°C/W

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	V _{GS} = 0V, I _D = 250μA
		P-Ch	-30	—	—		V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.032	—	V/°C	Reference to 25°C, I _D = 1mA
		P-Ch	—	-0.037	—		Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.050	Ω	V _{GS} = 10V, I _D = 2.4A ③
			—	—	0.080		V _{GS} = 4.5V, I _D = 2.0A ③
		P-Ch	—	—	0.10		V _{GS} = -10V, I _D = -1.8A ③
			—	—	0.16		V _{GS} = -4.5V, I _D = -1.5A ③
V _{GS(th)}	Gate Threshold Voltage	N-Ch	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
		P-Ch	-1.0	—	-3.0		V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Trans conductance	N-Ch	5.2	—	—	S	V _{DS} = 15V, I _D = 2.4A
		P-Ch	2.5	—	—		V _{DS} = -24V, I _D = -1.8A
I _{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		P-Ch	—	—	-1.0		V _{DS} = -24V, V _{GS} = 0V
		N-Ch	—	—	25		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
		P-Ch	—	—	-25		V _{DS} = -24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	nA	V _{GS} = ± 20V
	Gate-to-Source Reverse Leakage	N-P	—	—	± 100		V _{GS} = ± 20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q _g	Total Gate Charge	N-Ch	—	—	25	nC	N-Channel I _D = 2.6A, V _{DS} = 16V, V _{GS} = 4.5V ③
		P-Ch	—	—	25		
Q _{gs}	Gate-to-Source Charge	N-Ch	—	—	2.9	nC	P-Channel I _D = -2.2A, V _{DS} = -16V, V _{GS} = -4.5V
		P-Ch	—	—	2.9		
Q _{gd}	Gate-to-Drain Charge	N-Ch	—	—	7.9	nC	
		P-Ch	—	—	9.0		
t _{d(on)}	Turn-On Delay Time	N-Ch	—	6.8	—	ns	N-Channel V _{DD} = 10V, I _D = 2.6A, R _G = 6.0Ω, R _D = 3.8Ω
		P-Ch	—	11	—		
t _r	Rise Time	N-Ch	—	21	—		P-Channel V _{DD} = -10V, I _D = -2.2A, R _G = 6.0Ω, R _D = 4.5Ω
		P-Ch	—	17	—		
t _{d(off)}	Turn-Off Delay Time	N-Ch	—	22	—		
		P-Ch	—	25	—		
t _f	Fall Time	N-Ch	—	7.7	—		
		P-Ch	—	18	—		
L _D	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead, 6mm(0.25n) from package and center of die contact
L _S	Internal Source Inductance	N-P	—	6.0	—		
C _{iss}	Input Capacitance	N-Ch	—	520	—	pF	N-Channel V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz
		P-Ch	—	440	—		
C _{oss}	Output Capacitance	N-Ch	—	180	—		P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
		P-Ch	—	200	—		
C _{rss}	Reverse Transfer Capacitance	N-Ch	—	72	—	pF	
		P-Ch	—	93	—		

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.8	A	
		P-Ch	—	—	-1.8		
I _{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	16		
		P-Ch	—	—	-12		
V _{SD}	Diode Forward Voltage	N-Ch	—	—	1.0	V	T _J = 25°C, I _S = 1.8A, V _{GS} = 0V ③
		P-Ch	—	—	-1.0		T _J = 25°C, I _S = -1.8A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	N-Ch	—	47	71	ns	N-Channel
		P-Ch	—	53	80		T _J = 25°C ,I _F = 2.6A, di/dt = 100A/μs ③
Q _{rr}	Reverse Recovery Charge	N-Ch	—	56	84	nC	P-Channel
		P-Ch		66	99		T _J = 25°C, I _F = -2.2A, di/dt = 100A/μs ③
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)					

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 23)
- ② N-Channel I_{SD} ≤ 2.4A, di/dt ≤ 73A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C.
P-Channel I_{SD} ≤ -1.8A, di/dt ≤ 90A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

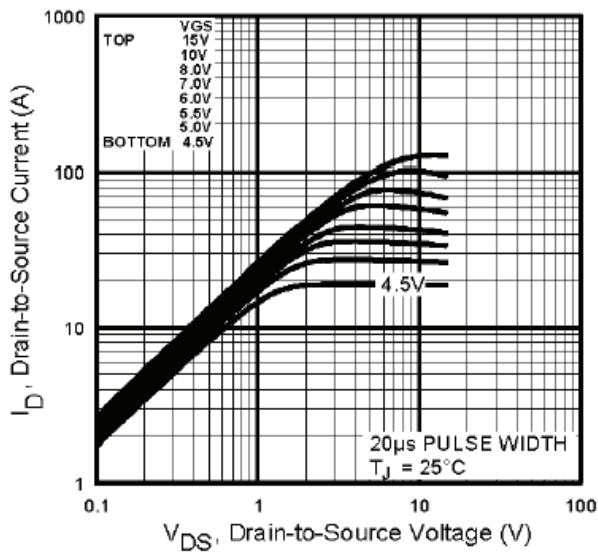


Fig. 1 Typical Output Characteristics
 $T_J = 25^\circ\text{C}$

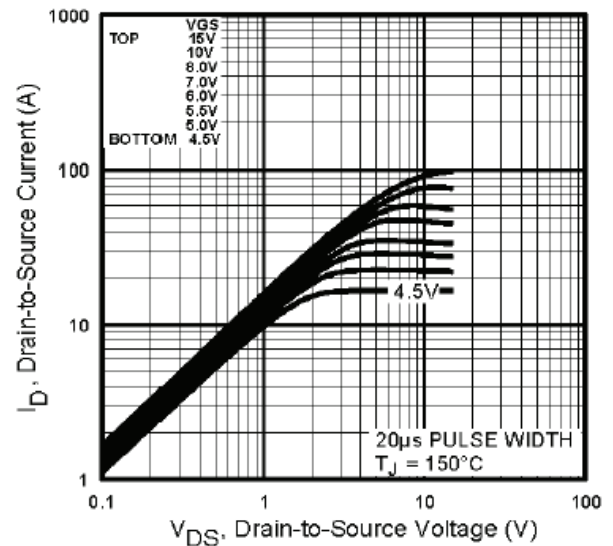


Fig. 2 Typical Output Characteristics
 $T_J = 150^\circ\text{C}$

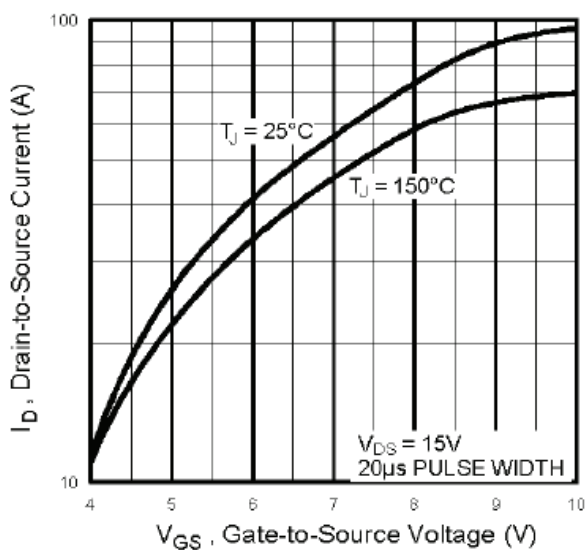


Fig. 3 Typical Transfer Characteristics

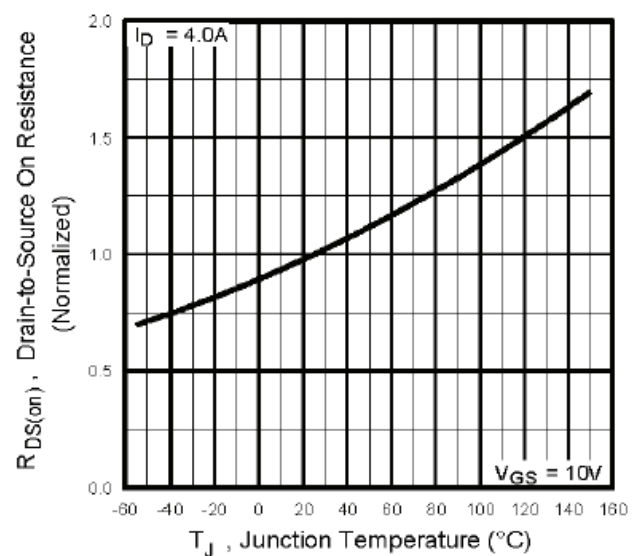


Fig. 4 Normalized On-Resistance
vs. Temperature

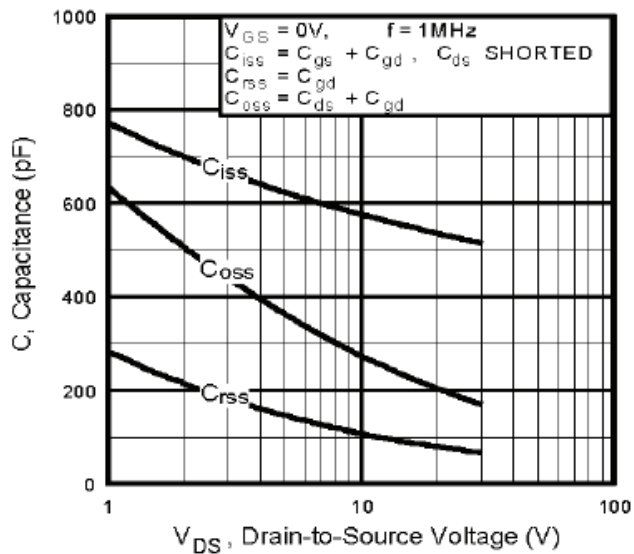


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

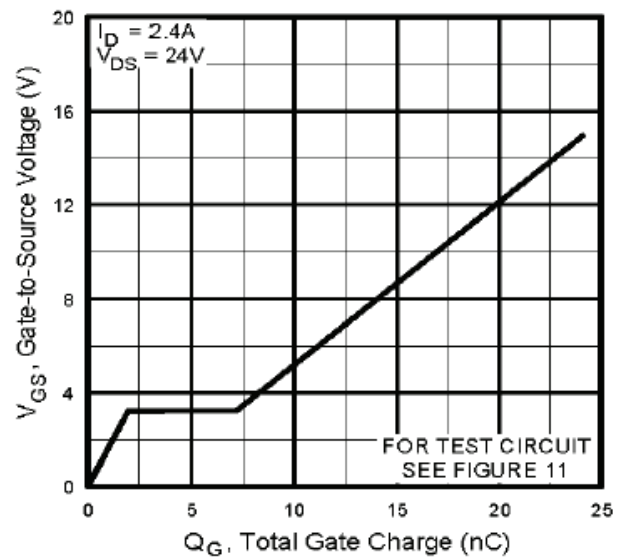


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

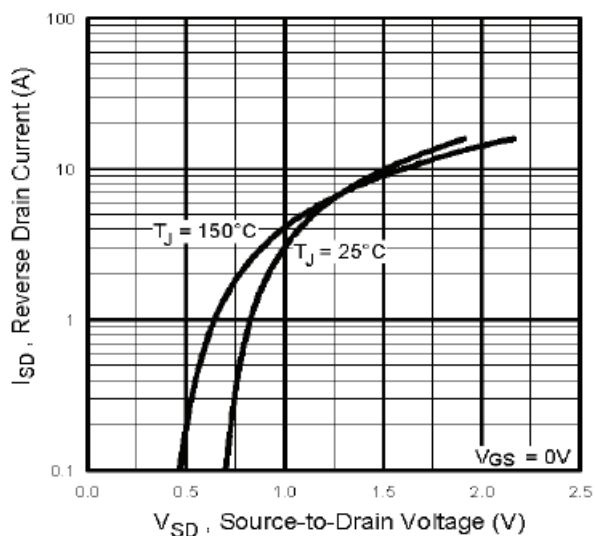


Fig. 7 Typical Source-to-Drain Diode
Forward Voltage

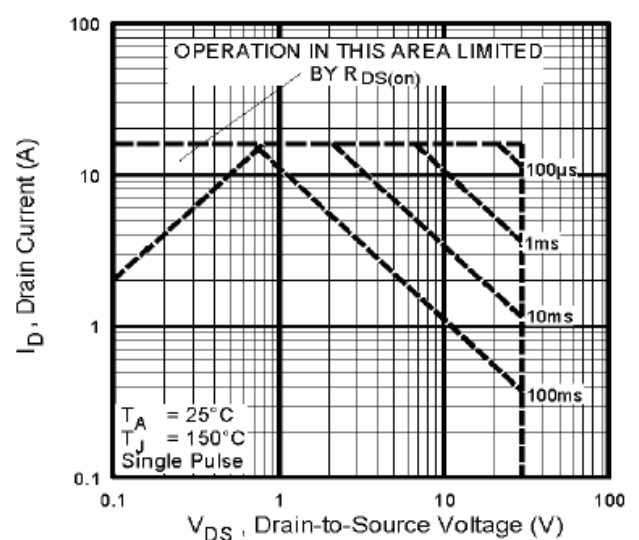


Fig 8. Maximum Safe Operating Area

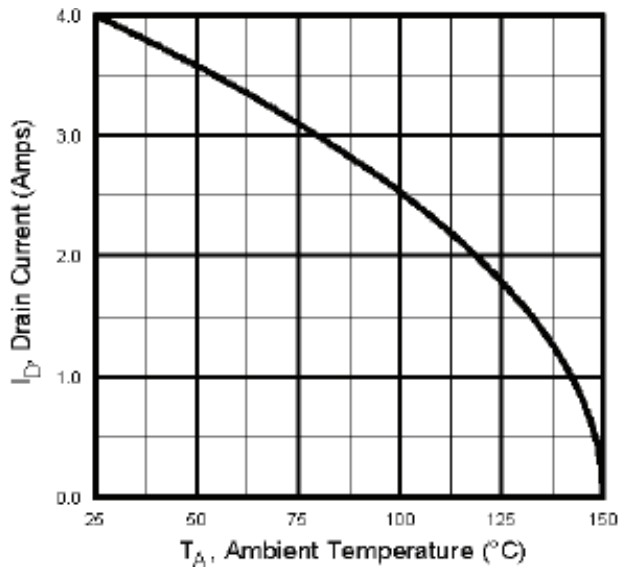


Fig 9. Maximum Drain Current vs. Case Temperature

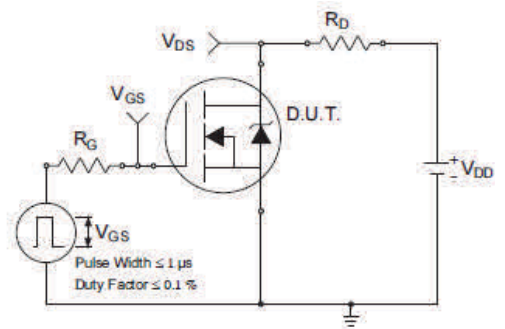


Fig 10a. Switching Time Test Circuit

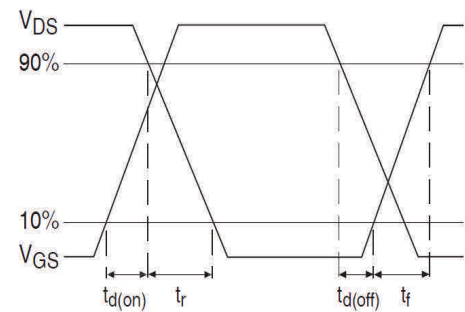


Fig 10b. Switching Time Waveforms

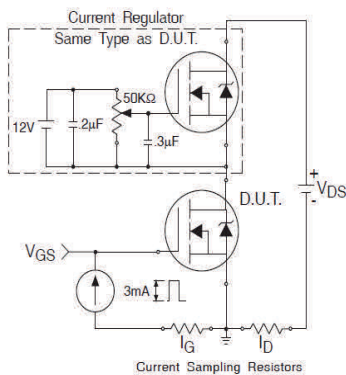


Fig 11a. Gate Charge Test Circuit

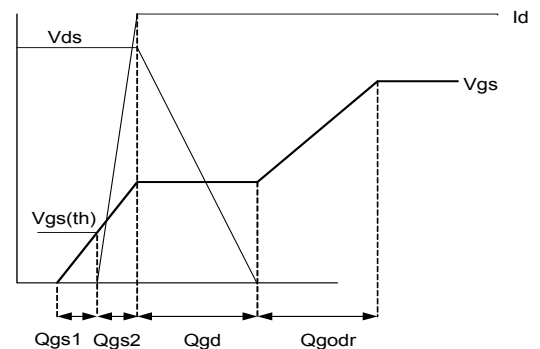


Fig 11b. Basic Gate Charge Waveform

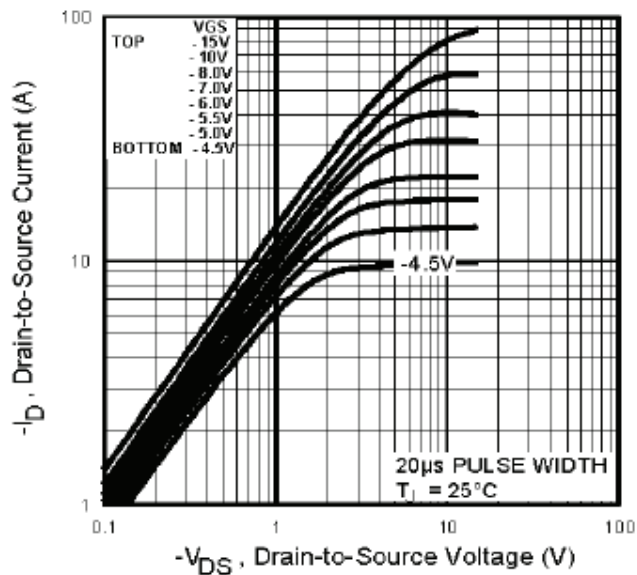


Fig. 12 Typical Output Characteristics
 $T_J = 25^\circ\text{C}$

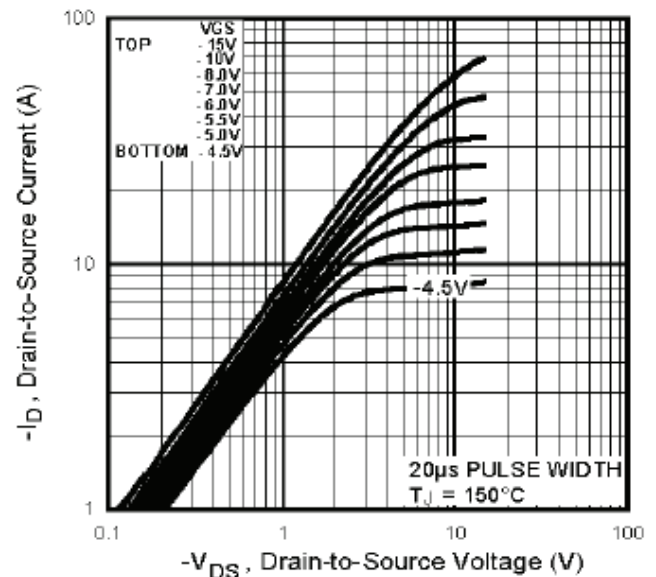


Fig. 13 Typical Output Characteristics
 $T_J = 150^\circ\text{C}$

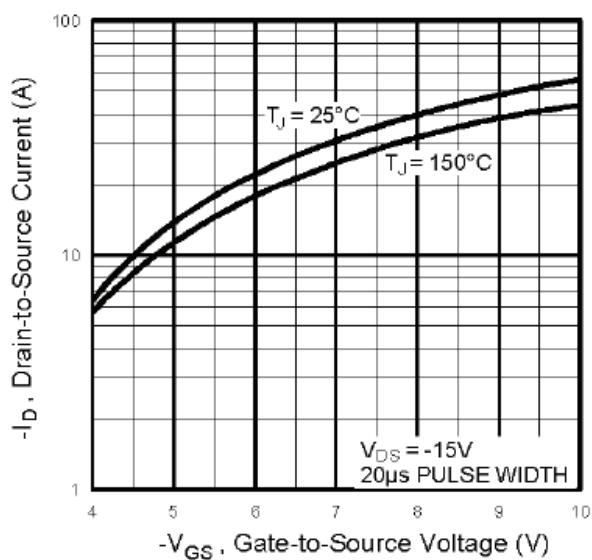


Fig. 14 Typical Transfer Characteristics

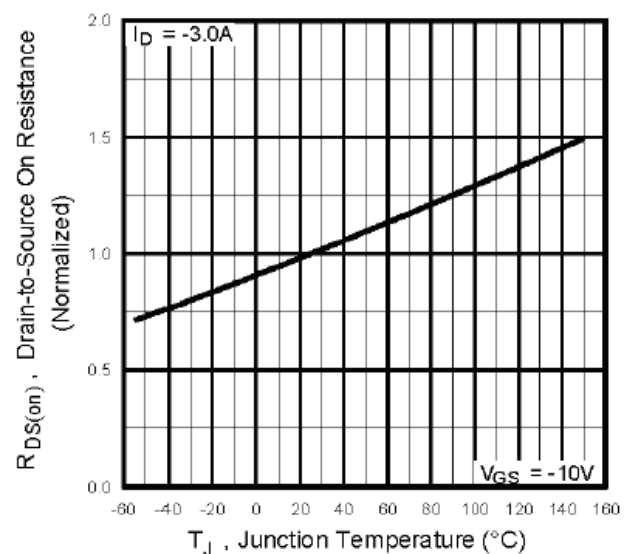


Fig. 15 Normalized On-Resistance
vs. Temperature

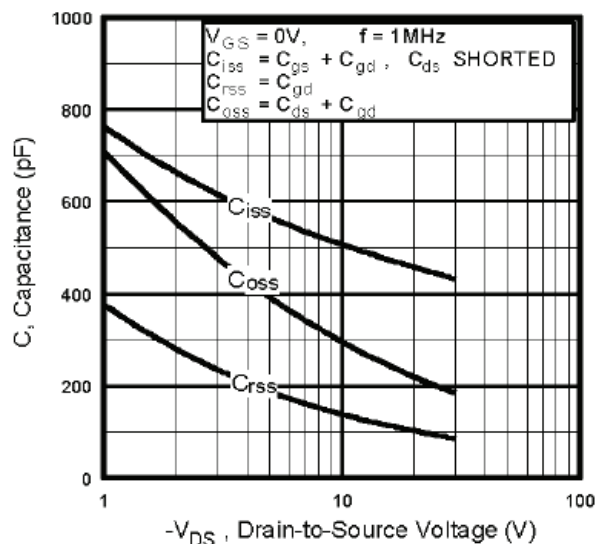


Fig 16. Typical Capacitance vs. Drain-to-Source Voltage

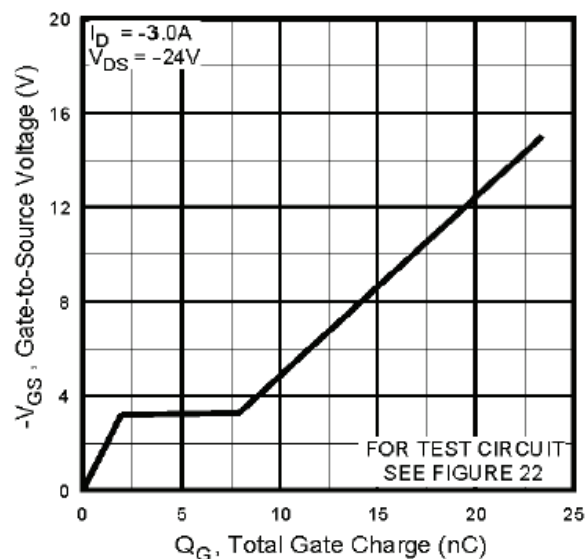


Fig 17. Typical Gate Charge vs. Gate-to-Source Voltage

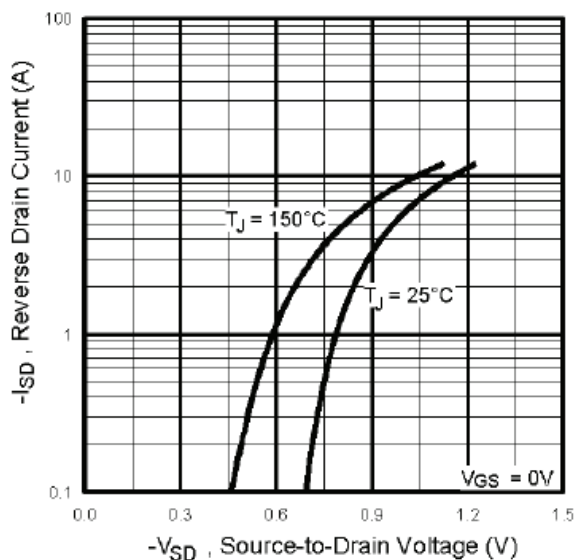


Fig. 18 Typical Source-to-Drain Diode Forward Voltage

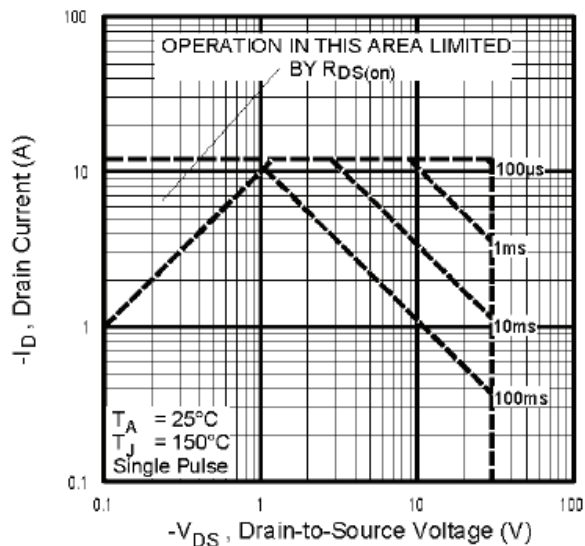


Fig 19. Maximum Safe Operating Area

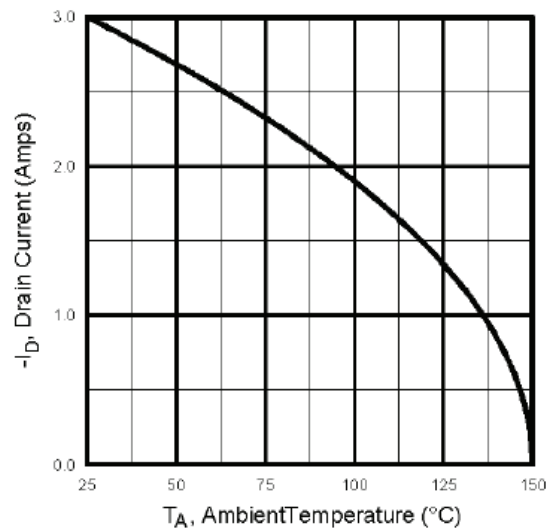


Fig 20. Maximum Drain Current vs. Case Temperature

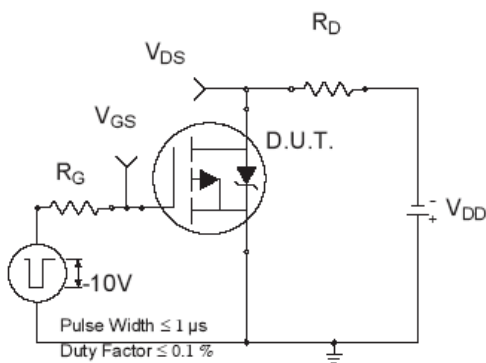


Fig 21a. Switching Time Test Circuit

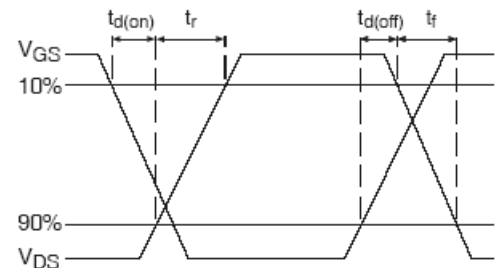


Fig 21b. Switching Time Waveforms

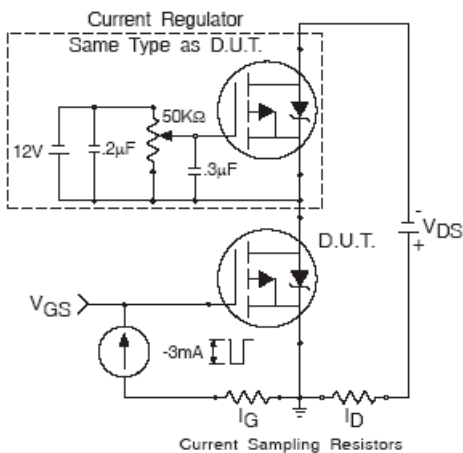


Fig 22a. Gate Charge Test Circuit

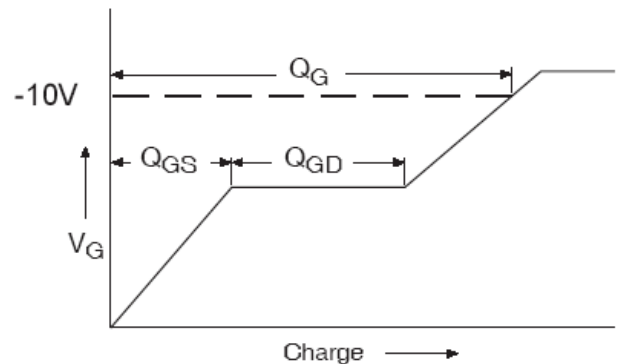


Fig 22b. Basic Gate Charge Waveform

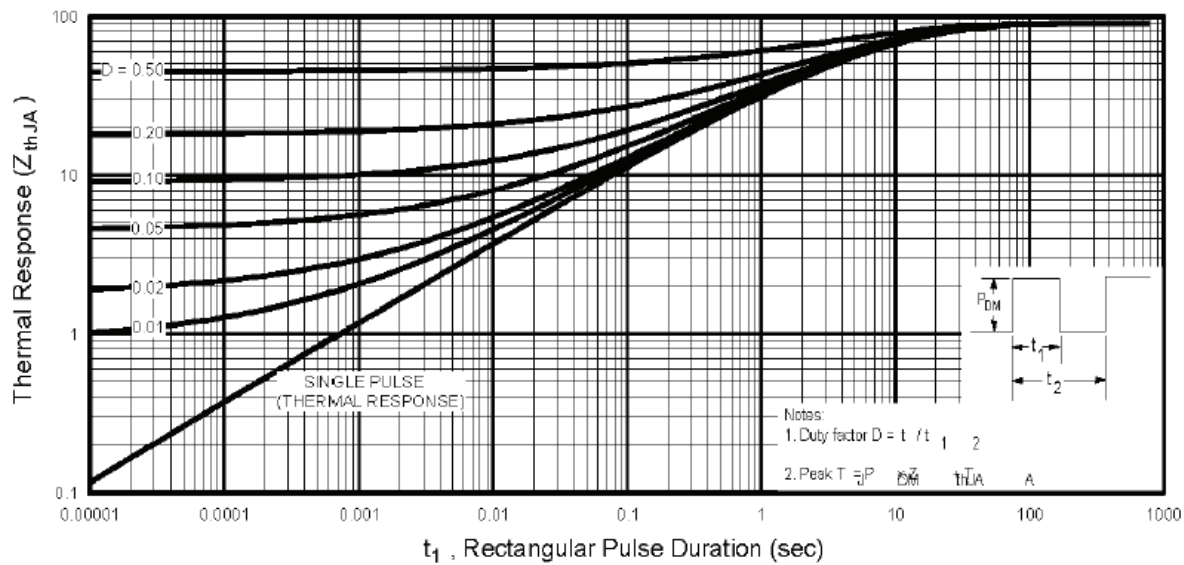


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

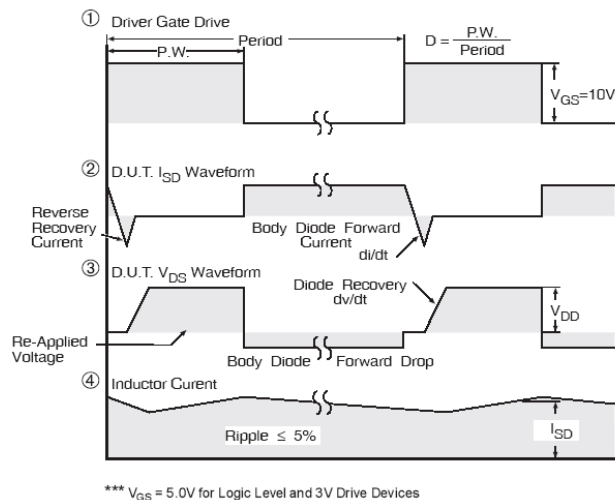
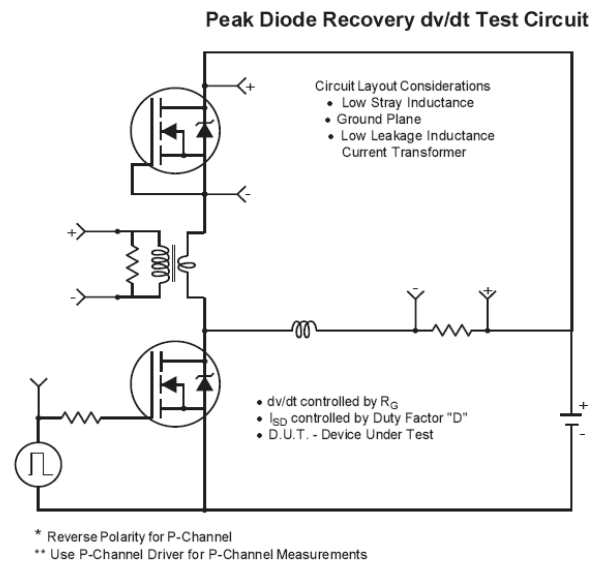


Fig 24. Peak Diode Recovery dv/dt Test Circuit for N & P-Channel HEXFET[®] Power MOSFETs

[illegible]

Technical drawing of a roof profile with dimensions: $K \times 45^\circ$, y , $8X L$, $8X c$, and a circled 7.

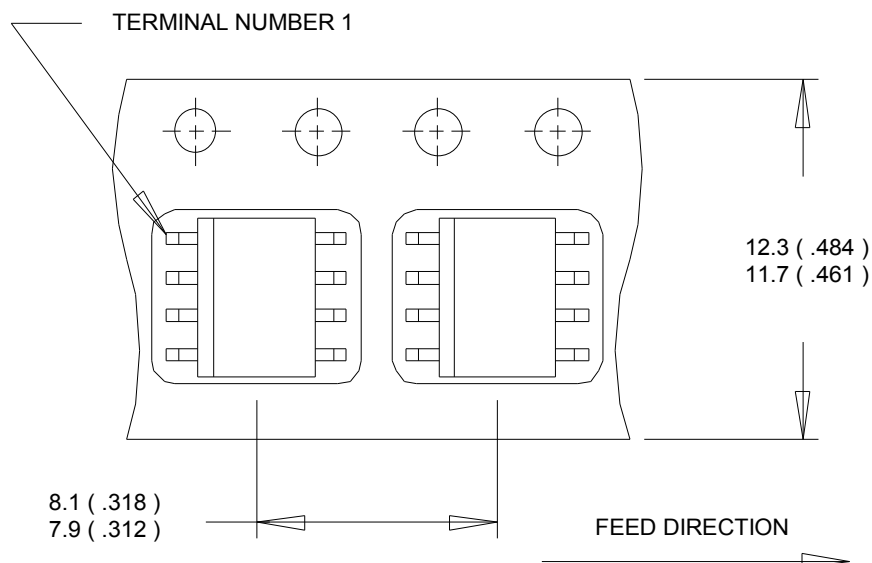
-
- FOOTPRINT
- 8 X 0.72 [.028]
- 6.46 [.255]
- 3 X 1.27 [.050]
- 8 X 1.78 [.070]

Diagram illustrating the marking and identification of a 16-pin automotive rectifier. The rectifier is shown with 16 pins (8 on each side) and a central marking area. The marking area contains the following information:

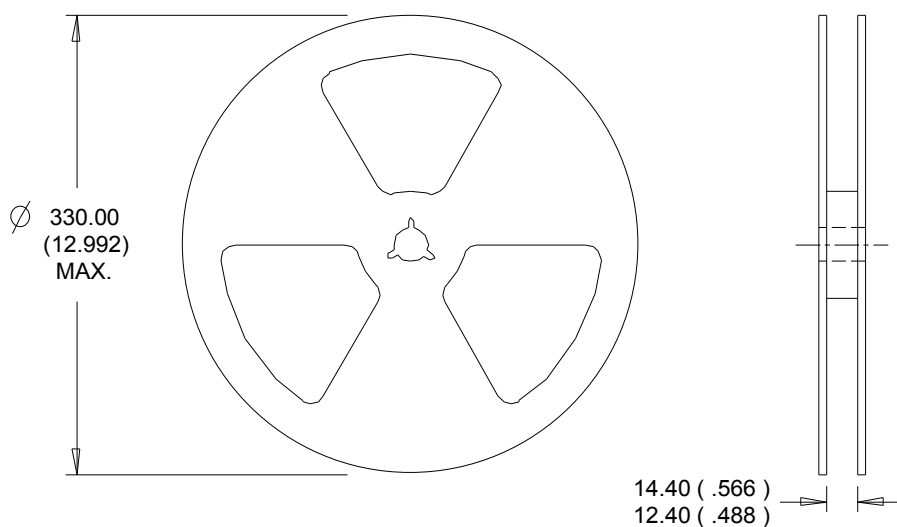
- INTERNATIONAL RECTIFIER LOGO**: The IOR logo.
- DATE CODE**: A code consisting of two digits, 8 and 7, enclosed in circles.
- MARKING CODE (Per Marking Spec.)**: A code consisting of four characters, AYWW?
- PIN 1 IDENTIFIER**: A small black dot.
- PART NUMBER**: A code consisting of seven characters, XXXXXX.
- LOT CODE**: A code consisting of seven characters, F7309Q.

Additional information provided below the diagram:

- (Eng mode – Min. last 4 digits of EATI #)
- (Prod mode – 4 digits SPN code)

SO-8 Tape and Reel (Dimensions are shown in millimeters (inches))

NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	N CH: Class M2 (+/- 150V) [†] P CH: Class M2(+/- 150V) [†] AEC-Q101-002	
	Human Body Model	N CH: Class H1A (+/- 500V) [†] P CH: Class H0 (+/- 250V) [†] AEC-Q101-001	
	Charged Device Model	N CH: Class C5 (+/- 2000V) [†] P CH: Class C5 (+/- 2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
3/28/2014	- Added "Logic Level Gate Drive" bullet in the features section on page 1 - Updated data sheet with new IR corporate template
9/30/2015	- Updated datasheet with corporate template - Corrected ordering table on page 1.

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