

XDP710 Hot-swap Controller

Wide input voltage range (5.5 V to 80 V) system monitoring and protection IC

Features

- Compatible with Infineon's OptiMOS™
- Compatible with Infineon's Linear FET
- Wide input voltage range: 5.5 V to 80 V
- Transient withstand: up to 100 V for 500 ms
- Dedicated current and voltage ADCs: 12-bit
- Programmable and pre-set FET active SOA protection
- Integrated gate driver and charge pump for external N-Channel MOSFET
- Configurable fast FET's shut down: two step turn-off or 1.5 A pull-down current
- PMBus interface: 1 MHz
- Precision input and output voltage monitoring and reporting: $\leq 1\%$
- Precision FET's current monitoring and reporting: $\leq 1\%$
- Precision input power monitoring and reporting: $\leq 2\%$
- Energy monitoring and reporting
- Programmable input and output OV and UV protections
- Support for external temperature sensor and OT protection
- Sequential turn-on capability
- 29-lead (6 mm x 6 mm) VQFN package
- -40°C to 125°C junction temperature

Potential applications

- Server and datacenter
- 24 V - 48 V Industrial systems
- Power distribution systems
- Intelligent e-fuse
- Network router and switches

Description

XDP710 is a wide input voltage Hot Swap and System monitoring Controller IC that drives a single or multiple parallel N-Channel MOSFETs. In addition to a controlled turn ON, XDP710 provides continuous system health monitoring and communication to the main MCU via PMBus interface. The high speed communication through PMBus allows system designers to disable the downstream sub-systems fully or partially.

It incorporates an extensive variety of system protections for safety operation and generates various protection responses depending on the severity of the incident. Latch off, reset, system shutdown and retry are some examples of response types. Its SOA protection effectively ensures that the system FET always operates under safe condition.

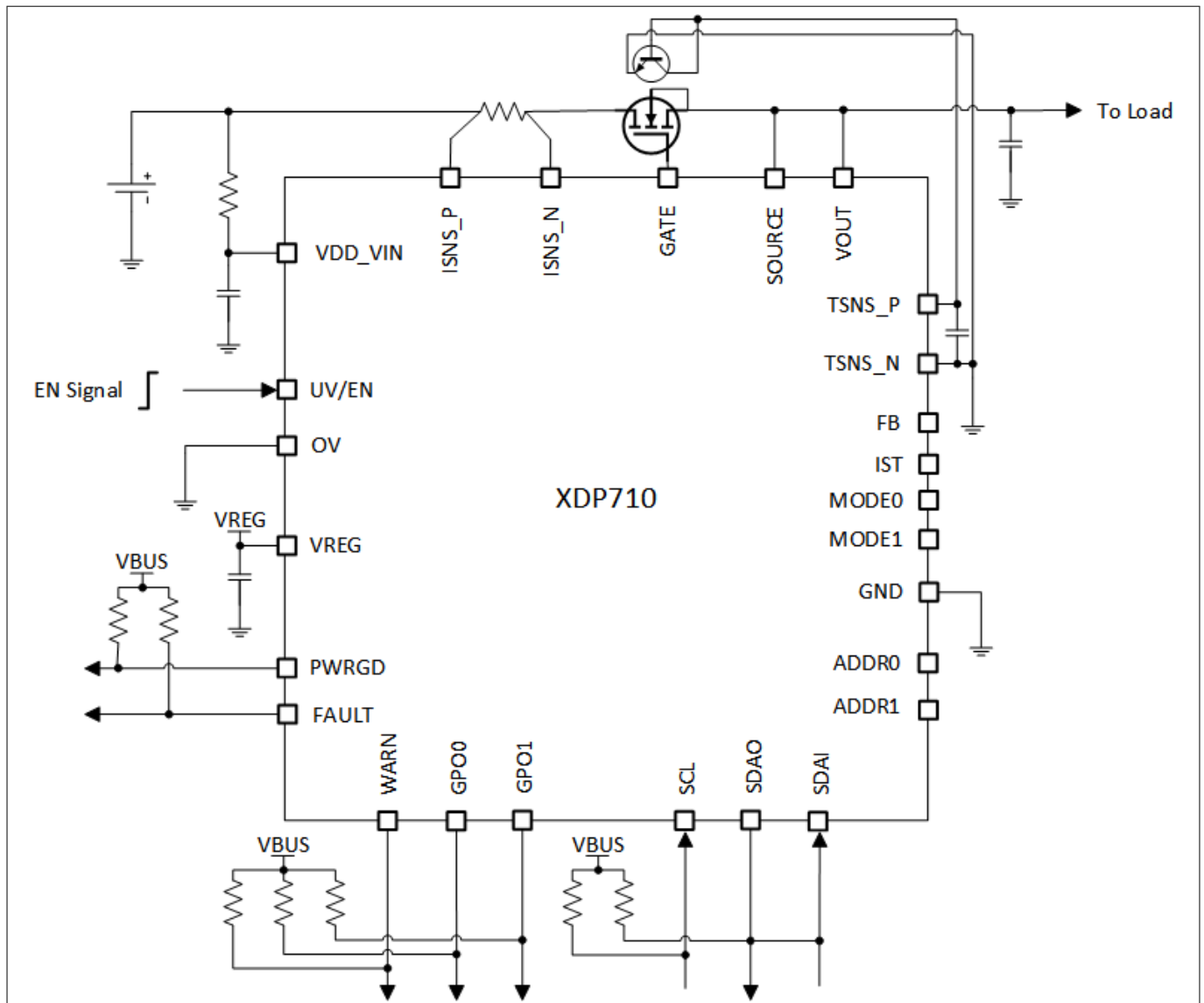


Figure 1 XDP710 Typical application diagram

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1 Block Diagram

1 Block Diagram

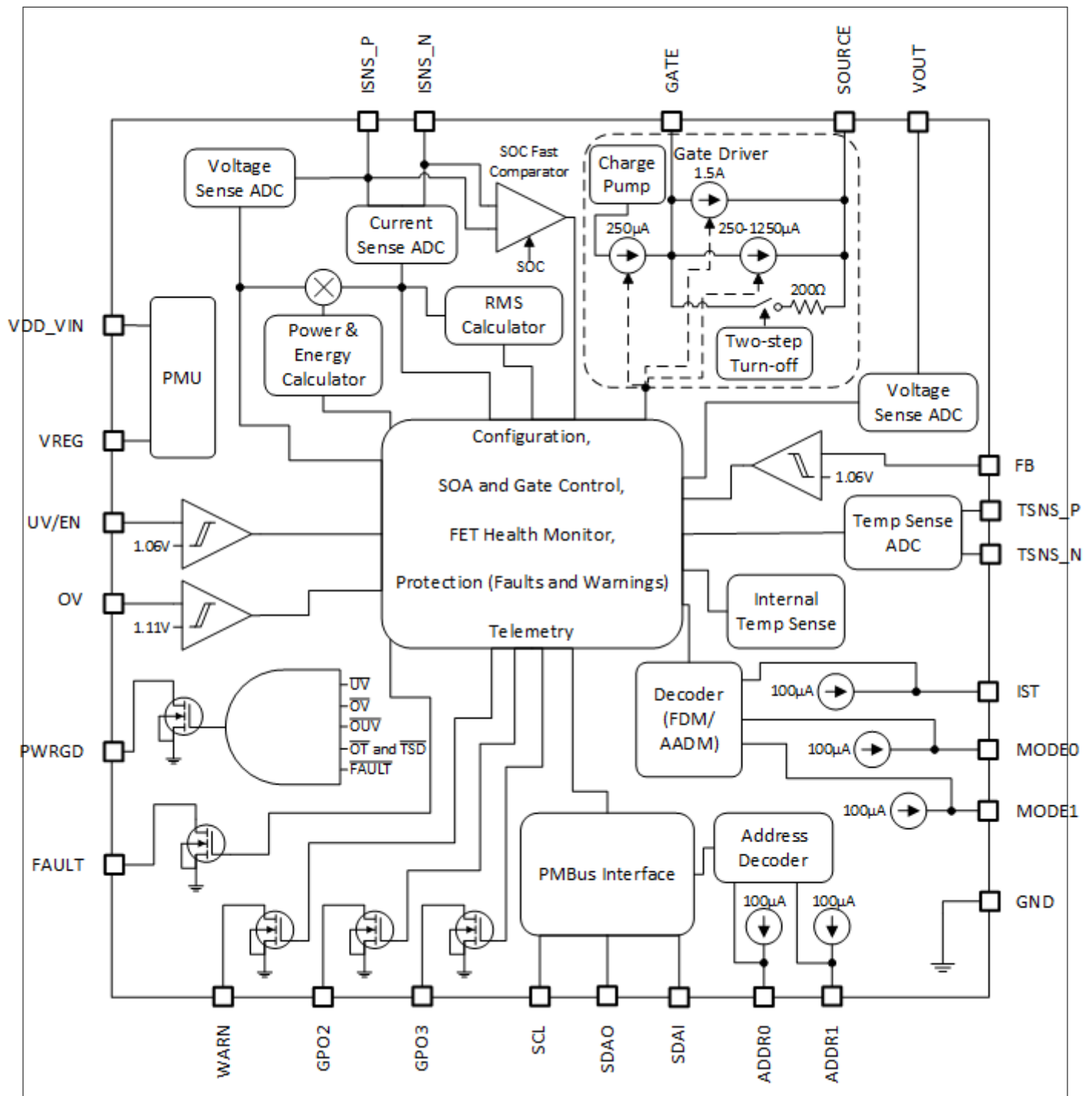


Figure 2 XDP710 Block diagram

2 Pin Configuration and Package

2 Pin Configuration and Package

Table 1 XDP710 pinout

Pin #	Name	I/O	Type	Description	Connection if unused
1	VDD_VIN		P	Power Supply pin	VDD_VIN
2	GND		G	Ground reference, to be connected to system ground	GND
3	UV/EN	I	A	Under Voltage Detection/Enable input. A voltage lower than lower threshold on this pin turns off the FET	VREG
4	OV	I	A	Over Voltage Detection input. A voltage higher than upper threshold on this pin turns off the FET	GND
5	GND		G	Ground reference, to be connected to system ground	GND
6	VREG		P	VREG (internal 5V regulator) output. Connect a 1 μ F capacitor from this pin to GND	Connect a 1 μ F capacitor from this pin to GND
7	PWRGD	O	D	Power Good open drain output. Pin is asserted when VOUT has reached its final level and steady state, FET is fully enhanced and no faults are detected. Its polarity is configurable	Open
8	GPO0/ FAULT	O	D	General-Purpose Digital Output 0. Pin configuration is programmable. Fault open drain output if configured. The pin asserts High/Low (programmable) when a fault occurs. The faults that can trigger the pin to be configured	Open
9	GPO1/ WARN	O	D	General-Purpose Digital Output 1. Pin configuration is programmable. Warning open drain output if configured. The pin asserts High/Low (programmable) when a warning occurs. The warnings that can trigger the pin to be configured	Open
10	GPO2	O	D	General-Purpose Digital Output 2. Pin configuration is programmable	Open
11	GPO3	O	D	General-Purpose Digital Output 3. Pin configuration is programmable	Open

(table continues...)

2 Pin Configuration and Package

Table 1 (continued) XDP710 pinout

12	SCL	I	D	PMBus Clock input. The interface is rated to 1MHz	Open
13	SDAO	O	D	PMBus Data Output . Open drain pin. The serial data is split into an input and an output for easy use with isolators	Pull-up to VREG or external source
14	SDAI	I	D	PMBus Data Input . The serial data is split into an input and an output for easy use with isolators	Pull-up to VREG or external source
15	ADDR0	I	A	Device Address Configuration 0 and 1 inputs. These pins can be tied to GND, left open or tied to GND through a resistor for a total of 16 unique PMBus device addresses	Open
16	ADDR1	I	A		
17	MODE0	I	A	Mode of Operation 0 and 1 inputs. These pins can be tied to GND, left open or tied to GND through a resistor to select between Fully Digital Mode and Analog Assisted Digital Mode. Leave both pins open to select Fully Digital Mode	Open
18	MODE1	I	A		
19	IST	I	A	Start-up Current setting input. A resistor to GND on this pin limits the maximum current allowed at start-up phase	Open
20	FB	I	A	Output Voltage Feedback input. A tap on the voltage divider placed from VOUT to GND is connected to this pin and sets the Output Under Voltage level. A voltage level lower than lower threshold will trigger the Output Under Voltage fault	VREG (ACM), Open (DCM)
21	TSNS_N	IO	A	Temperature Sense Negative terminal. Tie this pin to the emitter of an external NPN BJT to sense the FET's temperature. Connect a 1nF capacitor from this pin to TSNS_P. If unused, this pin must be connected to GND.	GND

(table continues...)

2 Pin Configuration and Package

Table 1 (continued) XDP710 pinout

22	TSNS_P	IO	A	Temperature Sense Positive terminal. Tie this pin to the base and collector of an external NPN BJT to sense the FET's temperature. Connect a 1nF capacitor from this pin to TSNS_N. If unused, this pin must be connected to GND.	GND
23	GND		G	Ground reference, to be connected to system ground	GND
24	VOUT	I	A	Output Voltage Sense input	VOUT
25	SOURCE	IO	A	Source terminal, single or multiple parallel external N channel FETs return path. Pin is directly connected to the source of the FET/FETs. The GATE pin is referenced from this pin and pull-down currents flow through this pin	SOURCE
26	GATE	O	A	Gate Driver output of single or multiple parallel external N channel FETs, referenced to SOURCE. It uses a charge pump to provide a pull-up current to charge the FET gate/gates. The FET/FETs is/are regulated to a maximum load current by regulating the GATE pin voltage. GATE is pulled down when the supply is not within UV and OV or fault occurs	GATE
27	DNC			Do not connect pin (to provide isolation between high and low voltage signals)	Open
28	ISNS_N	I	A	Current Sense Negative input	ISNS_N
29	ISNS_P	I	A	Current Sense Positive input	ISNS_P
EP	GND		G	Ground reference. The exposed pad to be connected to system ground	GND

2 Pin Configuration and Package

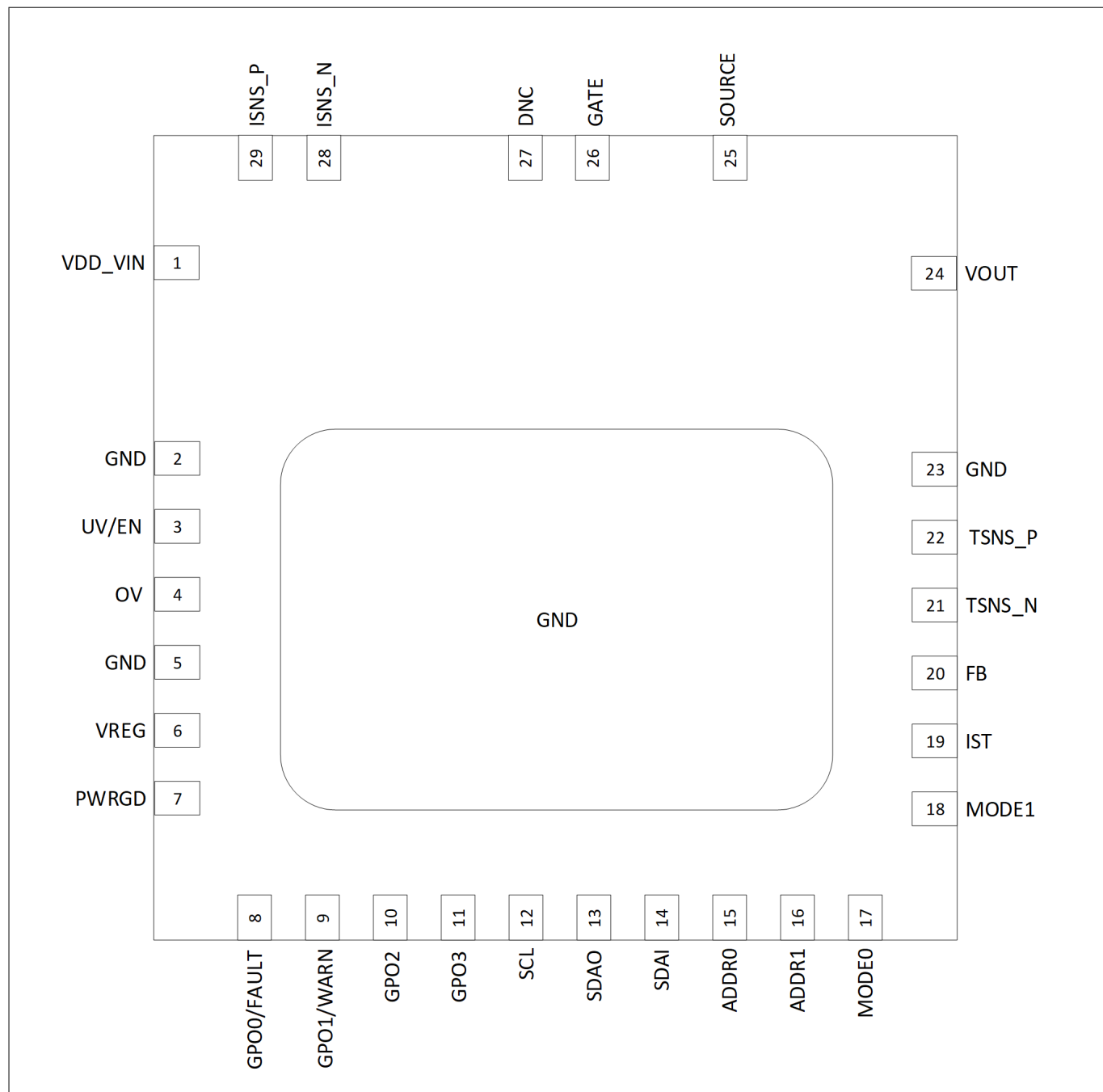


Figure 3 VQFN-29 6x6 pinout

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Wide input voltage range (5.5 V to 80 V) system monitoring and protection IC

2 Pin Configuration and Package

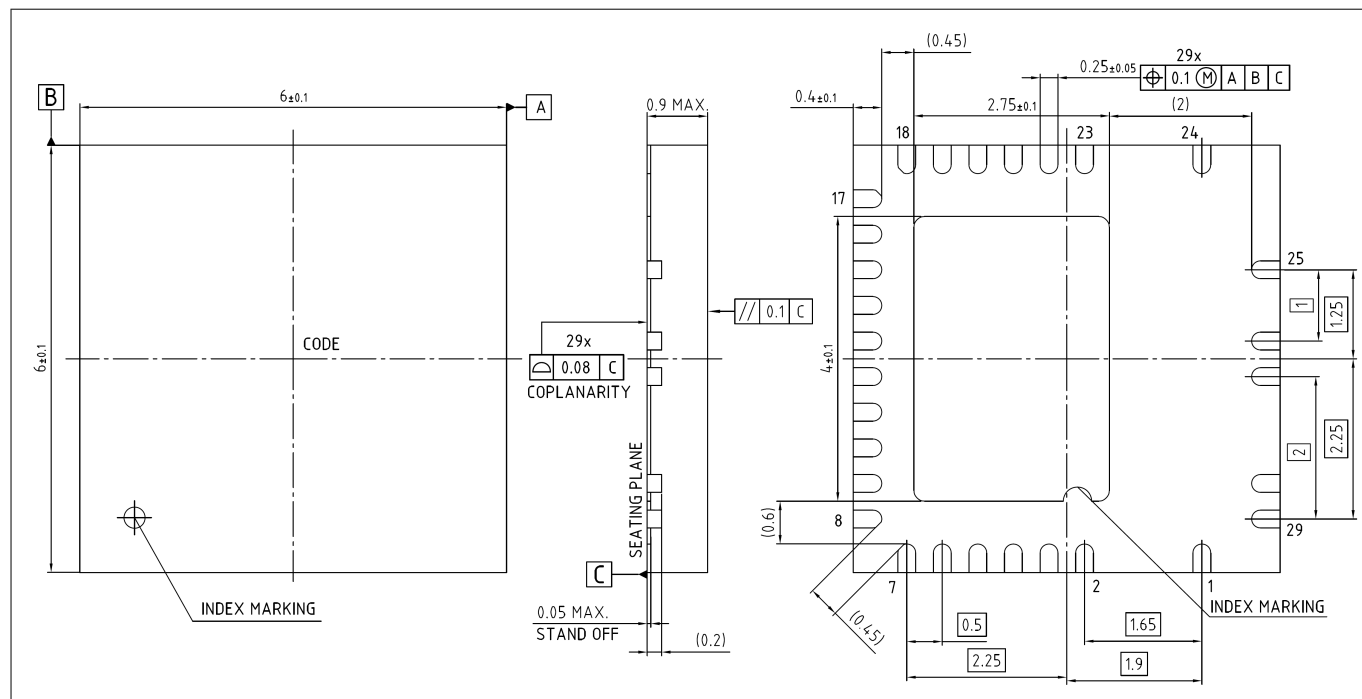


Figure 4 Package dimensions

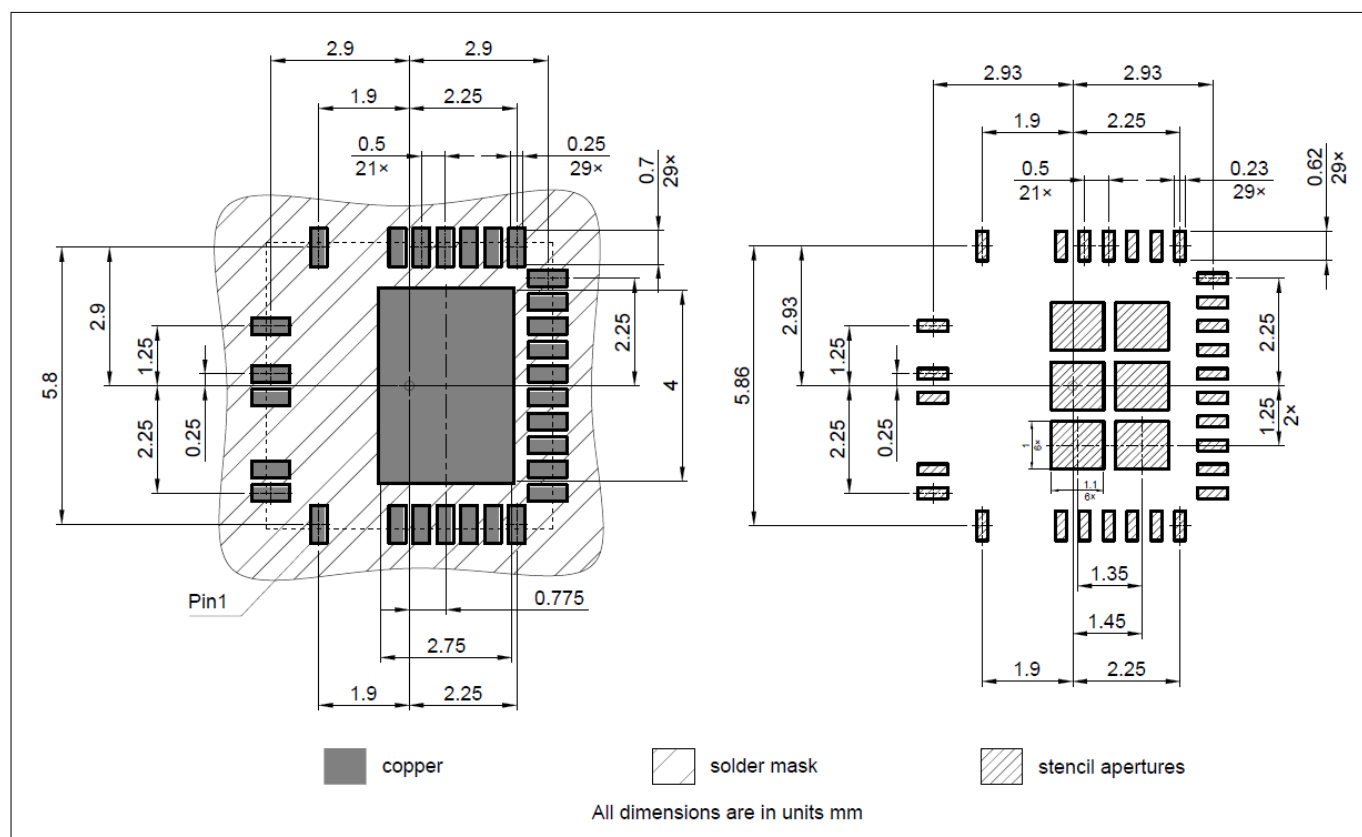


Figure 5 Recommended footprint

3 General Product Characteristics

3 General Product Characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, $T_A = 25^\circ\text{C}$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VDD_VIN pin	VDD_VIN _{DC}	-0.3		80	V	
Supply voltage transients at VDD_VIN pin	VDD_VIN _{AC}			100	V	For 500ms max
Voltage slew rate at VDD_VIN pin	VDD_VIN _{SR}			80	V/ μs	The RC filter (i.e. 10 Ω / 100nF, or 100 Ω / 10nF, etc.) on the pin is recommended, especially for high voltage (i.e. 48V) applications
Voltage slew rate at ISNS_P and ISNS_N pins	V _{ISNS_P_SR} , V _{ISNS_N_SR}			80	V/ μs	The resistor (i.e.10 Ω) in series to each pin is recommended if an excessive dV/dt may occur in the application
Voltage slew rate at SOURCE and VOUT pins	V _{SOURCE_SR} , V _{VOUT_SR}			80	V/ μs	An output cap (10 μF min) limits a slew rate on the pins
Voltage at SOURCE pin	V _{SOURCE_DC}	-0.3		80	V	
Voltage transients at SOURCE pin	V _{SOURCE_AC}			100	V	For 500ms max
Output voltage at GATE pin	V _{GATE_DC}	-0.3		92	V	
Voltage transients at GATE pin	V _{GATE_AC}			100	V	For 500ms max
GATE to SOURCE voltage	V _{GATE-SOURCE_DC}	-0.3		12	V	
GATE to SOURCE voltage transients	V _{GATE-SOURCE_AC}			15	V	For 500ms max
Output voltage at VREG pin	V _{VREG}	-0.3		6	V	

(table continues...)

3 General Product Characteristics
Table 2 (continued) Absolute maximum ratings

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, $T_A = 25^\circ\text{C}$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital pins output voltage (PWRGD, FAULT, WARN, GPOx, SDAO)	$V_{\text{PWRGD}}, V_{\text{FAULT}}, V_{\text{WARN}}, V_{\text{GPOx}}, V_{\text{SDAO}}$	-0.3		6	V	
Input voltage at VOUT pin	$V_{\text{OUT_DC}}$	-0.3		80	V	
Input voltage transients at VOUT pin	$V_{\text{OUT_AC}}$			100	V	For 500ms max
Input voltage at ISNS_P, ISNS_N pins	$V_{\text{ISNS_P_DC}}, V_{\text{ISNS_N_DC}}$	-0.3		80	V	
Input voltage transients at ISNS_P, ISNS_N pins	$V_{\text{ISNS_P_AC}}, V_{\text{ISNS_N_AC}}$			100	V	For 500ms max
Current Sense input voltage (ISNS_P - ISNS_N)	$V_{\Delta\text{ISNS}}$	-0.8		0.8	V	
Analog pins input voltage (UV/EN, OV, ADDR _x , MODE _x , IST, FB, TSNS_N)	$V_{\text{UV_EN}}, V_{\text{OV}}, V_{\text{ADDRx}}, V_{\text{MODEx}}, V_{\text{IST}}, V_{\text{FB}}, V_{\text{TSNS_N}}$	-0.3		6	V	
Input voltage at TSNS_P pin	$V_{\text{TSNS_P}}$	-0.3		2.5	V	
Digital pins input voltage (SCL, SDAI)	$V_{\text{SCL}}, V_{\text{SDAI}}$	-0.3		6	V	
Junction Temperature range	T_J	-40		150	°C	
Storage Temperature range	T_S	-55		150	°C	

3 General Product Characteristics

3.2 Functional range

Table 3 Functional and performance ranges description

Absolute Voltage Range at VDD_VIN (V)	Communication Interface	FET Gate	VREG
$0 \leq V_{in} < 5.5$	Off	Off (passive pull-down)	Off
$5.5 \leq V_{in} < 9$	On	Limited operation: - Off (active pull-down); - limited SOA regulation depending on gate driver supply; - On/enhancement is not guaranteed (but $\geq 4.5V$)	4.5V (min)
$9 \leq V_{in} \leq 80$		Full operation: - Off (active pull-down); - full SOA regulation; - On/enhancement (typ 10.5V)	5.0V (typ)

Table 4 Functional range

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, $T_A = 25^\circ C$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VDD_VIN pin	VDD_VIN	5.5	12, 24, 48	80	V	
Supply voltage at VDD_VIN pin to enable all features	VDD_VIN _{EN}	9			V	See Table 3 .
ISNS_P sense pin input voltage	V _{ISNS_P}	5.5		80	V	
VOOUT sense pin input voltage	VOOUTS	0	–	80	V	
Current Sense input voltage (ISNS_P - ISNS_N)	V _{ΔISNS}	-0.4		0.4	V	
Minimum overcurrent setting	I _{OC_MIN}	5	–	–	A	Minimum I _{OC} (I _{OC} = V _{SNS_CS} / R _{SNS} , see Setting I_{OC}) for optimum stability.

(table continues...)

3 General Product Characteristics
Table 4 (continued) Functional range

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, $T_A = 25^\circ\text{C}$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Analog pins input voltage (UV/EN, OV, ADDR _x , MODE _x , IST, FB)	$V_{UV_EN}, V_{OV}, V_{ADDRx}, V_{MODEx}, V_{IST}, V_{FB}$	0	–	5.5	V	
Analog pins input voltage TSNS_P/N	$V_{TSNS_P/N}$	0	–	1	V	Recommended range for best accuracy.
Digital pins input voltage (SCL, SDAI)	V_{SCL}, V_{SDAI}	0	–	5.5	V	
Output voltage at VREG pin	V_{VREG}	4.5	5	5.5	V	At 10 mA max external load.
Digital pins output voltage (PWRGD, FAULT, WARN, GPO _x , SDAO)	$V_{PWRGD}, V_{FAULT}, V_{WARN}, V_{GPOx}, V_{SDAO}$	0	–	5.5	V	
Junction temperature range	T_J	-40	–	125	°C	

3.3 Thermal characteristics
Table 5 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance Junction-to-case (bottom)	$R_{\Theta JC_Bot}$	–	5	–	K/W	PCB simulation setup as described in Table 6 .
Thermal resistance Junction-to-case (top)	$R_{\Theta JC_Top}$	–	30	–	K/W	PCB simulation setup as described in Table 6 .

(table continues...)

3 General Product Characteristics

Table 5 (continued) Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance Junction-to-Ambient	$R_{\Theta JA}$	–	33	–	K/W	PCB simulation setup as described in Table 6 .
Package power dissipation	P_{PAK}	–	–	0.8	W	

Table 6 PCB characteristics for thermal simulation

		λ_{therm} [W/m-K]
Metalization	JEDEC 2s2p (JESD 51-7, JESD 51-5)	388
Cooling Area [mm ²]	none	388

Note: Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

3.4 Current consumption

Table 7 Current consumption

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current Consumption	I_{VDD}	–	7	10	mA	VDD_VIN supply current: FET is fully ON, telemetry in ON.

3.5 ESD robustness

Table 8 ESD robustness

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD Robustness HBM	V_{ESD_HBM}			±2000	V	
ESD Robustness CDM	V_{ESD_CDM}			±500	V	

3 General Product Characteristics
3.6 Electrical characteristics
Table 9 Electrical characteristics

VDD_VIN - GND = 48 V, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0$ V, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UV/EN, OV and FB in AADM						
Input upper threshold	V _{UVEN_UTH} , V _{OV_UTH} , V _{FB_UTH}	1.09	1.11	1.13	V	
Input lower threshold	V _{UVEN_LTH} , V _{OV_LTH} , V _{FB_LTH}	1.04	1.06	1.08	V	
TSNS_P, TSNS_N						
TSNS_P operating voltage	V _{TSNS_P}	0.25	–	1	V	
TSNS_N operating voltage range	V _{TSNS_N}	–	0	–	V	
ISNS_P, ISNS_N						
Minimum detectable differential voltage level	V _{SNS_MIN}	0.01 * V _{SNS_CS}	–	–	mV	Between ISNS_P and ISNS_N pins.
Current sense differential voltage range	V _{SNS_CS}	–	12.5	–	mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 00
Current sense differential voltage range	V _{SNS_CS}	--	25		mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 01
Current sense differential voltage range	V _{SNS_CS}	–	50	–	mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 10
Current sense differential voltage range	V _{SNS_CS}	–	100	–	mV	Set by CS_RNG[1:0] bits: CS_RNG[1:0] = 11
SOC Differential voltage level	V _{SNS_SOC}	9.5	12.5	15.5	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 000 and CS_RNG[1:0] = 00 or 01

(table continues...)

3 General Product Characteristics
Table 9 (continued) Electrical characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SOC Differential voltage level	V_{SNS_SOC}	15.75	18.75	21.75	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 001 and CS_RNG[1:0] = 00 or 01
SOC Differential voltage level	V_{SNS_SOC}	22	25	28	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 010 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 000 and CS_RNG[1:0] = 10 or 11
SOC Differential voltage level	V_{SNS_SOC}	34.5	37.5	40.5	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 011 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 001 and CS_RNG[1:0] = 10 or 11
SOC Differential voltage level	V_{SNS_SOC}	47	50	53	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 100 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 010 and CS_RNG[1:0] = 10 or 11
SOC Differential voltage level	V_{SNS_SOC}	71	75	79	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 101 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 011 and CS_RNG[1:0] = 10 or 11
SOC Differential voltage level	V_{SNS_SOC}	96	100	104	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 110 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 100 and CS_RNG[1:0] = 10 or 11
SOC Differential voltage level	V_{SNS_SOC}	145	150	155	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 111 and CS_RNG[1:0] = 00 or 01; or SOC_FAULT_LIMIT[2:0] = 101 and CS_RNG[1:0] = 10 or 11
SOC Differential voltage level	V_{SNS_SOC}	193	200	207	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 110 and CS_RNG[1:0] = 10 or 11

(table continues...)

3 General Product Characteristics
Table 9 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, V_{ΔISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SOC Differential voltage level	V _{SNS_SOC}	290	300	310	mV	Set by SOC_FAULT_LIMIT[2:0] and CS_RNG[1:0] bits: SOC_FAULT_LIMIT[2:0] = 111 and CS_RNG[1:0] = 10 or 11
Current sense ADC resolution		–	12	–	bits	
Max allowed negative current	I _{NEG_MAX}	–	240	–	mA	To trigger INEG warning. V _{SNS_CS} = 12.5 mV, R _{sns} = 1 mΩ.
Max allowed negative current	I _{NEG_MAX}	–	520	–	mA	To trigger INEG warning. V _{SNS_CS} = 25 mV, R _{sns} = 1 mΩ.
Max allowed negative current	I _{NEG_MAX}	–	1100	–	mA	To trigger INEG warning. V _{SNS_CS} = 50 mV, R _{sns} = 1 mΩ.
Max allowed negative current	I _{NEG_MAX}	–	2200	–	mA	To trigger INEG warning. V _{SNS_CS} = 100 mV, R _{sns} = 1 mΩ.

GATE

Gate voltage	V _{GATE}	8.5	10.5	12.0	V	9V ≤ VDD_VIN ≤ 80V, I _{GATE} ≤ 5μA, FET is fully ON
Gate voltage	V _{GATE}	4.0			V	5.5V ≤ VDD_VIN < 9V, I _{GATE} ≤ 5μA
Pull-up current	I _{GATE_PU}	200	250	300	μA	At V _{GATE} = 5 V
Fast pull-down current	I _{GATE_FPD}	0.825	1.5	2.175	A	Set by GATE_FAST_PD[0]: GATE_FAST_PD[0] = 0
GATE pin two step turn-off fast pull-down	R _{GATE_2ST_FA} ST_PD	156	200	244	Ω	Set by GATE_FAST_PD[0]: GATE_FAST_PD[0] = 1
Slow pull-down current	I _{GATE_SPD}	200	250	300	μA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 00 Used for both regular/slow pull-down and second phase of the two-step turn-off.
Slow pull-down current	I _{GATE_SPD}	400	500	600	μA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 01 Used for both regular/slow pull-down and second phase of the two-step turn-off.

(table continues...)

3 General Product Characteristics
Table 9 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, $V_{ISNS_P} = VDD_VIN$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0$ V, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Slow pull-down current	I_{GATE_SPD}	600	750	900	μA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 10 Used for both regular/slow pull-down and second phase of the two-step turn-off.
Slow pull-down current	I_{GATE_SPD}	1000	1250	1500	μA	Set by GATE_SLOW_PD[1:0] bits: GATE_SLOW_PD[1:0] = 11 Used for both regular/slow pull-down and second phase of the two-step turn-off.

VDD_VIN

On-chip input over voltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	70	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 00
On-chip input over voltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	75	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 01
On-chip input over voltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	80	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 10
On-chip input over voltage upper threshold for on-chip input overvoltage fault assertion	OV_{IN_UTH}	–	85	–	V	Set by OVIN_FAULT_LIMIT[1:0] bits: OVIN_FAULT_LIMIT[1:0] = 11

(table continues...)

3 General Product Characteristics
Table 9 (continued) Electrical characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-chip input over voltage lower threshold for on-chip input overvoltage fault release	OV_{IN_LTH}	–	$OV_{IN_UTH} - 5\text{ V}$	–	V	For on-chip input overvoltage fault release.

VOUT

Input current	I_{VOUT}	–	15		μA	At 48 V
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Telemetry

Monitored voltage range (input and output voltages)	V_{TLM}	22	–	88	V	Set by VTLM_RNG[1:0] bits: 2'b00: 88 V 2'b01: 44 V 2'b10: 22 V 2'b11: n.a.
Input voltage measurement accuracy		-1.0	–	1.0	%	At ISNS_P vs GND: $ISNS_P = 40\text{ V}$ to 80 V , 20 V to 40 V or 10 V to 20 V depending on corresponding programmed range V_{TLM} .
Output voltage measurement accuracy		-1.0	–	1.0	%	At VOUT vs GND: $VOUT = (40\text{ V to } 80\text{ V}) / (20\text{ V to } 40\text{ V}) / (10\text{ V to } 20\text{ V})$ depending on corresponding programmed range V_{TLM} .
Current measurement accuracy		-1.0	–	1.0	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS} = 50\text{ mV}$ or 100 mV depending on corresponding programmed range V_{SNS_CS} .
Current measurement accuracy		-2.0	–	2.0	%	Between ISNS_P & ISNS_N pins. $V_{\Delta ISNS} = 12.5\text{ mV} / 25\text{ mV}$ depending on corresponding programmed range V_{SNS_CS} .
Calculated input power accuracy		-2.0	–	2.0	%	Input voltage: $ISNS_P = (40\text{ V to } 80\text{ V}) / (20\text{ V to } 40\text{ V}) / (10\text{ V to } 20\text{ V})$ depending on corresponding programmed range V_{TLM} . Current sensing: $V_{\Delta ISNS} = 50\text{ mV}$ or 100 mV depending on corresponding programmed range V_{SNS_CS} .
Calculated energy accuracy		-5.0	–	5.0	%	Input voltage: $ISNS_P = (40\text{ V to } 80\text{ V}) / (20\text{ V to } 40\text{ V}) / (10\text{ V to } 20\text{ V})$ depending on corresponding programmed range V_{TLM} . Current sensing: $V_{\Delta ISNS} = 50\text{ mV}$ or 100 mV depending on corresponding programmed range V_{SNS_CS} .

(table continues...)

3 General Product Characteristics
Table 9 (continued) Electrical characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-chip temperature monitored range		-40	–	150	$^\circ\text{C}$	
On-chip temperature measurement accuracy		-5	–	5	$^\circ\text{C}$	
Temperature measurements accuracy		–	± 4.0	± 12.5	$^\circ\text{C}$	Sourcing currents in TSNS_P pin. Sense the voltage between TSNS_P & TSNS_N pins. External transistor is: MMBT3904.

VREG

Output voltage	V_{REG}	4.7	5.0	5.3	V	$9\text{ V} \leq V_{DD_VIN} \leq 80\text{ V}$. $C_{VREG} = 1\text{ }\mu\text{F}$. Internal load + external load. Package maximum power dissipation limit (P_{PAK}) must not be violated.
Output voltage	V_{REG}	4.5	–	–	V	$5.5\text{ V} \leq V_{DD_VIN} \leq 9\text{ V}$. $C_{VREG} = 1\text{ }\mu\text{F}$. Internal load + external load. Package maximum power dissipation limit (P_{PAK}) must not be violated.
Current capability to supply external load	I_{REG}	–	–	10	mA	

PWRGD, GPOx, FAULT, WARN

Output low voltage		–	–	0.4	V	At 10 mA
Leakage current		–	–	5	μA	At 5.5 V, output is HiZ.
Current sink capability		–	–	10	mA	

SDAI, SDAO, SCL

Input high voltage		2.0	–	–	V	
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(table continues...)

3 General Product Characteristics
Table 9 (continued) Electrical characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, V_{ΔISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input low voltage		–	–	0.8	V	
Output low voltage		–	–	0.4	V	At 20 mA
Input leakage current		–	–	5.0	μA	At 5.5 V
Nominal bus voltage	V _{BUS}	3.0	3.3 or 5.0	5.5	V	
Capacitive load per bus segment		–	–	400	pF	
Pin capacitance		–	5	10	pF	

ADDRx

Pin sense current	I _{ADDR}	–	100	–	μA	
Programmability voltage step		–	0.8	–	V	See Table 13 for more info.

MODEx

MODEx pins sense current	I _{MODE}	–	100	–	μA	
Programmability voltage step		–	0.8	–	V	See Table 12 for more info.

IST

Pin sense current	I _{IST}	–	100	–	μA	
Programmability voltage step			See Table 19		V	

On-chip thermal shut-down

Protection trigger upper threshold	T _{TS_UTH}	130	–	145	°C	Set by ONCHIP_TSD_FAULT_LIMIT[1:0] bits: 2'b00: 130°C 2'b01: 135°C 2'b10: 140°C 2'b11: 145°C
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(table continues...)

3 General Product Characteristics
Table 9 (continued) Electrical characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Protection trigger lower threshold	T_{TS_LTH}	–	$T_{TS_U_{TH}} - 10$	–	$^\circ\text{C}$	
On-chip thermal shut-down warning upper limit	$TSDW_{UTH}$		125		$^\circ\text{C}$	
On-chip thermal shut-down warning lower threshold	$TSDW_{LTH}$		115		$^\circ\text{C}$	

3.7 Timing characteristics
Table 10 Timing characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UV/EN						
UV/EN input fixed deglitch time	t _{UVEN_DG}	6.5	10	13.5	μs	Input filter before processing the signal.
UV/EN deglitch time on rising edge before start the FET	t _{UVEN_ON}	0	–	256	ms	Defined by bits EN_DG[2:0] : 3'b000: 0 ms 3'b001: 4 ms 3'b010: 8 ms 3'b011: 16 ms 3'b100: 32 ms 3'b101: 64 ms 3'b110: 128 ms 3'b111: 256 ms
OV						
OV input fixed deglitch time	t _{OV_DG}	6.5	10	13.5	μs	Input filter before processing the signal.

(table continues...)

3 General Product Characteristics
Table 10 (continued) Timing characteristics

VDD_VIN - GND = 48 V, V_{ISNS_P} = VDD_VIN, V_{ΔISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0 V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FB						
FB input fixed deglitch time	t _{FB_DG}	6.5	10	13.5	μs	Input filter before processing the signal.
PWRGD						
Power good assertion deglitch time	t _{PG_DGR}	0	–	15	ms	Configurable by means of PWRGD_DG_TMR[3:0] bits.
Power good assertion deglitch time programming step	t _{PG_DGR_STP}	0.9	1.0	1.1	ms	
Power good deassertion deglitch time	t _{PG_DGF}	0	–	15	ms	Configurable by means of PWRGDN_DG_TMR[3:0] bits.
Power good deassertion deglitch time programming step	t _{PG_DGF_STP}	0.9	1.0	1.1	ms	
ADC						
Conversion rate of current and voltage measurements	t _{ADC_IV}	–	102.4	–	μs	
Faults, warnings and timers						
Time for any gate discharge in fault state	t _{FLT_PD_GATE}	9	10	11	ms	In FAULT state, when any gate pull down/discharge method is activated, a timer starts simultaneously. If FET's V _{GS} does not go below 1.04 V before this timer expires, SGD fault will be triggered.
Fault strong pull down activation time for fast gate discharge	t _{FLT_PD_FAST}	13.5	15	16.5	μs	When strong/fast gate pull down is configured, the 1.5 A switch is activated for this time.

(table continues...)

3 General Product Characteristics
Table 10 (continued) Timing characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fault reaction time	$t_{FLT_GATE_OFF}$	–	0.3	1.0	μs	Response time from fault triggered to activation of gate pin turn-off. In the case of timer dependent faults, fault triggered means "after timer has expired".
Hot swap retry cool down period		0	–	64	s	Defined by bits COOLD_TMR[2:0]: 3'b000: 0 s 3'b001: 1 s 3'b010: 2 s 3'b011: 4 s 3'b100: 8 s 3'b101: 16 s 3'b110: 32 s 3'b111: 64 s
Retry OK deglitch timer		0	–	8	s	Defined by bits RETD_TMR[2:0]: 3'b000: 0 s 3'b000: 0.5 s 3'b000: 1 s 3'b000: 2 s 3'b000: 3 s 3'b000: 4 s 3'b000: 6 s 3'b000: 8 s
First step power-down timer		0	–	6375	ns	Set by GATE_PD_TMR[7:0] Configurable in 25 ns steps.
UV timer	t_{UV}	0	–	1000	ms	Set by bits UV_TMR[2:0]: 3'b000: 0 ms 3'b001: 1 ms 3'b010: 5 ms 3'b011: 10 ms 3'b100: 50 ms 3'b101: 100 ms 3'b110: 500 ms 3'b111: 1000 ms

(table continues...)

3 General Product Characteristics
Table 10 (continued) Timing characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OV timer	t_{OV}	0	–	1000	ms	set by OV_TMR[2:0] bits: 3'b000: 0 ms 3'b001: 1 ms 3'b010: 5 ms 3'b011: 10 ms 3'b100: 50 ms 3'b101: 100 ms 3'b110: 500 ms 3'b111: 1000ms
OVin detection time	T_{OVin_DET}	–	–	2.0	μs	
OVin deglitch timer	t_{OV_DGLTCH}	0	–	1000	μs	Set by OVIN_TMR[2:0] bits: 3'b000: 0 μs 3'b001: 10 μs 3'b010: 20 μs 3'b011: 50 μs 3'b100: 100 μs 3'b101: 200 μs 3'b110: 500 μs 3'b111: 1000 μs
OUV timer	t_{OUV}	0	–	1000	ms	Set by OUV_TMR[2:0] bits: 3'b000: 0 ms 3'b001: 1 ms 3'b010: 5 ms 3'b011: 10 ms 3'b100: 50 ms 3'b101: 100 ms 3'b110: 500 ms 3'b111: 1000 ms

(table continues...)

3 General Product Characteristics
Table 10 (continued) Timing characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Watchdog timer	$t_{WATCHDOG}$	0	–	10000	ms	Set by WATCHDOG[2:0] bits: 3'b000: 0 ms 3'b001: 20 ms 3'b010: 50 ms 3'b011: 100 ms 3'b100: 200 ms 3'b101: 500 ms 3'b110: 1000 ms 3'b111: 10000 ms
OC/SOA deglitch timer	t_{SOAD}	0	–	10	ms	Set by SOAD_TMR[1:0] bits: 2'b00: 0 ms 2'b01: 0.1 ms 2'b10: 1 ms 2'b11: 10 ms
OC/SOA regulation timer	t_{SOAR}	0	–	1000	ms	Set by SOAR_TMR[2:0] bits: 3'b000: 0 ms 3'b001: 1 ms 3'b010: 5 ms 3'b011: 10 ms 3'b100: 50 ms 3'b101: 100 ms 3'b110: 500 ms 3'b111: 1000 ms
FAULT pin hold time	T_{FAULT}	20	–	–	μs	Hold time of the FAULT signal when it is set Open-drain output: At $C_L = 50\text{ pF}$; External pull-up resistor of 10 k Ω .
RMS current calculator integration time		1.64	–	838.86	ms	Set by RMS_SAMPLE_TMR[1:0] bits: 2'b00: 1.64 ms (16 samples) 2'b01: 13.11 ms (128 samples) 2'b10: 104.86 ms (1024 samples) 2'b11: 838.86 ms (8192 samples)

(table continues...)

3 General Product Characteristics

Table 10 (continued) Timing characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SOC fault digital deglitch timer		0	–	1000	ms	Set by SOC_TMR[2:0] bits: 3'b000: 0 ms 3'b001: 0.01 ms 3'b010: 0.1 ms 3'b011: 1 ms 3'b100: 10 ms 3'b101: 100 ms 3'b110: 500 ms 3'b111: 1000 ms
SOC fault analog deglitch timer		0	–	1000	ns	Set by SOC_DG_TMR[1:0] bits: 2'b00: 0 ns 2'b01: 200 ns 2'b10: 500 ns 2'b11: 1000 ns

Boost mode

Boost pulse timer		0.1	–	1	ms	Set by BOOSTMODE_TMR[0]: 1'b0 : 0.1 ms 1'b1: 1.0 ms
Boost mode duty cycle		2	–	20	%	Set by BOOSTMODE_DC[1:0] bits: 2'b00: 2 % 2'b01: 5 % 2'b10: 10 % 2'b11: 20 %

PMBus

Clock frequency	f_{SCL}	10	–	1000	KHz	
Detect clock low timeout	$t_{TIMEOUT}$	25	–	35	ms	
Bus free time between STOP and START Condition	t_{BUF}	0.5	–	–	μs	See Figure 13
Hold time after (REPEATED) START Condition	$t_{HD:STA}$	0.26	–	–	μs	After this period, the first clock is generated. See Figure 13

(table continues...)

3 General Product Characteristics
Table 10 (continued) Timing characteristics

$V_{DD_VIN} - GND = 48\text{ V}$, $V_{ISNS_P} = V_{DD_VIN}$, $V_{\Delta ISNS} = (V_{ISNS_P} - V_{ISNS_N}) = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
REPEATED START condition setup time	$t_{SU:STA}$	0.26	–	–	μs	See Figure 13
STOP condition setup time	$t_{SU:STO}$	0.26	–	–	μs	See Figure 13
Data hold time	$t_{HD:DAT}$	0	–	–	ns	See Figure 13
Data setup time	$t_{SU:DAT}$	50	–	–	ns	See Figure 13
Clock low period	t_{LOW}	0.5	–	–	μs	See Figure 13
Clock high period	t_{HIGH}	0.26	–	50	μs	See Figure 13
Clock/data fall time	t_F	–	–	120	ns	The fall time measurement limits are defined as follows: Fall time limits: $(V_{IH,MIN} + 0.15\text{ V})$ to $(V_{IL,MAX} - 0.15\text{ V})$ See Figure 13
Clock/data rise time	t_R	–	–	120	ns	The rise time measurement limits are defined as follows: Rise time limits: $(V_{IL,MAX} - 0.15\text{ V})$ to $(V_{IH,MIN} + 0.15\text{ V})$ See Figure 13

4 Product Features

4 Product Features

4.1 Functional Description

4.1.1 Modes of Operation

Fully Digital Mode (FDM)

This mode is recognized by keeping MODE0 and 1 pins open. In this mode, FET to be used can be selected by means of the FET_SELECT bits in the MODE PMBus command or a FET SOA can be programmed accurately in the SOA PMBus command so that controller effectively protects FET from going out of SOA.

If desired, analog comparators at the OV, FB and UV/EN pins, which have a faster response than digital comparators, can be used for OV and UV protection. This is specified by clearing the MODE bit in the MODE PMBus command, which selects the analog comparators mode (ACM).

Digital comparators can be used by leaving the MODE bit to its default (digital comparators mode, DCM). All other XDP710 features like voltage and current faults and warnings limits and timers can be programmed digitally too, including the IST limit, which is set in the START_ILIM bits in the I_SNS_CFG PMBus command. This reduces the amount of external components, as shown in [Figure 30](#). If the MODE bit is left to its default value of 1, UV/EN pin does not have a UV fault functionality, but it's only used to enable or disable the device.

The PMBus address shall be set at ADDR1 and ADDR0 (see [Table 13](#)) pins by keeping them open or tying to GND directly or via external resistors.

Analog Assisted Digital Mode (AADM)

Use simple analog programming at MODE0 and 1 pins for selecting the pre-programmed configurations for controlled FETs. FET can be selected by tying these pins through a resistor to GND.

There are two different SOA options to select from in pre-programmed FETs: DC line and 10 ms line. If second one is chosen, application has to be designed so that output capacitor is charged within this time and watchdog has to be programmed also to this time for protection. FET SOA DC line is programmed by default. This SOA line will be used for both INIT_SOA_REG and I_REG regulation described in [Operational States](#). Other lines can be selected or programmed manually if desired by means of the OTP memory.

MODE bit in MODE command is ignored in AADM. In this case, OV, OUV and UV faults limits are set via voltage dividers at the OV, FB and UV/EN pins respectively. Voltages are sensed via analog comparators at the corresponding pins. Warnings are disabled by default, unless they are enabled and programmed digitally.

The OC range and IST limit can be set by means of a resistor at the IST pin.

The PMBus address shall be set at ADDR1 and ADDR0 (see [Table 13](#)) pins by keeping them open or tying to GND directly or via external resistors.

Table 11 Modes of operation

Mode of operation	MODEx pins	MODE bit	Device address	FET selection	OV/UV detection	IST
FDM	Open	1	Set by means of ADDR _x pins or PMBUS_CFG command	Selected by means of FET_SELECT bits	Digital Comparators Mode (DCM)	Set by means of START_ILIM bits
		0			Analog Comparators Mode (ACM)	

(table continues...)

4 Product Features

Table 11 (continued) **Modes of operation**

Mode of operation	MODEx pins	MODE bit	Device address	FET selection	OV/UV detection	IST
AADM	Resistor to GND	X	Set by means of ADDR _x pins or PMBUS_CFG command	Selected by means of MODE _x pins	Analog Comparators Mode (ACM)	Set by means of IST pin

Configuration of MODE1/0 Pins

Setting the voltage level (between 0.8 V and 2.4 V) at MODE1 and MODE0 pins shall be done using external resistors (see [Setting the voltage at MODE1/0 pins in AADM](#)).

Table 12 **Configuration of MODE1/0 pins**

MODE1 pin voltage, V	MODE0 pin voltage, V	FET selection
MODE1 < 0.8 (GND)	MODE0 < 0.8 (GND)	BSC027N10NS5ATMA1
MODE1 < 0.8 (GND)	0.8 ≤ MODE0 < 1.6	BSC035N10NS5ATMA1
MODE1 < 0.8 (GND)	1.6 ≤ MODE0 < 2.4	Reserved
MODE1 < 0.8 (GND)	MODE0 ≥ 2.4 (Open)	IPT015N10N5ATMA1
0.8 ≤ MODE1 < 1.6	MODE0 < 0.8 (GND)	IPB017N10N5ATMA1
0.8 ≤ MODE1 < 1.6	0.8 ≤ MODE0 < 1.6	IPB017N10N5LFATMA1
0.8 ≤ MODE1 < 1.6	1.6 ≤ MODE0 < 2.4	IPB020N10N5ATMA1
0.8 ≤ MODE1 < 1.6	MODE0 ≥ 2.4 (Open)	IPB020N10N5LFATMA1
1.6 ≤ MODE1 < 2.4	MODE0 < 0.8 (GND)	IPB027N10N5ATMA1
1.6 ≤ MODE1 < 2.4	0.8 ≤ MODE0 < 1.6	IPB032N10N5ATMA1
1.6 ≤ MODE1 < 2.4	1.6 ≤ MODE0 < 2.4	IPB033N10N5LFATMA1
1.6 ≤ MODE1 < 2.4	MODE0 ≥ 2.4 (Open)	Reserved
MODE1 ≥ 2.4 (Open)	MODE0 < 0.8 (GND)	IPB072N15N3
MODE1 ≥ 2.4 (Open)	0.8 ≤ MODE0 < 1.6	IPB042N10
MODE1 ≥ 2.4 (Open)	1.6 ≤ MODE0 < 2.4	IPT016N10NM5LF
MODE1 ≥ 2.4 (Open)	MODE0 ≥ 2.4 (Open)	FET_SELECT (ROM or OTP)

Configuration of ADDR1/0 Pins

These pins can be tied to GND, left floating or tied low through a resistor for a total of 16 unique PMBus device addresses according to [Table 13](#).

Setting the voltage level (between 0.8 V and 2.4 V) at ADDR1 and ADDR0 pins shall be done using external resistors (see [Setting the voltage at ADDR1/0 pins](#)).

4 Product Features

Table 13 Configuration of ADDR1/0 pins

ADDR1 pin voltage, V	ADDR0 pin voltage, V	Base address field [6:4]	Device address field [3:0]
ADDR1 < 0.8 (GND)	ADDR0 < 0.8 (GND)	As configured in PMBUS_CFG command. Default = 001	0000
ADDR1 < 0.8 (GND)	0.8 ≤ ADDR0 < 1.6		0001
ADDR1 < 0.8 (GND)	1.6 ≤ ADDR0 < 2.4		0010
ADDR1 < 0.8 (GND)	ADDR0 ≥ 2.4 (Open)		0011
0.8 ≤ ADDR1 < 1.6	ADDR0 < 0.8 (GND)		0100
0.8 ≤ ADDR1 < 1.6	0.8 ≤ ADDR0 < 1.6		0101
0.8 ≤ ADDR1 < 1.6	1.6 ≤ ADDR0 < 2.4		0110
0.8 ≤ ADDR1 < 1.6	ADDR0 ≥ 2.4 (Open)		0111
1.6 ≤ ADDR1 < 2.4	ADDR0 < 0.8 (GND)		1000
1.6 ≤ ADDR1 < 2.4	0.8 ≤ ADDR0 < 1.6		1001
1.6 ≤ ADDR1 < 2.4	1.6 ≤ ADDR0 < 2.4		1010
1.6 ≤ ADDR1 < 2.4	ADDR0 ≥ 2.4 (Open)		1011
ADDR1 ≥ 2.4 (Open)	ADDR0 < 0.8 (GND)		1100
ADDR1 ≥ 2.4 (Open)	0.8 ≤ ADDR0 < 1.6		1101
ADDR1 ≥ 2.4 (Open)	1.6 ≤ ADDR0 < 2.4		1110
ADDR1 ≥ 2.4 (Open)	ADDR0 ≥ 2.4 (Open)		Program in OTP (PMBUS_CFG)

4.1.2 Operational states

Table 14 Operational states

	State	Name	Description	Next state No fault	Next state fault
Initialization	0	POR_INIT	Internal circuitry is initialized as soon as VDD_VIN > 5.5 V.	READ_CFG	NA
	1	READ_CFG	POR and initialization complete. OTP and external pins configuration are read at this point.	CHK_FET	NA

(table continues...)

4 Product Features
Table 14 (continued) Operational states

	State	Name	Description	Next state No fault	Next state fault
Power-up procedure	2	CHK_FET	Controller checks FET for drain to source or gate to drain shorts.	STANDBY	FAULT
	3	STANDBY	Controller checks that VDD_VIN is within a valid range (within UV and OV), device temperature is in appropriate range and EN signal is deasserted or ON bit in OPERATION command is cleared. Before going out of STANDBY and into INIT_SOA_REG state, XDP710 checks the input voltage level according to OV, UV and OVin limits. If it's out of range, it will go to FAULT state.	INIT_SOA_REG	FAULT
	4	INIT_SOA_REG	EN signal is asserted and ON bit in OPERATION command is set. Turn-on Watchdog timer starts running. SOA regulation phase: Controller regulates the current according to the programmed SOA (see section Current Limit During Operation for more info), depending on VDS value in order to charge the output capacitor. INIT_SOA_REG phase stops when FET $V_{DS} < 1.0$ V, $V_{GS} > 7.8$ V and no faults are detected during this procedure. Due to the current regulation nature of the Power-up algorithm, start-up time depends on the output capacitance.	ON	FAULT

(table continues...)

4 Product Features
Table 14 (continued) Operational states

	State	Name	Description	Next state No fault	Next state fault
Normal operation	5	ON	Normal operation phase starts. FET is fully enhanced. Current regulation can start again if OC is detected or FET SOA is violated. Turn-on watchdog reset procedure starts at this point.	ON or I_REG	FAULT
	6	I_REG	If I_{OC} level is exceeded or programmed FET SOA limits are violated, SOAD_TMR timer will start. If condition persists after SOAD_TMR timer expires, the SOA regulation timer SOAR_TMR starts and FET's current will be regulated at I_{OC} or FET SOA level by lowering FET VGS.	ON	FAULT
Idle	7	FAULT	Fault that turns off the FET has occurred. System will stay idle in FAULT state until: a) Fault conditions are cleared in the case of non-retry dependent faults. b) Cool down timer expires in the case of retry dependent faults. If retry counter has expired, system will go to LATCH_OFF state directly after FAULT.	CHK_FET/ STANDBY or LATCH_OFF	NA
	8	LATCH_OFF	If the maximum number of retries has been reached, system will latch off until faults are cleared and restart has been issued (power cycling or PMBus command).	POR_INIT (power cycling) or CHK_FET (PMBus command) or LATCH_OFF	NA
	9	MEM_FAULT	If an OTP read or write error is detected, XDP710 will go to FAULT and consecutively MEM_FAULT state, which initiates controller's latch-off. A power cycle is required in order to go out of MEM_FAULT.	POR_INIT (power cycling)	NA

4 Product Features

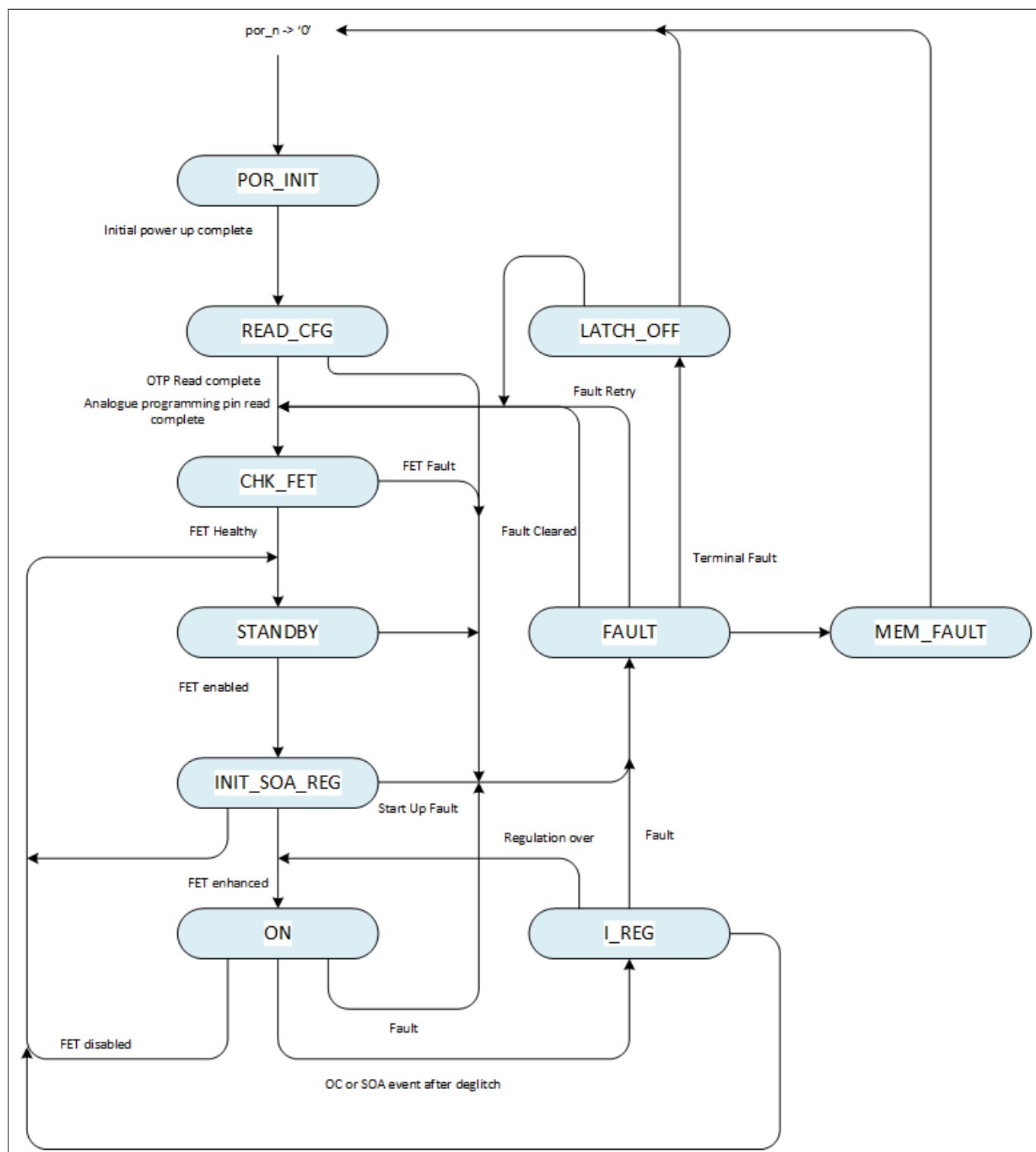


Figure 6 XDP710 State machine

4.1.3 Enable and disable

The PMBus interface communication and controller's programmability is functional at minimum operative VDD_VIN.

XDP710's gate pin can be enabled or disabled by means of the UV/EN pin or PMBus command. By default, it starts up as soon as the necessary conditions are detected: proper voltage level between UV and OV pins. In order to disable this "enabled by default" feature, the corresponding bit has to be programmed accordingly in OPERATION PMBus command.

4 Product Features

In DCM, the UV/EN pin has a deglitch timer EN_DG[2:0]. This timer starts running as soon as the voltage at this pin rises above V_{UVEN_UTH} (see Table 9). The system turns on as soon as it expires if voltage is still above this level.

When UV/EN pin is tied low, FET turns off, but communication circuitry is still available. When device is disabled but in STANDBY state, VREG and communication via PMBus will still be enabled so that the device can be programmed and FAULT status bits will keep their latest status.

Also in DCM, it is possible to implement a manual input voltage deglitch by delaying the toggling of the UV/EN signal. Faults detection starts when UV/EN signal is toggled. In this case, EN_DG can be set to 0.

The UV input (under-voltage monitoring input to support the UV fault) and EN input are combined in one pin. The UV/EN pin configuration is dependent on mode of operation:

Table 15 UV/EN Input Configuration

Mode of operation	UV/EN pin configuration
FDM - DCM (digital comparators for OV and UV faults)	EN input
FDM - ACM (analog comparators for OV and UV faults)	UV input
AADM	UV input

If the pin is configured as UV input its voltage is sensed by an analog comparator to support UV fault detection and release. Turn-on and off of the device can still be controlled by toggling the pin high or low respectively. When pin is toggled low, XDP710 follows the configured UV fault procedure before turning off.

If pin is configured as EN, turn-on and off of the device can be controlled without following UV fault procedure. The EN input controls the state of the controlled FET together with PMBus OPERATION command:

- EN = Low (voltage level is $\leq V_{UVEN_LTH}$) --> FET is OFF;
- EN = High (voltage level is $\geq V_{UVEN_UTH}$) --> the FET's state depends on the PMBus OPERATION command.

The EN High-to-Low transition clears any fault (including ones that cause Latch-off) as it is described in [Latch-off](#). Only the memory OTP (MEM) fault is not affected.

4.1.4 Control of FET's current

XDP710 controls the FET's current according to four different limits:

- **Programmed FET SOA limit:** To protect the FET, current flow through the FET is regulated according to its V_{DS} , following the FET's SOA line, which is stored in ROM or OTP. Pre-programmed SOA lines correspond to 65°C or 125°C temperature, this is in order to account for systems that will be working at temperatures higher than the usual ambient of 25°C. They are selectable between DC and 10 ms in FDM. DC only in AADM. Care must be taken to program the corresponding SOA fault timers according to the voltage and current levels so that maximum FET capabilities are not exceeded. If FET temperature monitoring feature (TSNS_x pins) is used, the SOA line to be used is adjusted automatically according to the sensed temperature. Below 95°C, the 65°C line is used, and above 95°C, the 125°C line is used. SOA can also be manually programmed to give the user the flexibility to work with different SOA curves or limit the power allowed;
- **Overcurrent (OC) limit:** To protect the load and source, this limit is normally set according to the maximum allowed current flow through the circuit by means of I_{OC} . This limit is active during INIT_SOA_REG, ON and I_REG states. See [Setting \$I_{OC}\$](#) for info about how to set it.
- **FET Start-up current (IST) limit:** To reduce voltage overshoots due to the output capacitance by increasing start-up time, this limit can be set in case SOA and OC limits are too high. This limit is taken into account during INIT_SOA_REG state only and disregarded as soon as ON state is reached.
- **SOC limit:** The severe overcurrent limit provides a fast response in case current reaches critical levels.

4.1.4.1 MOSFET's Power-up - Continuous Safe Operating Area (SOA) Control

During a system initialization, XDP710 provides bias current to turn on the MOSFET in a controlled manner to avoid any SOA violations, while ensuring that the system is turned on without any inrush event.

4 Product Features

During power-up, the lowest of the three limits:

- FET SOA
- OC: Programmed overcurrent limit
- IST: Programmed system startup current limit

defines the system maximum allowed current.

In the following example, the green dotted line indicates the maximum current allowed through the MOSFET (IPB020N10N5LF) during a startup. The programmed safe operating area (SOA) of the MOSFET is indicated by the solid blue line. In this example, the maximum current allowed by the controller is limited by IST since it is the lowest current limit allowed by this specific application.

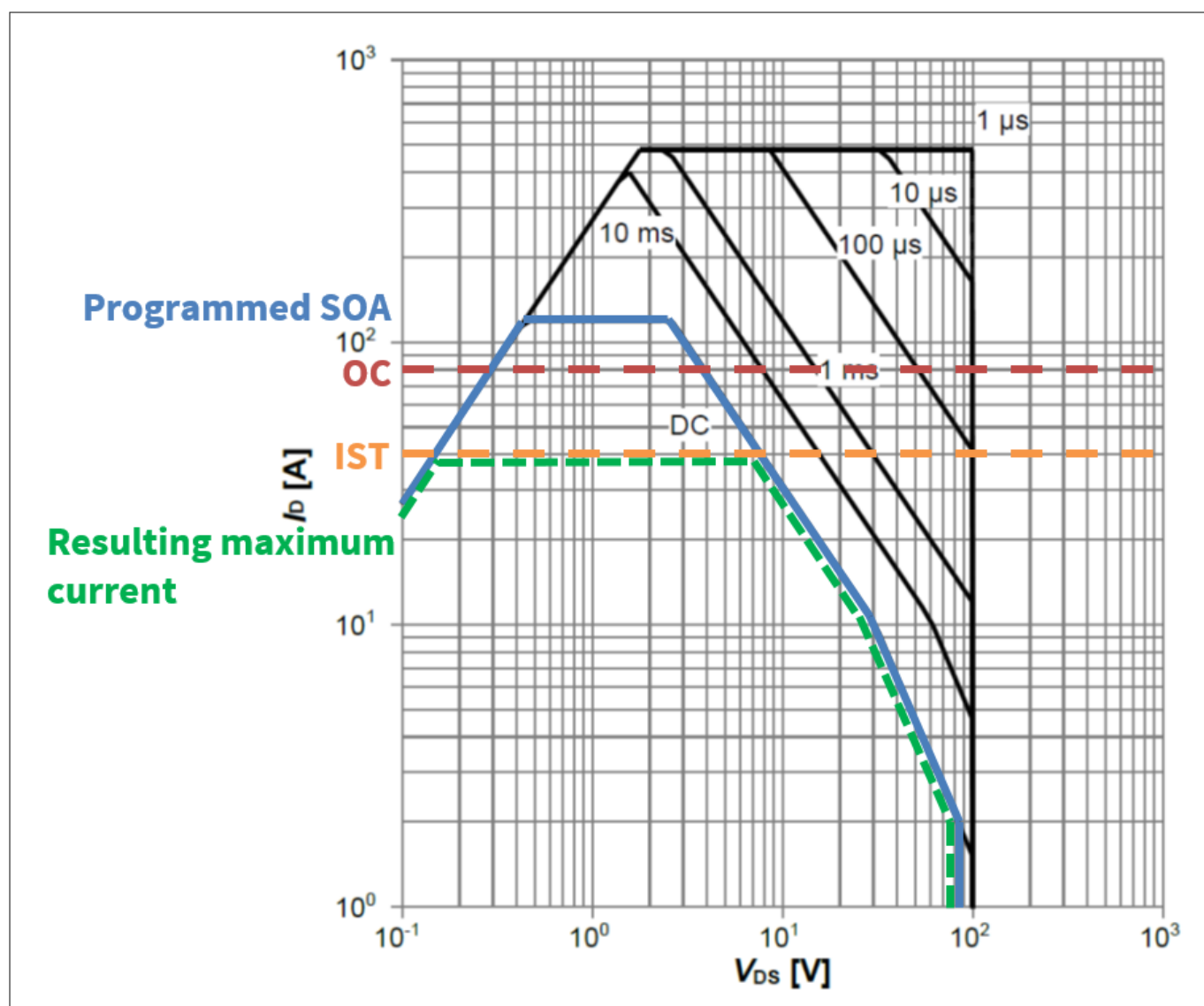


Figure 7 Safe operating area

SOA is digitally programmed in the SOA command as a look-up table with 80 values, corresponding to $V_{DS} = 1$ V to 80 V. Each value represents the current I_D allowed for each voltage point. The following table contains the DC curve data shown in the previous figure for FET IPB020N10N5LF at 65°C. XDP710 target SOA has a resolution of 0.5 A. The **Target SOA I_{SOA} (A)** column shows the rounded values:

4 Product Features
Table 16 SOA Table for IPB020N10N5LF

V_{DS} (V)	I_D (A)	Target SOA I_{SOA} (A)
1	120	120
2	120	120
3	104.2	104
4	78.1	78
5	62.5	62.5
6	52.1	52
7	44.6	44.5
8	39.1	39
...	...	...
73	2.5	2.5
74	2.5	2.5
75	2.4	2
76	2.4	2
77	2.3	2
78	2.2	2
79	2.2	2
80	2.1	2

As an example, a typical 48 V input application with the DC line of figure above is taken.

- Before the FET is turned on, there are 48 V at the input (with respect to GND) and 0 V at the output, since the output capacitor is discharged. So $V_{DS} = 48$ V.
- XDP710 starts charging the output capacitor by regulating the current through the FET according to the maximum allowed in the SOA. From [Figure 7](#), the DC line allows an $I_{SOA} \cong 4.5$ A at 48 V.
- While the capacitor charges, V_{DS} of the FET will be reduced, allowing current increase according to SOA. For example, $V_{DS} = 40$ V allows a current of $I_{SOA} \cong 6.5$ A, so, when V_{DS} reaches 40 V, XDP710 increases the current through the FET to 6.5 A.
- Current keeps increasing while voltage keeps decreasing until output voltage is charged to the desired level and FET gets fully enhanced. This current limitation delays the charging of the output capacitor, significantly reducing the inrush current at start-up while keeping the FET safe at all times.

4.1.4.1.1 Control loop

XDP710's control loop consists on a closed loop system that senses the FET current by means of the voltage drop on the sense resistor and input and output voltages. It calculates the FET's V_{DS} by subtracting $V_{OUT} - V_{IN}$ and regulates the current according to the maximum allowed in the SOA table, depending on the sensed V_{DS} . This regulation is done by adjusting the FET's V_{GS} .

4 Product Features

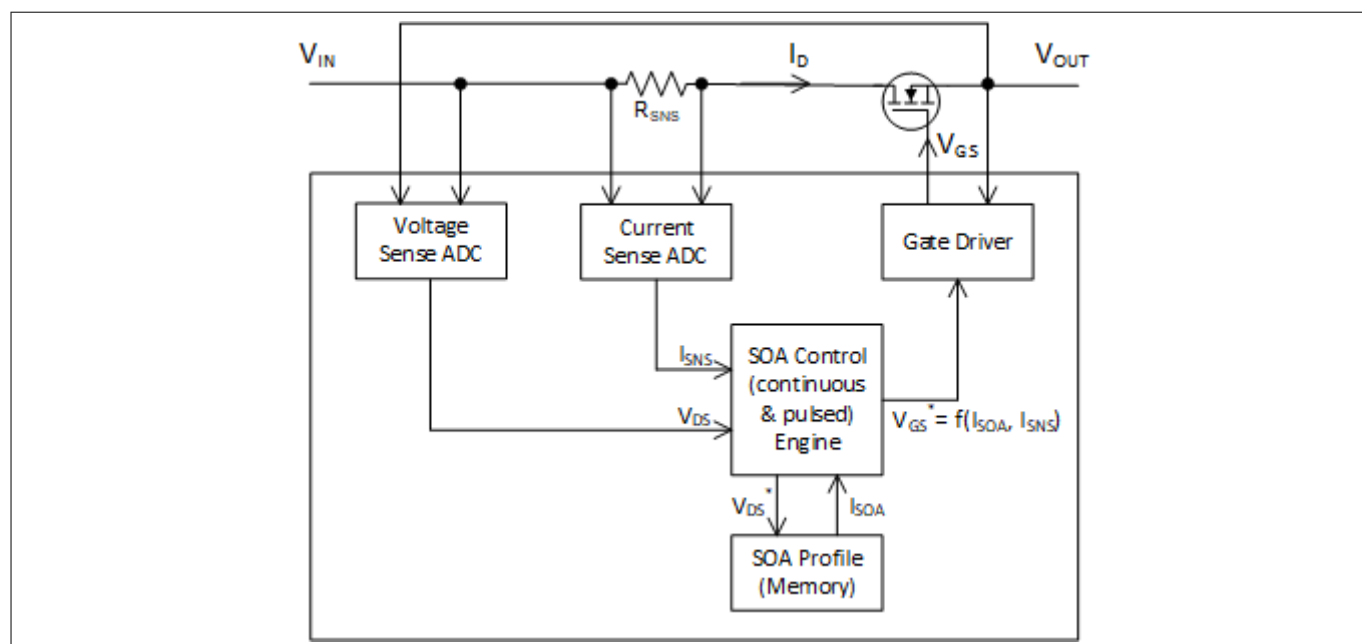


Figure 8 XDP710's Control loop block diagram

4.1.4.1.2 Setting OC and IST levels

In XDP710 FDM the current sense (CS) range and overcurrent (OC) level are set digitally by means of CS_RNG bits in I_SNS_CFG PMBus command.

Table 17 CS_RNG values

CS_RNG[1:0]	OC Level (mV)
00	12.5
01	25
10	50
11	100

If required, the Non-RMS and RMS OC levels can be trimmed by CS_RNG_TRIM.

The start-up current limit (IST) through the FET is set digitally using dedicated START_ILIM bits in I_SNS_CFG command:

Table 18 START_ILIM current limit

START_ILIM[2:0]	Start-up current limit (IST)
000	100% of OC level (disabled, default)
001	87.5% of OC level
010	75% of OC level
011	62.5% of OC level
100	50% of OC level

(table continues...)

4 Product Features
Table 18 (continued) START_ILIM current limit

START_ILIM[2:0]	Start-up current limit (IST)
101	37.5% of OC level
110	25% of OC level
111	12.5% of OC level

In AADM, the default OC range and the start-up current limit (IST) through the FET can be set by means of a voltage on IST pin. If settings different than the ones in [Table 19](#) are desired, they can be configured manually in the corresponding PMBus commands.

Table 19 IST pin configuration

IST pin voltage, V	OC level, mV	Start-up current limit (IST)
IST > 2.8 (Open)	25	Set by START_ILIM bits in I_SNS_CFG command
2.2 < IST ≤ 2.8		50% of OC level (25mV)
1.7 < IST ≤ 2.2		25% of OC level (25mV)
1.3 < IST ≤ 1.7		12.5% of OC level (25mV)
0.9 < IST ≤ 1.3	12.5	12.5% of OC level (12.5mV)
0.6 < IST ≤ 0.9		25% of OC level (12.5mV)
0.3 < IST ≤ 0.6		50% of OC level (12.5mV)
IST ≤ 0.3 (GND)		Set by START_ILIM bits in I_SNS_CFG command

Setting the voltage level (between 0.3 V and 2.8 V) at IST pin shall be done using external resistor connected to GND.

To set the desired voltage level at the pin, choose the resistor by simply dividing desired voltage over sourced pin current ($100 \mu\text{A} \pm 7\%$).

The 1% (or lower) tolerant resistors are recommended in this case. For example:

Table 20 IST pin resistor

Voltage, V	IST pin resistor, kΩ
2.49	24.9
1.96	19.6
1.5	15
1.1	11
0.75	7.5
0.453	4.53

4 Product Features

4.1.4.2 Control of Current during FET's Normal Operation

In normal operation (during ON and I_REG states) the FET's current is limited by OC and FET's SOA limits. If RMS OC fault is enabled, the FET's current limitation set by OC limit is disregarded, the OC_{RMS} event comes from the digital RMS overcurrent detector.

4.1.5 Boost mode power-up

For high V_{DS} values, the I_{SOA} target is often in low current range, that is, below 1 A. For some FETs it could be even lower than the target SOA resolution (0.5 A). Running FET's power-up with continuous SOA control under those conditions may result in FET overstress and failing, especially in the systems with large output capacitors.

There is a programmable option in the XDP710 which pulses ("boosts") the I_D to make use of FET's higher current capability with shorter pulses and sets a cool down time between boost pulses to keep the FET safe. MOSFET gate is enhanced in bursts to mimic switching type of operation and allow the output capacitor to be charged. This ensures the safety of the FET by cooling down in between bursts instead of constant flow. If this function is enabled by means of the BOOSTMODE_EN bit in the REF_CFG command, XDP710 executes the following procedure at power-up:

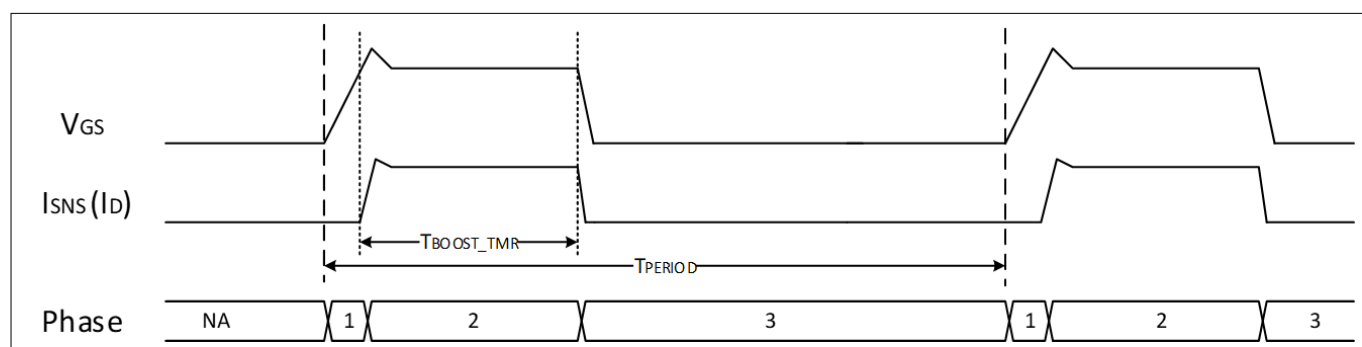


Figure 9 Boost mode power-up

- 1st phase:** The V_{GS} starts ramping when INIT_SOA_REG state is entered. The T_{PERIOD} timer, defined by BOOSTMODE_TMR and BOOSTMODE_DC, activates at start of V_{GS} ramp.
- 2nd phase:** The pulse timer T_{BOOST_TMR} (value set in BOOSTMODE_TMR) starts after the V_{GS} ramp has ended. The FET's current target is set to boost target I_{BOOST} :
 - If I_{SOA} (programmed SOA current at actual V_{DS}) programmed value > 0 : $I_{BOOST} = 4 \times I_{SOA}$ typ.
 - If I_{SOA} programmed value = 0: $I_{BOOST} = 0.5$ A typ.
- 3rd phase:** After T_{BOOST_TMR} has expired, the FET current is set to 0 by turning off the FET.
- After T_{PERIOD} has expired, next V_{GS} ramp starts and system continues from 1st phase until target $I_{SOA} \geq 1.5$ A.
- After target I_{SOA} reaches this point of 1.5 A, FET's power-up will be finalized via continuous SOA.

The duty cycle (BOOSTMODE_DC) of the period can be configured to 2, 5, 10 or 20%. To calculate T_{PERIOD} :

$$T_{PERIOD} = \frac{BOOSTMODE_TMR}{BOOSTMODE_DC}$$

Equation 1

For example, if BOOSTMODE_TMR = 1ms and BOOSTMODE_DC = 10%:

$$T_{PERIOD} = \frac{1ms}{10\%} = 10ms$$

Equation 2

4 Product Features

Boost Mode Considerations

- BOOSTMODE_TMR and BOOSTMODE_DC must be configured according to FET max SOA capabilities.

4.1.6 Power good

The power good signal is asserted to indicate when the following conditions are met:

- The input voltage is within the UV and OV/OVin limits, the output voltage is above OUV limit (no any under- or overvoltage fault is present)
- FET's and controller's over-temperature protection limits are not violated (no OT or TSD fault is present)
- FET is fully enhanced after its power-up and no OC or SOA regulation fault is present
- No any other fault is present

All above means that controller is in ON or I_REG state.

The power good assertion shall be performed after a programmable power good assertion deglitch time (see [Table 10](#)).

the power good de-assertion shall involve a programmable power good de-assertion deglitch time, which helps to avoid unnecessary signal's re-toggling due to short voltage or current jumps.

PWRGD signal polarity is configurable (active low or active high) by means of the PWRGD_POLARITY bit in order to support sequential turn-on capability.

4.1.7 Support of Sequential Turn-On

PWRGD, FAULT and UV/EN pins are used for communication between different devices if sequential turn-on implementation is desired based on "Master/Slave" approach.

Voltage levels of UV/EN, PWRGD and FAULT pins are compatible so that PWRGD or FAULT pins of a "Master" device can drive the UV/EN pin of a "Secondary" device and control its turn-on or off.

4.1.8 Support of OR-ing Capability

When PWRGD output pin is configured as active Low, two controllers can be connected to the same output voltage, so that, when output of the "Master" goes down, the "Secondary" can supply the necessary voltage. It is a backup supply scenario. A deglitch period can be configured between "Master" undervoltage and "Secondary" (backup) enable by means of an UV/EN pin response delay or deglitch period. System has to be designed so that a capacitor can supply the necessary power during this supply outage. The power-up latency of the "Secondary" controller has to be taken into account too.

4.1.9 FET power down

Turn-off of the FET can be triggered manually or automatically due to a fault. In general, FET is turned-off by pulling I_{GATE_SPD} from its gate, except for the cases of OVIn and SOC faults. In these cases, a configurable two step turn-off has been implemented in order to avoid FET drain-source voltage overshoots.

4 Product Features

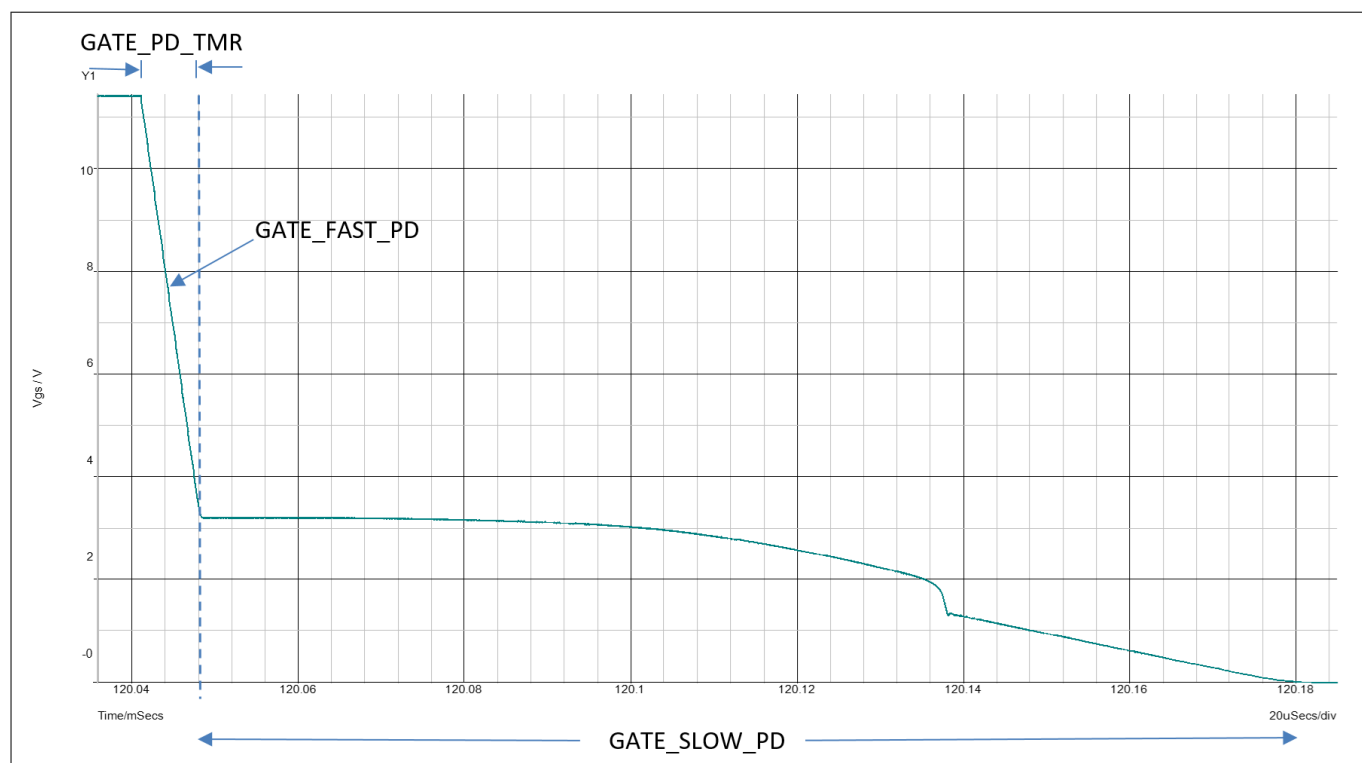


Figure 10 FET power down

The first step is configurable to 1.5 A current source or 200 Ω resistor through the bit GATE_FAST_PD[0]. If 1.5 A is selected, this current will be pulled out of the gate of the FET until it is completely turned off, ignoring the second step. If the 200 Ω resistor is selected, it discharges the gate of the FET for a time defined by the GATE_PD_TMR timer. This timer will start running when the turn-off process starts as soon as fault is detected. The timer must be calculated depending on the FET gate charge so that the plateau voltage is passed in this first stage. This “fast” stage avoids the increase of the current by reaching the FET’s linear region as fast as possible.

Then, the second stage limits the voltage overshoot by slowing down the di/dt of the system. This stage starts when GATE_PD_TMR expires. When it does, level of current being pulled out of the gate changes according to what is programmed in GATE_SLOW_PD[1:0] bits. A lower level of current will keep the FET in linear region for a longer time, which will, as a result, slow down the di/dt until the threshold voltage of the FET is passed and the FET is completely off.

If GATE_PD_TMR is 0 and GATE_FAST_PD[0] = 1, gate discharges slowly with GATE_SLOW_PD only, without a fast pull-down phase. The minimum allowed time to be programmed in GATE_PD_TMR (if it's not 0) is 250ns.

Note: Due to the benefits of the two-step turn-off, it is recommended to always use it after OVin and SOC faults.

4.2 Faults

XDP710 incorporates many protections that ensure safe operation for the FET, source and load in different scenarios.

Faults are events that could stop system operation or even potentially damage some part of the circuit, so protective actions are taken in response to this kind of events.

For this purpose, different FET gate pull-down mechanisms are incorporated as described in [FET power down](#):

4 Product Features

- Regular/slow pull-down: In case of a fault event that is not dangerous for the system, FET is turned off by pulling a typical current of 250 μ A / 500 μ A / 750 μ A / 1.25 mA (programmable by means of GATE_SLOW_PD bits in TURN_OFF_CTRL PMBus command) from its gate.
- Strong/fast pull-down: In case of an emergency fault,
 - 1) a typical current of 1.5 A are pulled from the FET's gate for extremely fast turn-off or
 - 2) a two step FET's turn-off is applied to keep FET's V_{DS} below avalanche breakdown. Method 1) or 2) has to be selected by means of GATE_FAST_PD bits in TURN_OFF_CTRL command depending on the system setup and requirements.

There are two ways in which XDP710 reports when a fault has occurred:

- Read Fault Status commands via PMBus interface: Each one of the faults has a corresponding bit in the STATUS_FAULTS command which is set after a fault has occurred.
- Via GPO0/FAULT NMOS open drain pin (output polarity is programmable): The status bits can be reflected on the FAULT pin to alert the processor/MCU that any of these events has happened. Mask command is provided for the user to select which faults are to be reflected on the FAULT pin.

As a result of the fault, PWRGD pin is also deasserted.

Faults can be disabled by clearing their enable bits, which means they are not detected nor reported.

The fault status bits will remain set until they are cleared:

- by means of the CLEAR_FAULTS PMBus command
- or by a controller restart (toggling EN pin) or a power cycle

The FAULT pin alerts the processor/MCU that any of fault has happened, it reflects the state of the internal fault signals (detected fault conditions), not the fault status bits. This pin's state is an OR of all unmasked faults, leading to the possibility that if a masked higher priority fault is processed with the pin correctly in inactive state, a lower priority unmasked fault might cause the pin to be driven active.

To service the faults properly, CLEAR_FAULTS command and EN pin toggling are ignored in fault state and until fault process has finished and XDP710 has gone to LATCH_OFF state, or, in case of automatic restart, STANDBY or ON. Once the controller has left FAULT state, faults can be cleared (if fault conditions are not present anymore) and device can be restarted. LATCH_OFF state can be monitored by reading the STATUS_LATCH_OFF bit in STATUS_MFR_SPECIFIC command.

Note: For a correct functionality of the faults and in order to avoid enabling/disabling them while any fault conditions are actually present, all faults must only be enabled or disabled while controller is in STANDBY state.

Faults are divided in priority groups. In case a second fault with higher priority comes while servicing another fault, the first one is put on hold until the higher priority is served. When finished serving the high priority fault, system resumes servicing the fault that was put on hold. If the fault being serviced has same or higher priority than the second fault, system will act in a first-come, first-served fashion.

Priority groups are:

Group 1: MEM, SDS, SGD, SGS, UR.

Group 2: SOC.

Group 3: OT, TSD.

Group 4: UV, OV, OVin.

Group 5: OUV.

Group 6: WD, OC, SOAR.

The table below shows when particular faults detection and processing is active:

Table 21 **Faults during operation states**

Activation (X) of FAULT's detection during operation states
(table continues...)

4 Product Features
Table 21 (continued) Faults during operation states

FAULT NAME (prio)	State of controller								
	POR_INIT	READ_CFG	CHK_FET	STANDBY	INIT_SOAR_REG	ON	I_REG	FAULT	MEM_FAULT/ LATCH_OFF
MEM (1)	--	X	--	X	--	--	--	--	--
SDS (1)	--	--	X	X	--	--	--	X	--
SGD (1)	--	--	X	X	--	--	--	X	--
SGS (1)	--	--	--	--	X*1	--	--	--	--
UR (1)	--	--	--	--	--	--	--	X*2	--
SOC (2)	--	--	--	--	X	X	X	--	--
OT (3)	--	--	--	X	X	X	X	X	--
TSD (3)	--	--	--	X	X	X	X	X	--
UV (4)	--	--	--	X	X	X	X	X	--
OV (4)	--	--	--	X	X	X	X	X	--
OVin (4)	--	--	--	X	X	X	X	X	--
OUV (5)	--	--	--	--	--	X	X	--	--
WD (6)	--	--	--	--	X	--	--	--	--
OC (6)	--	--	--	--	--	X	X	--	--
SOAR (6)	--	--	--	--	--	X	X	--	--

Notes:

*1): Right at the point when watchdog timer expires.

*2): The UR fault can occur only in FAULT state when retry counter expires after any of the retry fault events (SOC, OUV, WD, OC, SOAR).

4.2.1 Memory fault

Memory OTP (MEM) Fault

If an OTP read or write error is detected during READ_CFG state, XDP710 switches to FAULT and consecutively to the MEM_FAULT state, which initiates controller's latch-off. FET is switched off and PWRGD signal are not be asserted. This fault can be cleared by means of a power cycle only, in which case the system restarts from the POR_INIT state.

4.2.2 Damaged FET faults

There is a FET healthy check phase after READ_CFG state and until STANDBY phase has finished.

The drain-source and gate-drain low voltage checks start as soon as the READ_CFG phase is over at first plug-in or just before starting any retry attempt.

As a consequence of any of these faults, XDP710 switches to FAULT state and then pass directly to the LATCH_OFF state.

4 Product Features

Shorted FET Drain-Source (SDS) Fault

If current above SDS limit (see table below) through the sense resistor is detected in CHK_FET, STANDBY or FAULT states, and V_{GS} of the FET is lower than 1 V while gate pin is weakly driven low, an SDS fault is issued. The following table shows the corresponding typical current limit in Amp at $R_{SNS} = 1\text{ m}\Omega$.

Table 22 SDS limit

V_{SNS_CS} (mV)	12.5	25	50	100
SDS limit (A)	0.24	0.52	1.1	2.2

Shorted FET Gate-Drain (SGD) Fault

SGD fault is triggered in the CHK_FET, FAULT or STANDBY states:

- In CHK_FET state: If the FET's V_{GS} goes above 1 V.
- When controller enters the FAULT or STANDBY state and activates any gate pull down. If the FET's V_{GS} does not go below 1 V within 10 ms.
- In FAULT and STANDBY state: If, after FET's V_{GS} goes below 1 V within 10 ms when FET's gate is weakly driven low (regular/slow gate pull down), the FET's V_{GS} goes back above 1 V.

Shorted FET Gate-Source (SGS) Fault

If no power good is achieved in power-up procedure when the watchdog timer expires and $V_{GS} < 1\text{ V}$ at this point, SGS fault will be issued.

Note: WATCHDOG timer is used for this fault even if watchdog fault is disabled. If a specific timer value is desired to cover SGS in this case, the timer must be configured accordingly.

4.2.3 Input voltage faults

System Input Undervoltage (UV) Fault

In FDM mode, if MODE bit = 1 (DCM), the UV fault limit is set digitally by VIN_UV_FAULT_LIMIT.

In AADM mode or FDM mode, if MODE bit = 0 (ACM), the limit V_{UVEN_LTH} is set by means of external components (see [Setting OV, UV and OUV in ACM](#)).

If the input voltage reaches or falls below the corresponding limit, UV_TMR[2:0] starts running. If voltage raises above VIN_UV_FAULT_LIMIT or V_{UVEN_UTH} before the timer expires, system stays in ON state. Otherwise, if voltage is still low when timer expires, fault will be triggered and FET is turned off with a regular pull-down.

XDP710 waits until FET is completely turned-off, then keeps monitoring the input voltage and stay idle in FAULT state until it raises above VIN_UV_FAULT_LIMIT plus a hysteresis of 0x60 (DCM mode) or V_{UVEN_UTH} (ACM mode). In this case, the power-up sequence is initiated.

Hysteresis of 0x60 corresponds to the following voltages, depending on the V_{TLM_RNG} setting:

Table 23 Voltage hysteresis

V_{TLM_RNG} (V)	88	44	22
Voltage (V)	2.06	1.03	0.52

4 Product Features

System Input Overvoltage (OV) Fault

In FDM mode, if MODE bit = 1 (DCM), OV fault limit is set digitally by VIN_OV_FAULT_LIMIT.

In AADM mode or FDM mode, if MODE bit = 0 (ACM), the limit V_{OV_UTH} is set by means of external components (see [Setting OV, UV and OUV in ACM](#)).

If the input voltage reaches or raises above the corresponding limit, OV_TMR[2:0] starts running. If the voltage falls below VIN_OV_FAULT_LIMIT or V_{OV_LTH} before the timer expires, the system stays in ON state. Otherwise, if the voltage is still high when timer expires, a fault is triggered and FET is turned off with a regular pull-down.

XDP710 waits until FET is completely turned-off, then keep monitoring the input voltage and stay idle in the FAULT state until it falls below VIN_OV_FAULT_LIMIT minus a hysteresis of 0x60 (DCM mode, see [Table 23](#)) or V_{OV_LTH} (ACM mode). In this case, the power-up sequence is initiated.

On-chip Input Overvoltage (OVin) Fault

If, during STANDBY, INIT_SOA_REG, normal operation or FAULT state, the input voltage goes above the limit set by OVIN_FAULT_LIMIT bits in V_SNS_CFG PMBus command, OVIN_TMR starts running. When it expires, a fault is triggered and FET is immediately turned-off with a fast or two-step pull-down (depending on configuration). XDP710 waits until FET is completely turned-off, then stays idle in FAULT state until input voltage goes below the lower OVin threshold of OVIN_FAULT_LIMIT minus a hysteresis of 5 V. Then power-up sequence is initiated.

4.2.4 Output voltage faults

Output Undervoltage (OUV) Fault

If, during normal operation, the output voltage falls below the OUV threshold set by a voltage divider at the FB pin (ACM mode) or the limit set by VOUT_UV_FAULT_LIMIT (DCM mode), OUV_TMR[2:0] timer starts running. If voltage goes back up before timer expires, the system continues normal operation. If OUV condition persists when timer expires, a fault is issued and FET is turned-off with a regular pull-down.

The system will retry to power-up after a cool-down period according to the RETRY command settings.

It is recommended to set OUV to a level lower than UV. This is because OUV sends the device to LATCH_OFF state, while UV sends it to FAULT. If both of them are set to the same level or if OUV is set to a level above UV, the device will be sent to LATCH_OFF state, instead of FAULT due to UV.

4.2.5 Current and temperature faults

Overcurrent (OC) Fault

An OC condition is detected if, during normal operation, FET current reaches its programmed level of I_{OC} . If this condition occurs, the SOAD_TMR[1:0] timer starts. If the FET current goes below I_{OC} before timer expires, the system continues normal operation. If the OC condition persists when the timer expires, XDP710 starts the OC/SOA regulation timer (SOAR_TMR[2:0]) and current regulation at I_{OC} level (I_REG state) by lowering FET's V_{GS} voltage. If I_REG state ends (FET is fully enhanced again) before this second timer expires, the system goes back to normal. Otherwise an OC fault is triggered and FET is turned off with a regular pull-down.

The system will retry power-up after cool down period according to RETRY command settings.

The SOA regulation timer configurable steps are compliant with common SOA lines so that the protection can be implemented according to the maximum allowed timer for a specific V_{DS} vs I_{DS} scenario.

Note: For safety reasons during I_REG state, if current through the FET goes below 1 A, the regulation will stop, FET is turned off and a SOAR fault is declared.

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Severe Overcurrent (SOC) Fault

An SOC event is detected when, during INIT_SOA_REG or normal operation, FET's I_{DS} current reaches the level which creates a voltage drop over the sense resistor exceeding programmable level of V_{SNS_SOC} . The detection is done by means of an analog comparator for a faster reaction. This comparator has a programmable SOC_DG_TMR deglitch time for detection.

If V_{SNS_SOC} level of current is detected, SOC_TMR will start running. If the SOC conditions are cleared before timer expires and no other fault conditions are present, the system goes back to normal. Otherwise a fault is triggered and FET is opened with a fast or two-step pull-down (depending on configuration) as soon as this timer expires.

The system will retry a power-up after a cool down period according to RETRY command setting. The FAULT pin is automatically deasserted when fault conditions are cleared and PWRGD asserted after a successful retry.

SOC fault configuration is done by means of the SOC_FAULT_LIMIT bits, and it depends on CS_RNG configuration, according to the following table:

Table 24 Configuration of SOC levels (in mV)

		I_SNS_CFG.CS_RNG[1:0]			
		00	01	10	11
I_SNS_CFG.SOC_FAULT_LIMIT[2:0]	000	12.5		25	
	001	18.75		37.5	
	010	25		50	
	011	37.5		75	
	100	50		100	
	101	75		150	
	110	100		200	
	111	150		300	

RMS Current (RMS)

OC protection can be configured to react at RMS current calculation limit instead of instantaneous measurements.

RMS_EN bit in REG_CFG command enables or disabled the RMS calculation function of the OC protection. If enabled, the protection level is based on RMS calculation. Since RMS is a sub-function of OC, OC must be enabled (by means of the OC bit in ENABLE_FAULTS command) if the RMS function is desired.

RMS does not have mask and status bits, but OC corresponding mask and status bits are used instead.

RMS_SAMPLE_TMR specifies the integration time for the RMS current protection calculation.

If the RMS_EN bit is set (RMS function is enabled), the CS_RNG_TRIM bits specifies the RMS current level (as a proportion of V_{SNS_CS}) at which the OC fault is triggered. If this RMS current level is exceeded, FET is turned off immediately with a regular pull-down, skipping the regulation phase configured in the SOAR_TMR[2:0] bits.

SOA Regulation (SOAR) Fault

After ON state is reached and FET is fully enhanced, there could be different possible scenarios in which FET SOA limits are violated. For example:

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- Input voltage suddenly increases generating a certain V_{DS} meanwhile the output cap is charged up to the new voltage level
- $R_{DS(on)}$ is too high
- During I_{REG} state after an OC event, V_{DS} has to increase too much in order to keep the current at an appropriate level

In this scenario, the SOAD_TMR[1:0] deglitch timer starts. If FET V_{DS} and I_{DS} go back within the SOA limits before the timer expires, the system continues normal operation in ON state. Otherwise the SOAR_TMR[2:0] regulation timer starts while the system continues to regulate the current to stay within the SOA limits. If SOAR condition is cleared before this second timer expires, system goes back to ON state. If it persists, a SOA regulation fault is triggered and FET is opened with a regular pull-down.

If the regulated current through the FET goes below a level of 1 A, regulation stops, FET is turned off and a SOAR fault is declared.

The system will retry power-up after a cool down period according to RETRY command settings.

Note: The SOAR fault disabling means that a fault is never triggered and FET is never turned off in case of a SOA limits violation. It is recommended to keep the SOAR fault enabled for safety reasons.

Overtemperature (OT) Fault

If, during STANDBY, INIT_SOA_REG, normal operation or FAULT, the temperature measured between the TSNS_P and TSNS_N pins raises above the OT_FAULT_LIMIT value, a fault is triggered and FET is opened with a regular pull-down.

XDP710 waits until FET is completely turned off, then keeps monitoring the FET temperature and stays in the FAULT state until it drops below OT_FAULT_LIMIT - 12°C. In this case, the power-up sequence initiates, FAULT pin deasserts and PWRGD pin asserts as soon as the necessary conditions are met.

On-chip Thermal Shut-down (TSD) Fault

XDP710 has an on-chip temperature sensor with a programmable fault limit of T_{TS_UTH} . If die temperature exceeds this value, a fault is triggered and FET is opened with a regular pull-down. XDP710 waits until FET is completely turned-off, then remains idle in the FAULT state until the temperature drops below T_{TS_LTH} (which is equivalent to $T_{TS_UTH} - 10^{\circ}\text{C}$), at which point the power-up procedure is started.

4.2.6 Power-up faults

Unsuccessful Power-up (Watchdog, WD) Fault

The watchdog timer can be configured from 10 ms to 10000 ms by means of the WATCHDOG[2:0] bits. Its configurable steps are compliant with common SOA lines so that protection can be implemented according to the maximum allowed timer for a specific V_{DS} vs I_{DS} scenario. It starts running as soon as power-up procedure starts in the INIT_SOA_REG state. If FET is not fully enhanced ($V_{DS} < 1.0\text{ V}$ and $V_{GS} > 7.8\text{ V}$) before the timer expires, a WD fault is triggered and FET is turned-off with a regular pull-down.

A power-up is retried according to the RETRY command settings, in which case, the FAULT pin is cleared when leaving FAULT state before any retry attempt. The corresponding status bit remains set until it is manually cleared or device is restarted or power cycled.

Unsuccessful Retry (UR) Fault

The UR fault can only occur in FAULT state when the retry counter expires after one of the retry fault events (SOC, OUV, WD, OC, SOAR). The retry counter decrements on each retry event. If it reaches a value of zero

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(maximum number of programmed retries has been reached), a UR fault is triggered and the system goes to and remains in LATCH_OFF state.

4.2.7 Internal protection fault

VREG Fault

If, at any point of operation, voltage at VREG pin goes below 4.15 V, FET will be turned off. This fault is not signaled at the FAULT pin, nor does it have a bit in the STATUS_FAULTS PMBus command. Instead of going to FAULT state, this fault puts the device in STANDBY state.

4.3 Retry

XDP710 can be configured to automatically retry FET's power-up after FET shut down due to the following faults: OUV, Watchdog, OC, SOAR, SOC.

Retry mask bits are provided so that retry function can be turned on or off for any of these faults.

The number of retries can be configured from 0 (system latches off after first fault event) to 32 by setting the corresponding number in the RETRY_COUNTER[2:0] bits in the RETRY PMBus command.

The retry counter can also be disabled, which means the system will keep retrying an infinite number of times until it is turned off or reset.

The controller waits for a cool down period configurable from 0 to 64 seconds (COOLD_TMR[2:0] bits in RETRY PMBus command) before every retry attempt. During this period, the controller remains in FAULT state and CLEAR_FAULTS command and EN pin toggling will be ignored.

If a successful FET's power-up is achieved during a retry attempt, the retry OK deglitch timer (RETD_TMR[2:0] bits in RETRY PMBus command) starts running as soon as ON state is reached.

If no fault has occurred when this timer expires, the retry counter is set to its initial state.

If the maximum number of retries is reached without success, an unsuccessful retry fault, which initiates Latch-off, is issued.

If the retry feature is used to avoid long start-up times due to the fault that caused the retry, it is recommended to enable the watchdog (WD) fault and its corresponding watchdog retry mask in MASK_FAULTS PMBus command.

Gate Voltage Fast Recovery

The gate voltage fast recovery is turning FET on as fast as possible avoiding FET's regulation during retry attempts after an SOC fault.

When the feature is enabled by setting the GATE_REC_EN bit in the RETRY command, the cool down period before retry is ignored after an SOC fault.

For all cases when GATE_REC_EN='1' and entering INIT_SOA_REG, if the control loop recognizes NO regulation conditions (FET's V_{DS} is low enough), the gate strong pull-up with typically 10 mA current capability is activated for a fast FET turn-on within a time of 100 μ s. System retries with fast recovery as many times as configured by the RETRY_COUNTER. If recovery is not successful before RETRY_COUNTER expires, system goes to latch-off state.

4.4 Latch-off

LATCH_OFF and MEM_FAULT are latch-off states. In case of a latch-off fault, the controller's FAULT state is followed by the LATCH_OFF or MEM_FAULT state and controller:

- Keeps FET off and remains in LATCH_OFF or MEM_FAULT state
- Latches the state of all status commands including fault and warning ones
- Latches the state of status pins (PWRGD, FAULT, WARN)
- Keeps service blocks (including VREG), communication PMBus interface and necessary digital running to support data communication

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Latch-off is immediately triggered by the following faults:

- Memory OTP fault
- FET's Drain-source short fault
- FET's Gate-drain short fault
- FET's Gate-source short fault

Latch-off is triggered if during the following faults the max number of retries has been reached without successful recovery from fault (Unsuccessful retry (UR) fault occurs):

- Output undervoltage (OUV) fault
- Unsuccessful power-up (watchdog) fault
- Overcurrent (OC) fault
- SOA regulation fault
- Severe overcurrent (SOC) fault

If the retry counter set to zero the Latch-off is triggered right after any fault listed above occurs.

XDP710 can go out of LATCH_OFF or MEM_FAULT states by means of a power cycle. In which case, it starts operation from POR_INIT state.

Alternative ways to go out of LATCH_OFF (not applicable to MEM_FAULT) are the PMBus CLEAR_FAULTS command or the external EN signal High-to-Low transition (if the pin is configured as EN, see [Enable and Disable](#)). If either of these methods is used, the following actions take place:

- De-assert/release status pins (PWRGD, FAULT, WARN)
- Clear the FAULT and WARNING status commands
- Continue operation from CHK_FET state

4.5 Warnings

Warnings are defined as alerts that do not turn off the FET. They are alerted through the WARN pin to the processor/MCU so that it can decide if any action is needed in response.

Each one of the warnings has a corresponding bit in the STATUS_WARN command that is set when a warning has occurred.

These bits can be reflected in the WARN pin to alert the processor/MCU that any of these events has happened. A mask command is provided for the user to select which warnings are to be reflected on the WARN pin.

Warnings can be disabled by clearing their enable bits, which means they are not detected and are not reported.

Each one of the warnings descriptions below specifies when the "warning is cleared". This means the WARN pin is de-asserted automatically when the conditions that generate one or more warnings are cleared.

The warning status bits remain set until they are cleared:

- by means of the CLEAR_FAULTS PMBus command
- or by a controller restart or a power cycle

Note: Due to the nature of the COM warning, there are some exceptions on the way it is reported through the WARN pin and the way it is cleared. See details in [Communication warning](#).

The table below shows when particular warning's processing is active.

Table 25 Warnings during operation states

Activation (X) of WARNING's processing during operation states	
(table continues...)	

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Table 25 (continued) Warnings during operation states

WARNING NAME	State of controller								
	POR_INIT	READ_CFG	CHK_FET	STANDBY	INIT_SOA_REG	ON	I_REG	FAULT	MEM_FAULT/LATCH_OFF
VGSL	--	--	--	--	--	X	--	--	--
OT	--	--	--	X	X	X	X	X	--
TSD	--	--	--	X	X	X	X	X	--
UV	--	--	--	X	X	X	X	X	--
OV	--	--	--	X	X	X	X	X	--
OOV	--	--	--	X	X	X	X	X	--
OUV	--	--	--	--	--	X	X	--	--
SOAR	--	--	--	--	--	X	X	--	--
OUC	--	--	--	--	--	X	X	--	--
OOC	--	--	--	--	--	X	X	--	--
INeg	--	--	--	--	--	X	X	--	--
OP	--	--	--	--	X	X	X	--	--
COM	--	--	--	X	X	X	X	X	X

The following figure shows flow of all warnings.

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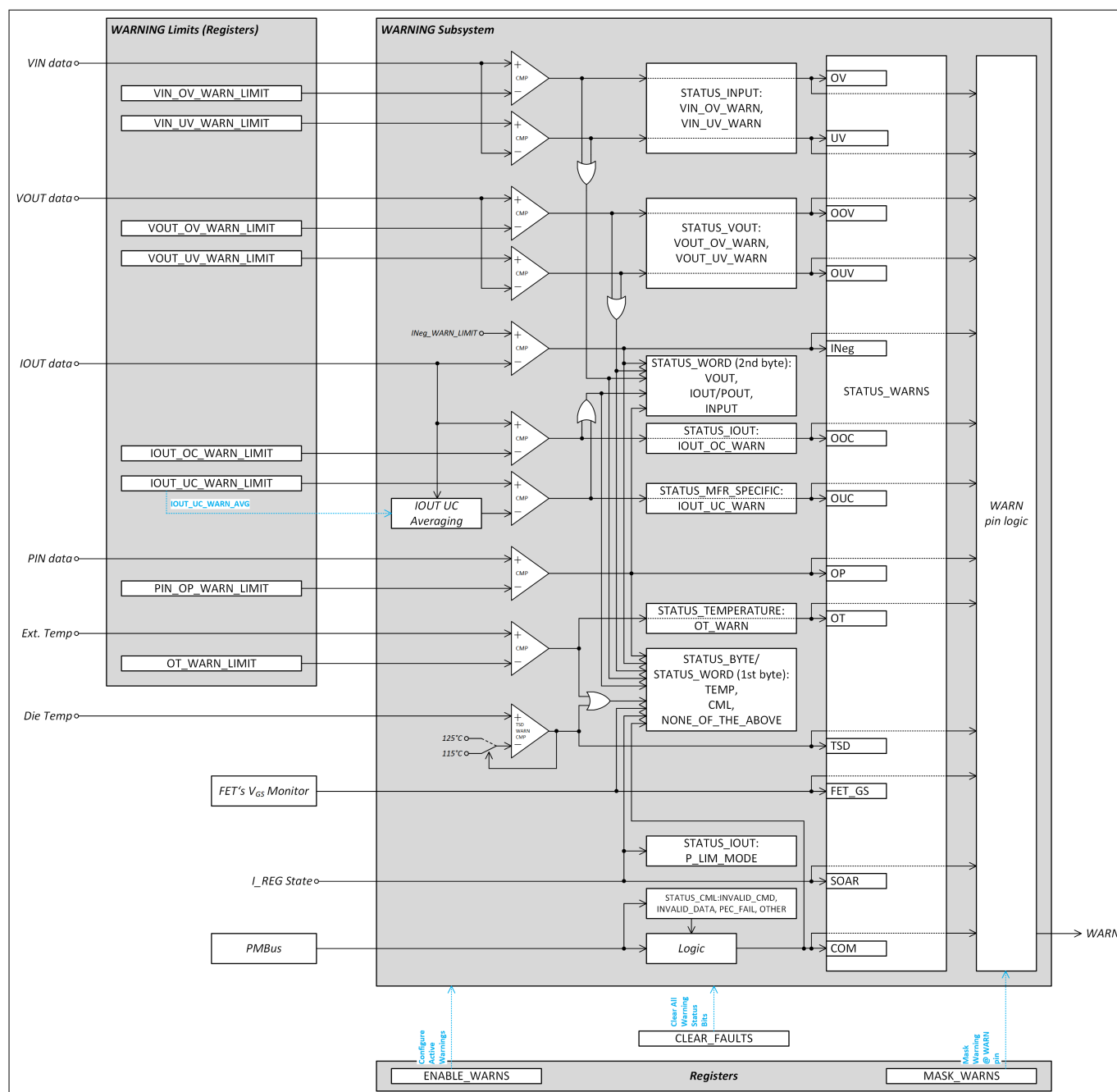


Figure 11 Warnings flow

4.5.1 Damaged FET warning

Gate-Source Low Voltage (VGSL) Warning

If, during ON state, V_{GS} of the FET goes below 7.8 V, a VGSL warning is triggered indicating that there might be gate-source or gate-drain issues over life time. The warning is cleared as soon as V_{GS} of the FET raises above the same limit.

4.5.2 Input voltage and power warnings

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Input Undervoltage (UV) Warning

If the input voltage reaches or falls below VIN_UV_WARN_LIMIT, a warning is triggered. If the voltage raises above this limit plus a hysteresis of 0x60 (see Table 23), the warning is cleared.

Input Overvoltage (OV) Warning

If the input voltage reaches or raises above VIN_OV_WARN_LIMIT, a warning is triggered. If the voltage falls below this limit minus a hysteresis of 0x60 (see Table 23), the warning is cleared.

Input Overpower (OP) Warning

If the input power (as a product of VIN * IOUT) goes above the programmed PIN_OP_WARN_LIMIT, the system generates an OP warning. If the input power goes below the limit minus a digital hysteresis of 0x100 (which corresponds to typically 0.4% of the maximum power), the warning is cleared. Averaging of power for this warning is done by the same setting as telemetry: P_TELEMETRY_AVG bits in TELEMETRY_AVG PMBus command.

4.5.3 Output voltage warnings

Output Undervoltage (OUV) Warning

If the output voltage reaches or falls below VOUT_UV_WARN_LIMIT, a warning is triggered. If the voltage raises above this limit plus a hysteresis of 0x60 (see Table 23), the warning is cleared.

Output overvoltage

This warning bit will be set if, during Power-up Procedure, Normal Operation or FAULT state, the output voltage exceeds the limit set by VOUT_OV_WARN_LIMIT PMBus command.

4.5.4 Current and temperature warnings

Output Overcurrent (OOC) Warning

An OOC warning is detected if the load current sensed by the voltage drop in the sense resistor exceeds the limit set by the IOUT_OC_WARN_LIMIT PMBus command. The warning is cleared if the current goes below the IOUT_OC_WARN_LIMIT minus a digital hysteresis of 0x80 (see Table 26).

Output Undercurrent (OUC) Warning

If, during normal operation, the FET I_{DS} current is less than a programmable value of the IOUT_UC_WARN_LIMIT PMBus command, an undercurrent event is triggered. The warning is cleared as soon as the current goes back above the IOUT_UC_WARN_LIMIT value plus a digital hysteresis of 0x80, which corresponds to the following current levels, depending on the V_{SNS_RNG} setting and assuming a 1 mΩ sense resistor:

Table 26 Current hysteresis

V _{SNS_CS} (mV)	12.5	25	50	100
Current (A)	0.55	1.11	2.2	4.4

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SOA Regulation (SOAR) Warning

A warning is issued when the controller enters the I_REG state due to OC or SOA conditions violation if SOAR_TMR[2:0] is not programmed to 0. The warning remains set until the controller leaves the I_REG state.

Negative Current (INeg) Warning

If negative current through the FET over I_{NEG_MAX} level is detected, an I_{Neg} warning is triggered. The warning is cleared when the FET/load current sample returns to positive level (≥ 0 A).

Overtemperature (OT) Warning

If temperature raises above OT_WARN_LIMIT, an OT warning is issued. The WARN pin remains asserted until the temperature falls below OT_WARN_LIMIT minus a hysteresis of 12°C.

On-chip Thermal Shut-Down (TSD) Warning

XDP710 has an on-chip temperature sensor. If, during power-up procedure, normal operation or FAULT state, temperature exceeds an upper threshold of 125°C, a warning is triggered. The warning is cleared when the temperature falls below 115°C.

4.5.5 Communication warning

PMBus Interface Communication (COM) Warning

This warning is triggered if the PMBus communication (read or write) is detected with fails. COM is the only warning that is enabled during LATCH_OFF state. Since the WARN pin status is latched during this state, the warning is not reported through the pin. The only way to detect this warning during LATCH_OFF is to read the STATUS_WARNINGS command.

Due to the nature of this warning, it is not cleared automatically. To clear its status bits and the WARN pin after this warning has been set, a CLEAR_FAULTS command must be issued.

4.6 Telemetry

XDP710 provides real time accurate measurement and calculation data for:

- Input voltage
- Output voltage
- Load/FET current (by means of voltage drop over external shunt resistor), including its squared RMS value (if enabled)
- Input power
- Energy
- External FET temperature
- On-chip temperature

All information is provided through the PMBus interface by issuing the corresponding commands.

The figure below shows the telemetry flow:

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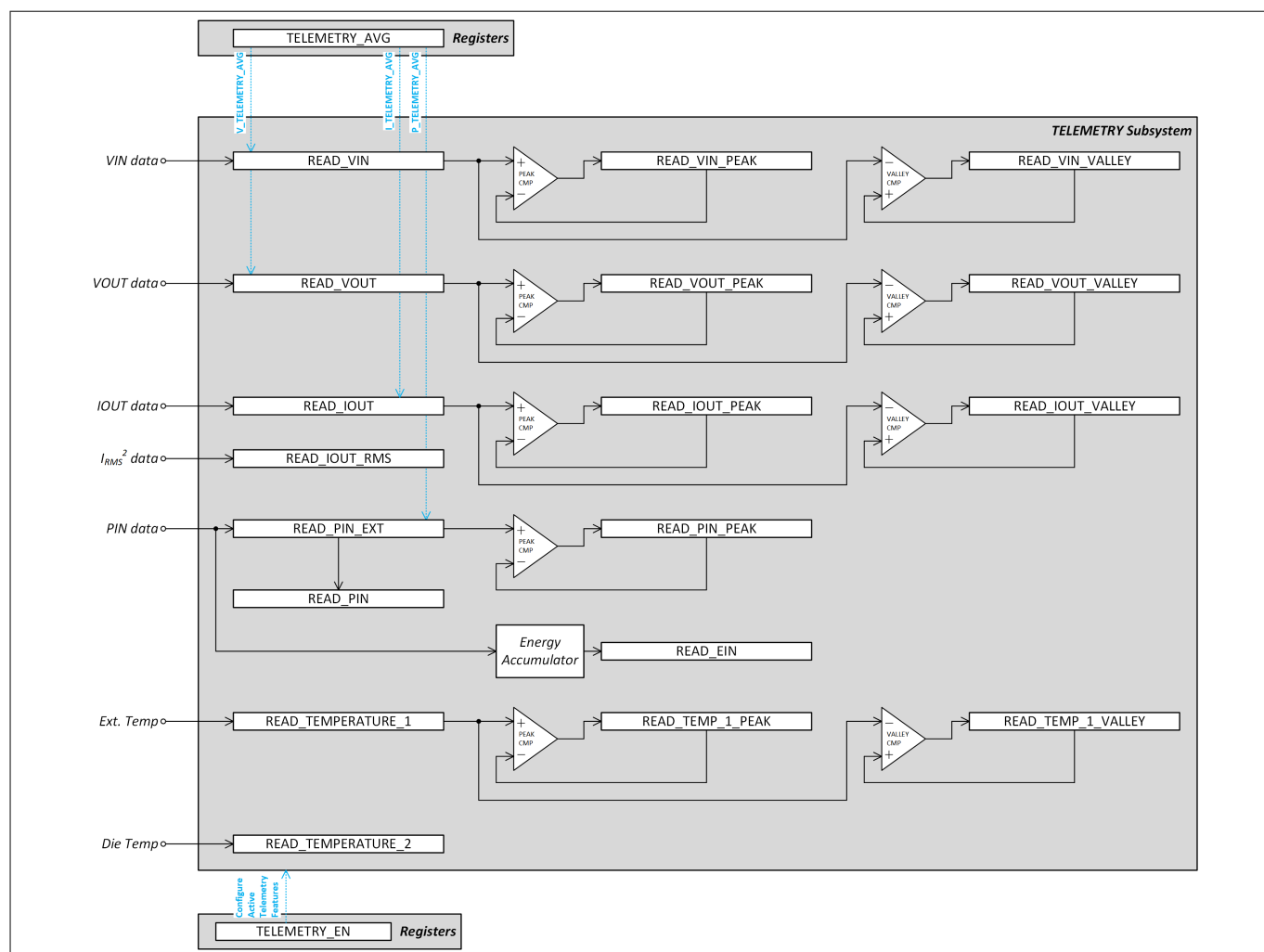


Figure 12 Telemetry flow

4.6.1 Telemetry summary table

The following table shows the sensing points of the different telemetry features and the commands to be used for configuration and to get the data read.

Table 27 Telemetry summary

Parameter	Sensing	Averaging configuration	Instantaneous/ averaged	Peak	Valley
Input voltage	ISNS_P pin	V_TELEMETRY_AVG	READ_VIN	READ_VIN_PEAK	READ_VIN_VALLEY
Load/FET current	ISNS_P/ISNS_N pins	I_TELEMETRY_AVG	READ_IOUT	READ_IOUT_PEAK	READ_IOUT_VALLEY
RMS Load/FET current	ISNS_P/ISNS_N pins		READ_IOUT_RMS		
Output voltage	VOUT pin	V_TELEMETRY_AVG	READ_VOUT	READ_VOUT_PEAK	READ_VOUT_VALLEY

(table continues...)

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Table 27 (continued) Telemetry summary

Parameter	Sensing	Averaging configuration	Instantaneous/averaged	Peak	Valley
Input power (16 bits)	Input voltage x Load/FET current	P_TELEMETRY_A VG	READ_PIN		
Input power (24 bits)			READ_PIN_EXT	READ_PIN_PEAK	
Energy	Input power accumulated over time		READ_EIN		
External FET temperature	TSNS_P/TSNS_N pins		READ_TEMPERA TURE_1	READ_TEMP_1_ PEAK	READ_TEMP_1_V ALLEY
On-Chip temperature	On-chip temperature sensor		READ_TEMPERA TURE_2		

4.6.2 Averaged and instantaneous telemetry
4.6.2.1 Averaging telemetry data

Input voltage and power and output voltage and current measurements can be averaged by means of their corresponding bit fields: V_TELEMETRY_AVG[2:0], I_TELEMETRY_AVG[2:0] and P_TELEMETRY_AVG[2:0]. Each one consisting in 3 bits.

Table 28 Telemetry averaging

Bits settings	Averaged amount of samples
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

4.6.2.2 Instantaneous telemetry data

Instantaneous measurements can be obtained by setting the corresponding x_TELEMETRY_AVG[2:0] bits to 000, so that only one sample is taken.

4.6.3 Peaks and valleys

x_PEAK and x_VALLEY commands report the maximum and minimum values (respectively) measured since the last time the command was cleared.

Peaks apply for the following parameters:

- Input voltage

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- Output voltage
- Load/FET current
- Input power
- External FET temperature

Valleys apply for the following parameters:

- Input voltage
- Output voltage
- Load/FET current
- External FET temperature

The x_PEAK and x_VALLEY commands are cleared after reading their contents or by means of a power on reset. After reset, the first value read is compared to 0x000 (peaks) or 0xFF (valleys) and it becomes a new peak or valley respectively.

4.6.4 Telemetry via PMBus

The following formula converts from PMBus direct format to "real world" values:

$$X = \frac{1}{m} * (Y * 10^{-R} - b)$$

Equation 3

Where:

X = Calculated "real world" value in the appropriate units (A, V, °C, etc)

m = Slope coefficient, is a two byte, two's complement integer

Y = Two byte two's complement integer received from the PMBus device

b = Offset, is a two byte, two's complement integer

R = Exponent, is a one byte, two's complement integer

To convert from "real world" values to PMBus direct format, use the following formula:

$$Y = (mX + b) * 10^R$$

Equation 4

Where:

Y = two byte two's complement integer to be sent to the unit

m = Slope coefficient, is the two byte, two's complement integer

X = "real world" value, in units such as Amperes or Volts, to be converted for transmission

b = Offset, is the two byte, two's complement integer

R = Exponent, is the decimal value equivalent to the one byte, two's complement integer.

Coefficients for these formulas are specified in the following table:

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Table 29 PMBus coefficients

Command	VTLM_RNG	VSNS_CS	m	b	r
VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, VIN_OV_FAULT_LIMIT, VIN_OV_WARN_LIMIT, VIN_UV_FAULT_LIMIT, READ_VIN, READ_VIN_PEAK, READ_VIN_VALLEY, READ_VOUT, READ_VOUT_PEAK, READ_VOUT_VALLEY	88	-	4653	0	-2
	44		9307	0	-2
	22		18614	0	-2
IOUT_OC_WARN_LIMIT, IOUT_UC_WARN_LIMIT, READ_IOUT, READ_IOUT_PEAK, READ_IOUT_VALLEY	-	12.5	23165	0	-2
		25	11582	0	-2
		50	5791	0	-2
		100	28956	0	-3
READ_IOUT_RMS	-	12.5	20808	0	-2
		25	5202	0	-2
		50	13005	0	-3
		100	32513	0	-4
READ_PIN_EXT, READ_PIN_PEAK	88	12.5	10780	0	0
		25	5390	0	0
		50	26949	0	-1
		100	13474	0	-1
	44	12.5	21559	0	0
		25	10780	0	0
		50	5390	0	0
		100	26949	0	-1
	22	12.5	4312	0	1
		25	21559	0	0
		50	10780	0	0
		100	5390	0	0

(table continues...)

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Table 29 (continued) PMBus coefficients

Command	VTLM_RNG	VSNS_CS	m	b	r
PIN_OP_WARN_LIMIT, READ_PIN, READ_EIN	88	12.5	4211	0	-2
		25	21054	0	-3
		50	10527	0	-3
		100	5263	0	-3
	44	12.5	8422	0	-2
		25	4211	0	-2
		50	21054	0	-3
		100	10527	0	-3
	22	12.5	16843	0	-2
		25	8422	0	-2
		50	4211	0	-2
		100	21054	0	-3
OT_FAULT_LIMIT, OT_WARN_LIMIT, READ_TEMPERATURE_1, READ_TEMP_1_PEAK, READ_TEMP_1_VALLEY	-	-	52	14321	-1
READ_TEMPERATURE_2	-	-	23	6225	-1

Note: Current and power coefficients are normalized to a 1 mΩ sense resistor. See [Calculating PMBus direct format limits from "real world" values and vice-versa](#) for examples on how to calculate current and power.

4.6.5 RMS current calculation

RMS current is calculated by integrating the current measurements over a specific period of time set by RMS_SAMPLE_TMR[1:0] bits in the SOA_TMR command.

4.6.6 Input power calculation

Input power is a multiplication of the load/FET current and the input voltage values.

Each time a current measurement is performed, a power calculation is performed, multiplying the recent values of load/FET current and the input voltage together before their corresponding averaging. Input power can be reported in 16 bits format (READ_PIN) or an extended 24 bits format (READ_PIN_EXT).

4.6.7 Energy calculation

Energy is the input power accumulated over time.

The calculated input power value is added to a power accumulator command that may increment a rollover counter if the value exceeds the maximum accumulator value. The power accumulator command also increments a power sample counter. The power accumulator and power sample counter are read using the same READ_EIN command to ensure that the accumulated value and sample count are from the same point in time.

The MCU reading the data assigns a time stamp when the data is read. By calculating the time difference between consecutive uses of READ_EIN and determining the delta in power consumed, it is possible for the MCU to determine the total energy consumed over that period.

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4.7 Communication Interfaces

4.7.1 PMBus

The power management bus (PMBus) is an open-standard digital power management protocol: simple, standard, flexible, extensible, and easy to program. The PMBus command language enables communication between components of a power system: CPUs, power supplies, power converters, and more.

XDP710 supported features and commands are based on the PMBus Specification Rev 1.3.1 parts I, II and III.

Communication via PMBus is possible right after internal circuitry initialization, which takes around 2 ms after input voltage is applied.

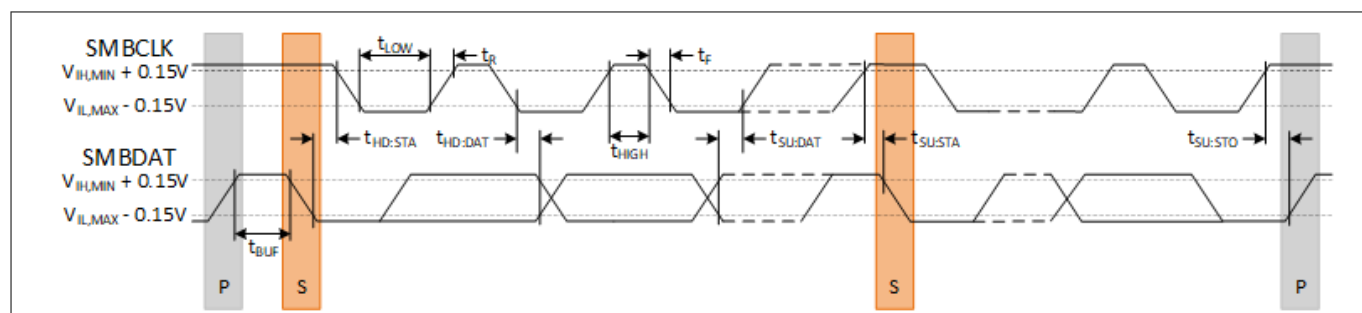


Figure 13 PMBus timing diagram

4.7.1.1 Supported functions

The PMBus is specified to cover a lot of different applications in the realm of power management. For a hot-swap application, only a subset of commands is used.

4.7.1.1.1 Addressing

The device has a slave address controlled by PMBUS_CFG command or by address pins. There are 16 different addresses available for external resistor setting. See [Table 13](#).

4.7.1.1.2 Protocol violations

XDP710 supports the following protocol violations:

- Command not valid
- Command too short
- Data not valid
- Error at repeated start
- Extra Byte in command
- Page not valid
- Read bit set in address
- Read too few bits
- Read too many bytes
- Send too few bits
- Send too many bytes

4.7.1.1.3 Timeout

If a device is holding onto the bus then the bus may freeze. If the microcontroller sees such an issue it may stop the clock for $t_{TIMEOUT}$. This may also happen if another slave holds the bus incorrectly. This causes all slaves to reset their PMBus interfaces and be ready for a new start command.

4 Product Features

4.7.1.2 Protocol

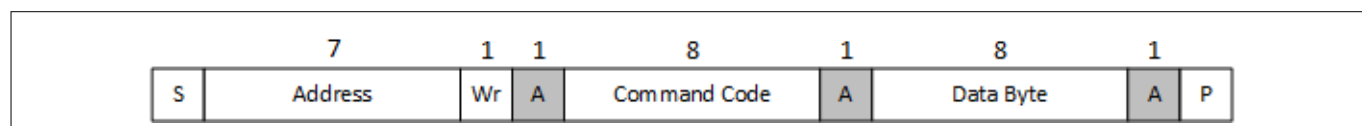


Figure 14 Write Byte protocol

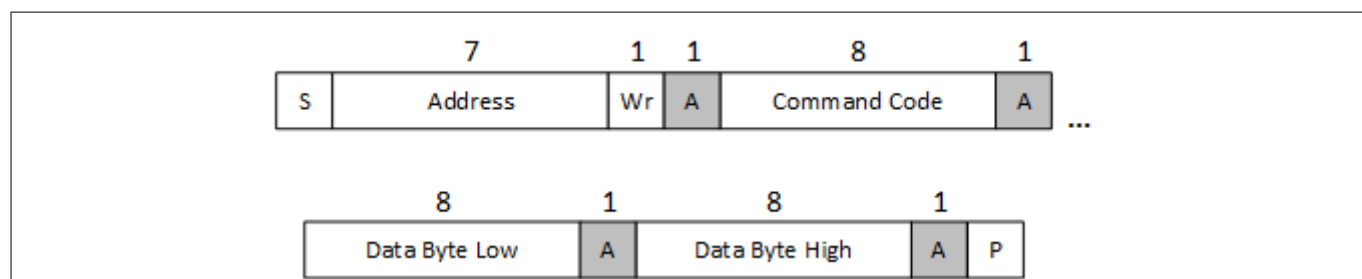


Figure 15 Write Word protocol

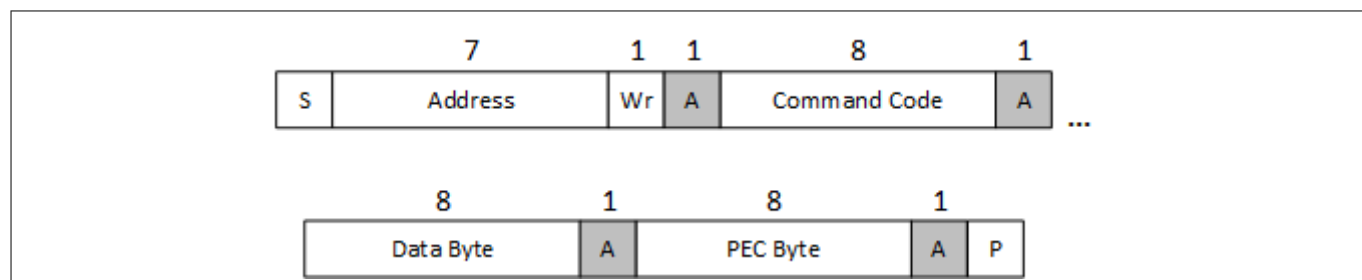


Figure 16 Write Byte protocol with PEC

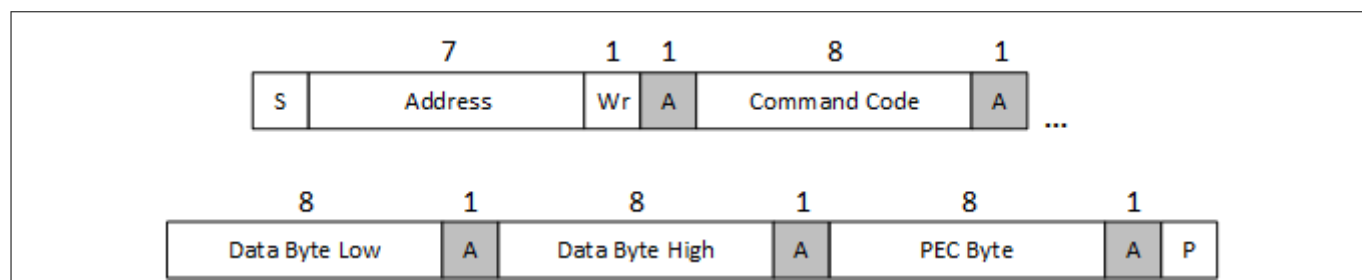


Figure 17 Write Word protocol with PEC

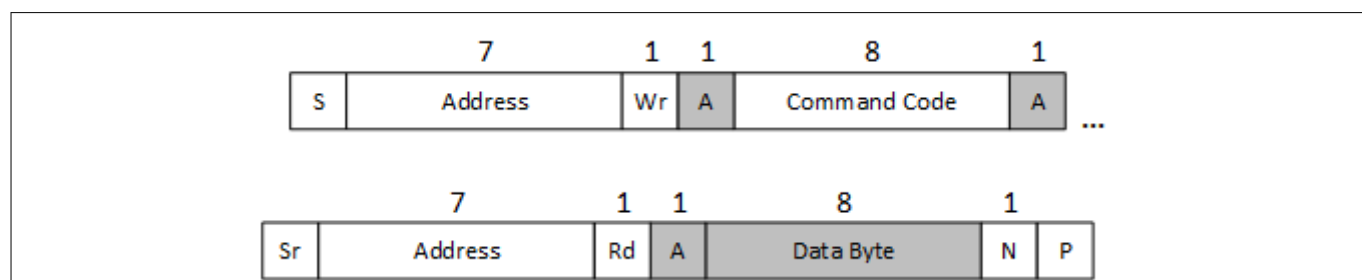


Figure 18 Read Byte protocol

4 Product Features

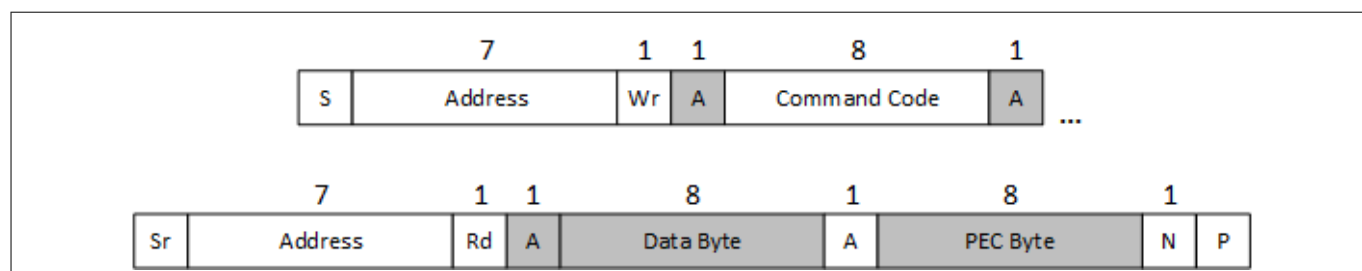


Figure 19 Read Byte protocol with PEC

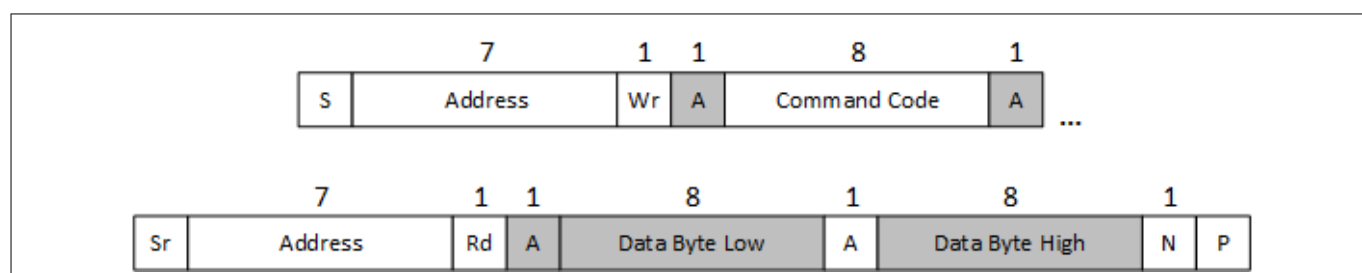


Figure 20 Read Word protocol

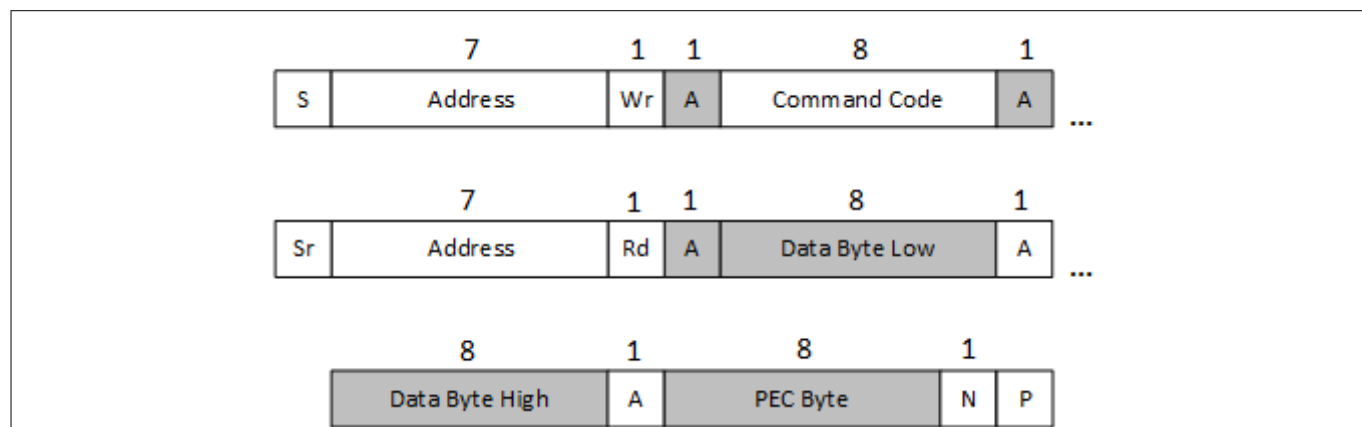


Figure 21 Read Word protocol with PEC

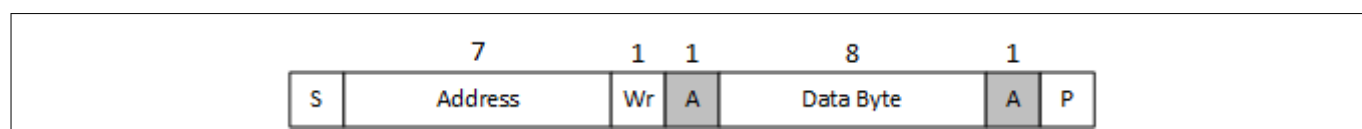


Figure 22 Send Byte protocol

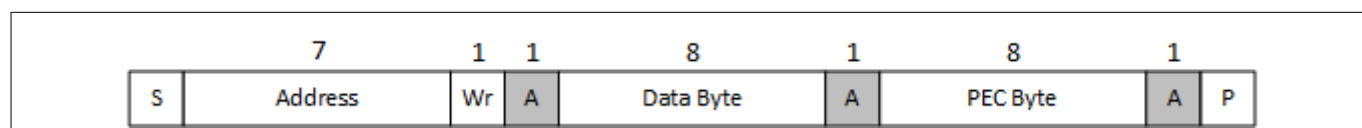


Figure 23 Send Byte protocol with PEC

4 Product Features

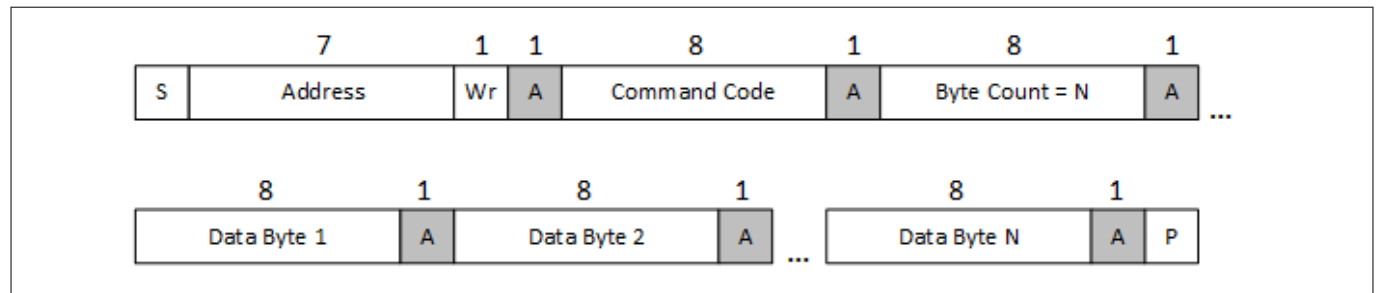


Figure 24 **Block Write**

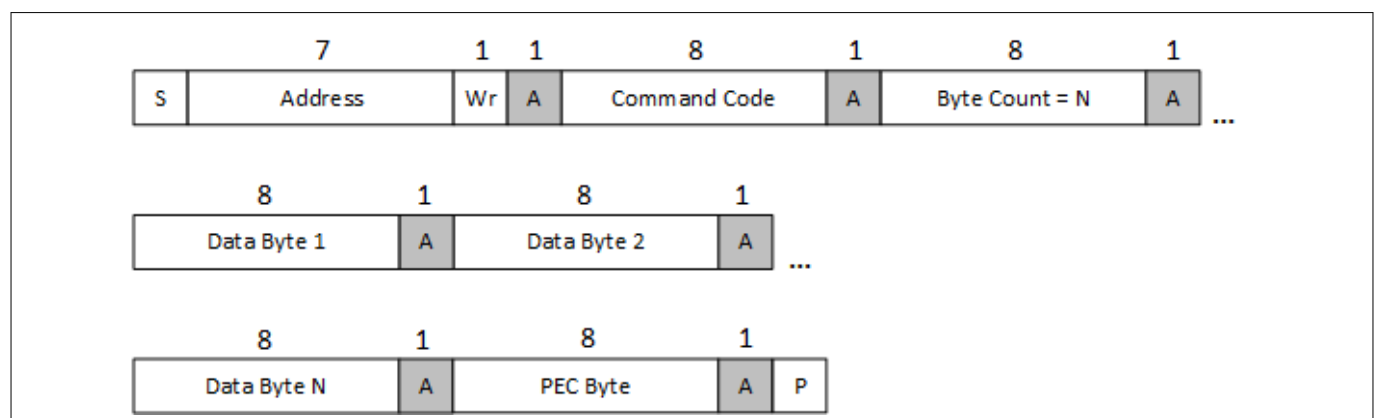


Figure 25 **Block Write with PEC**

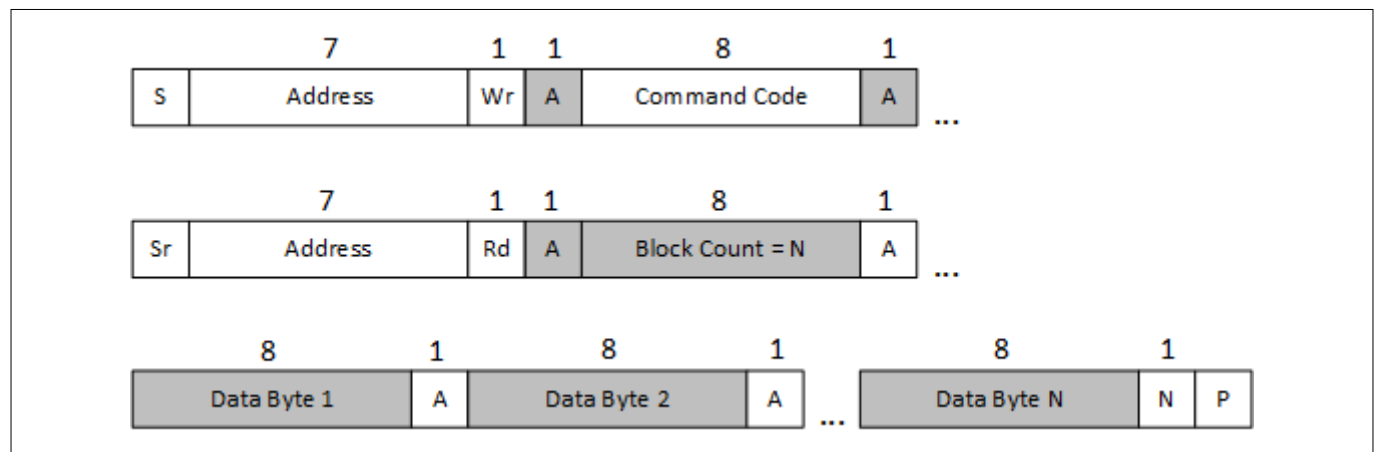


Figure 26 **Block Read**

4 Product Features

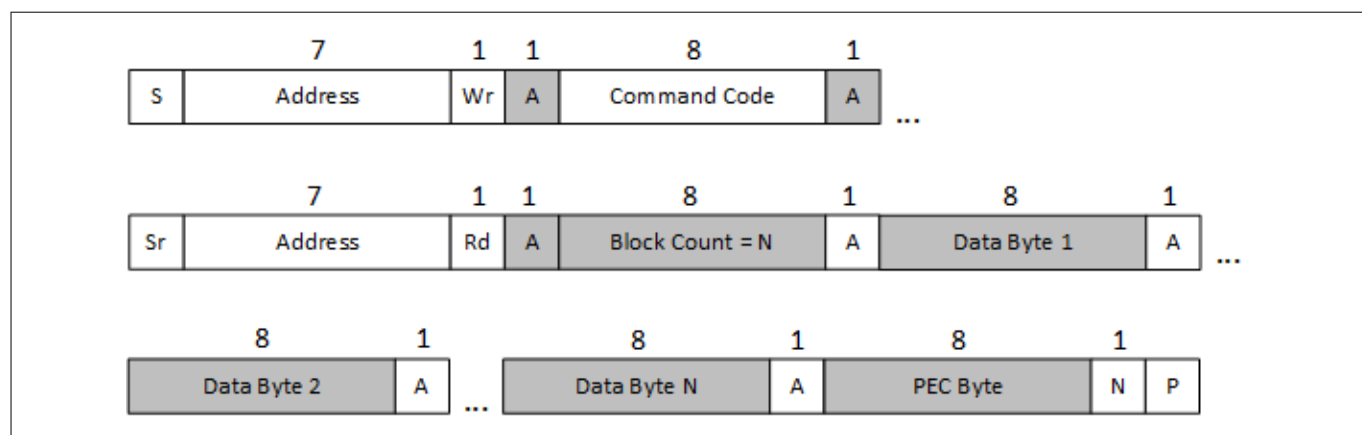


Figure 27 Block Read with PEC

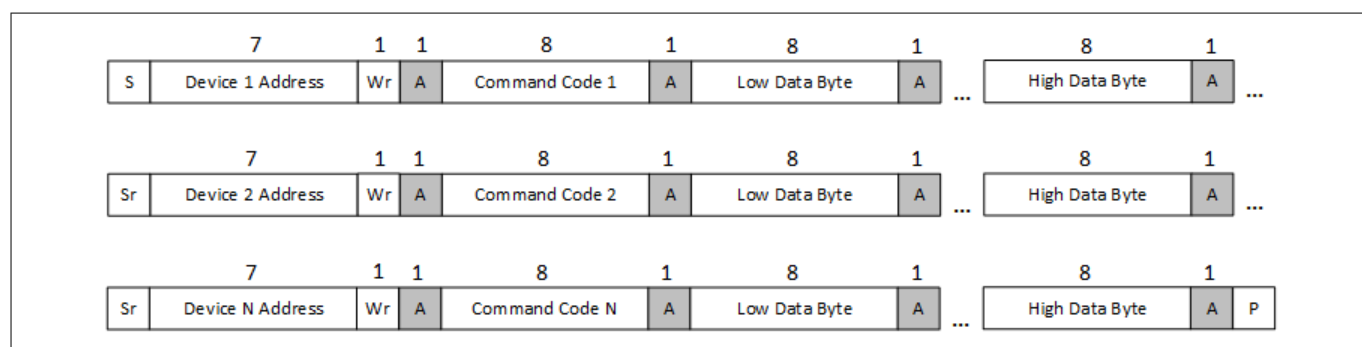


Figure 28 Group Command protocol

4 Product Features

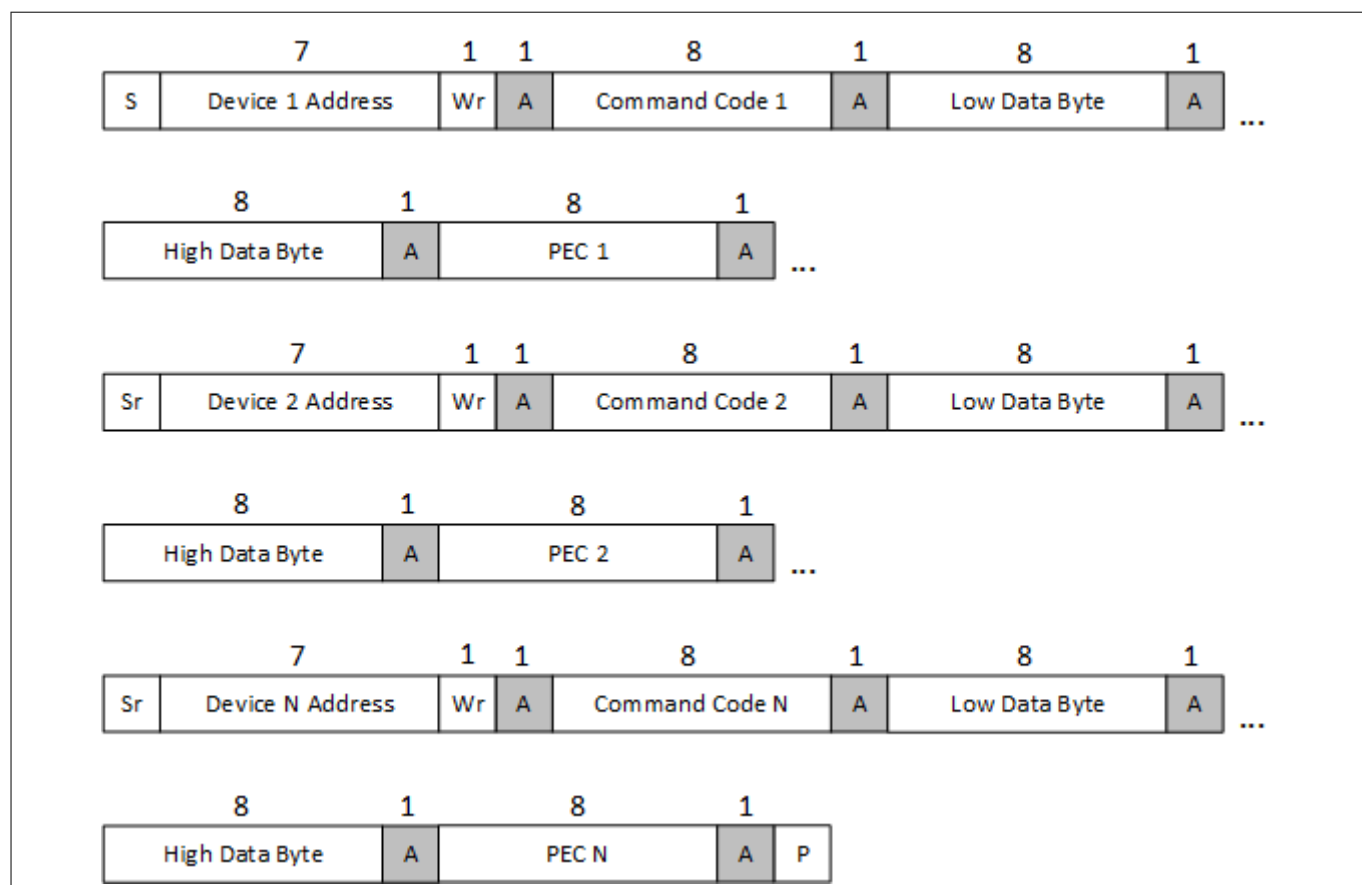


Figure 29 Group Command protocol with PEC

4.8 Memory

XDP710 has three types of memory for programmability:

- Volatile memory
- One time programmable (OTP)
- Multiple time programmable (MTP)

The one time programmable (OTP) memory can be used to fix and save specific command settings. At power-up, during READ_CFG state, all the settings saved in the OTP memory are copied into volatile memory.

XDP710 contains 10 pages of MTP for a multiple time programmability. When the number of reprogramming reaches 10 (indicated by MTP_FULL bit in STATUS_MEM command), the circuit keeps the latest programmed values. The command contained in this memory section is I_SNS_CFG, which contains the following configuration bits: CS_RNG, CS_RNG_TRIM, SOC_FAULT_LIMIT and START_ILIM.

To program the desired settings in internal commands or OTP at power-up, the following steps must be followed:

- Apply a voltage at the VDD_VIN pin:
 - ≥ 5.5 V to program commands
 - ≥ 20 V to program OTP or MTP memory
- Keep the UV/EN pin at chip GND potential
- Communication via PMBus is possible as soon as STANDBY state is entered. At this point, commands, OTP or MTP memory can be programmed.
- For a successful programming, internal temperature of the device must stay below 125°C at all times.

To program OTP or MTP sections:

1. Program the commands in volatile memory as desired.

4 Product Features

2. Select the section to be programmed by means of the SEL_SEC bits in WRITE_OTP command.
3. Set the WRITE_OTP bit.
4. The command configuration is automatically copied to the selected section.

If the MTP section is selected, XDP710 automatically locates the latest available page and program it.

PROG_BLOCK and OTP_FAIL indicate the status of the OTP and MTP memory programming according to the following table:

Table 30 OTP programming status

PROG_BLOCK	OTP_FAIL	Meaning
0	0	OTP programming has succeeded.
0	1	OTP programming started but failed during programming because of OTP issue. Part must be discarded.
1	0	OTP programming must not be started since temperature or VIN are out of range.
1	1	OTP programming started but failed during programming because temperature or voltage going out of range during programming. Part must be discarded.

Once programmed, OTP_USER bit indicates that the OTP memory has been programmed successfully and MTP_USER bits indicates that MTP memory is in use.

Before programming, PROG_BLOCK must be checked in order to determine if temperature and VIN are in range and programming is allowed. PROG_BLOCK indicates the temperature and voltage status in real time. If, after checking PROG_BLOCK, but before programming starts, any of these conditions goes out of range, programming will be blocked, PROG_BLOCK will be set and OTP_FAIL will remain 0. It is possible that, after a blocked attempt of programming, temperature and voltage go back in range, so PROG_BLOCK will read 0 again. Due to this, it is important to bear in mind that, as long as OTP_USER and OTP_FAIL are 0, it is still possible to program OTP.

If temperature and voltage conditions go out of range during programming, OTP_FAIL will indicate an unsuccessful programming after the operation. If temperature and voltage go back in range, PROG_BLOCK will read 0 again and it is only OTP_FAIL that indicates the programming failed.

5 Application Information

5.1 Typical application schematics

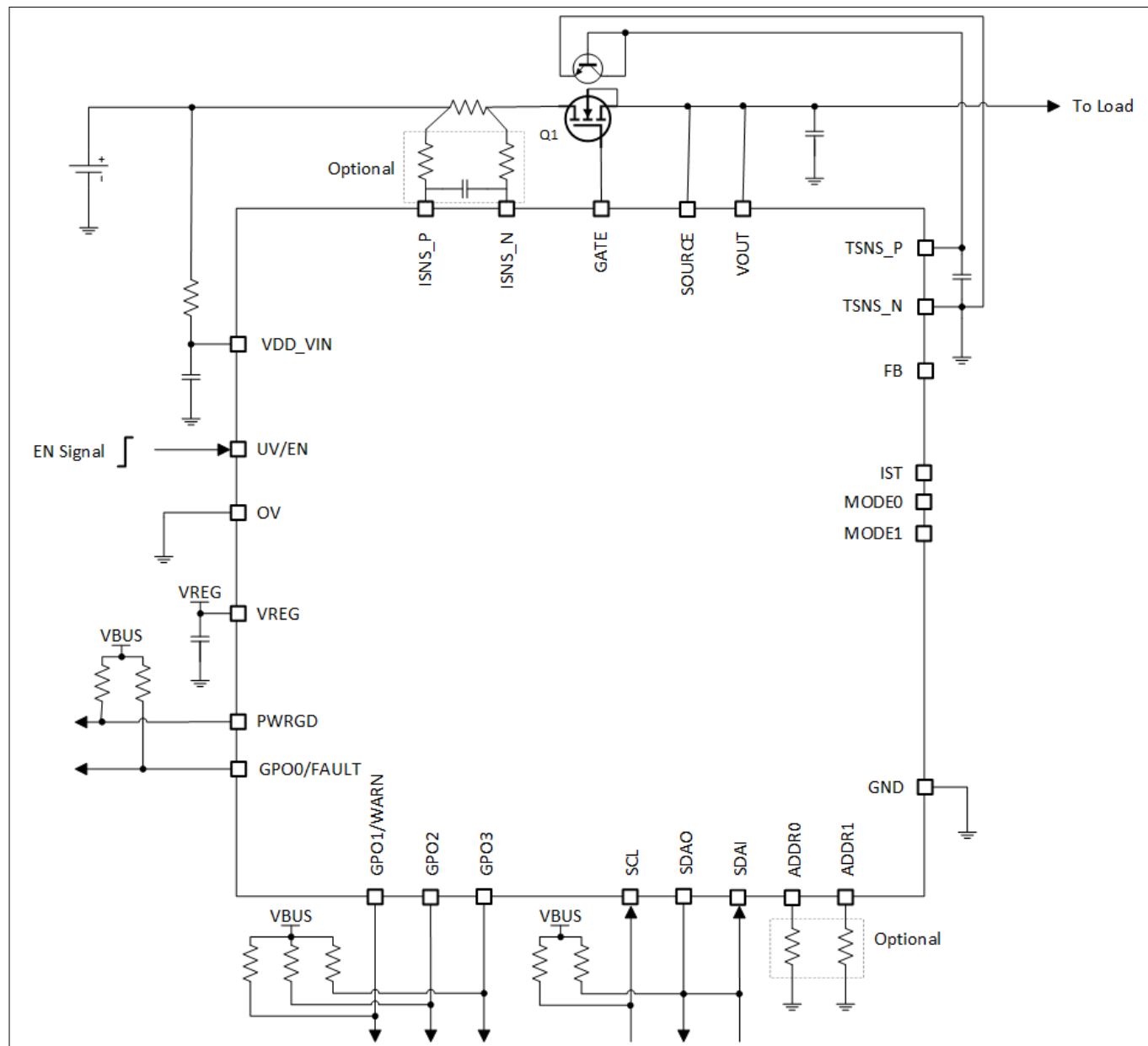


Figure 30 Fully digital mode DCM (MODE:MODE=0x1) application schematic

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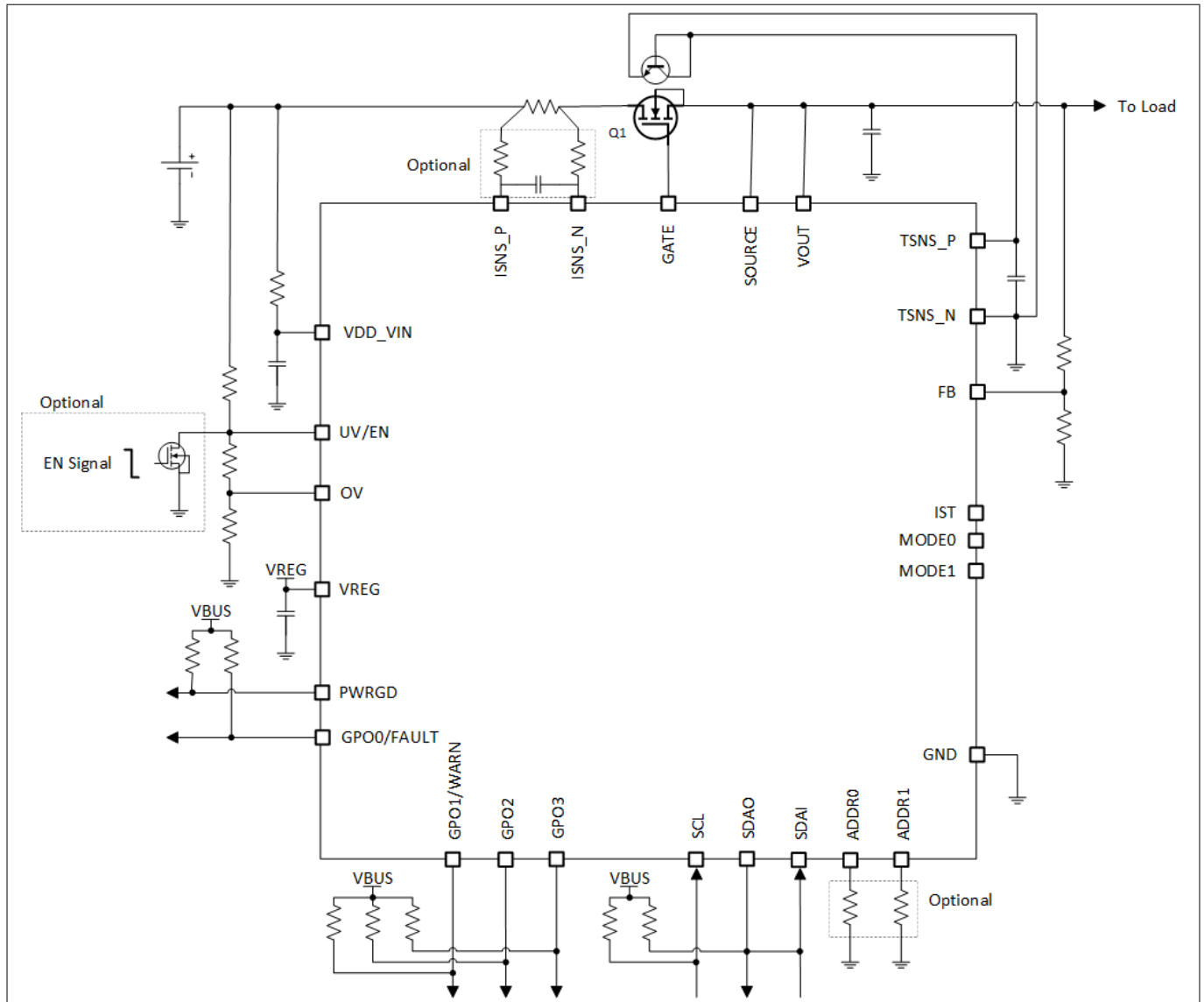


Figure 31 Fully digital mode ACM (MODE:MODE=0x0) application schematic

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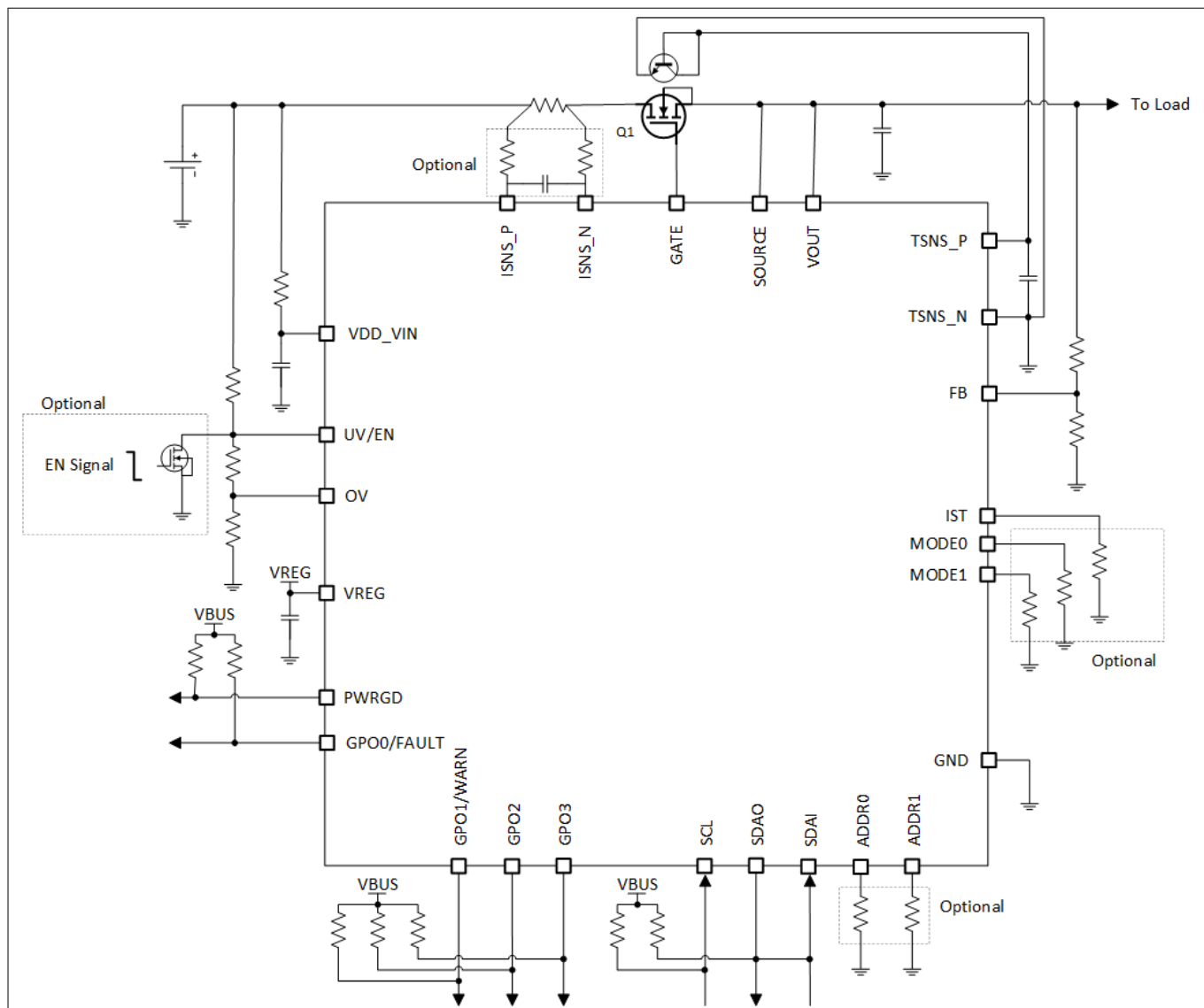


Figure 32 Analog assisted digital mode application schematic

5.2 Setting I_{OC}

The overcurrent (I_{OC}) limit is set by means of programming the maximum allowed voltage drop between the ISNS_P and ISNS_N pins V_{SNS_CS} . This voltage can be programmed to 12.5 mV, 25 mV, 50 mV or 100 mV.

Lower voltages are more convenient for high current applications and vice-versa. Lower voltages also give the advantage of reducing the power dissipation over the resistor. Higher voltages help improve the accuracy of the measurement due to the ADC resolution.

To select the current sense shunt resistor R_{SNS} calculate:

$$R_{SNS}(m\Omega) = \frac{V_{SNS_CS}(mV)}{I_{OC}(A)}$$

Equation 5

where I_{OC} is the maximum desired/allowed constant OC current in Amperes.

Once the resistor is calculated, its value must be chosen from the list provided in the description of the RSNS[5:0] bits of the REG_CFG command. Its value must be set accordingly in these bits. To reduce the

5 Application Information

power dissipation and for an optimum regulation performance, a sense resistor value between 0.25 mΩ and 10 mΩ is mandatory. In addition to the V_{SNS_CS} level, the current limit can be trimmed by means of the CS_RNG_TRIM[7:0] bits, according to the following formula:

$$LIMIT = \frac{I_{OC} * R_{SNS} * 180.31}{V_{SNS_CS}}$$

Equation 6

Where LIMIT is the decimal value to be programmed in the command, I_{OC} is the desired current limit value in Amperes, R_{SNS} is the value of the chosen current sense resistor in mΩ and V_{SNS_CS} is the programmed OC value in mV.

Note: For an optimum stability operation, I_{OC} must be $\geq I_{OC_MIN}$. If a current limit lower than this is needed, it can be trimmed by means of the CS_RNG_TRIM[7:0] bits. The following table shows minimum and maximum recommended sense resistor values for each one of the V_{SNS_CS} settings:

Table 31 Minimum and maximum recommended sense resistor values

VSNS_CS	Min R_{SNS} (mΩ)	Equivalent I_{OC} with Min R_{SNS} (A)	Max R_{SNS} (mΩ)	Equivalent I_{OC} with Max R_{SNS} (A)
12.5	0.25	50	2.5	5
25	0.3	83.3	5	5
50	0.6	83.3	10	5
100	1.2	83.3	10	10

5.3 Setting OV, UV and OUV in ACM

OV and UV values are set with a three resistor voltage divider, as shown in the following figure:

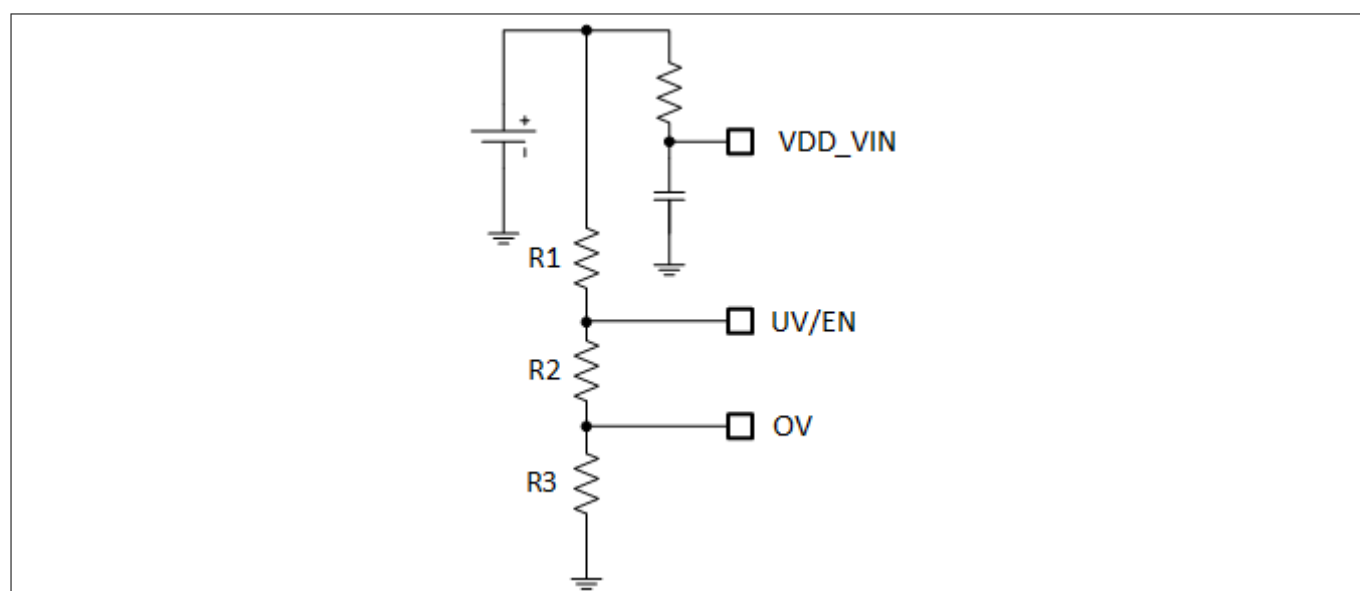


Figure 33 Setting OV and UV in ACM

Calculate the resistors values according to the application specific parameters using the following formulas:

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$$R3 = \frac{R_{TOTAL} * OV_{REF}}{V_{OV}}$$

Equation 7

$$R2 = \frac{R_{TOTAL} * UV_{REF}}{V_{UV}} - R3$$

Equation 8

$$R1 = R_{TOTAL} - R2 - R3$$

Equation 9

Where V_{OV} and V_{UV} are desired OV and UV levels respectively, $OV_{REF} = V_{OV_UTH}$, $UV_{REF} = V_{UVEN_LTH}$ and R_{TOTAL} is calculated after the desired current flow (typically hundreds of μA).

Care must be taken to avoid exceeding the maximum voltage level at the OV or UV pins.

Output Under Voltage (OUV) feature monitors the output voltage and detects when it goes down due to FET gate-to-drain leakage, degraded $R_{DS(on)}$ or high FET V_{DS} due to current regulation.

The FB pin has an internal comparator with a reference V_{REF} of 1.11V and a hysteresis of 50mV.

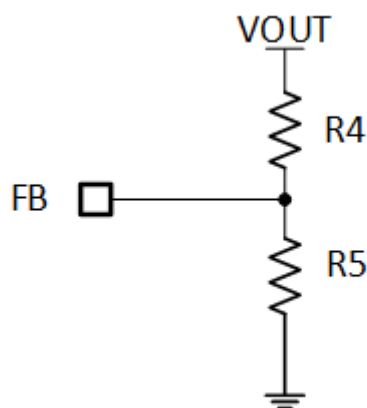


Figure 34 Setting OUV in ACM

To set the minimum allowed output voltage, choose $R4$ around 100K Ω , then calculate $R5$:

$$R5 = \frac{V_{REF} * R4}{OUV - V_{REF}}$$

Equation 10

where OUV is the minimum allowed output voltage.

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5.4 Setting the Voltage at MODE1/0 pins in AADM

To set the desired voltage at the MODE1/0 pins, choose the resistor from corresponding pin to GND by dividing desired voltage over pin current ($100 \mu\text{A} \pm 7\%$).

Due to the wide voltage range, 5% tolerance resistors can be used:

Table 32 Setting MODEx pins voltage

Voltage (V)	MODE1/0 pin resistor (k Ω)
1.2	12
2.0	20

5.5 Setting the Voltage at ADDR1/0 pins

To set the voltage at the ADDR1/0 pins, choose the resistor from corresponding pin to GND by dividing desired voltage over pin current ($100 \mu\text{A} \pm 7\%$).

Due to the wide voltage range, 5% tolerance resistors can be used:

Table 33 Setting ADDRx pins voltage

Voltage (V)	ADDR1/0 pin resistor (k Ω)
1.2	12
2.0	20

5.6 Handling external current at VREG pin

An internal LDO provides 5 V (typically) supply for the internal circuitry and could also be used as voltage reference for communication pull-up resistors.

Its current capability to supply external circuitry is 10 mA. Make sure not to exceed the package maximum power dissipation P_{PAK} .

To calculate the additional power due to external load:

$$P_{\text{REG_EXT}} = \text{ABS}(V_{\text{DD_VIN}} - V_{\text{REG}}) * i_{\text{REG}}$$

Equation 11

So, in the case of a -48 V input application (where $V_{\text{DD_VIN}} = 48 \text{ V}$ with respect to the input voltage), with a 10 mA load on $V_{\text{REG}} = 5 \text{ V}$:

$$P_{\text{REG_EXT}} = \text{ABS}(48\text{V} - 5\text{V}) * 10\text{mA} = 430\text{mW}$$

Equation 12

The rest of current consumption comes from controller's circuitry.

To keep the package power dissipation within the P_{PAK} limit and allow additional consumption due to external load of LDO, a shunt resistor may be required at the $V_{\text{DD_VIN}}$ pin in high input voltage applications. It helps not to exceed the P_{PAK} limit:

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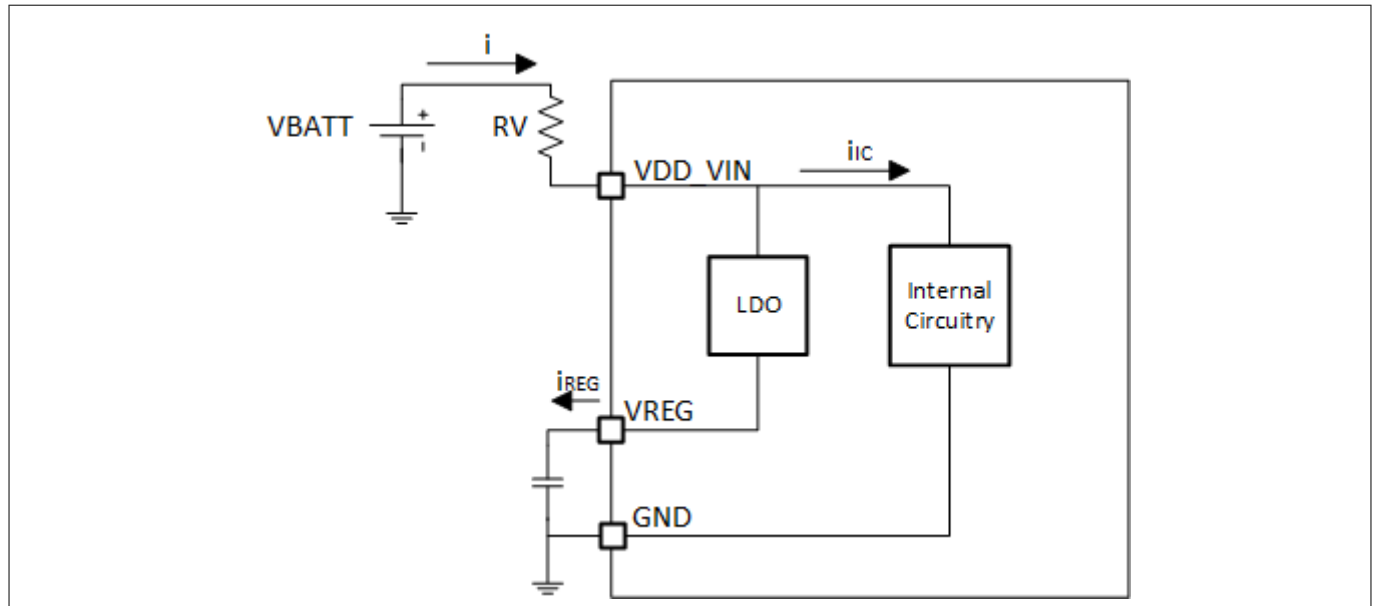


Figure 35 Handling external current at VREG pin

To calculate RV:

$$RV = \frac{P_{TOT} - P_{PAK}}{i^2} = \frac{VBATT}{i} - \frac{V_{REG} \times i_{REG} + P_{PAK}}{i^2}$$

Equation 13

where:

$$P_{TOT} = VBATT \times i - V_{REG} \times i_{REG}$$

Equation 14

and $P_{PAK} = 0.8 \text{ W}$, $V_{REG} = 5 \text{ V}$ (typically), i_{REG} is the expected current consumption of the external circuitries supplied by VREG and i is the expected current consumption of the whole device supplied by VBATT.

So, for an expected maximum internal current consumption (i_{IC}) of 10 mA:

$$i = i_{IC} + i_{REG} = 10\text{mA} + 10\text{mA} = 20\text{mA}$$

Equation 15

$$RV = \frac{VBATT}{i} + \frac{V_{REG} \times i_{REG} + P_{PAK}}{i^2} = \frac{48\text{V}}{20\text{mA}} - \frac{5\text{V} \times 10\text{mA} + 0.8\text{W}}{(20\text{mA})^2} = 275\Omega$$

Equation 16

The power dissipated by the resistor is:

$$P_{RV} = i^2 \times RV = (20\text{mA})^2 \times 275\Omega = 0.11\text{W}$$

Equation 17

Note: A negative result in the calculation of the resistance RV means that the total power dissipation of the package P_{PAK} is not being exceeded. In this case, RV is not needed.

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To protect XDP710, if the die temperature goes above $163 \pm 10^\circ\text{C}$, VREG is turned off. Thus, communication is not possible and the status of FAULT, WARN, PWRGD and GPOs is not reliable.

5.7 ISNS input filter

In noisy or high dV/dt applications, an input filter from RSNS to ISNS_P and ISNS_N pins is recommended as shown in the following figure.

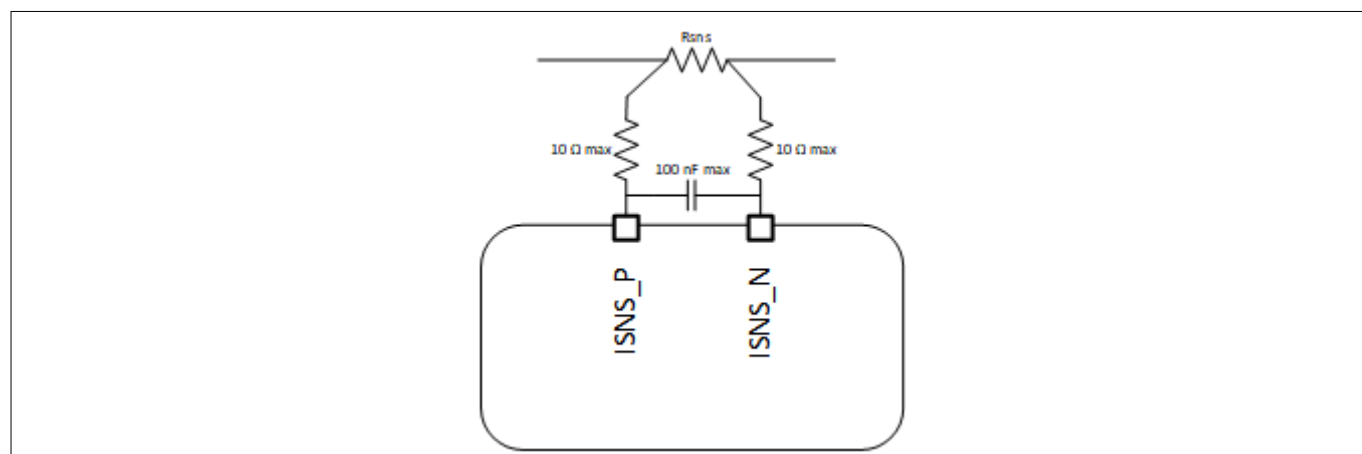


Figure 36 ISNS input filter

5.8 FET selection considerations

Due to the increased gate current of Infineon's Linear FET over 125°C , its compatibility with XDP710 is limited to this temperature level. Make sure that the junction temperature of the Linear FET does not exceed this value and that the corresponding temperature protections are set accordingly.

When selecting a FET, the following guidelines must be observed:

- Plateau voltage of the FET must be lower than XDP710 detection level of enhancement (7.8 V typically).
- SOA of the FET and system input voltage will determine the current with which the output capacitor will be charged, thus, the start-up time. Wide SOA will translate into faster start-up time. If a specific start-up time is required, care must be taken to select a FET with an SOA that allows it.
- Control loop's resolution, or, in other words, minimum current regulation capability is 0.5 A. Any FET's target I_{SOA} values lower than this value will be rounded up. Therefore, if, for example, a specific FET's SOA specifies a maximum current I_D of 0.25 A at a V_{DS} of 48 V, the current is regulated to 0.5 A and the SOA is violated. It is recommended for the FET to withstand a minimum current of 0.5 A at any point of its SOA. Alternatively, Boost Mode can be used to turn on weak FETs.
- If multiple FETs in parallel are used, their SOA must not be divided by the number of FETs, but single FET SOA must be programmed. Paralleling must be considered to reduce R_{dson} only.
- IREG feature must be disabled when using Linear FET in the system. In other words, SOAR_TMR must be set to 0.
- At FET power up, the V_{gs} control by the loop might be affected by reaching FET's plateau level, but FET's current continues to be limited as well as SOA target follows FET's V_{ds} . This can be more pronounced with LinearFETs. For LinearFETs, it is recommended to set start-up current limit IST in the way that V_{gs} is below plateau level at the end of regulation phase. It will ensure a smooth start-up behavior. The same is valid for OC level with standard FETs to ensure proper current regulation.
- Low Z_{thjc} helps with power dissipation during linear mode.
- Low zero temperature coefficient (ZTC) point avoids staying in thermal instability region for too long.

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5.9 Calculating PMBus direct format limits from "real world" values and vice-versa

Voltage

Voltage limits calculations are straight forward using the formulas and coefficients specified in . As an example, the VIN_OV_FAULT_LIMIT is taken.

System characteristics and configuration:

VTLM_RNG = 88 V

Based on VTLM_RNG value, from the coefficients table:

$m = 4653$

$b = 0$

$R = -2$

For a VIN_OV_FAULT_LIMIT of 64 V, the following formula is applied:

$$Y = (mX + b) * 10^R$$

Equation 18

$$Y = (4653 * 64 + 0) * 10^{-2}$$

Equation 19

$$Y = 2978 = 0xBA2$$

Equation 20

So the value to be programmed in VIN_OV_FAULT_LIMIT is 0xBA2.

To convert from PMBus direct format to "real world" value, let's suppose the value from the ADC in the READ_VIN command is 0x8B9 = 2233 decimal. System characteristics, configuration and coefficients are the same as above. The following formula is applied:

$$X = \frac{1}{m} * (Y * 10^{-R} - b)$$

Equation 21

$$X = \frac{1}{4653} * (2233 * 10^2 - 0)$$

Equation 22

$$X = 48V$$

Equation 23

Current

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Values in Table 29 are normalized to a 1 mΩ resistor. Therefore, to convert to a PMBus direct format value, result has to be divided over the value of the sense resistor in mΩ. And to convert to a "real world" value, the result must be multiplied. For example, if a value of 42 A is desired for IOUT_OC_WARN_LIMIT:

System characteristics and configuration:

$R_{sns} = 0.5 \text{ m}\Omega$

$V_{SNS_CS} = 12.5 \text{ mV}$

Based on V_{SNS_CS} value, the coefficients are:

$m = 23165$

$b = 0$

$R = -2$

To get the limit value, the following formula is applied:

$$Y = ((mX + b) * 10^R) * R_{sns}(m\Omega)$$

Equation 24

$$Y = ((23165 * 42 + 0) * 10^{-2}) * 0.5$$

Equation 25

$$Y = 9729 * 0.5$$

Equation 26

$$Y = 4865 = 0x1301$$

Equation 27

So the value 0x1301 must be programmed in IOUT_OC_WARN_LIMIT.

Similarly, to obtain the "real world" value from the ADC reading in READ_IOUT. Let's suppose the reading is 0x910 = 2320 decimal. The following formula is applied:

$$X = \frac{\frac{1}{m} * (Y * 10^{-R} - b)}{R_{sns}(m\Omega)}$$

Equation 28

$$X = \frac{\frac{1}{23165} * (2320 * 10^2 - 0)}{0.5}$$

Equation 29

$$X = \frac{10}{0.5} = 20A$$

Equation 30

READ_IOUT_RMS is a 16 bit field, so coefficients are different:

$m = 20808$

$b = 0$

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R = -2

If the ADC reading is 0x1048 = 4168 decimal, the "real world" value is obtained as follows:

$$X = \frac{\frac{1}{20808} * (4168 * 10^{-2} - 0)}{0.5}$$

Equation 31

$$X = \frac{20}{0.5} = 40A^2$$

Equation 32**Power**

Input power is the result of multiplying input voltage times the current. Power coefficients are also normalized to 1 mΩ, so it is also necessary to multiply or divide by the sense resistor value in mΩ to obtain direct format or "real world" values respectively.

If a 1100 W value is desired as PIN_OP_WARN_LIMIT:

System characteristics and configuration:

VTLM_RNG = 88 V

Rsns = 0.5 mΩ

V_{SNS_CS} = 12.5 mV

Based on these, coefficients are:

m = 4211

b = 0

R = -2

To obtain the limit, the following formula is applied:

$$Y = ((mX + b) * 10^R) * Rsns(m\Omega)$$

Equation 33

$$Y = ((4211 * 1100 + 0) * 10^{-2}) * 0.5$$

Equation 34

$$Y = 23159 = 0x5A77$$

Equation 35

So the value 0x5A77 must be programmed in PIN_OP_WARN_LIMIT.

The power reading can be 16 bits (READ_PIN) or 24 bits (READ_PIN_EXT). In the case of READ_PIN, coefficients are the same as specified for PIN_OP_WARN_LIMIT. So, if the reading of READ_PIN is 0xCD9A = 52634 decimal, the following formula is applied:

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$$X = \frac{\frac{1}{m} * (Y * 10^{-R} - b)}{Rsns(m\Omega)}$$

Equation 36

$$X = \frac{\frac{1}{4211} * (52634 * 10^2 - 0)}{0.5}$$

Equation 37

$$X = 2500W$$

Equation 38

If 24 bits power reading is desired (READ_PIN_EXT), corresponding coefficients based on the system characteristics and configuration specified above are:

$m = 10780$

$b = 0$

$R = 0$

For an example reading of 0xB4EE53 = 11857491 decimal, the formula becomes:

$$X = \frac{\frac{1}{10780} * (11857491 * 10^0 - 0)}{0.5}$$

Equation 39

$$X = 2200W$$

Equation 40**Temperature**

Temperature calculation is straight forward too and it only requires to apply the coefficients to the formulas. If an OT_FAULT_LIMIT of 150°C is desired, the corresponding coefficients are:

$m = 52$

$b = 14321$

$R = -1$

By applying the direct format formula, the following is obtained:

$$Y = (mX + b) * 10^R$$

Equation 41

$$Y = (52 * 150 + 14321) * 10^{-1}$$

Equation 42

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$$Y = 2212 = 0x8A4$$

Equation 43

So the value 0x8A4 must be programmed in OT_FAULT_LIMIT.

Note: OT_FAULT_LIMIT can be programmed from -273°C (0x000) to 512°C (0xFFFF). Care must be taken to program it within the FET operating temperature range.

The reading from READ_TEMPERATURE_1 is translated to "real world" by solving the equation for X. If the reading is 0x7A0 = 1952 decimal:

$$X = \frac{1}{m} * (Y * 10^{-R} - b)$$

Equation 44

$$X = \frac{1}{52} * (1952 * 10^1 - 14321)$$

Equation 45

$$X = 100^{\circ}C$$

Equation 46

Energy

Energy is calculated based on 16 bits power, therefore, the same coefficients shall be used. Two readings of the READ_EIN register are required. Since energy is power times time, it is also required to know the time between the samples.

In the following example, system characteristics and configuration are:

VTLM_RNG = 88 V

Rsns = 0.5 mΩ

V_{SNS_CS} = 12.5 mV

Based on these, from [Table 29](#), coefficients are:

m = 4211

b = 0

R = -2

The samples read are:

Table 34 **Energy read samples**

	First Sample		Second Sample	
	Hex	Dec	Hex	Dec
SAMPLE_COUNT	1000	4096	3FFF	16383

(table continues...)

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Table 34 (continued) Energy read samples

ROLLOVER_COUNT	10	16	FF	255
ENERGY_COUNT	01FF	511	1FAC	8108

And the time between the samples for this example is 1200ms.

First, the power difference shall be calculated by subtracting the ENERGY_COUNT of the first sample from the second sample. Note that the ENERGY_COUNT is concatenated with the ROLLOVER_COUNT:

$$\text{Power difference} = 0xFF1FAC - 0x1001FF = 0xEF1DAD$$

Equation 47

Next step is to calculate the SAMPLE_COUNT difference by subtracting the SAMPLE_COUNT of both samples:

$$\text{Sample count difference} = 0x3FFF - 0x1000 = 0x2FFF$$

Equation 48

Then the average power per sample is calculated by dividing the power difference over the sample count difference:

$$\text{Average power} = \frac{0xEF1DAD}{0x2FFF} = 0x4FB = 1275d$$

Equation 49

Now X can be determined by using the PMBus direct format formula:

$$X = \frac{\frac{1}{m} * (Y * 10^{-R} - b)}{Rsns(m\Omega)}$$

Equation 50

$$X = \frac{\frac{1}{4211} * (1275 * 10^2 - 0)}{0.5}$$

Equation 51

$$X = 60.55W$$

Equation 52

5 Application Information

Finally, energy is determined by multiplying power times time:

$$E = 60.55W * 1.2s$$

Equation 53

$$E = 36.33J$$

Equation 54**5.10 Layout guidelines**

The following guidelines shall be followed when designing an XDP710 PCB:

- Maximum supply current of the XDP710 is 10mA. The traces at supply pin VDD_VIN don't need to be that thick.
- VREG capacitor must be placed right next to the VREG pin. - I2C traces need a single-ended controlled impedance of 50 Ω. Therefore their width must be adjusted accordingly. - TSNS filter capacitor must be placed right next to the TSNS pins.
- If used, TSNS BJT shall be placed right next to the FET or to the point to be sensed. It is best to place the sensor next to the hottest part of the FET package. In the case of our D2PAK FETs, the die is attached to the drain pad on bottom of the package, so this is the section that will get hotter in case of high power dissipation.
- Keep gate trace as short as possible in order to reduce parasitics. This trace and the source one must be able to handle 1.5 A current, which is the current that will flow through them in order to discharge the gate of the FET in case of a fast turn-off event.
- ISNS filter capacitor also has to be placed right next to the ISNS pins. - Exposed pad must have a solid connection to GND through many vias.
- The path that will need to handle the highest amount of current goes from the input voltage source, through the sense resistor, FET and output capacitor to the load, including its corresponding return path to ground. Make sure this path is robust enough to support the current level required by the system.
- ISNS lines must be connected directly to sense pins of the sense resistor, separately from the power plane. - Connect SOURCE pin directly to the source of the FET, separate from Vout plane. This can be a thin trace. VOUT pin can be connected with a thin trace directly to the Vout plane.

6 Ordering information

6 Ordering information

Table 35 Ordering information

Basic part number	Orderable part number	Description
XDP710-001	XDP710001XUMA1	Positive input voltage hot-swap controller.

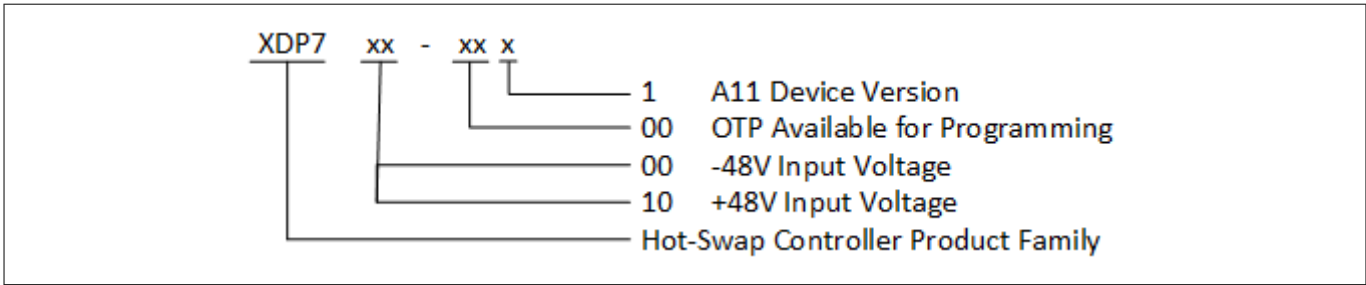


Figure 37

7 Revision history

Revision	Date	Subjects (major changes since last revision)
2.0	2022-11-22	First release.

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Edition 2022-11-22

Published by

Infineon Technologies AG
81726 Munich, Germany

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Document reference
IFX-jnf1668526912102

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