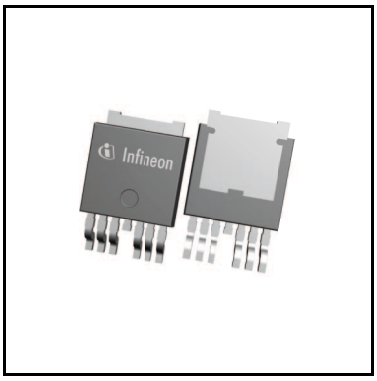
OPTIREG™ linear TLS850F3TUV50

Low dropout linear voltage regulator with watchdog and reset



Features

- Output voltage 5 V ±2%
- Current capability 500 mA
- Input voltage range from 3 V to 42 V
- Stable with 1 µF ceramic output capacitor
- Ultra low current consumption: typically 26 µA
- Very low drop out voltage: typically 300 mV at 250 mA
- Watchdog circuit for monitoring a microprocessor
- Watchdog inhibit
- Output voltage supervision by reset circuit:
  - Programmable delay time
- Output current limitation
- Overtemperature shutdown
- Green Product (RoHS compliant)

Potential applications

- Automotive general ECUs
- Telematics systems
- ADAS cameras and radar systems
- Navigation systems
- Body control modules

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLS850F3TUV50 is a high performance low drop out fixed output voltage regulator in a PG-TO252-7 package. With an input voltage range of 3 V to 42 V and very low quiescent current of only 26 µA, these regulators are perfectly suitable for automotive systems or other supply systems connected to the battery permanently. The TLS850F3TUV50 provides an output voltage accuracy of ±2% and a maximum output current of 500 mA.

The loop concept combines fast regulation and very good stability while requiring only one small ceramic capacitor of 1 µF at the output. The operating range starts already at an input voltage of only 3 V (extended operating range). This makes the TLS850F3TUV50 also suitable to supply automotive systems that need to operate during cranking condition.

The **Reset** supervises the output voltage, including undervoltage reset and delay reset at power-on.

An integrated **Watchdog** circuit with adjustable timing monitors the microcontroller's operation. A shared external delay capacitor sets both reset timing and watchdog timing.

Internal protection features such as output current limitation and overtemperature shutdown are implemented to protect the device against immediate damage due to failures such as output short circuit to GND, overcurrent and overtemperature.

Type	Package	Marking
TLS850F3TUV50	PG-TO252-7	850F3V5

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1 Block diagram

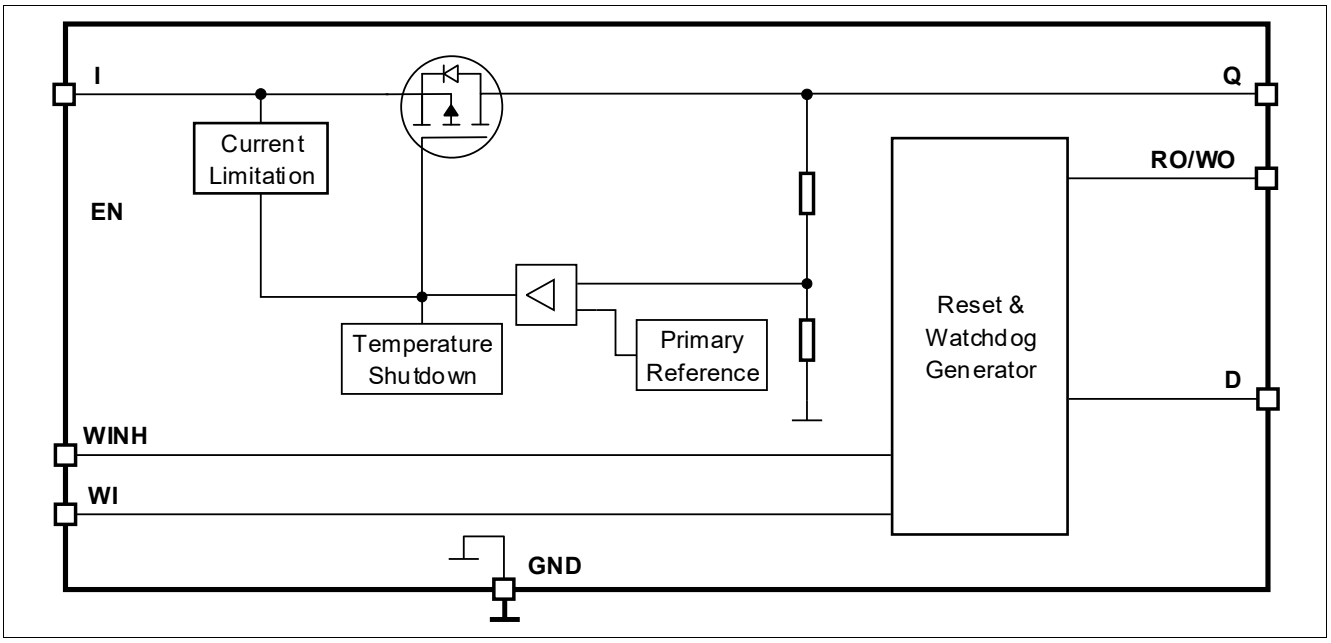


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

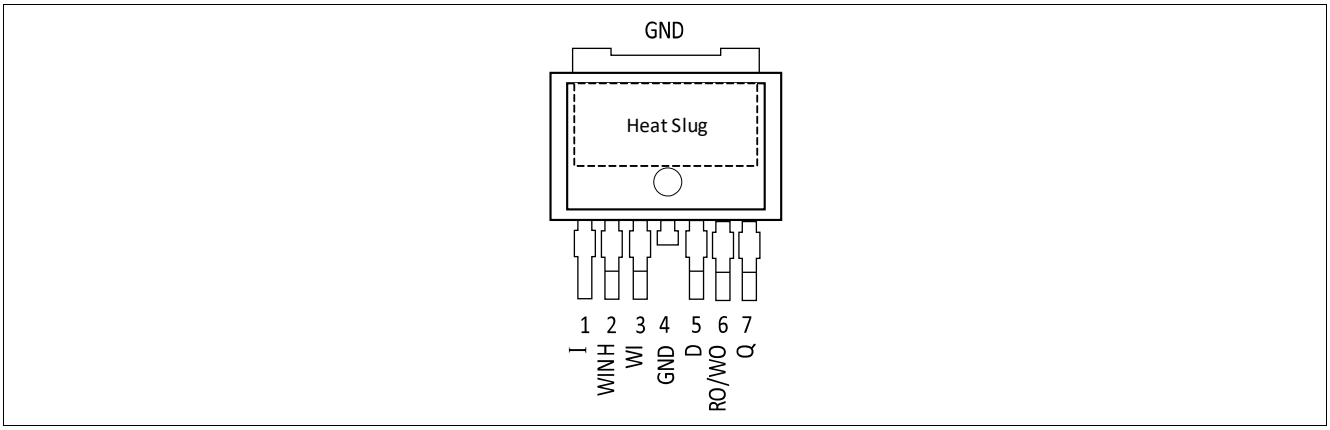


Figure 2 Pin assignment PG-TO252-7

2.2 Pin definitions and functions

Pin	Symbol	Function
1	I	**Input** It is recommended to connect a small ceramic capacitor from this pin to GND, close to the pins, in order to compensate line influences.
2	WINH	**Watchdog inhibit input** “Low” activates the watchdog function. “High” deactivates the watchdog function. This pin has an integrated pull-down resistor.
3	WI	**Watchdog input** Serve watchdog with trigger input signal (usable for microcontroller monitoring). This pin has an integrated pull-down resistor.
4	GND	**Ground**
5	D	**Delay input** Connect an external capacitor from this pin to GND to set reset timing and watchdog timing. If no capacitor is placed, then disable the watchdog.
6	RO/WO	**Reset output/Watchdog output** This pin has an integrated pull-up resistor to Q. It is an open collector output. If the reset and watchdog functions are not needed, then leave this pin open.
7	Q	**Regulator output** Connect the output capacitor C_Q from this pin to GND close to the pin, respecting the values specified for its capacitance and ESR in **Functional range**.
Pad	–	**Exposed pad** Connect the exposed pad to a heatsink area. Connect the exposed pad to GND.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage rating							
Input voltage I	V_I	-0.3	–	45	V	–	P_3.1.15
Output voltage Q	V_Q	-0.3	–	7	V	–	P_3.1.16
Reset output RO/WO	$V_{RO/WO}$	-0.3	–	7	V	–	P_3.1.17
Delay voltage D	V_D	-0.3	–	7	V	–	P_3.1.18
Watchdog input WI	V_{WI}	-0.3	–	7	V	–	P_3.1.19
Watchdog inhibit WINH	V_{WINH}	-0.3	–	7	V	–	P_3.1.20
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_3.1.21
Storage temperature	T_{stg}	-55	–	150	°C	–	P_3.1.22
ESD robustness							
ESD robustness to GND	$V_{ESD,HBM}$	-2	–	2	kV	[2)] HBM all pins	P_3.1.23
ESD robustness to GND	$V_{ESD, CDM}$	-500	–	500	V	[3)] CDM all pins except 1, 7	P_3.1.24
ESD robustness pins 1, 7 to GND	V_{ESD}	-750	–	750	V	[3)] CDM	P_3.1.25

1) Not subject to production test, specified by design.
2) Human body model (HBM) robustness according to AEC-Q100-002.
3) Charged device model (CDM) robustness according to AEC-Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*
3. *Latchup robustness: class II according to AEC - Q100-04.*

3.2 Functional range

Table 2 Functional range

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	$V_{Q,nom}$ + V_{dr}	–	42	V	1)	P_3.2.1
Extended input voltage range	$V_{I(ext)}$	3	–	42	V	2)	P_3.2.2
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.4
Output capacitance for stable operation	C_Q	1	–	–	µF	3)4)	P_3.2.5
ESR of output capacitor	ESR_{CQ}	–	–	20	Ω	4)5)	P_3.2.6

1) See the values of output voltage V_Q and drop out voltage V_{dr}, in **Voltage regulator**.
2) The output voltage V_Q follows the input voltage, but is outside the specified range, see **Voltage regulator**.
3) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
4) Not subject to production test, specified by design.
5) Relevant ESR value at f = 10 kHz.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	3	–	K/W	1)	P_3.3.6
Junction to ambient	R_{thJA}	–	112	–	K/W	1)2) Footprint only	P_3.3.7
Junction to ambient	R_{thJA}	–	66	–	K/W	1)2) 300 mm² heatsink area on PCB	P_3.3.8
Junction to ambient	R_{thJA}	–	50	–	K/W	1)2) 600 mm² heatsink area on PCB	P_3.3.9
Junction to ambient	R_{thJA}	–	30	–	K/W	1)3) 2s2p PCB	P_3.3.10

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board; The Product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 inner copper layer (1 × 70 µm Cu).

3) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4 Block description and electrical characteristics

4.1 Voltage regulator

A resistor network divides the output voltage V_Q. The device compares this fractional voltage to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the following factors:

- Output capacitor
- Load current I_Q
- Chip temperature T_j
- Internal circuit design

Output capacitor

To ensure stable operation, the capacitance of the output capacitor C_Q and its equivalent series resistor ESR_{CQ} requirements must be maintained, see **Functional range**. The output capacitor must be sized according to the requirements of the application, for example to buffer steps in the load current I_Q.

Input capacitors, reverse polarity protection diode

An input capacitor C_I is recommended to compensate line influences. In order to block influences, such as pulses and high frequency distortion at the input, use a reverse polarity protection diode and a combination of several capacitors. Connect the capacitors close to the component's terminals.

Smooth ramp-up

In order to prevent overshoot during startup, a smooth ramp-up function is implemented. This ensures a reduced output voltage overshoot during startup, mostly independent from load and output capacitor.

Output current limitation

Due to a short circuit or overload condition the load current can exceed the specified limit. In this case the device limits the output current and the output voltage decreases.

Overtemperature shutdown

The overtemperature shutdown circuit prevents the device from immediate destruction in case of a fault condition, for example due to a permanent short circuit at the output. In such a condition the overtemperature shutdown circuit switches off the device. After the device cools down, the regulator restarts. This leads to an oscillatory behavior of the output voltage V_Q. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the lifetime of the device.

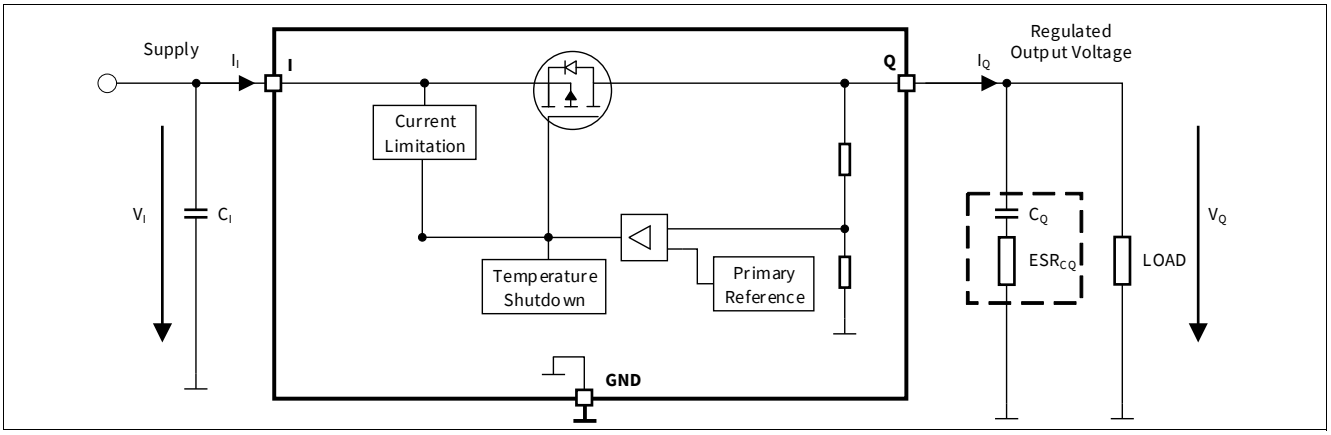


Figure 3 Functional block diagram voltage regulator circuit

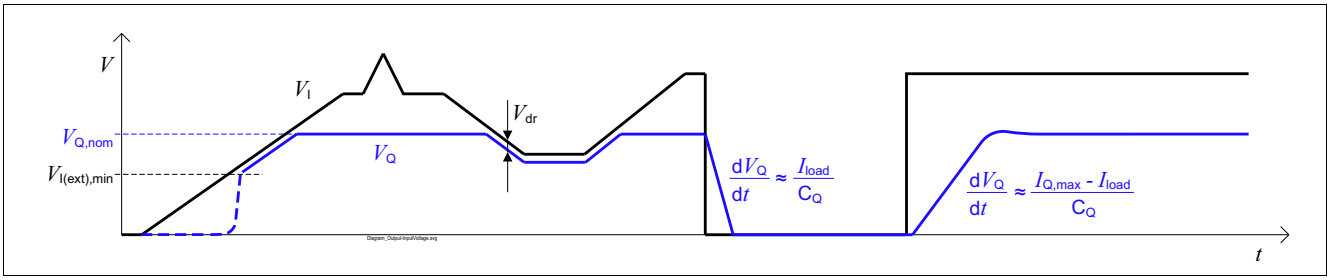


Figure 4 Output voltage versus input voltage

4.1.1 Electrical characteristics voltage regulator

Table 4 Electrical characteristics voltage regulator

V_I = 13.5 V; T_j = -40°C to 150°C; all voltages with respect to ground, direction of currents as shown in **Figure 3** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	50 µA ≤ I_Q ≤ 200 mA; $V_{Q,nom}$ + V_{dr} ≤ V_I ≤ 42 V	P_4.1.1
Output voltage accuracy	V_Q	4.9	5.0	5.2	V	I_Q ≤ 50 µA; $V_{Q,nom}$ + V_{dr} ≤ V_I ≤ 42 V	P_4.1.5
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	50 µA ≤ I_Q ≤ 500 mA; $V_{Q,nom}$ + V_{dr} ≤ V_I ≤ 28 V	P_4.1.8
Output voltage startup slew rate	$\Delta V_Q/\Delta t$	7	–	70	V/ms	$\Delta V_I/\Delta t$ = 50 V/ms; C_Q = 1 µF; 0.5 V ≤ V_Q ≤ 4.5 V	P_4.1.10
Load regulation steady state	$\Delta V_{Q,load}$	–15	-5	5	mV	I_Q = 0.05 mA to 500 mA; V_I = 6.5 V	P_4.1.13
Line regulation steady state	$\Delta V_{Q,line}$	–5	1	10	mV	V_I = 8 V to 32 V; I_Q = 5 mA	P_4.1.14
Power supply ripple rejection	*PSRR*	–	60	–	dB	[2] f_{ripple} = 100 Hz; V_{ripple} = 0.5 V_{pp}; I_Q=10 mA	P_4.1.15

Table 4 Electrical characteristics voltage regulator (cont'd)

V_I = 13.5 V; T_j = -40°C to 150°C; all voltages with respect to ground, direction of currents as shown in **Figure 3** (unless otherwise specified)

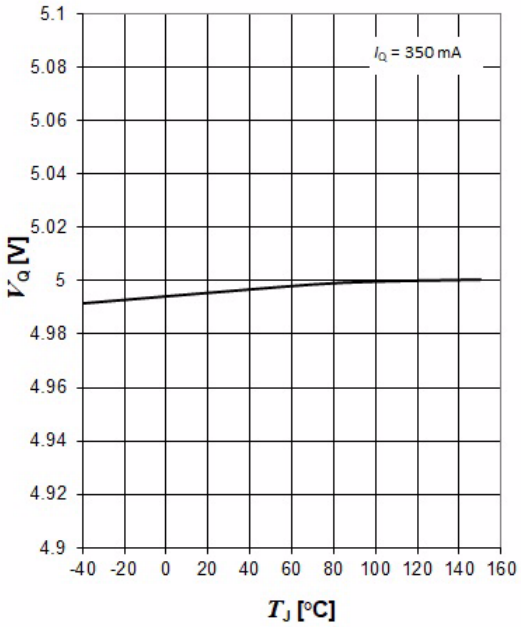
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	125	350	mV	1) I_Q = 100 mA	P_4.1.21
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	300	750	mV	1) I_Q = 250 mA	P_4.1.22
Output current limitation	$I_{Q,max}$	501	700	1100	mA	0 V ≤ V_Q ≤ $V_{Q,nom}$ - 0.1 V	P_4.1.26
Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	°C	2) T_j increasing	P_4.1.27
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	2) T_j decreasing	P_4.1.28

1) Measured when the output voltage V_Q has dropped 100 mV from its nominal value obtained at V_I = 13.5 V.

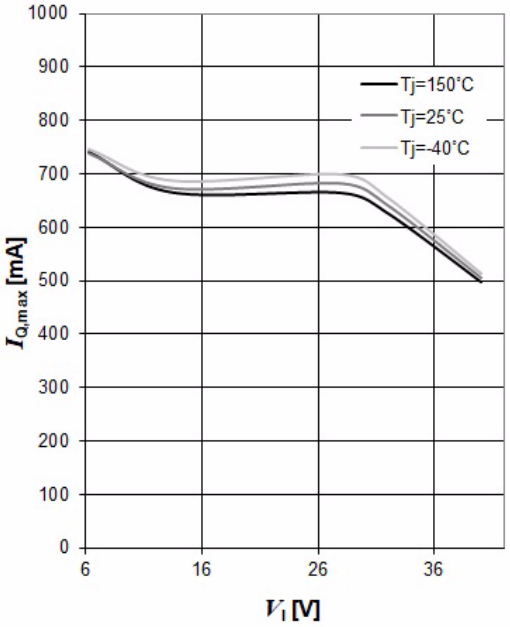
2) Not subject to production test, specified by design.

4.1.2 Typical performance characteristics voltage regulator

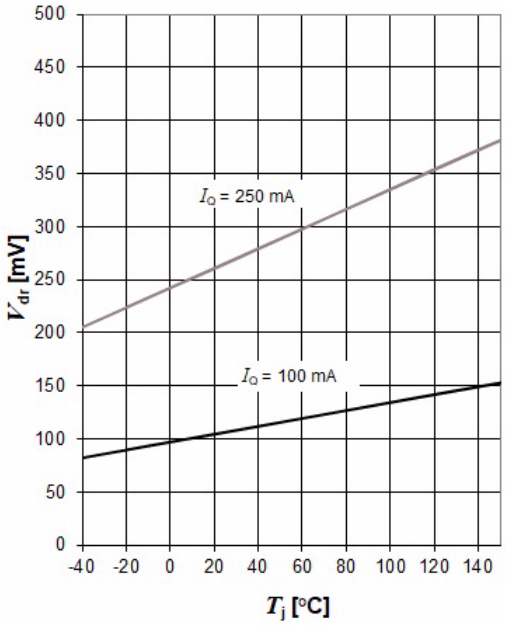
Output voltage V_Q versus junction temperature T_j



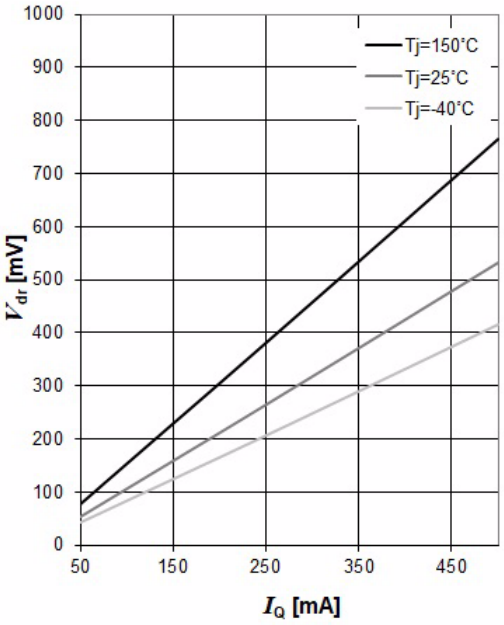
Output current limitation I_{Qmax} versus input voltage V_I



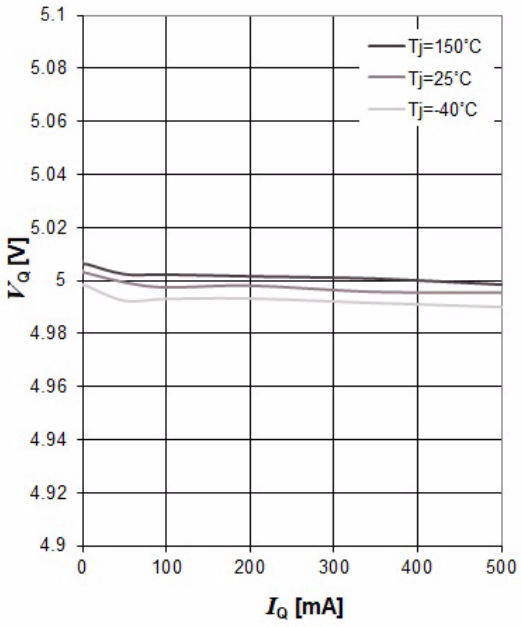
Dropout voltage V_{dr} versus junction temperature T_j



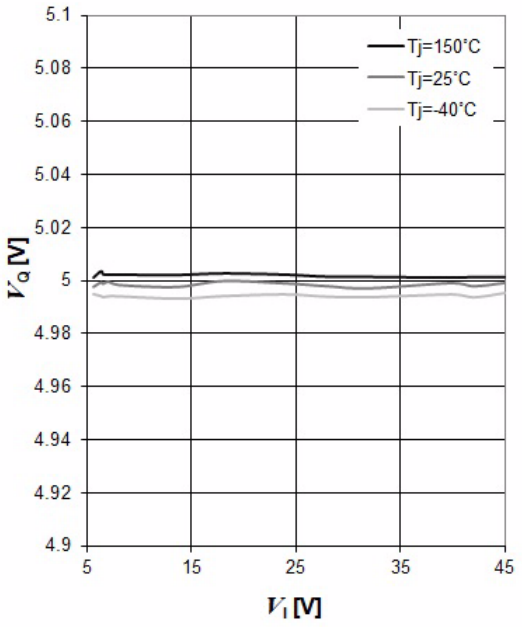
Dropout voltage V_{dr} versus output current I_Q



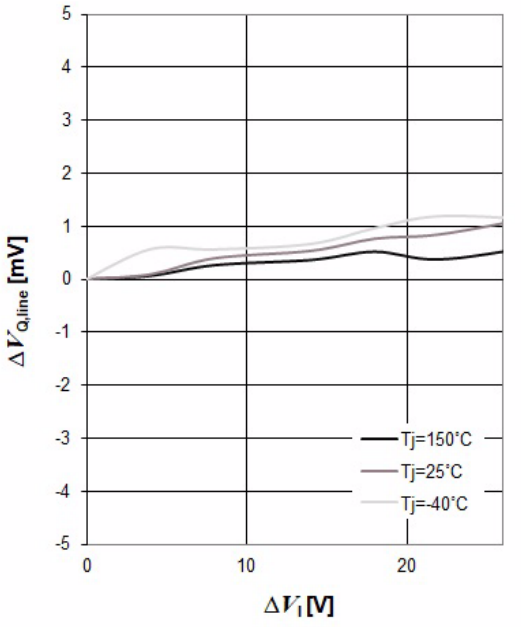
Output voltage V_Q versus output current I_Q



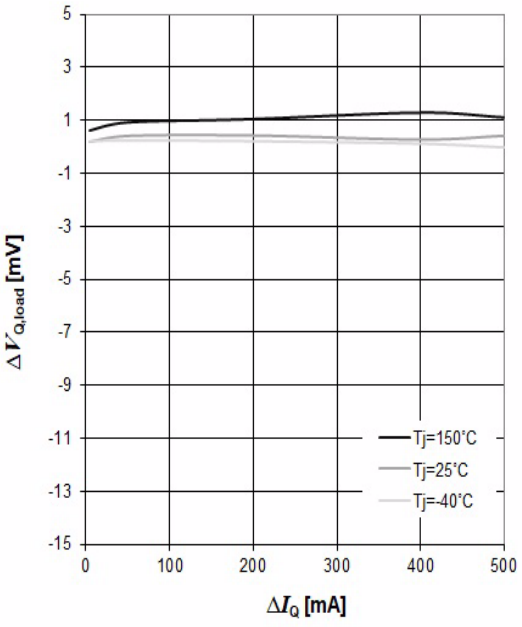
Output voltage V_Q versus input voltage V_I



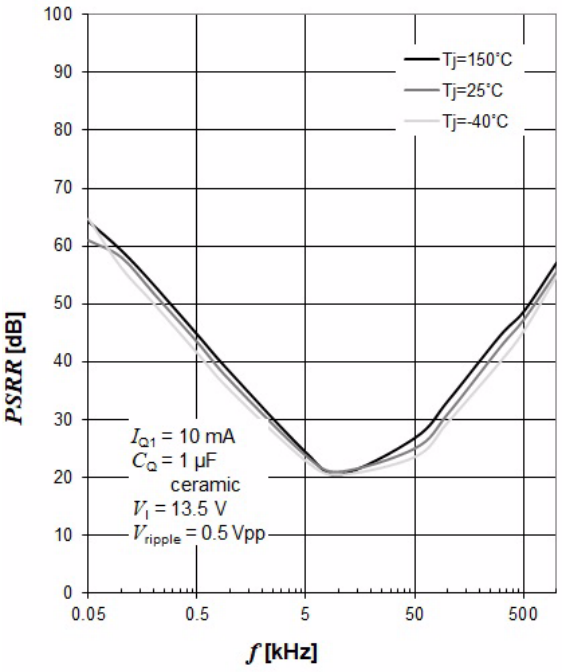
Line regulation $\Delta V_{Q,line}$ versus input voltage change ΔV_I



Load regulation $\Delta V_{Q,load}$ versus output current change ΔI_Q



Power supply ripple rejection *PSRR* versus frequency *f*



4.2 Current consumption

Table 5 Electrical characteristics current consumption

V_I = 13.5 V, T_j = -40°C to 150°C; all voltages with respect to ground; direction of currents see **Figure 5** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I - I_Q$	I_q	–	23	35	µA	I_Q = 50 µA; T_j = 25°C; watchdog disabled	P_4.2.4
Current consumption $I_q = I_I - I_Q$	I_q	–	26	43	µA	I_Q = 50 µA; $T_j \leq$ 125°C; watchdog disabled	P_4.2.5
Current consumption $I_q = I_I - I_Q$	I_q	–	29	51	µA	I_Q = 50 µA; $T_j \leq$ 150°C; watchdog disabled	P_4.2.6
Current consumption $I_q = I_I - I_Q$	I_q	–	26	39	µA	I_Q = 50 µA; T_j = 25°C; watchdog enabled	P_4.2.7
Current consumption $I_q = I_I - I_Q$	I_q	–	30	47	µA	I_Q = 50 µA; $T_j \leq$ 125°C; watchdog enabled	P_4.2.8
Current consumption $I_q = I_I - I_Q$	I_q	–	33	55	µA	I_Q = 50 µA; $T_j \leq$ 150°C; watchdog enabled	P_4.2.9
Current consumption $I_q = I_I - I_Q$	I_q	–	33	55	µA	[1] I_Q = 500 mA ; $T_j \leq$ 125°C; watchdog enabled	P_4.2.11

1) Not subject to production test, specified by design.

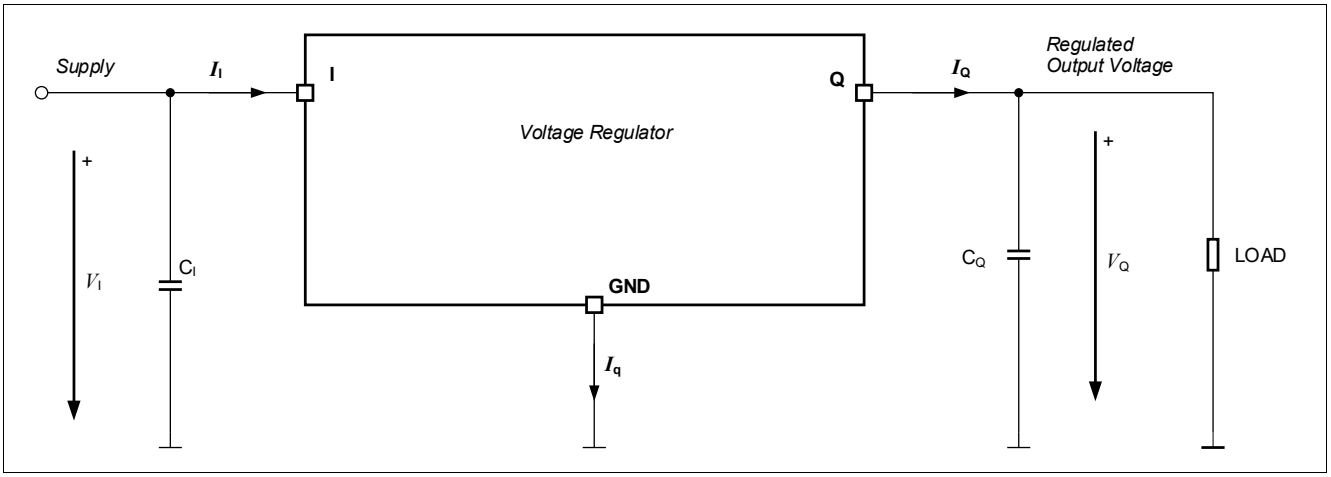
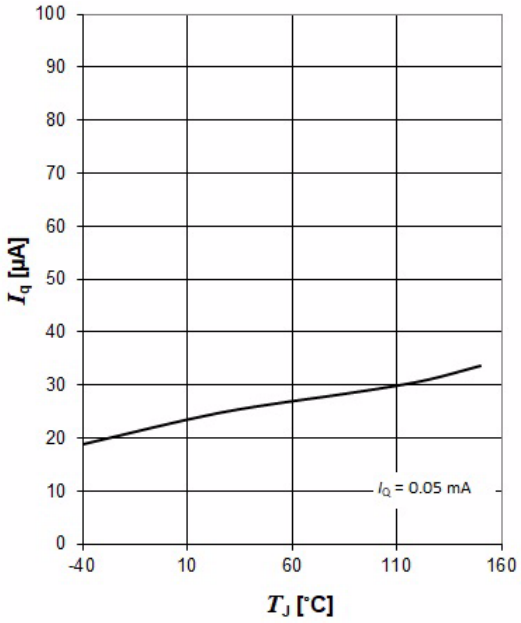


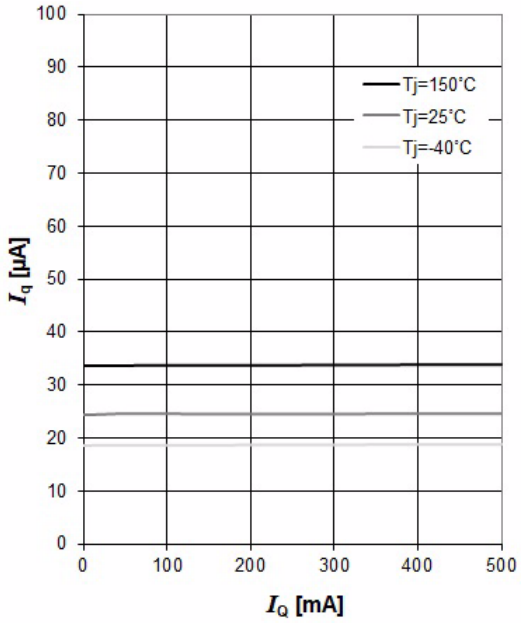
Figure 5 Parameter definition

4.2.1 Typical performance characteristics current consumption

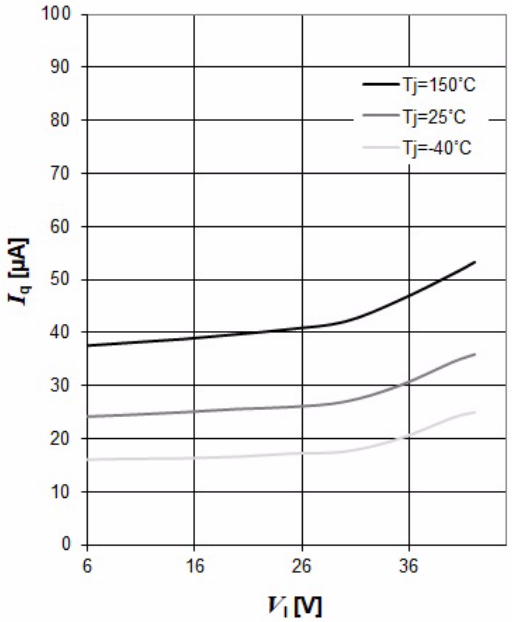
Current consumption I_q versus junction temperature T_j



Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I



4.3 Reset

The reset function monitors the output voltage V_Q. It allows a connected system or microcontroller to react to an imminent loss of power. To meet the requirements of the application, some reset related parameters can be adjusted by measures described below.

Output undervoltage reset event

If V_Q drops below the output undervoltage reset lower switching threshold $V_{RT,low}$, then the device detects an output undervoltage event and sets the reset output pin RO/WO to “low”. This signal can be used to reset a microcontroller, which is supplied by V_Q.

Reset reaction time

If the output voltage of the regulator drops below the output undervoltage reset lower switching threshold $V_{RT,low}$, then the delay capacitor C_D discharges with the discharge current $I_{DR,dsch}$. As soon as the delay capacitor’s voltage V_D reaches the lower delay switching threshold $V_{DR,lo}$, then the device sets the reset output RO/WO to “low”. The time from V_Q dropping below $V_{RT,low}$ and the transition of the reset output RO/WO to “low” is the total reset reaction time $t_{rr,total}$.

The total reset reaction time $t_{rr,total}$ is related to the delay capacitor discharge time $t_{rr,d}$ and the internal reaction time $t_{rr,int}$:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \quad (4.1)$$

with

- $t_{rr,total}$: Total reset reaction time
- $t_{rr,int}$: Internal reset reaction time, see **Internal reset reaction time**
- $t_{rr,d}$: Delay capacitor discharge time. For C_D = 10 nF see value specified in **Delay capacitor discharge time**.

If the output voltage drop lasts shorter than the reset blanking time $t_{rr,blank}$, then the delay capacitor does not discharge and the device does not set the reset output RO/WO to “low”. The reset blanking time prevents unintentional microcontroller reset due to very short distortion of the output voltage, see **Timing diagram reset**.

Power-on reset delay time

Before startup of the regulator or after an undervoltage reset event, the delay capacitor C_D discharges. If the output voltage of the regulator exceeds the output undervoltage reset upper switching threshold $V_{RT,hi}$, then this triggers the charging cycle of C_D. C_D is charged with the delay capacitor charge current $I_{D,ch}$. If V_D reaches the higher delay switching threshold $V_{DR,hi}$, then the device sets the reset output RO/WO to “high”. The time from V_Q exceeding $V_{RT,hi}$ until the device sets the reset output RO/WO to “high” is the power-on reset delay time $t_{d,PWR-ON}$. The power-on reset delay time allows a microcontroller to start up properly before the reset output RO/WO is released to “high”. The power-on reset delay time $t_{d,PWR-ON}$ can be configured with the capacitance of the delay capacitor C_D connected to pin D.

If a power-on reset delay time $t_{d,PWR-ON}$ different from the value for C_D = 10 nF is required, then the necessary delay capacitor’s value can be derived from the specified value given in **Reset delay timing** by:

$$C_D = 10\ \text{nF} \times t_{d,PWR-ON} / t_{d,PWR-ON,10nF} \quad (4.2)$$

with

- $t_{d,PWR-ON}$: Desired power-on reset delay time
- $t_{d,PWR-ON,10nF}$: Power-on reset delay time, see **Power-on reset delay time**
- C_D: Delay capacitor required

The formula is valid for $C_D \geq 1$ nF. For precise timing calculations also consider the delay capacitor’s tolerance.

Reset output RO/WO

The reset output RO/WO is an open collector output with an integrated pull-up resistor. If a lower-ohmic RO/WO signal is desired, then connect an external pull-up resistor to the output Q. Since the maximum RO/WO sink current is limited, the minimum optional external resistor $R_{RO/WO,ext}$ is specified in **Reset output, external pull-up resistor to Q**.

Reset output RO/WO “low” for $V_Q \geq 1$ V

If an undervoltage reset condition occurs, then the device keeps the reset output RO/WO “low” for $V_Q \geq 1$ V, even if the input voltage V_I is 0 V. This is achieved by supplying the reset circuit from the output capacitor.

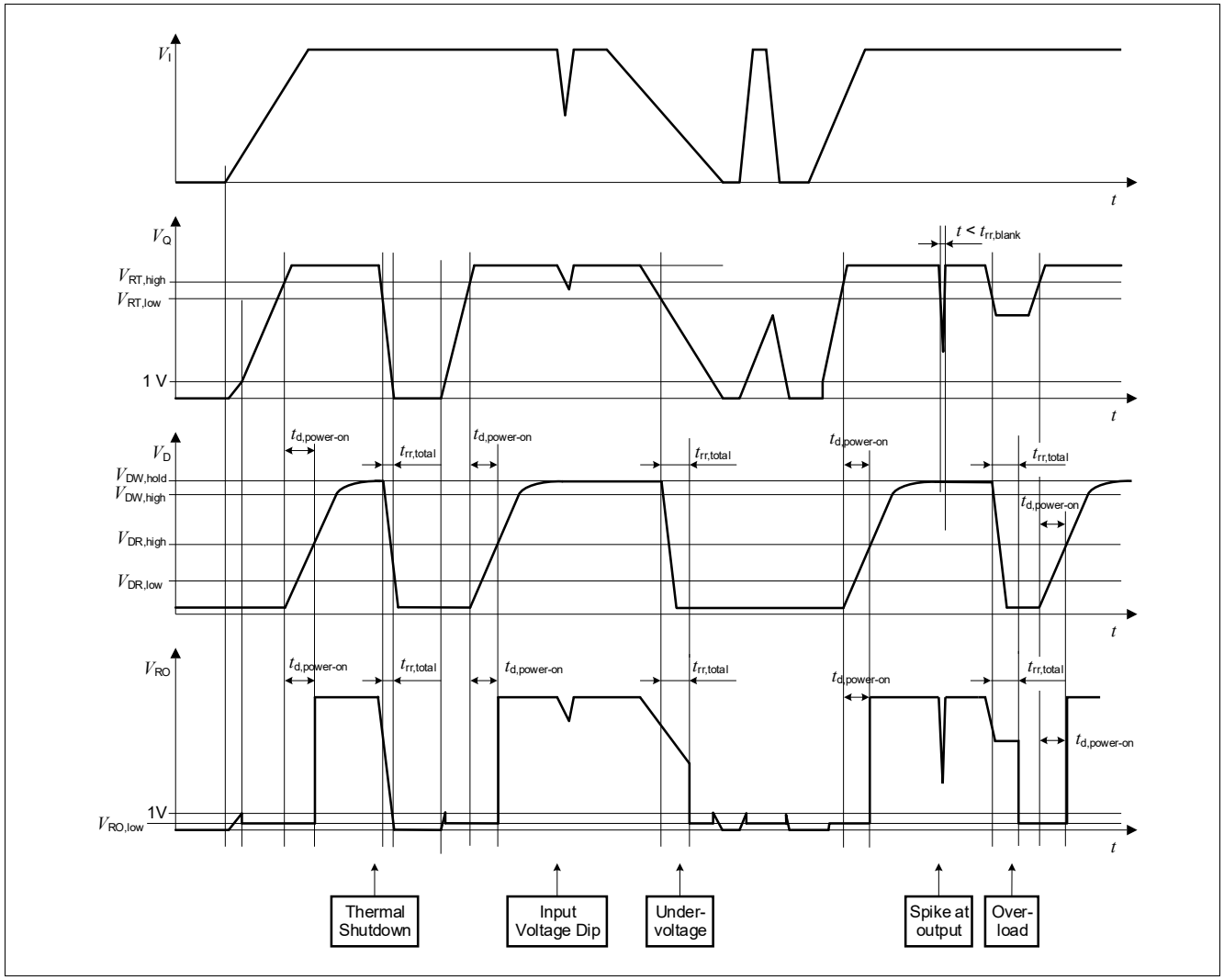


Figure 6 Timing diagram reset

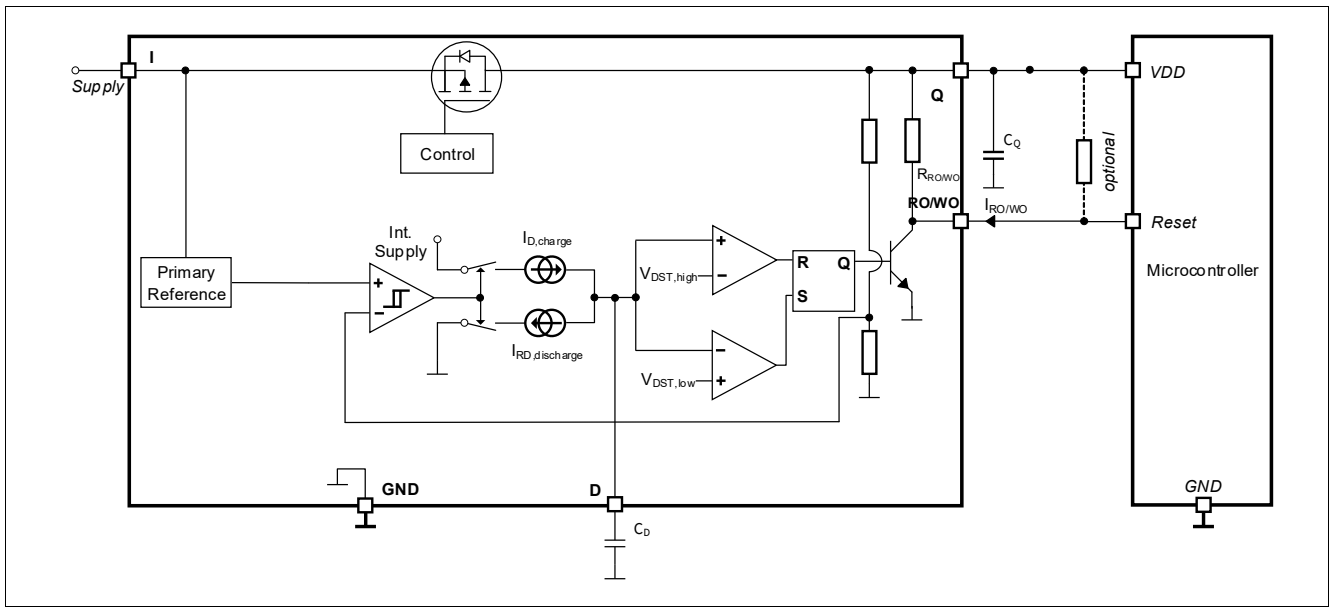


Figure 7 Functional block diagram reset

4.3.1 Electrical characteristics reset

Table 6 Electrical characteristics reset

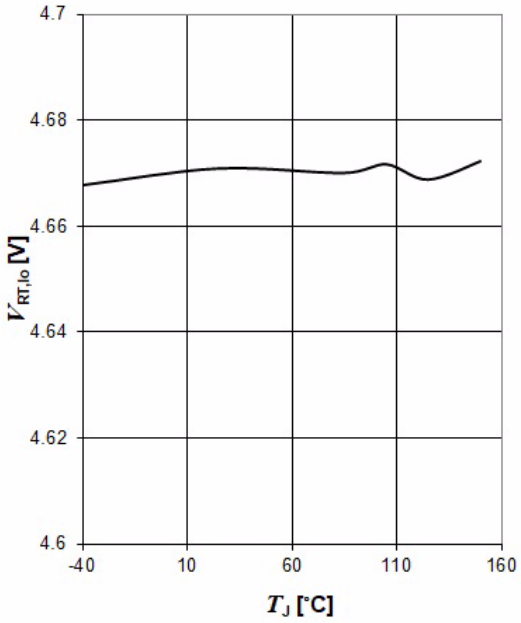
V_I = 13.5 V, T_j = -40°C to 150°C; all voltages with respect to ground; direction of currents see **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output undervoltage reset comparator default values							
Output undervoltage reset lower switching threshold	$V_{RT,low}$	4.5	4.6	4.75	V	V_Q decreasing; $V_{RT,low} \le V_I \le 42$ V	P_4.4.3
Output undervoltage reset upper switching threshold	$V_{RT,high}$	4.6	4.7	4.85	V	V_Q increasing; $V_{RT,high} \le V_I \le 42$ V	P_4.4.4
Output undervoltage reset switching hysteresis	$V_{RT,hy}$	30	100	200	mV	V_I within operating range	P_4.4.10
Reset output RO/WO							
Reset output “low” voltage	$V_{RO/WO,low}$	–	0.2	0.4	V	1 V ≤ $V_Q \le V_{RT}$; $R_{RO,ext} \ge 6.2$ kΩ	P_4.4.16
Reset output, external pull-up resistor to Q	$R_{RO/WO,ext}$	6.2	–	–	kΩ	1 V ≤ $V_Q \le V_{RT}$; $V_{RO} \le 0.4$ V	P_4.4.17
Reset output, internal pull-up resistor	$R_{RO/WO,int}$	10	20	35	kΩ	Internally connected to Q	P_4.4.18
Reset delay timing							
Lower delay switching threshold	$V_{DR,low}$	–	0.6	–	V	–	P_4.4.20
Delay capacitor charge current	$I_{D,ch}$	–	1.6	–	µA	V_D = 1.2 V	P_4.4.21
Delay capacitor reset discharge current	$I_{DR,dsch}$	–	180	–	mA	V_D = 1.2 V	P_4.4.22
Power-on reset delay time	$t_{d,PWR-ON,10nF}$	3	6	9	ms	[1] Calculated value; C_D = 10 nF; C_D discharged to 0 V	P_4.4.23
Internal reset reaction time	$t_{rr,int}$	3	8	40	µs	C_D = 0 nF, V_Q = 4 V; $V_{WINH,high} \le V_{WINH}$	P_4.4.24
Delay capacitor discharge time	$t_{rr,d,10nF}$	–	0.2	0.3	µs	[1] C_D = 10 nF	P_4.4.26
Total reset reaction time	$t_{rr,total,10nF}$	–	10	41	µs	Calculated value: $t_{rr,d,10nF} + t_{rr,int}$; C_D = 10 nF	P_4.4.27
Reset blanking time	$t_{rr,blank}$	–	3	–	µs	[2]	P_4.4.28

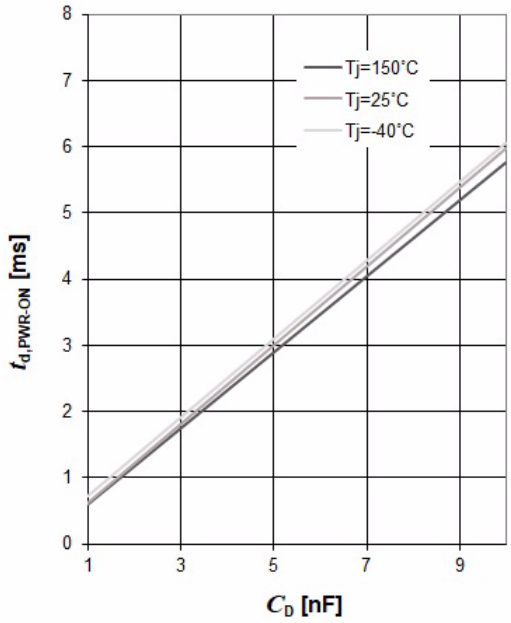
1) For programming a different delay and reset reaction time, see **Reset**.
2) Not subject to production test, specified by design.

4.3.2 Typical performance characteristics reset

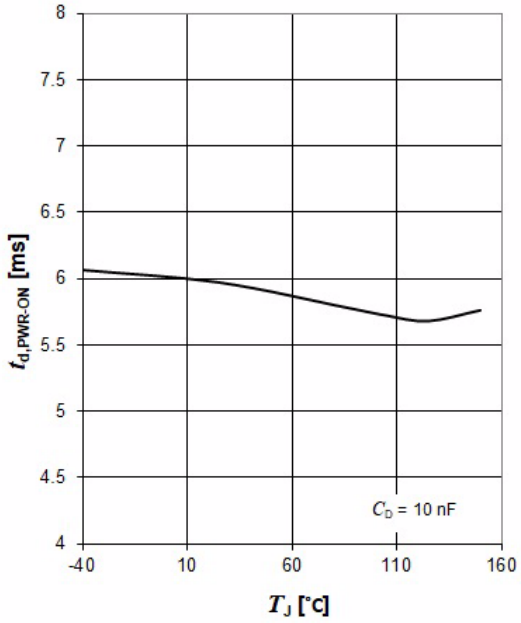
Undervoltage reset lower switching threshold $V_{RT,lo}$ versus junction temperature T_j



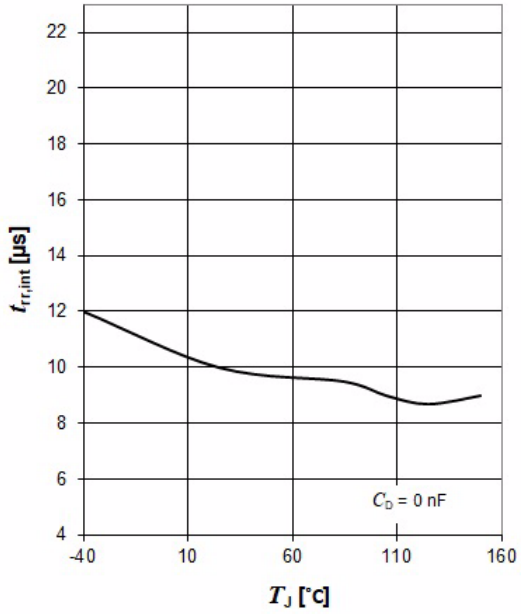
Power-on reset delay time $t_{d,PWR-ON}$ versus delay capacitance C_D



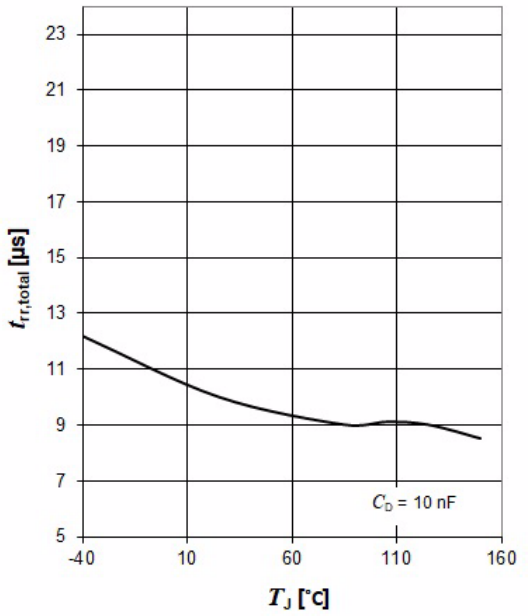
Power-on reset delay time $t_{d,PWR-ON}$ versus junction temperature T_j



Internal reset reaction time $t_{rr,int}$ versus junction temperature T_j



Total reset reaction time $t_{rr,total}$ versus junction temperature T_j



4.4 Watchdog

The device offers a watchdog with inhibit feature and programmable watchdog timing. The watchdog function monitors a microcontroller to detect time based failures. If the device detects a missing rising edge at the WI pin, then it sets the watchdog output to “low” after a defined time. An external delay capacitor C_D is used to configure the timing. For details on how the WI signal can comply with watchdog timing, see **Timing diagram watchdog**.

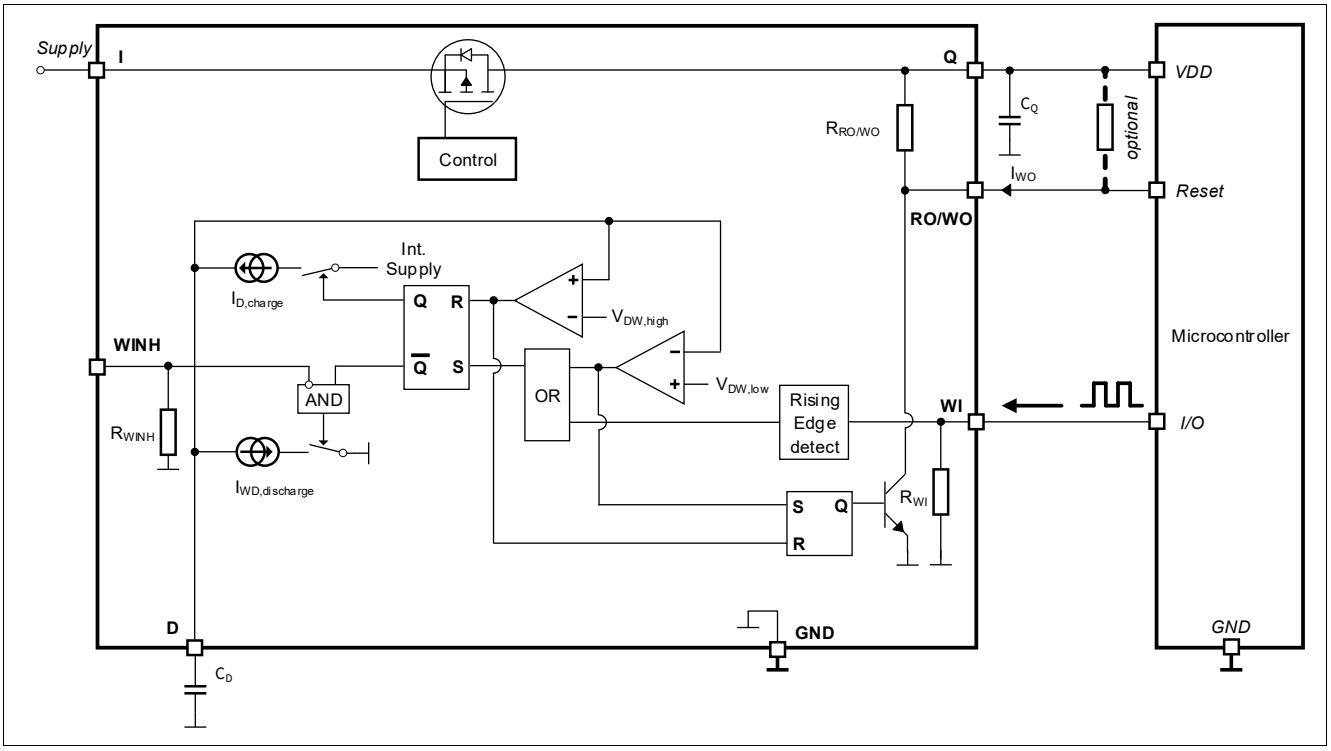


Figure 8 Functional block diagram watchdog circuit

Watchdog inhibit input WINH

The watchdog inhibit input WINH enables or disables the watchdog function. A “high” signal at WINH disables the watchdog. When disabled, the capacitor at the D pin is charged to the watchdog deactivation hold voltage $V_{DW,hold}$. The signal applied to WINH must comply with the values in **Watchdog inhibit WINH**.

Watchdog output RO/WO

The watchdog output RO/WO is an open collector output with an integrated pull-up resistor. If a lower-ohmic RO/WO signal is desired, then connect an external pull-up resistor to the output Q. Since the maximum RO/WO sink current is limited, the minimum external resistor value $R_{RO/WO,ext}$ is specified in **Watchdog output external pull-up resistor**.

Watchdog input WI

A positive edge at the watchdog input WI triggers the watchdog. Because of the integrated high pass filter, the amplitude and slope of the signal at WI pin must comply with the values in **Watchdog input WI**. For details on the test pulse applied, see **Figure 9**.

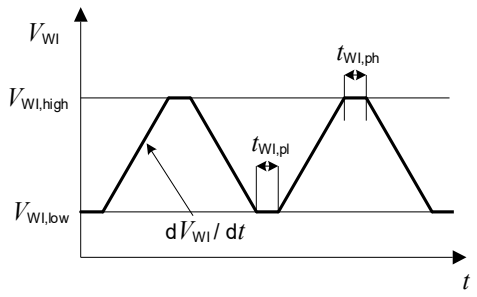


Figure 9 Test pulses watchdog input WI

Watchdog timing

If the watchdog is enabled and the device does not detect a rising edge at the WI pin, then the delay capacitor C_D is continuously charged and discharged between $V_{DW,low}$ and $V_{DW,high}$, see **Functional block diagram watchdog circuit**. The RO/WO pin goes “low” for $t_{WD,lo}$ when the delay capacitor voltage V_D discharges to $V_{DW,low}$. Due to the cyclic nature of this behavior, this pattern repeats with the watchdog period $t_{WD,p}$.

If the device detects a rising edge at the WI pin during the C_D discharge cycle, then a new charge cycle starts. To prevent the device from setting RO/WO to “low”, a rising edge on the WI pin must occur within the watchdog trigger time $t_{WI,tr}$. For timing details see **Timing diagram watchdog**.

If a watchdog trigger time $t_{WI,tr}$ different from the one for C_D = 10 nF is required, then the delay capacitor’s value can be derived from the value in **Watchdog timing** by:

$$C_D = 10\ \text{nF} \times t_{WI,tr} / t_{WI,tr,10nF} \quad (4.3)$$

The watchdog output “low” time $t_{WD,lo}$ and the watchdog period $t_{WD,p}$ equate to:

$$t_{WD,lo} = t_{WD,lo,10nF} \times C_D / 10\ \text{nF} \quad (4.4)$$

$$t_{WD,p} = t_{WI,tr} + t_{WD,lo} \quad (4.5)$$

The formula applies for $C_D \geq 1$ nF. For precise timing calculations consider the delay capacitor’s tolerance.

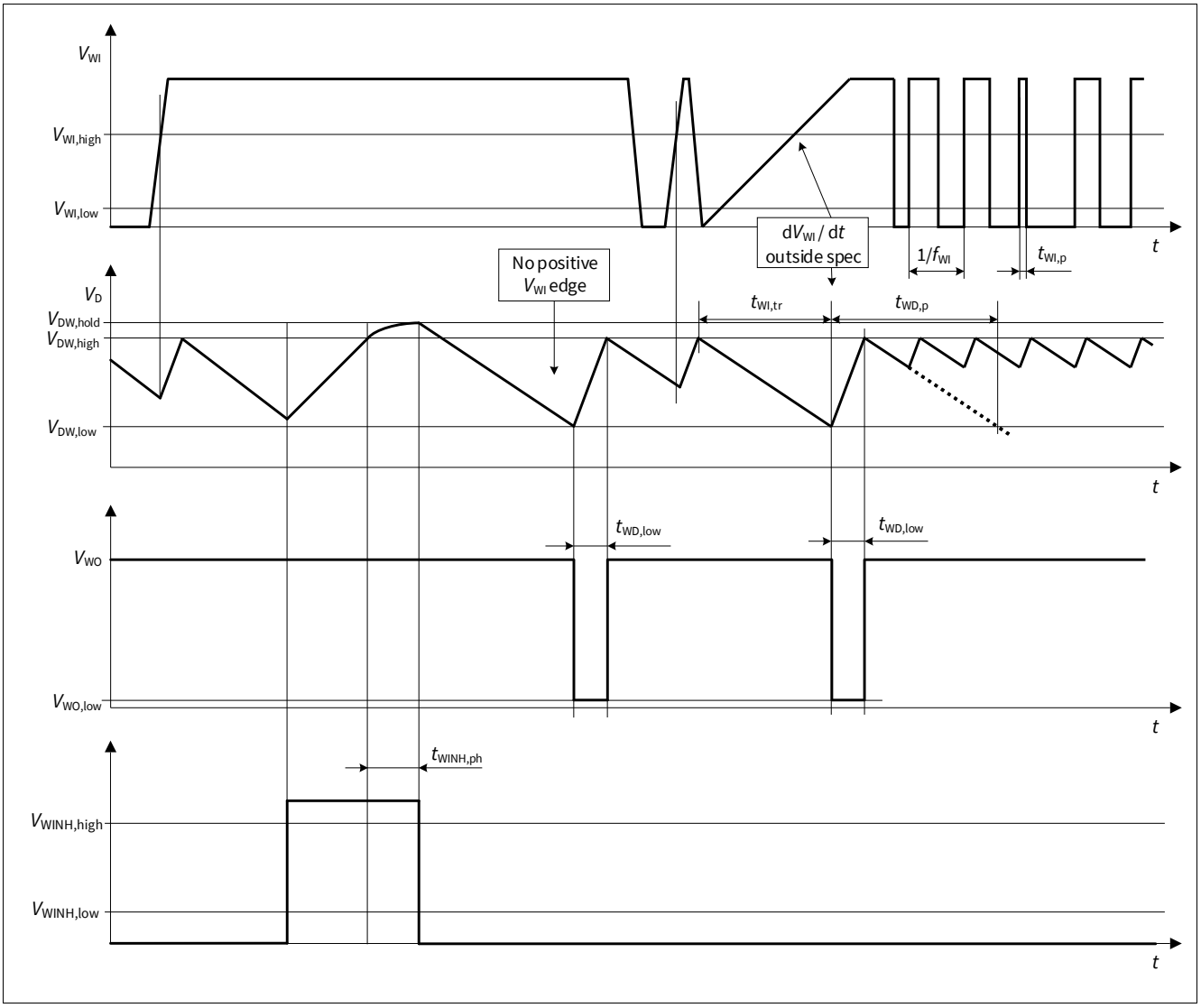


Figure 10 Timing diagram watchdog

4.4.1 Electrical characteristics watchdog

Table 7 Electrical characteristics watchdog

V_I = 13.5 V, T_j = -40°C to 150°C; all voltages with respect to ground, direction of currents see **Figure 8** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Watchdog inhibit WINH							
Watchdog inhibit “low” signal valid	$V_{WINH,low}$	–	–	0.8	V	–	P_4.5.1
Watchdog inhibit “high” signal valid	$V_{WINH,high}$	2	–	–	V	–	P_4.5.2
Watchdog inhibit “high” level input current	$I_{WINH,high}$	–	–	4	µA	V_{WINH} = 3.3 V	P_4.5.3
Watchdog inhibit “high” signal pulse length	$t_{WINH,ph}$	–	2.5	–	ms	C_D = 10 nF; $V_{WINH} \geq V_{WINH.high}$	P_4.5.5
Watchdog inhibit internal pull-down resistor	R_{WINH}	0.825	1.5	2.6	MΩ	–	P_4.5.6
Watchdog input WI							
Watchdog input “low” signal valid	$V_{WI,low}$	–	–	0.8	V	1)	P_4.5.7
Watchdog input “high” signal valid	$V_{WI,high}$	2	–	–	V	1)	P_4.5.8
Watchdog input “low” signal pulse length	$t_{WI,pl}$	1	–	–	µs	1) $V_{WI} \leq V_{WI,low}$	P_4.5.9
Watchdog input “high” signal pulse length	$t_{WI,ph}$	1	–	–	µs	1) $V_{WI} \geq V_{WI,high}$	P_4.5.10
Watchdog input “high” level input current	$I_{WI,H}$	–	–	4	µA	V_{WI} = 3.3 V	P_4.5.11
Watchdog input signal slew rate	$\Delta V_{WI}/\Delta t$	1	–	–	V/µs	1) $V_{WI,low} \leq V_{WI} \leq V_{WI,high}$	P_4.5.12
Watchdog input internal pull-down resistor	R_{WI}	0.825	1.5	2.6	MΩ	–	P_4.5.13
Watchdog output WO							
Watchdog output “low” voltage	$V_{WO,low}$	–	0.2	0.4	V	$V_Q \geq$ 2.5 V; $R_{WO} \geq$ 6.2 kΩ	P_4.5.14
Watchdog output external pull-up resistor	$R_{WO,ext}$	6.2	–	–	kΩ	$V_Q \geq$ 2.5 V; $V_{WO} \leq$ 0.4 V	P_4.5.15
Watchdog output internal pull-up resistor	$R_{WO,int}$	10	20	35	kΩ	–	P_4.5.16
Watchdog timing							
Delay capacitor charge current	I_D	–	1.6	–	µA	V_D = 1.2 V	P_4.5.17

Table 7 Electrical characteristics watchdog (cont'd)

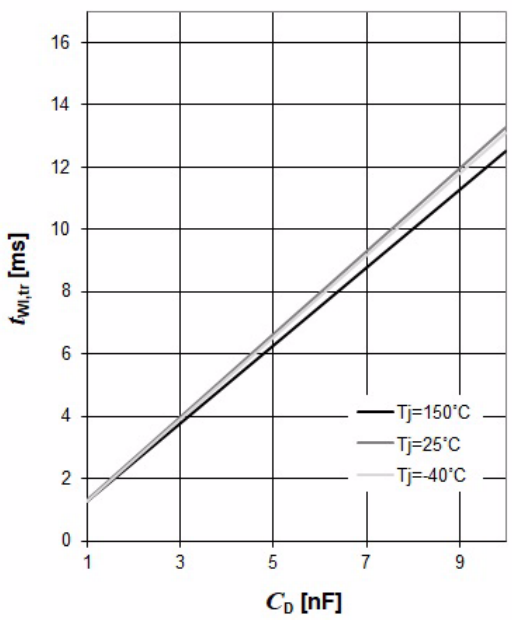
V_I = 13.5 V, T_j = -40°C to 150°C; all voltages with respect to ground, direction of currents see **Figure 8** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay capacitor deactivation charge current	$I_{DW,ch,deact}$	–	1.6	–	µA	V_D = 1.2 V	P_4.5.18
Delay capacitor watchdog discharge current	$I_{DW,disch}$	–	0.5	–	µA	V_D = 1.2 V	P_4.5.19
Upper watchdog timing threshold	$V_{DW,high}$	–	1.45	–	V	–	P_4.5.20
Lower watchdog timing threshold	$V_{DW,low}$	–	0.9	–	V	–	P_4.5.21
Upper delay watchdog deactivated hold voltage	$V_{DW,deact}$	–	1.5	–	V	$V_{WINH} \geq V_{WINH.high}$	P_4.5.22
Watchdog trigger time	$t_{WI,tr,10nF}$	3.5	13	21	ms	2) Calculated value; C_D = 10 nF	P_4.5.23
Watchdog output "low" time	$t_{WD,lo,10nF}$	1.5	4	6	ms	2) Calculated value; C_D = 10 nF	P_4.5.24
Watchdog period	$t_{WD,p,10nF}$	5	17	27	ms	2) Calculated value; $t_{WI,tr,10nF} + t_{WD,lo,10nF}$; C_D = 10 nF	P_4.5.25

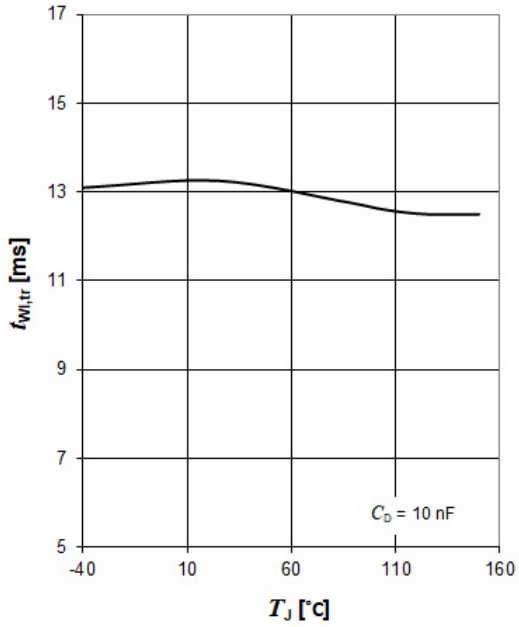
1) For details on the test pulse applied, see **Figure 9**.
2) For programming the watchdog timing, see **Watchdog**.

4.4.2 Typical performance characteristics watchdog

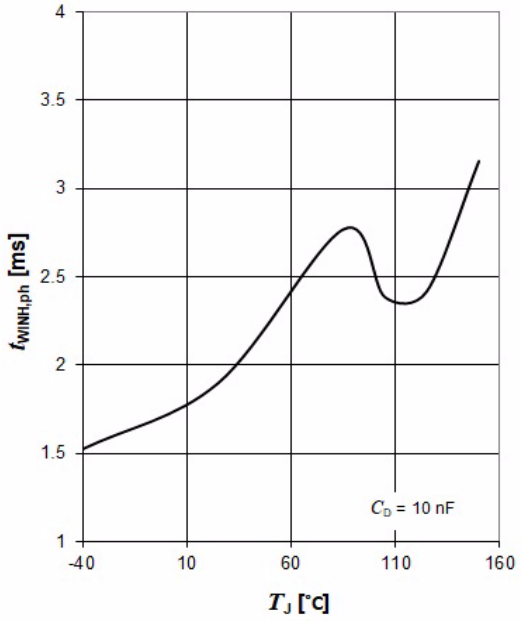
Watchdog trigger time $t_{WI,tr}$ versus delay capacitance C_D



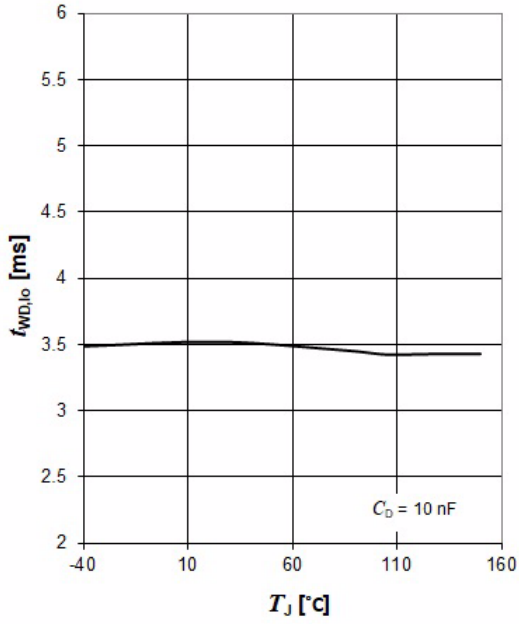
Watchdog trigger time $t_{WI,tr}$ versus junction temperature T_j



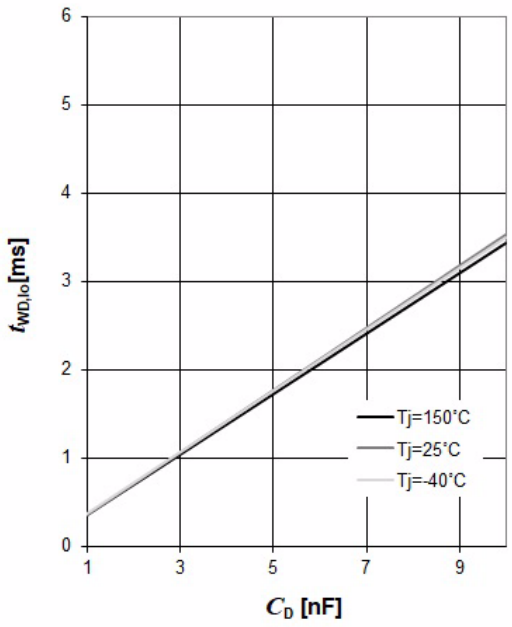
Watchdog inhibit high signal pulse length $t_{WINH,ph}$ versus junction temperature T_j



Watchdog output "low" time $t_{WD,lo}$ versus junction temperature T_j



Watchdog output “low” time $t_{WD,lo}$ versus delay capacitance C_D



5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

5.1 Application diagram

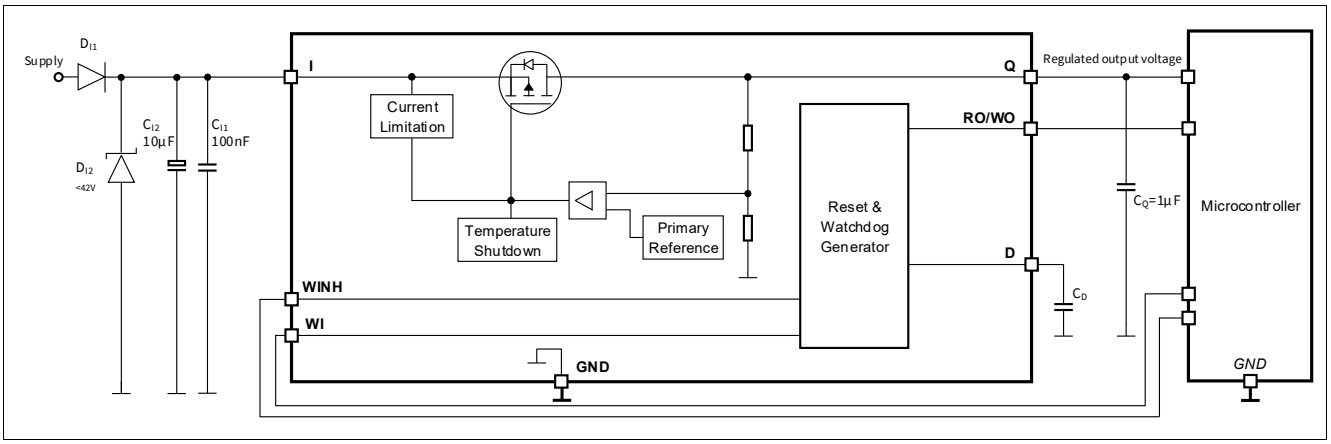


Figure 11 Application diagram

5.2 Selection of external components

5.2.1 Input pin

Figure 11 shows the typical input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out high frequency disturbances imposed by the line, such as ISO pulses 3a/b. The capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any voltage exceeding the maximum rating of the linear voltage regulator and protect the device against damage due to overvoltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

5.2.2 Output pin

An output capacitor is mandatory for the stability of a linear voltage regulator. The requirement to the output capacitor is given in **Functional range**.

The device is designed to be stable with extremely low ESR capacitors. According to automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and to GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application to fulfill the output stability requirements.

5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (5.1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (5.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **Thermal resistance**.

Example

Application conditions:

V_I = 13.5 V

V_Q = 5 V

I_Q = 50 mA

T_a = 85°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$

= (13.5 V - 5 V) × 50 mA + 13.5 V × 33 µA

= 0.425 W + 0.000446 W

= 0.425446 W

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$

= (150°C - 85°C) / 0.425446 W = 152.781 K/W

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 152.781 K/W. According to **Thermal resistance**, at least 300 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

5.4 Reverse polarity protection

The device must be protected from reverse polarity by external components. An external reverse polarity diode is required. The **Absolute maximum ratings** of the device must be maintained.

5.5 Further application information

- Please contact Infineon for information on pin behavior assessment
- Existing application note
- For further information you may contact **https://www.infineon.com**

6 Package information

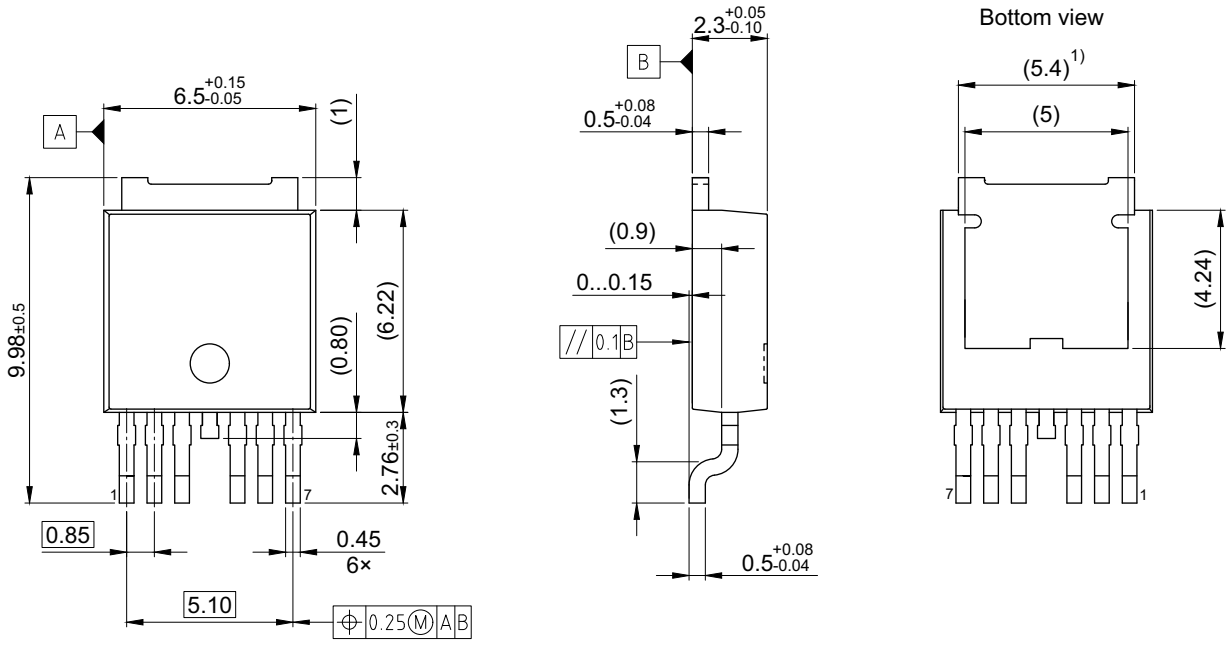


Figure 12 PG-TO252-7[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

7 Revision history

Revision	Date	Changes
1.1	2023-10-16	Editorial changes
1.0	2022-11-29	Datasheet created

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