

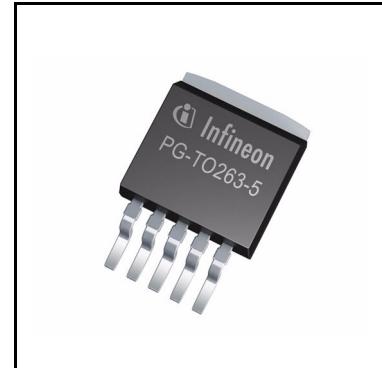
# OPTIREG™ linear TLS850B0TBV33

## Low dropout linear voltage regulator



### Features

- Wide input voltage range from 3.0 V to 40 V
- Fixed output voltage 3.3 V
- Output voltage accuracy  $\leq \pm 2\%$
- Output current capability up to 500 mA
- Ultra low current consumption, typical 20  $\mu$ A
- Very low dropout voltage, typical 120 mV at 100 mA
- Stable with ceramic output capacitor of 1  $\mu$ F
- Enable function
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS-compliant)



### Potential applications

- Automotive or other supply systems that are connected to the battery permanently
- Automotive supply systems that need to operate in cranking condition

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

### Description

The OPTIREG™ linear TLS850B0TBV33 is a high performance, very low dropout linear voltage regulator for 3.3 V supply in a PG-T0263-5 package.

The input voltage range of 3 V to 40 V and a very low quiescent current of 20  $\mu$ A make it the perfect match for automotive or other supply systems connected to the battery permanently.

The new loop concept combines fast regulation and very high stability. Below an output current of 100 mA, the typical dropout voltage is below 100 mV. The operating range starts at an input voltage of only 3 V (extended operating range). This makes the TLS850B0TBV33 suitable for automotive systems that need to operate during cranking condition.

The device can be switched on and off by the enable feature.

Internal protection features such as output current limitation and overtemperature shutdown protect the device from immediate damage due to failures such as output shorted to GND, overcurrent, and overtemperature.

## Choosing external components

An input capacitor  $C_i$  is recommended to compensate line influences.

The output capacitor  $C_Q$  is necessary for the stability of the regulating circuit. TLS850B0TBV33 is designed to operate stable with low-ESR ceramic capacitors.

Type	Package	Marking
TLS850B0TBV33	PG-T0263-5	850B0V33

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Block diagram

1 Block diagram

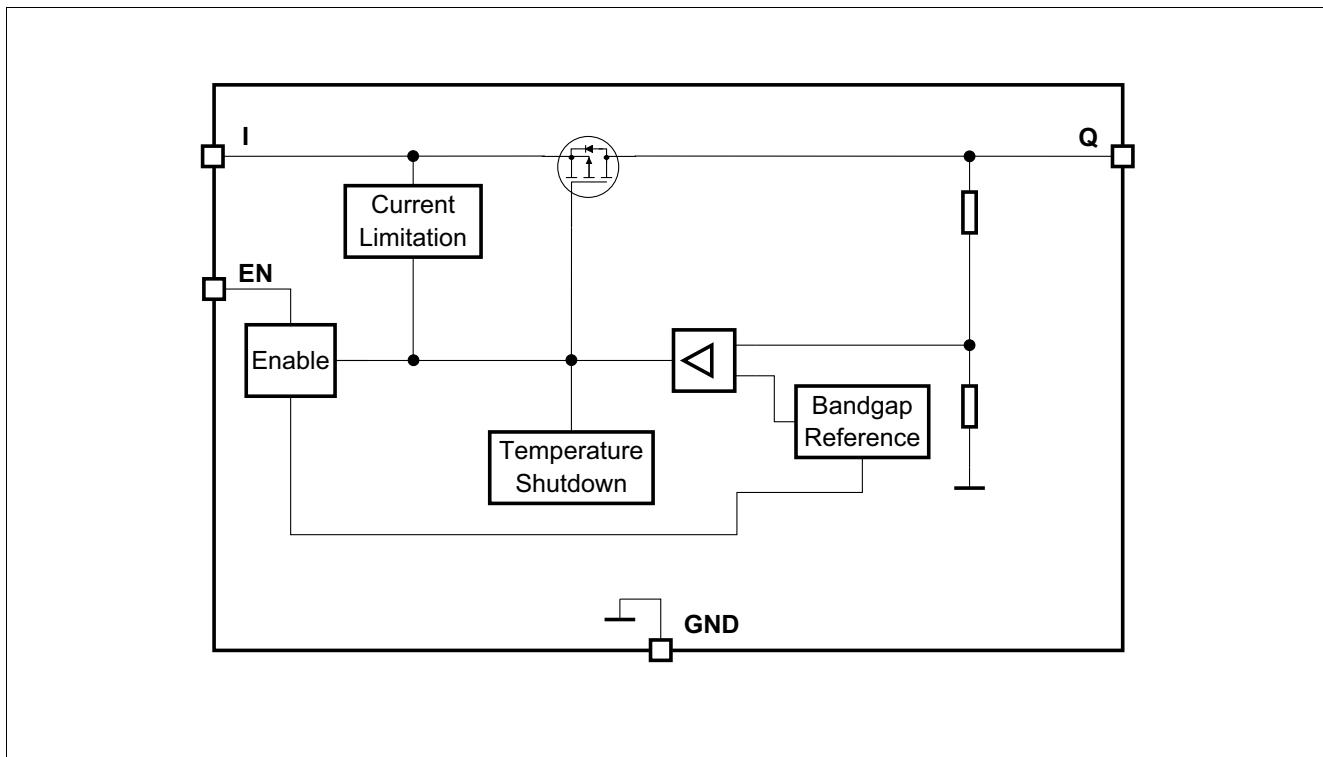


Figure 1 Block diagram

## Pin configuration

## 2 Pin configuration

### 2.1 Pin assignment

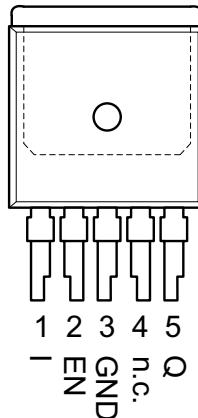


Figure 2 Pin configuration

### 2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	I	<b>Input</b> It is recommended to place a small ceramic capacitor (for example, 100 nF) to GND, close to the pins, in order to compensate line influences
2	EN	<b>Enable</b> (integrated pull-down resistor) Enable the IC with high input signal Disable the IC with low input signal
3	GND	<b>Ground</b>
4	n.c.	<b>Not connected</b> Leave open or connect to GND
5	Q	<b>Output</b> Connect output capacitor $C_Q$ to GND close to the pin, respecting the values specified for its capacitance and ESR in <b>Functional range</b>
Heat slug	GND	<b>Heat slug</b> Connect to heatsink area; Connect to GND

**General product characteristics**

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_j$  = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Input I, Enable EN</b>							
Voltage	$V_I, V_{EN}$	-0.3	-	45	V	-	P_4.1.1
<b>Output Q</b>							
Voltage	$V_Q$	-0.3	-	7	V	-	P_4.1.2
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	-	150	°C	-	P_4.1.3
Storage temperature	$T_{stg}$	-55	-	150	°C	-	P_4.1.4
<b>ESD susceptibility</b>							
ESD susceptibility to GND	$V_{ESD}$	-2	-	2	kV	<sup>2)</sup> Human body model (HBM)	P_4.1.5
ESD susceptibility to GND	$V_{ESD}$	-500	-	500	V	<sup>3)</sup> Charged device model (CDM)	P_4.1.6
ESD susceptibility of corner pins to GND	$V_{ESD1,5}$	-750	-	750	V	<sup>3)</sup> Charged device model (CDM)	P_4.1.7

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).

3) ESD susceptibility, charged device model (CDM) according to JEDEC JESD22-C101.

#### Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent device destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

**General product characteristics**

**3.2 Functional range**

**Table 3 Functional range**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

<b>Parameter</b>	<b>Symbol</b>	<b>Values</b>			<b>Unit</b>	<b>Note or Test Condition</b>	<b>Number</b>
		<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>			
Input voltage range	$V_I$	$V_{Q,\text{nom}} + V_{\text{dr}}$	–	40	V	<sup>1)</sup> –	P_4.2.1
Extended input voltage range	$V_{I,\text{ext}}$	3.0	–	40	V	<sup>2)</sup> –	P_4.2.2
Enable voltage range	$V_{\text{EN}}$	0	–	40	V	–	P_4.2.3
Output capacitor's requirements for stability	$C_Q$	1	–	–	$\mu\text{F}$	<sup>3)</sup> <sup>4)</sup> –	P_4.2.4
ESR of output capacitor	$ESR(C_Q)$	–	–	50	$\Omega$	<sup>3)</sup> –	P_4.2.5
ESR of output capacitor	$ESR(C_Q)$	–	–	100	$\Omega$	<sup>3)</sup> $V_{\text{IN}} < 25\text{ V}$	P_4.2.5
Junction temperature	$T_j$	-40	–	150	$^\circ\text{C}$	–	P_4.2.6

1) Output current is limited internally and depends on the input voltage. See Electrical Characteristics for more details.

2) If  $V_{I,\text{ext,min}} \leq V_I \leq V_{Q,\text{nom}} + V_{\text{dr}}$ , then  $V_Q = V_I - V_{\text{dr}}$ . If  $V_I < V_{I,\text{ext,min}}$ , then  $V_Q$  can drop to 0 V.

3) Not subject to production test, specified by design.

4) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

**Note:** *Within the functional or operating range, the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

**General product characteristics**

**3.3 Thermal resistance**

**Note:** *This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).*

**Table 4 Thermal resistance<sup>1)</sup>**

<b>Parameter</b>	<b>Symbol</b>	<b>Values</b>			<b>Unit</b>	<b>Note or Test Condition</b>	<b>Number</b>
		<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>			
Junction to case	$R_{thJC}$	–	3.2	–	K/W	–	P_4.3.1
Junction to ambient	$R_{thJA}$	–	21	–	K/W	<sup>2)</sup> 2s2p board	P_4.3.2
Junction to ambient	$R_{thJA}$	–	60	–	K/W	<sup>3)</sup> 1s0p board, footprint only	P_4.3.3
Junction to ambient	$R_{thJA}$	–	36	–	K/W	<sup>3)</sup> 1s0p board, 300 mm <sup>2</sup> heatsink area on PCB	P_4.3.4
Junction to ambient	$R_{thJA}$	–	30	–	K/W	<sup>3)</sup> 1s0p board, 600 mm <sup>2</sup> heatsink area on PCB	P_4.3.5

1) Not subject to production test, specified by design.

- 2) The specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on an FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.
- 3) The specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on an FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with one copper layer (1 × 70 µm Cu).

## Block description and electrical characteristics

## 4 Block description and electrical characteristics

### 4.1 Voltage regulation

The output voltage  $V_Q$  is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the following factors:

- Output capacitor  $C_Q$
- Load current
- Chip temperature  $T_j$
- Internal circuit design

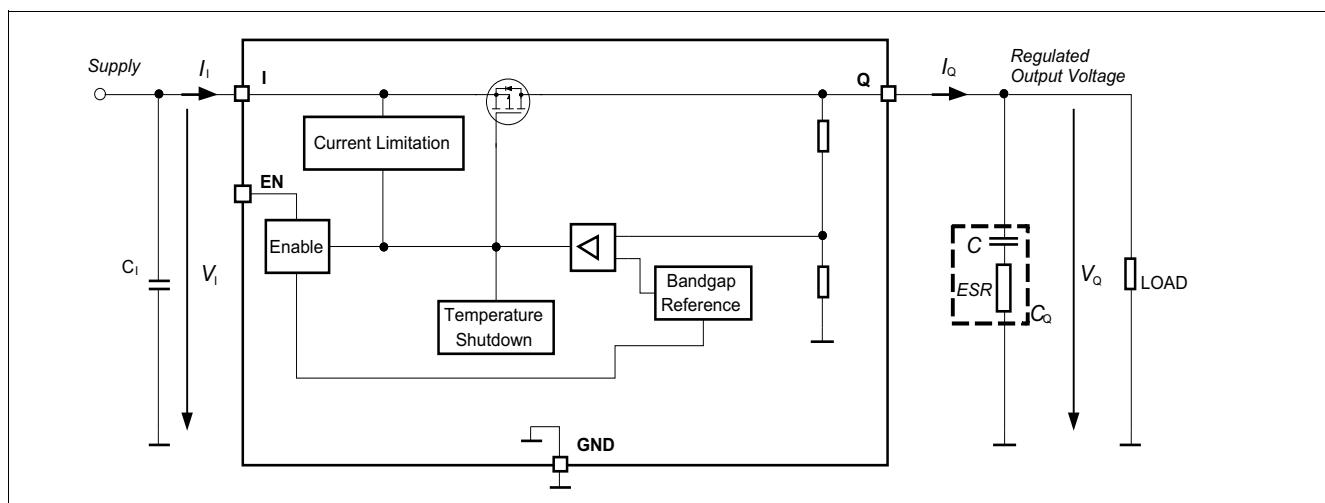
To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor  $ESR(C_Q)$  requirements given in **Table 3** must be maintained. Because the output capacitor must buffer load steps, it must be sized according to the requirements of the application.

An input capacitor  $C_I$  is recommended to compensate line influences. In order to block influences such as pulses and high frequency distortion at the input, an additional reverse-polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

In order to prevent overshoots during start-up, a slope-control function is implemented. This significantly reduces output voltage overshoots during start-up, mostly independent from the load.

If the load current exceeds the specified limit, for example, due to a short circuit, then the device limits the output current, and the output voltage decreases.

The overtemperature shutdown circuit prevents the device from immediate destruction in fault condition, for example, due to a permanent short-circuit at the output, by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the lifetime of the device.



**Figure 3 Block diagram: voltage regulation**

## Block description and electrical characteristics

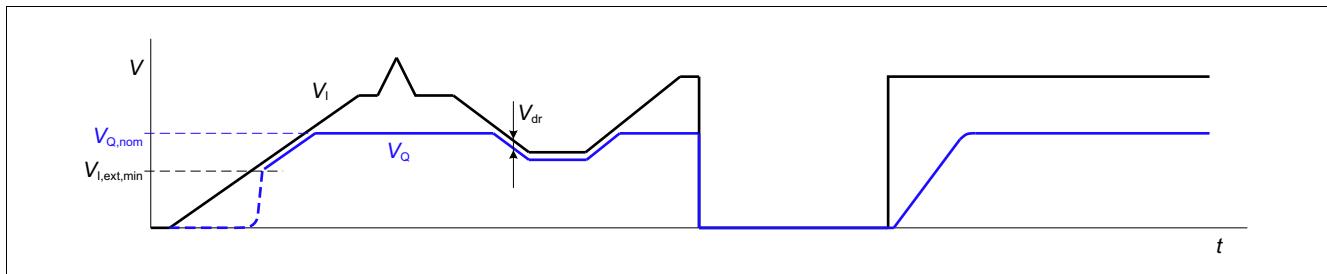


Figure 4 Output voltage versus input voltage

## Block description and electrical characteristics

**Table 5 Electrical characteristics: voltage regulator** $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_i = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified)Typical values are given at  $T_j = 25^\circ\text{C}$ 

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage accuracy	$V_Q$	3.23	3.3	3.37	V	$0.05\text{ mA} < I_Q < 500\text{ mA}$ $4.6\text{ V} < V_i < 28\text{ V}$	P_5.1.19
Output voltage accuracy	$V_Q$	3.23	3.3	3.37	V	$0.05\text{ mA} < I_Q < 200\text{ mA}$ $3.85\text{ V} < V_i < 40\text{ V}$	P_5.1.20
Output voltage startup slew rate	$dV_Q/dt$	3.0	35	90	V/ms	$V_i > 18\text{ V/ms}$ $C_Q = 1\text{ }\mu\text{F}$ $0.33\text{ V} < V_Q < 2.97\text{ V}$	P_5.1.27
Output current limitation	$I_{Q,\text{max}}$	501	750	1100	mA	$0\text{ V} < V_Q < V_{Q,\text{nom}} - 0.1\text{ V}$	P_5.1.28
Load regulation steady state	$\Delta V_{Q,\text{load}}$	-15	-5	-	mV	$I_Q = 0.05\text{ mA}$ to $500\text{ mA}$ $V_i = 6.5\text{ V}$	P_5.1.30
Line regulation steady state	$\Delta V_{Q,\text{line}}$	-	1	10	mV	$V_i = 8\text{ V}$ to $32\text{ V}$ $I_Q = 5\text{ mA}$	P_5.1.31
Dropout voltage $V_{\text{dr}} = V_i - V_Q$	$V_{\text{dr}}$	-	300	600	mV	<sup>1)</sup> $I_Q = 250\text{ mA}$	P_5.1.32
Dropout voltage $V_{\text{dr}} = V_i - V_Q$	$V_{\text{dr}}$	-	120	240	mV	<sup>1)</sup> $I_Q = 100\text{ mA}$	P_5.1.33
Power supply ripple rejection	$PSRR$	-	63	-	dB	<sup>2)</sup> $f_{\text{ripple}} = 100\text{ Hz}$ $V_{\text{ripple}} = 0.5\text{ Vpp}$	P_5.1.34
Overtemperature shutdown threshold	$T_{j,\text{sd}}$	151	-	200	°C	<sup>2)</sup> $T_j$ increasing	P_5.1.35
Overtemperature shutdown threshold hysteresis	$T_{j,\text{sdh}}$	-	15	-	K	<sup>2)</sup> $T_j$ decreasing	P_5.1.36

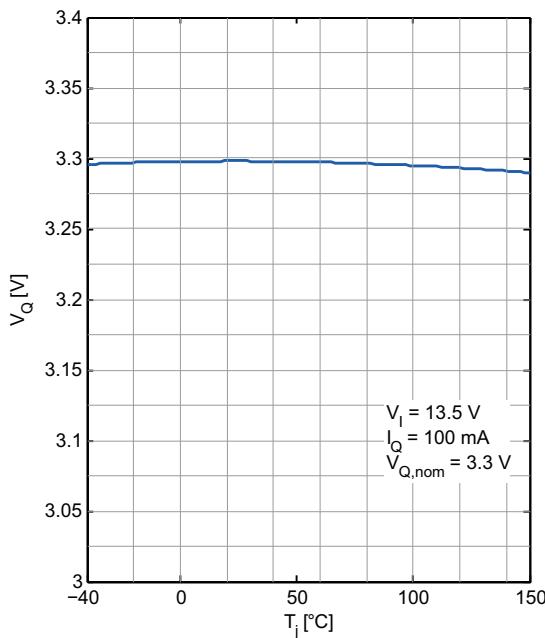
1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_i = 13.5\text{ V}$ .

2) Not subject to production test, specified by design.

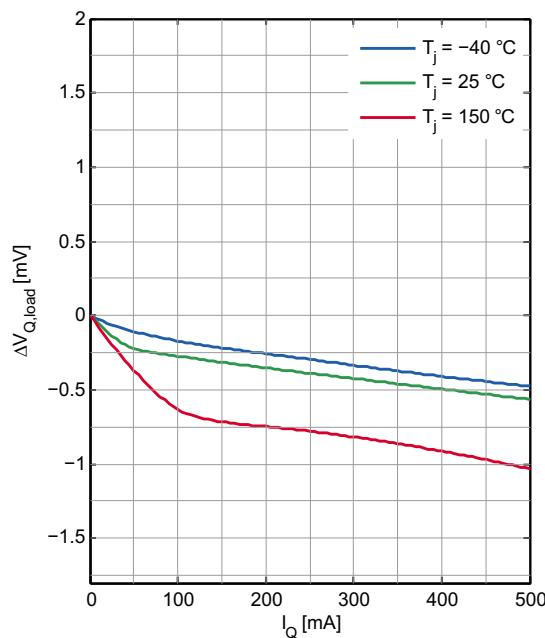
**Block description and electrical characteristics**

**4.2 Typical performance characteristics: voltage regulator**

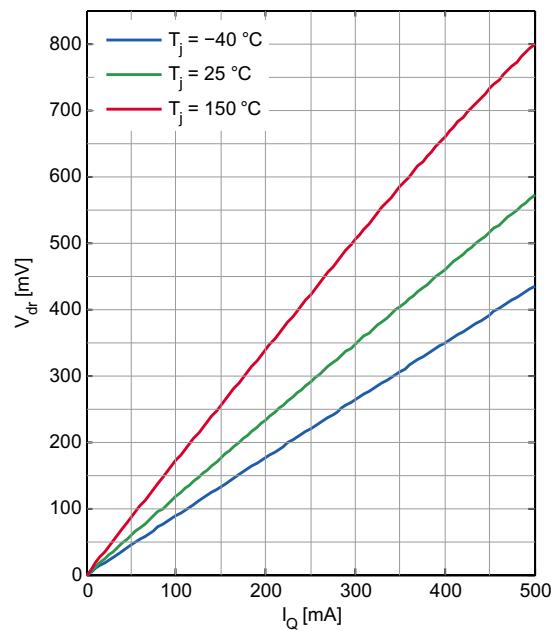
**Output voltage  $V_Q$  versus junction temperature  $T_j$**



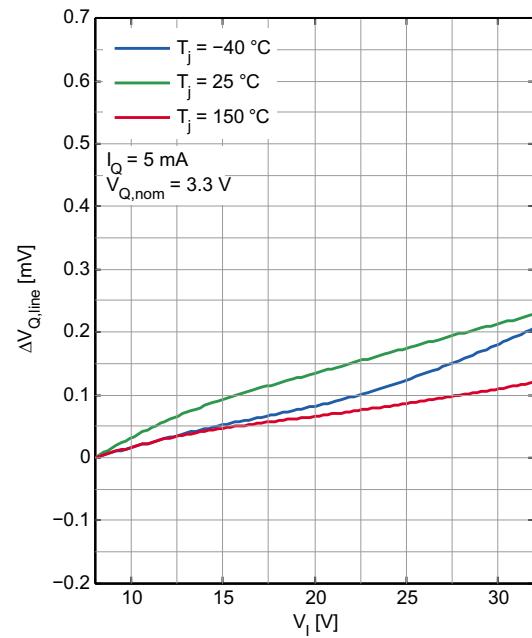
**Load regulation  $\Delta V_{Q,load}$  versus output current  $I_Q$**



**Dropout voltage  $V_{dr}$  versus output current  $I_Q$**

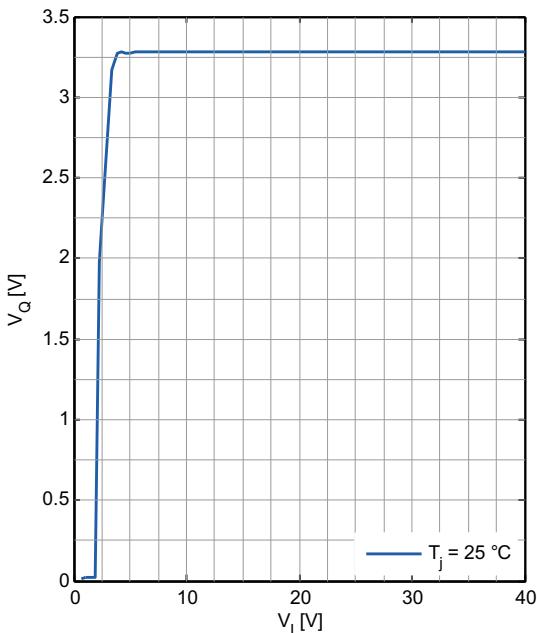


**Line regulation  $\Delta V_{Q,line}$  versus input voltage  $V_I$**

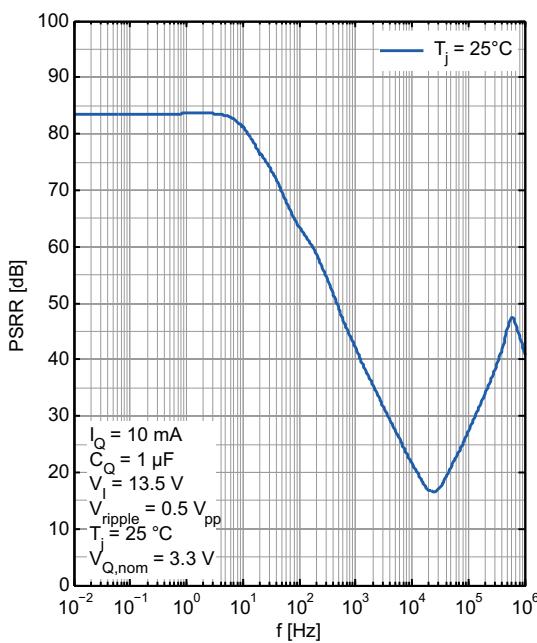


**Block description and electrical characteristics**

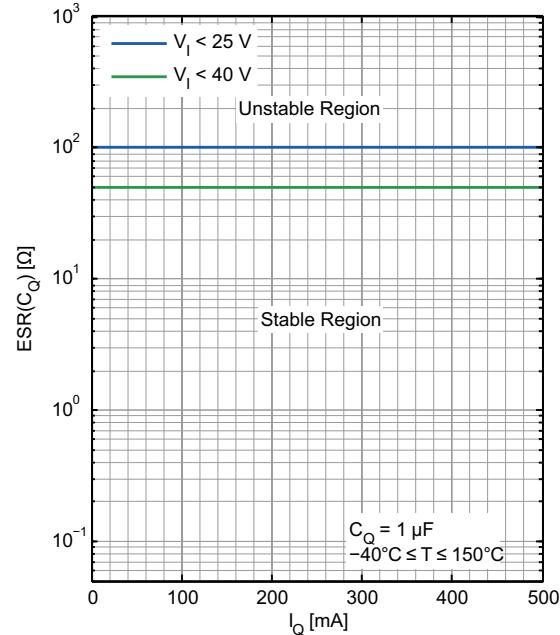
**Output voltage  $V_Q$  versus  
input voltage  $V_I$**



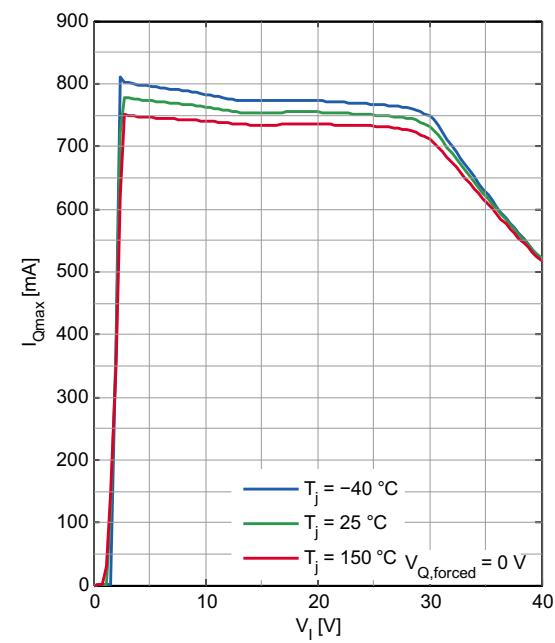
**Power supply ripple rejection  $PSRR$  versus  
ripple frequency  $f$**



**Output capacitor  $ESR(C_Q)$  versus  
output current  $I_Q$**



**Maximum output current  $I_Q$  versus  
input voltage  $V_I$**



**Block description and electrical characteristics**

**4.3 Current consumption**

**Table 6 Electrical characteristics: current consumption**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_i = 13.5\text{ V}$  (unless otherwise specified)

Typical values are given at  $T_j = 25^\circ\text{C}$

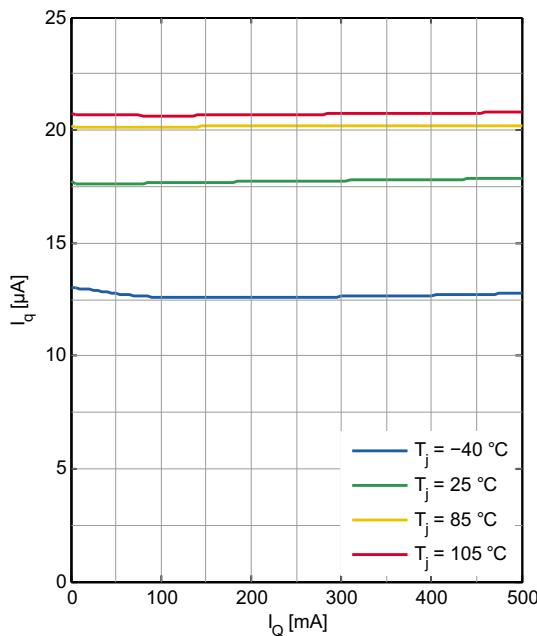
<b>Parameter</b>	<b>Symbol</b>	<b>Values</b>			<b>Unit</b>	<b>Note or Test Condition</b>	<b>Number</b>
		<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>			
Current consumption $I_q = I_i$	$I_{q,\text{off}}$	–	–	1	µA	$V_{\text{EN}} = 0\text{ V}$ ; $T_j < 105^\circ\text{C}$	P_5.3.1
Current consumption $I_q = I_i$	$I_{q,\text{off}}$	–	–	2	µA	$V_{\text{EN}} = 0.4\text{ V}$ ; $T_j < 125^\circ\text{C}$	P_5.3.3
Current consumption $I_q = I_i - I_Q$	$I_q$	–	20	25	µA	$I_Q = 0.05\text{ mA}$ $T_j = 25^\circ\text{C}$	P_5.3.4
Current consumption $I_q = I_i - I_Q$	$I_q$	–	23	30	µA	$I_Q = 0.05\text{ mA}$ $T_j < 125^\circ\text{C}$	P_5.3.5
Current consumption $I_q = I_i - I_Q$	$I_q$	–	25	33	µA	<sup>1)</sup> $I_Q = 500\text{ mA}$ $T_j < 125^\circ\text{C}$	P_5.3.6

1) Not subject to production test, specified by design.

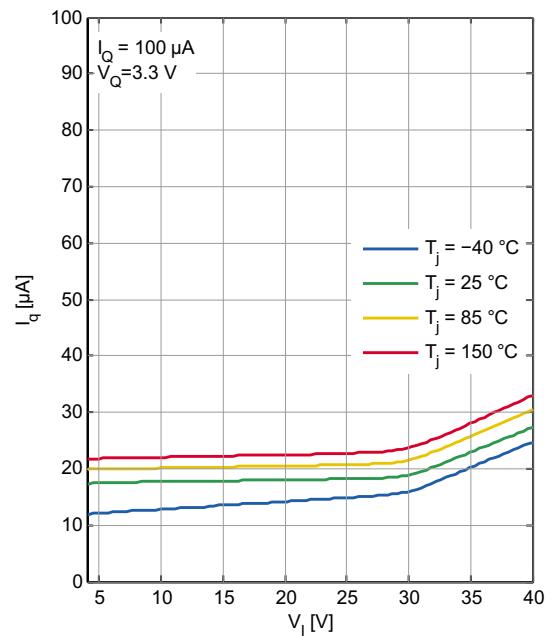
**Block description and electrical characteristics**

**4.4 Typical performance characteristics: current consumption**

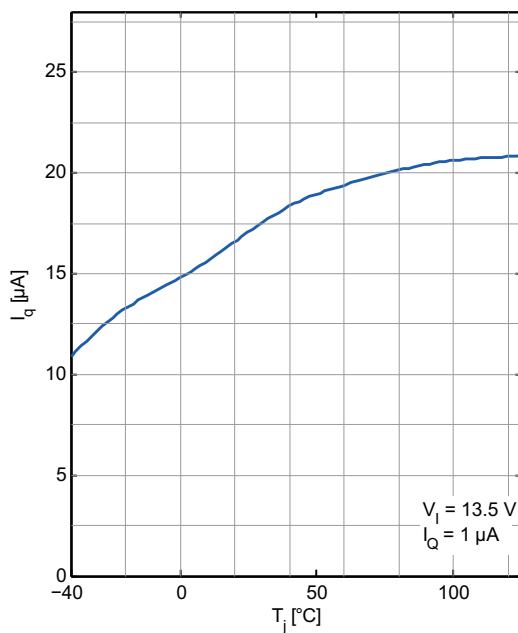
**Current consumption  $I_q$  versus output current  $I_Q$**



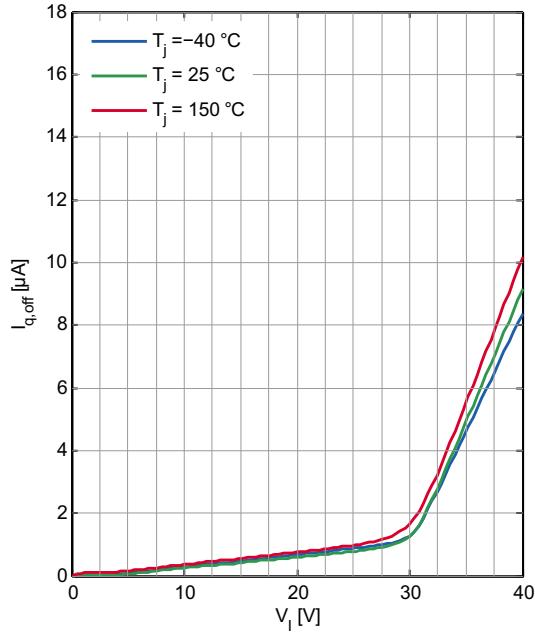
**Current consumption  $I_q$  versus input voltage  $V_I$**



**Current consumption  $I_q$  versus junction temperature  $T_j$**

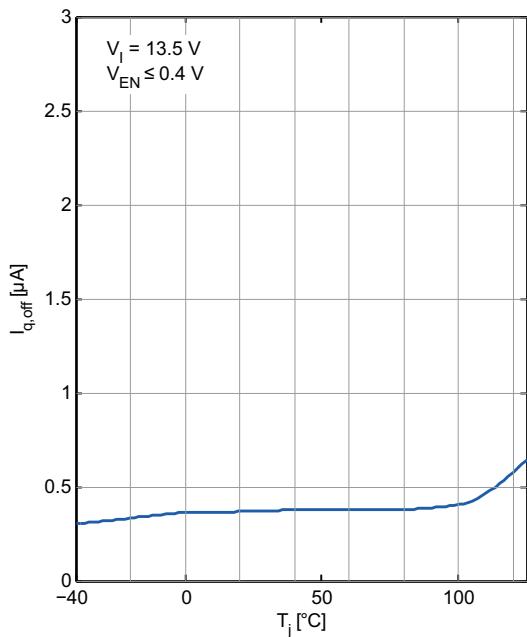


**Current consumption  $I_{q,off}$  versus input voltage  $V_I$  (disabled)**



**Block description and electrical characteristics**

**Current consumption  $I_{q,off}$  versus  
junction temperature  $T_j$  (disabled)**



**Block description and electrical characteristics**

**4.5 Enable function**

The TLS850B0TBV33 can be switched on and off by the enable feature. Applying a high level as specified below (for example, battery voltage) to the EN pin enables the device. Applying a low level as specified below (for example, GND) shuts down the device. If a signal with slow slope is applied to the EN pin, the built-in hysteresis of the enable feature avoids toggling between the ON/OFF states.

**Table 7 Electrical characteristics: enable function**

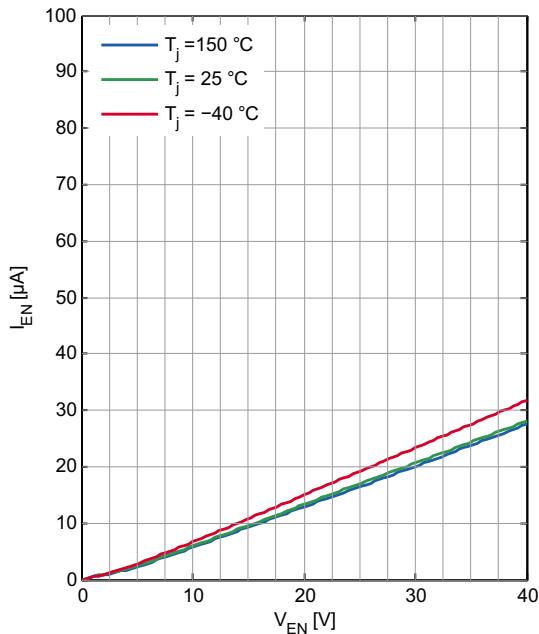
$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_i = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified)  
 Typical values are given at  $T_j = 25^\circ\text{C}$

<b>Parameter</b>	<b>Symbol</b>	<b>Values</b>			<b>Unit</b>	<b>Note or Test Condition</b>	<b>Number</b>
		<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>			
High-level input voltage	$V_{EN,H}$	2	–	–	V	$V_Q$ settled	P_5.5.1
Low-level input voltage	$V_{EN,L}$	–	–	0.8	V	$V_Q \leq 0.1\text{ V}$	P_5.5.2
Enable threshold hysteresis	$V_{EN,Hy}$	90	–	–	mV	–	P_5.5.3
High-level input current	$I_{EN,H}$	–	–	4	$\mu\text{A}$	$V_{EN} = 5\text{ V}$	P_5.5.4
High-level input current	$I_{EN,H}$	–	–	20	$\mu\text{A}$	$V_{EN} \leq 18\text{ V}$	P_5.5.5
Enable internal pull-down resistor	$R_{EN}$	1.25	2	3.5	$\text{M}\Omega$	–	P_5.5.6

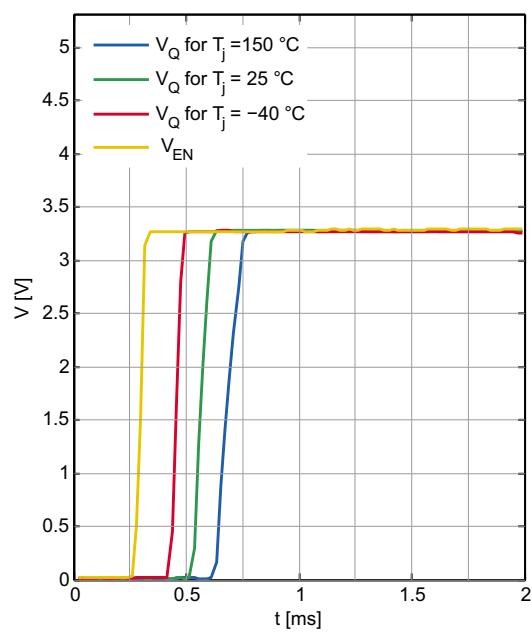
**Block description and electrical characteristics**

**4.6 Typical performance characteristics: enable function**

**Enable input current  $I_{EN}$  versus  
enable input voltage  $V_{EN}$**



**Output voltage  $V_Q$  versus  
time  $t$  (EN switched on)**

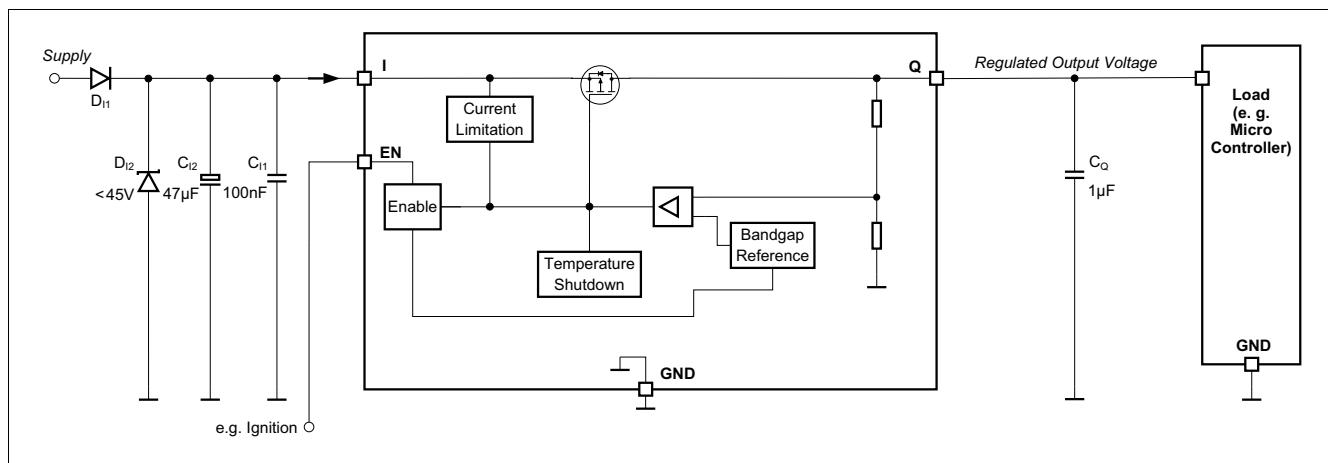


## Application information

### 5 Application information

#### 5.1 Application diagram

**Note:** *The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device.*



**Figure 5 Application diagram**

**Note:** *This is a very simplified example of an application circuit. The function must be verified in the real application.*

#### 5.2 Selection of external components

##### 5.2.1 Input pin

**Figure 5** shows the typical input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter the high frequency disturbances imposed by the line, for example, ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10  $\mu$ F to 470  $\mu$ F is recommended as an input buffer to damp high energy pulses, such as ISO pulse 2a. This capacitor must be placed close to the input pin of the linear voltage regulator.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and to protect the device from damage due to overvoltage.

The external components at the input pin are optional, but they are recommended in case of possible external disturbances.

##### 5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **Table 3**.

## Application information

TLS850B0TBV33 is designed to also be stable with low-ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator's output pin and GND pin, on the same side of the PCB as the regulator itself.

In case of input voltage transients or load current transients, the capacitance should be dimensioned in accordance, and verified in the real application that the output stability requirements are fulfilled.

### 5.3 Thermal considerations

The total power dissipation can be calculated from the known input voltage, the output voltage and the load profile of the application:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (5.1)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  is:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (5.2)$$

with

- $T_{j,max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation, the proper PCB type and the necessary heat sink area can be determined with reference to the specification in [Thermal resistance](#).

### 5.4 Reverse-polarity protection

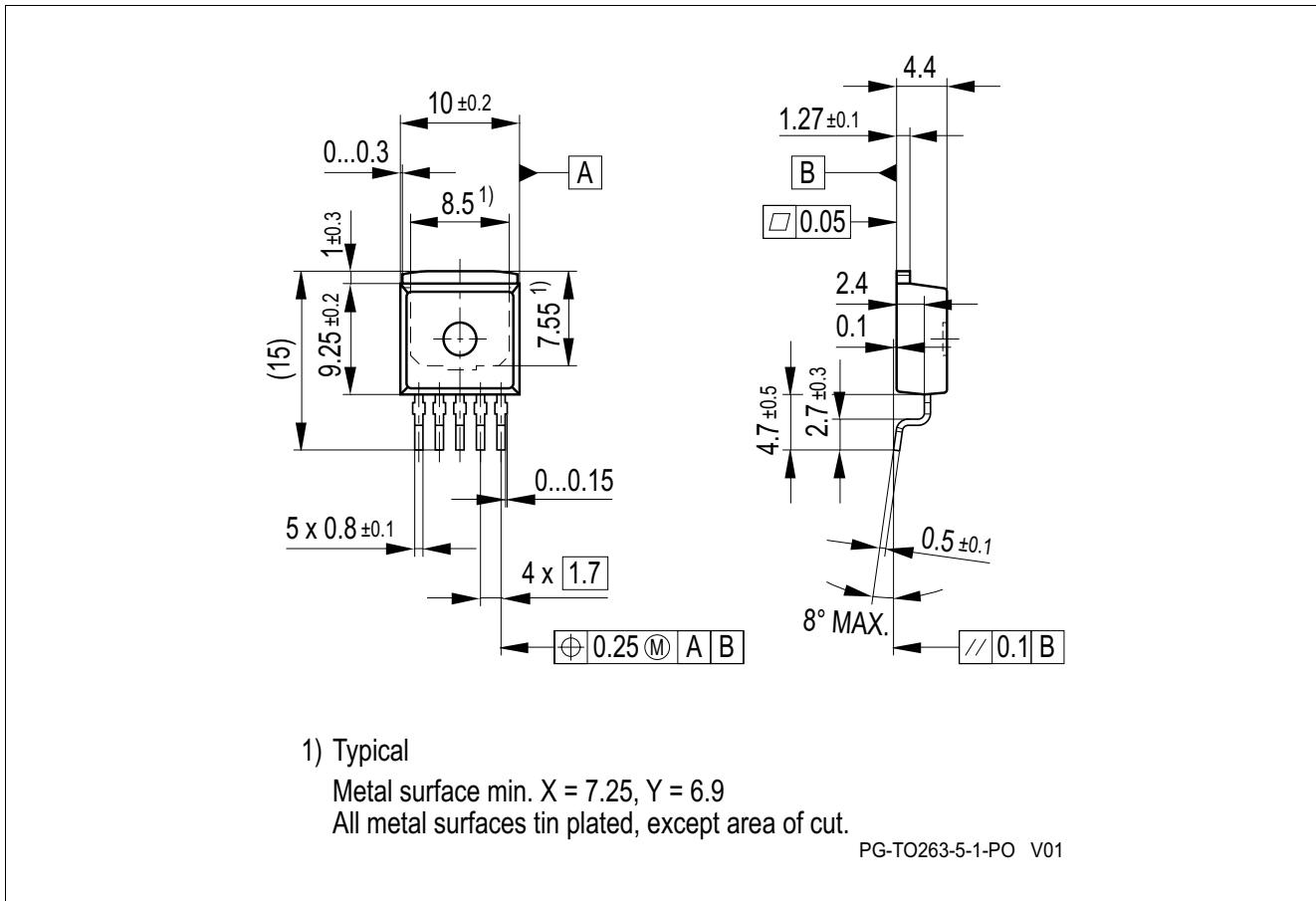
TLS850B0TBV33 is not protected against reverse-polarity faults and must be protected by external components against negative supply voltage. An external reverse-polarity diode is necessary. The absolute maximum ratings of the device as specified in [Absolute maximum ratings](#) must be maintained.

### 5.5 Further application information

For further information, visit <http://www.infineon.com/>

## Package outlines

## 6 Package outlines



**Figure 6 PG-T0263-5<sup>1)</sup>**

### Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## Further information on packages

<https://www.infineon.com/packages>

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### 1) Dimensions in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.01	2024-05-03	Editorial changes and template update
1.00	2017-09-12	Initial version

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**Edition 2024-05-03**

**Published by**

**Infineon Technologies AG  
81726 Munich, Germany**

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**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

**Document reference  
Z8F57667262**

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