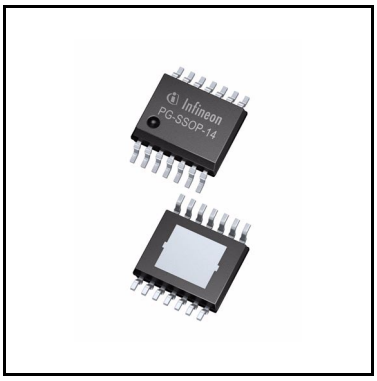
OPTIREG™ linear TLS820F0ELVxx

Low dropout linear voltage regulator



Features

- Wide input voltage range from 3.0 V to 40 V
- Fixed output voltage 5 V or 3.3 V
- Output voltage precision ≤ ±2 %
- Output current capability up to 200 mA
- Ultra low current consumption typ. 40 µA
- Very low dropout voltage typ. 70 mV @100 mA
- Stable with ceramic output capacitor of 1 µF
- Delayed reset at power-on with 2 Programmable delay times 8.5 ms / 16.5 ms
- Adjustable reset threshold down to 2.50 V
- Watchdog with flexible timings and current dependent deactivation: 16 ms / 32 ms / 48 ms / 96 ms, Activated at I_Q > 5.5 mA
- Enable, undervoltage reset, overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green product (RoHS compliant)

Potential applications

- Automotive general ECUs
- Dashboard and cluster supplies
- Powertrain and EPS applications
- Microcontroller supply for safety applications

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ linear TLS820F0ELVxx is a high performance very low dropout linear voltage regulator for 5 V (TLS820F0ELV50) or 3.3 V (TLS820F0ELV33) supply in a PG-SSOP-14 package.

With an input voltage range of 3 V to 40 V and very low quiescent of only 40 µA, these regulators are perfectly suitable for automotive or any other supply systems connected to the battery permanently. The TLS820F0 provides an output voltage accuracy of 2 % and a maximum output current up to 200 mA.

The new loop concept combines fast regulation and very good stability while requiring only one small ceramic capacitor of 1 µF at the output. At currents below 100 mA the device will have a very low typical dropout voltage of only 70 mV (for 5 V device) and 80 mV (for 3.3 V device). The operating range starts already at input voltages of only 3 V (extended operating range). This makes the TLS820F0 also suitable to supply automotive systems that need to operate during cranking condition.

The device can be switched on and off by the enable feature as described in **Chapter 4.5**.

The output voltage is supervised by the reset feature, including undervoltage reset, delayed reset at power-on and an adjustable lower reset threshold. More details can be found in **Chapter 4.7**.

In addition, a watchdog circuit with flexible timings is integrated to monitor the microcontroller‘s operation.

Internal protection features like output current limitation and overtemperature shutdown are implemented to protect the device against immediate damage due to failures like output short circuit to GND, over-current and over-temperatures.

External components

An input capacitor C_I is recommended to compensate line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. TLS820F0 is designed to be also stable with low ESR ceramic capacitors.

Type	Package	Marking
TLS820F0ELV50	PG-SSOP-14	820F0V50
TLS820F0ELV33	PG-SSOP-14	820F0V33

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1 Block diagram

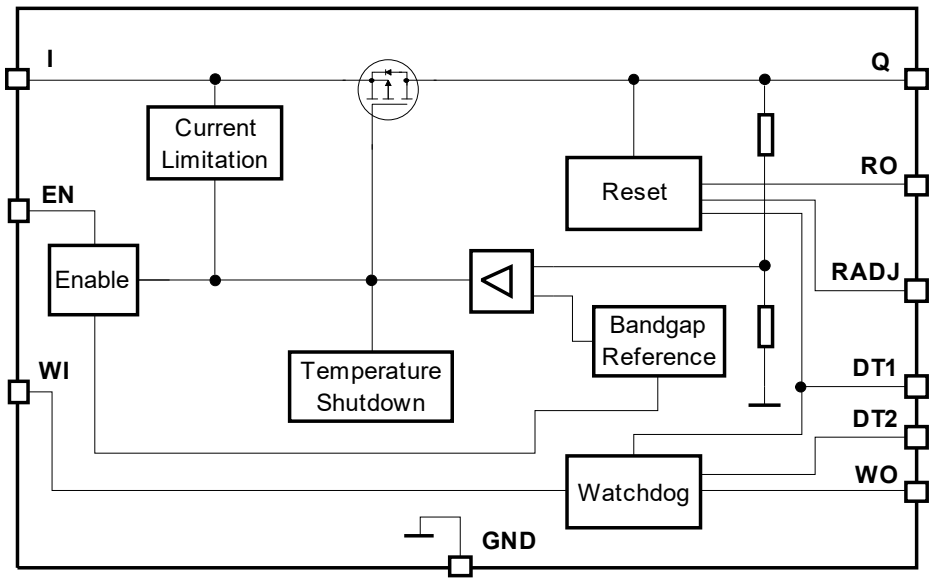


Figure 1 Block diagram TLS820F0ELV50 and TLS820F0ELV33

2 Pin configuration

2.1 Pin assignment TLS820F0ELV50 and TLS820F0ELV33

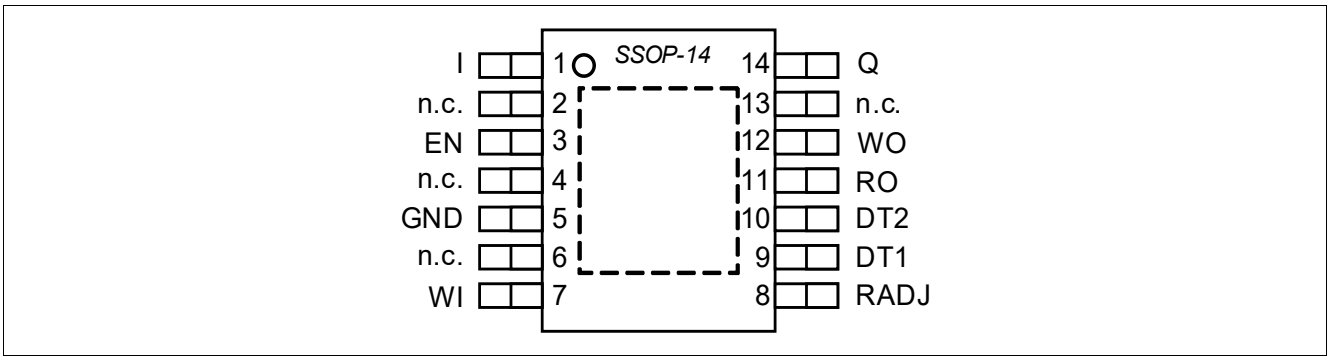


Figure 2 Pin configuration

2.2 Pin definitions and functions TLS820F0ELV50 and TLS820F0ELV33

Pin	Symbol	Function
1	I	**Input** It is recommended to place a small ceramic capacitor (e.g. 100 nF) to GND, close to the IC terminals, in order to compensate line influences. See also **Chapter 5.2.1**
2, 4, 6	n.c.	**Not connected** Leave open or connect to GND
3	EN	**Enable** (integrated pull-down resistor) Enable the IC with high level input signal; Disable the IC with low level input signal;
5	GND	**Ground**
7	WI	**Watchdog input** (integrated pull-down resistor) Serve Watchdog with trigger input signal (usable for microcontroller monitoring)
8	RADJ	**Reset threshold adjustment** Connect to GND to use standard value; Connect an external voltage divider to adjust reset threshold
9	DT1	**Delay timing 1** (integrated pull-down resistor) Connect to GND or Q to select Reset timing acc. to **Table 8** Connect to GND or Q to select Watchdog timing acc. to **Table 11**
10	DT2	**Delay timing 2** (integrated pull-down resistor) Connect to GND or Q to select Watchdog timing acc. to **Table 11**
11	RO	**Reset output** (integrated pull-up resistor to Q) Open collector output; Leave open if the reset function is not needed

Pin configuration

Pin	Symbol	Function
12	WO	**Watchdog output** (integrated pull-up resistor to Q) Open collector output; Leave open if the watchdog function is not needed
13	n.c.	**Not connected** Leave open or connect to GND
14	Q	**Output voltage** Connect output capacitor C_Q to GND close to the IC's terminals, respecting the values specified for its capacitance and ESR in **"Functional range" on Page 8**
Pad	–	**Exposed pad** Connect to heatsink area; Connect to GND

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, Enable EN							
Voltage	V_I, V_{EN}	-0.3	–	45	V	–	P_4.1.1
Output Q, Watchdog output WO							
Voltage	V_Q, V_{RO}, V_{WO}	-0.3	–	7	V	–	P_4.1.3
Watchdog input WI, Delay timing DT1 and DT2, Reset threshold adjustment RADJ							
Voltage	V_{WI},V_{DT1}, V_{DT2}, V_{RADJ}	-0.3	–	7	V	–	P_4.1.5
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.7
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.8
ESD absorption							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	2) HBM	P_4.1.9
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	3) CDM	P_4.1.10
ESD susceptibility pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750	–	750	V	3) CDM	P_4.1.11

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 2 Functional range

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	$V_{Q,nom} + V_{dr}$	–	40	V	1) –	P_4.2.1
Extended input voltage range	$V_{I,ext}$	3.0	–	40	V	2) –	P_4.2.3
Enable voltage range	V_{EN}	0	–	40	V	–	P_4.2.5
Output capacitor's requirements for stability	C_Q	1	–	–	µF	3)4) –	P_4.2.6
ESR	$ESR(C_Q)$	–	–	100	Ω	3) –	P_4.2.7
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.9

1) Output current is limited internally and depends on the input voltage, see Electrical Characteristics for more details.
2) When V_I is between $V_{I,ext,min}$ and $V_{Q,nom} + V_{dr}$, $V_Q = V_I - V_{dr}$. When V_I is below $V_{I,ext,min}$, V_Q can drop down to 0 V.
3) Not subject to production test, specified by design.
4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Package version PG-SSOP-14							
Junction to case	R_{thJC}	–	9	–	K/W	1) –	P_4.3.1
Junction to ambient	R_{thJA}	–	43	–	K/W	1)2) 2s2p board	P_4.3.2
Junction to ambient	R_{thJA}	–	128	–	K/W	1)3) 1s0p board, footprint only	P_4.3.3
Junction to ambient	R_{thJA}	–	58	–	K/W	1)3) 1s0p board, 300 mm^2 heatsink area on PCB	P_4.3.4
Junction to ambient	R_{thJA}	–	50	–	K/W	1)3) 1s0p board, 600 mm^2 heatsink area on PCB	P_4.3.5

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor (ESR) requirements given in **"Functional range" on Page 8** have to be maintained. For details, also see the typical performance graph **"Output capacitor series resistor ESR(CQ) versus output current IQ" on Page 15**. As the output capacitor also has to buffer load steps, it should be sized according to the application's needs.

An input capacitor C_I is recommended to compensate line influences. In order to block influences like pulses and HF distortion at input side, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

In order to prevent overshoots during start-up, a smooth ramp up function is implemented. This ensures almost no output voltage overshoots during start-up, mostly independent from load and output capacitance.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuit) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

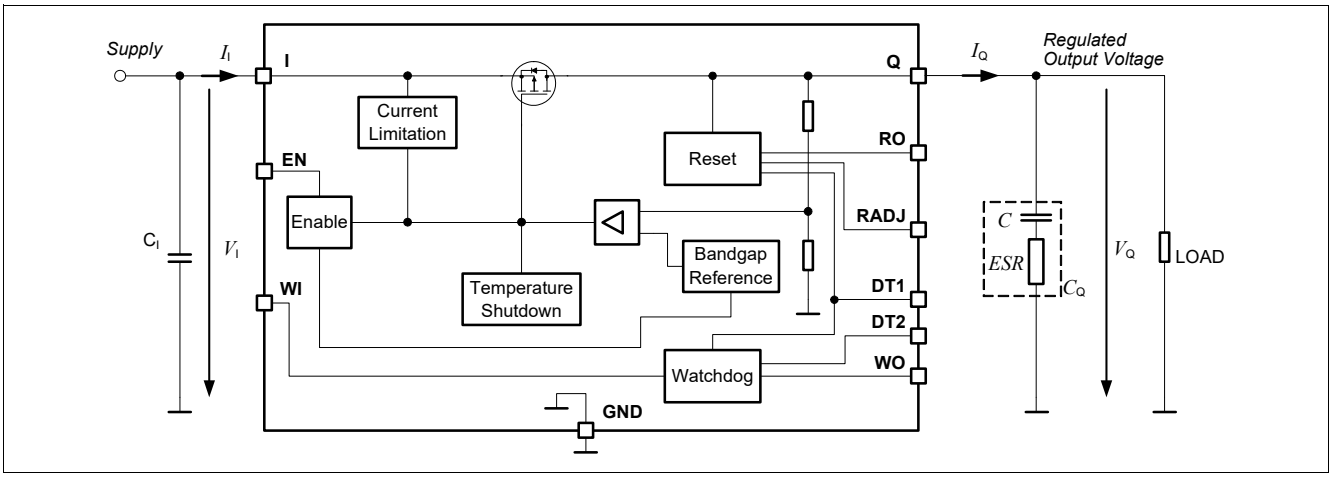


Figure 3 Voltage regulation

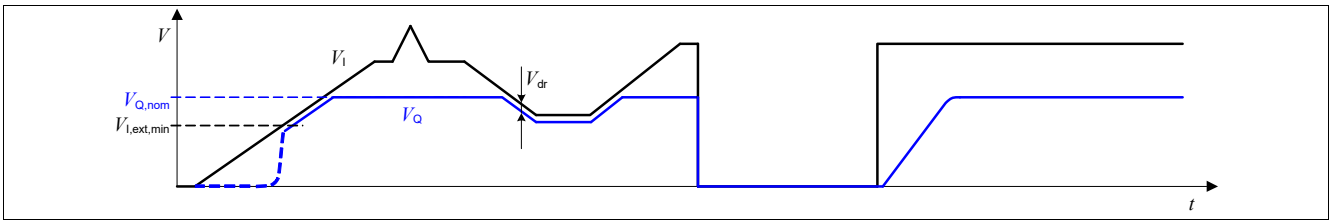


Figure 4 Output voltage vs. input voltage

Table 4 Electrical characteristics voltage regulator 5 V version

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage precision	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 200 mA 5.44 V < V_I < 28 V	P_5.1.1
Output Voltage Precision	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 100 mA 5.27 V < V_I < 40 V	P_5.1.2
Output voltage start-up slew rate	dV_Q/dt	3.0	7.5	18	V/ms	V_I > 18 V/ms C_Q = 1 µF 0.5 V < V_Q < 4.5 V	P_5.1.7
Output current limitation	$I_{Q,max}$	201	350	550	mA	0 V < V_Q < 4.8 V	P_5.1.8
Load regulation steady-state	$\Delta V_{Q,load}$	-15	-1.5	5	mV	I_Q = 0.05 mA to 200 mA V_I = 6 V	P_5.1.10
Line regulation steady-state	$\Delta V_{Q,line}$	-25	0	25	mV	V_I = 8 V to 32 V I_Q = 1 mA	P_5.1.12
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	140	340	mV	[1] I_Q = 200 mA	P_5.1.14
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	70	170	mV	[1] I_Q = 100 mA	P_5.1.15
Power supply ripple rejection	*PSRR*	–	59	–	dB	[2] f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp	P_5.1.18
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	[2] T_j increasing	P_5.1.19
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	[2] T_j decreasing	P_5.1.20

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5V
2) Not subject to production test, specified by design

Table 5 Electrical characteristics voltage regulator 3.3 V version

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

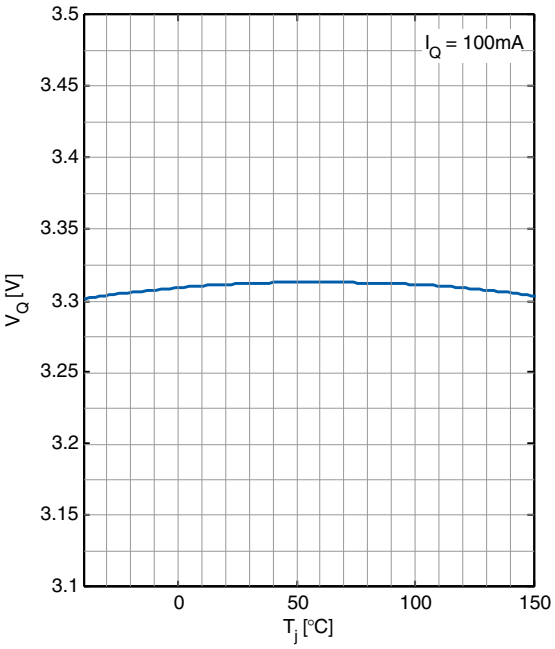
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage precision	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 200 mA 3.72 V < V_I < 28 V	P_5.1.21
Output voltage precision	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 100 mA 3.55 V < V_I < 40 V	P_5.1.22
Output voltage start-up slew rate	dV_Q/dt	3.0	7.5	18	V/ms	V_I > 18 V/ms C_Q = 1 µF 0.33 V < V_Q < 2.97 V	P_5.1.27
Output current limitation	$I_{Q,max}$	201	350	550	mA	0 V < V_Q < 3.1 V	P_5.1.28
Load regulation steady-state	$\Delta V_{Q,load}$	-15	-1.5	5	mV	I_Q = 0.05 mA to 200 mA V_I = 6 V	P_5.1.30
Line regulation steady-state	$\Delta V_{Q,line}$	-20	0	20	mV	V_I = 8 V to 32 V I_Q = 1 mA	P_5.1.32
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	160	350	mV	[1] I_Q = 200 mA	P_5.1.34
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	80	175	mV	[1] I_Q = 100 mA	P_5.1.35
Power supply ripple rejection	*PSRR*	–	63	–	dB	[2] f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp	P_5.1.38
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	[2] T_j increasing	P_5.1.39
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	[2] T_j decreasing	P_5.1.40

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5V
2) Not subject to production test, specified by design

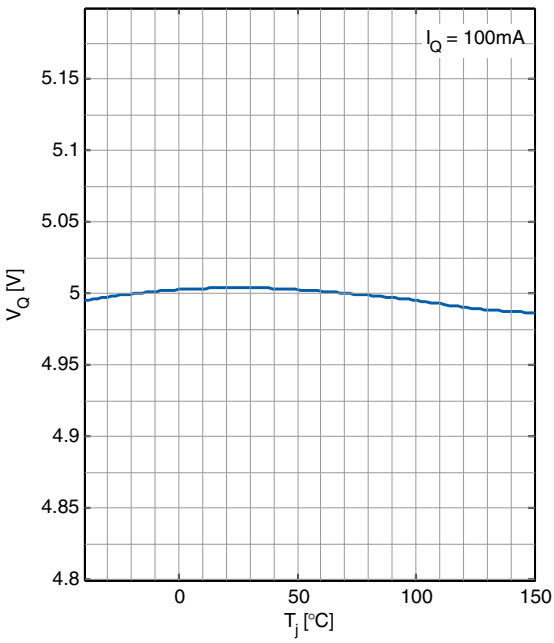
4.2 Typical performance characteristics voltage regulator

Typical performance characteristics

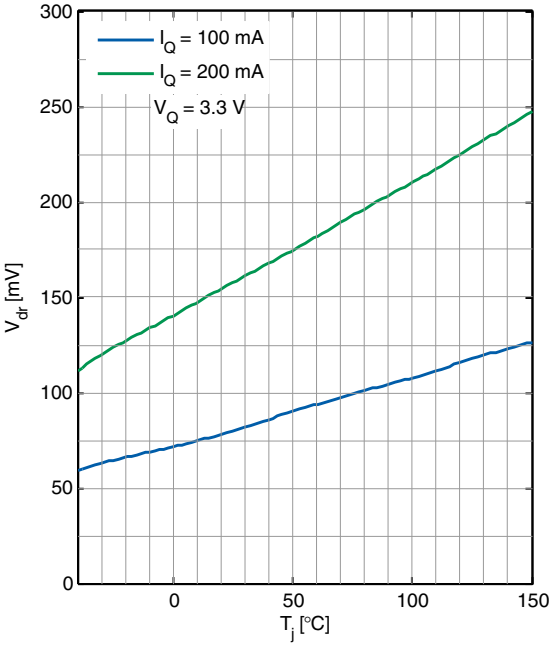
Output voltage V_Q versus junction temperature T_j (3.3 V version)



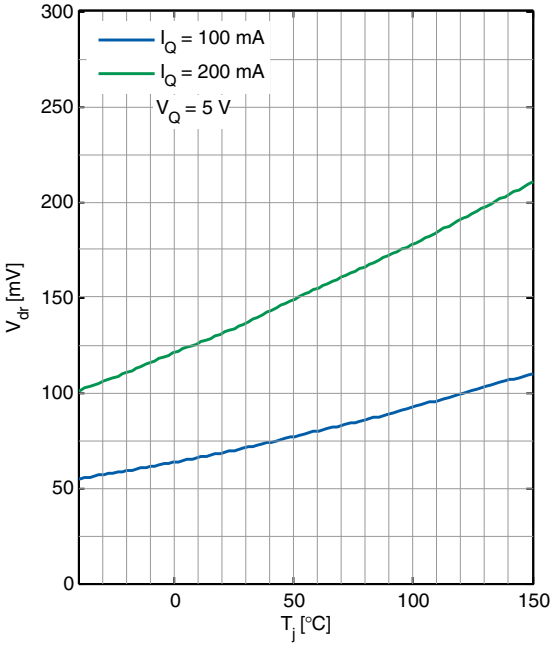
Output voltage V_Q versus junction temperature T_j (5 V version)



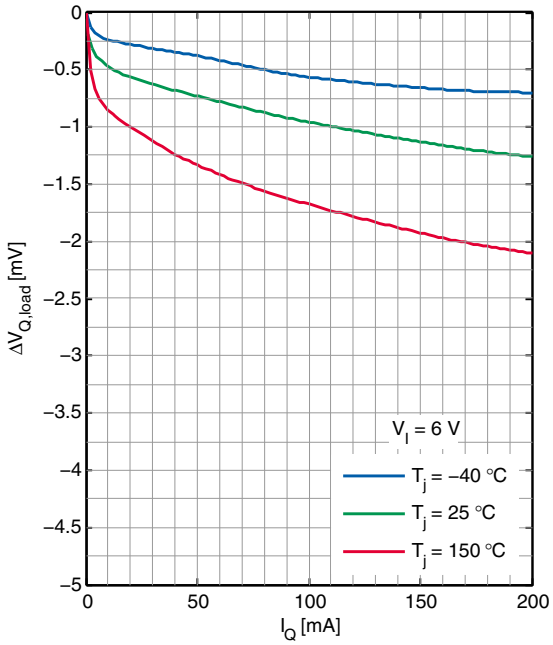
Dropout voltage V_{dr} versus junction temperature T_j (3.3 V version)



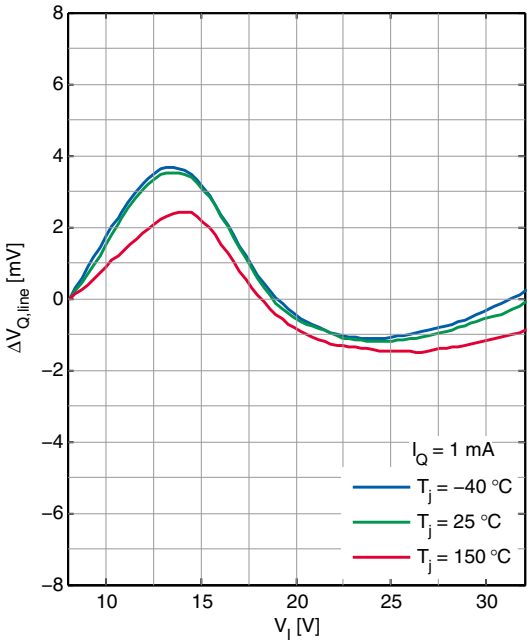
Dropout voltage V_{dr} versus junction temperature T_j (5 V version)



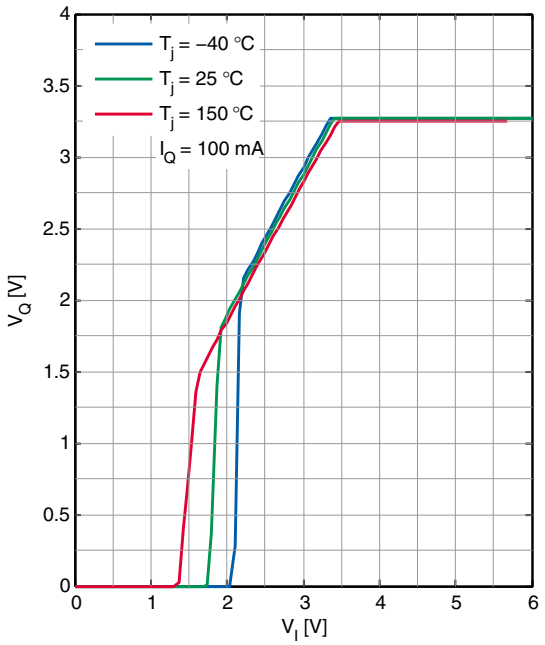
Load regulation $\Delta V_{Q,load}$ versus output current change I_Q



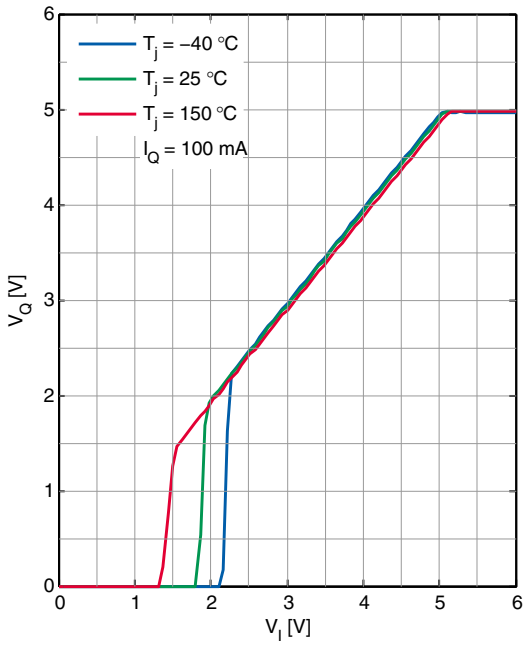
Line regulation $\Delta V_{Q,line}$ versus input voltage V_I



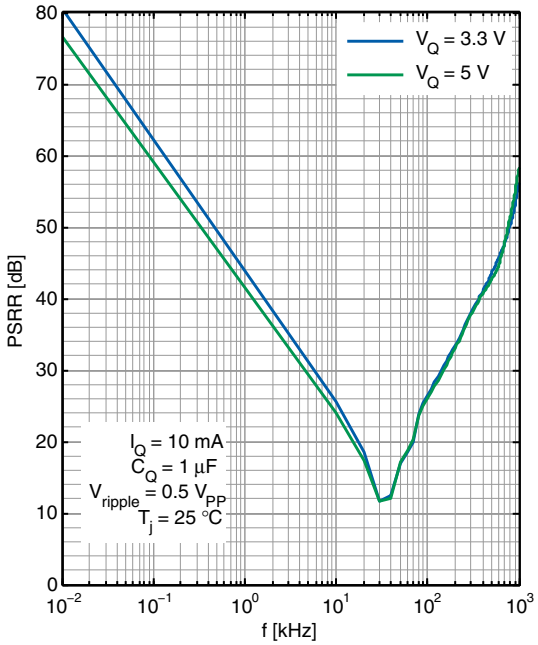
Output voltage V_Q versus Input voltage V_I (3.3 V version)



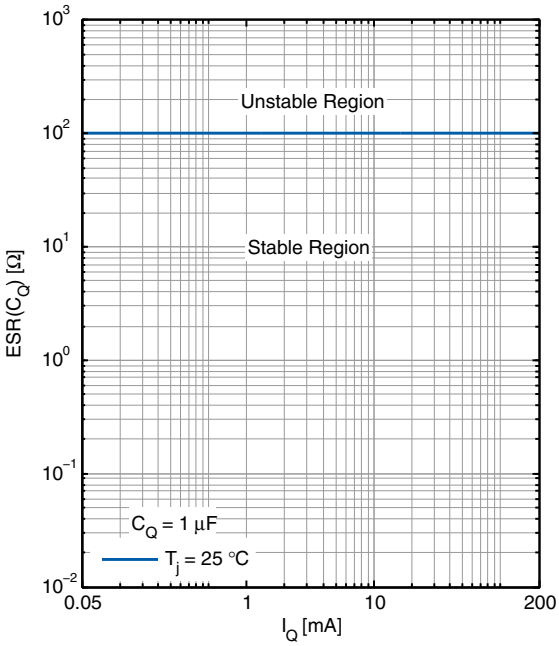
Output voltage V_Q versus Input voltage V_I (5 V version)



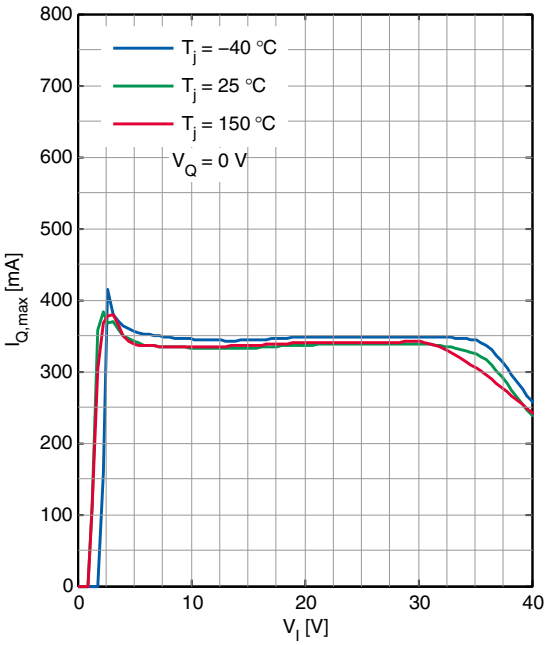
Power supply ripple rejection *PSRR* versus ripple frequency *f*



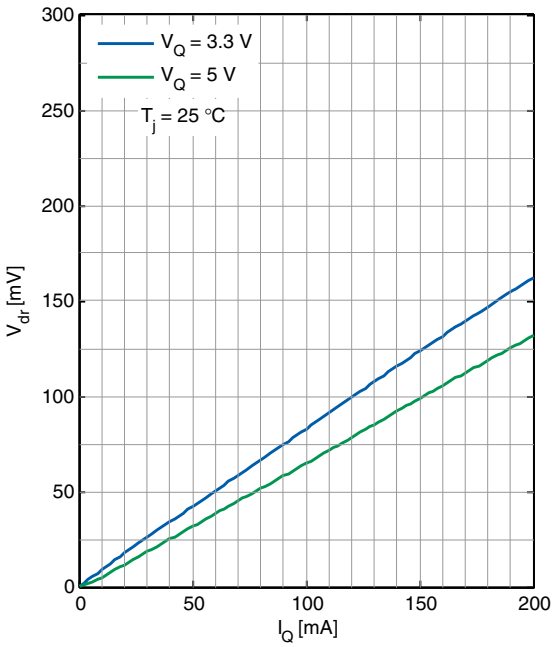
Output capacitor series resistor *ESR*(C_Q) versus output current I_Q



Maximum output current I_Q versus input voltage V_I



Dropout voltage V_{dr} versus output current I_Q



4.3 Current consumption

Table 6 Electrical characteristics current consumption

T_j = -40°C to 150°C, V_I = 13.5 V (unless otherwise specified)
Typical values are given at T_j = 25 °C
Conditions of other pins: DT1 = DT2 = WI = GND

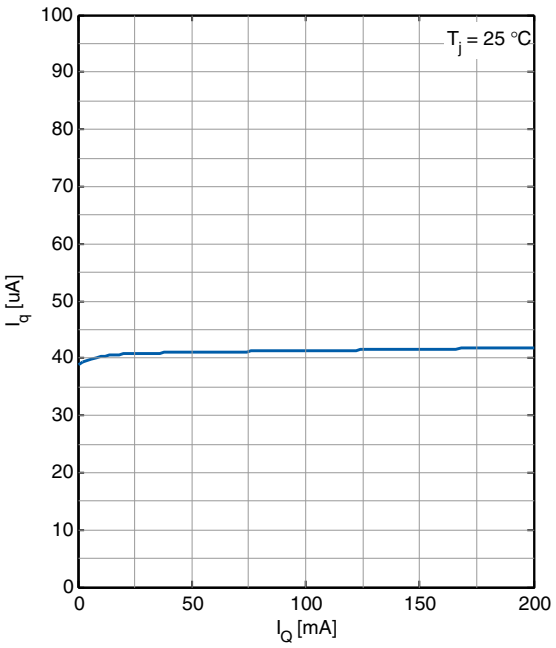
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I$	$I_{q,off}$	–	1.3	5	µA	V_{EN} = 0 V; T_j < 105 °C	P_5.3.1
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	8	µA	V_{EN} = 0.4 V; T_j < 125 °C	P_5.3.3
Current consumption $I_q = I_I - I_Q$	I_q	–	40	52	µA	I_Q = 0.05 mA T_j = 25 °C	P_5.3.4
Current consumption $I_q = I_I - I_Q$	I_q	–	62	77	µA	I_Q = 0.05 mA T_j < 125 °C	P_5.3.7
Current consumption $I_q = I_I - I_Q$	I_q	–	62	80	µA	[1] I_Q = 200 mA T_j < 125 °C	P_5.3.9

1) Not subject to production test, specified by design

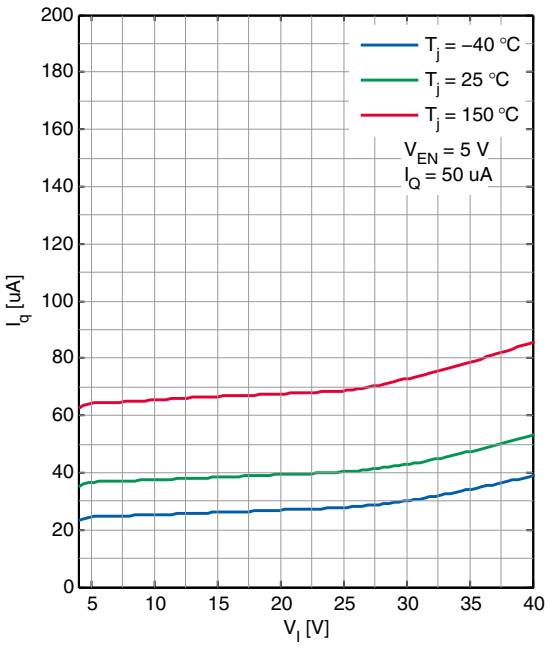
4.4 Typical performance characteristics current consumption

Typical performance characteristics

Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I



4.5 Enable

The TLS820F0 can be switched on and off by the enable feature: connect a HIGH level as specified below (e.g. the battery voltage) to pin EN to enable the device; connect a LOW level as specified below (e.g. GND) to shut it down. The enable has a built in hysteresis to avoid toggling between ON/OFF state, if signals with slow slopes are applied to the EN input.

Table 7 Electrical characteristics enable

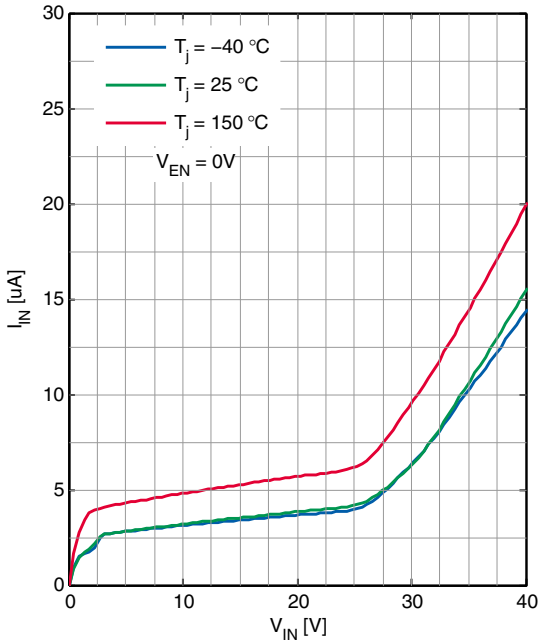
T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High level input voltage	$V_{EN,H}$	2	–	–	V	V_Q settled	P_5.5.1
Low level input voltage	$V_{EN,L}$	–	–	0.8	V	$V_Q \leq 0.1$ V	P_5.5.2
Enable threshold hysteresis	$V_{EN,Hy}$	100	–	–	mV	–	P_5.5.3
High level input current	$I_{EN,H}$	–	–	3.5	µA	V_{EN} = 3.3 V	P_5.5.4
High level input current	$I_{EN,H}$	–	–	22	µA	$V_{EN} \leq 18$ V	P_5.5.6
Enable internal pull-down resistor	R_{EN}	0.95	1.5	2.6	MΩ	–	P_5.5.7

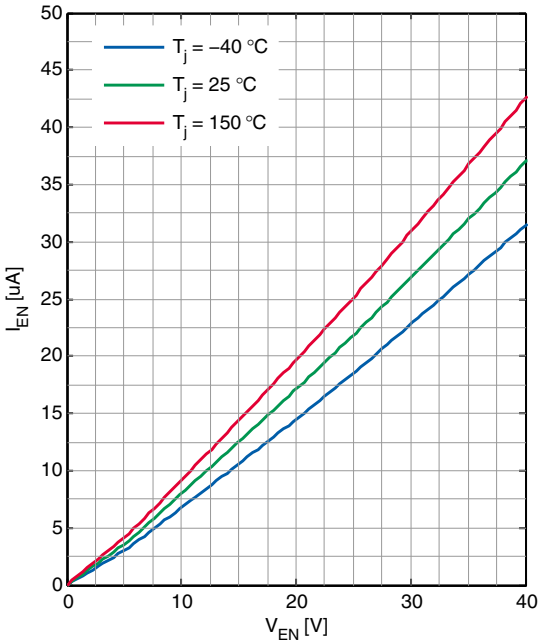
4.6 Typical performance characteristics enable

Typical performance characteristics

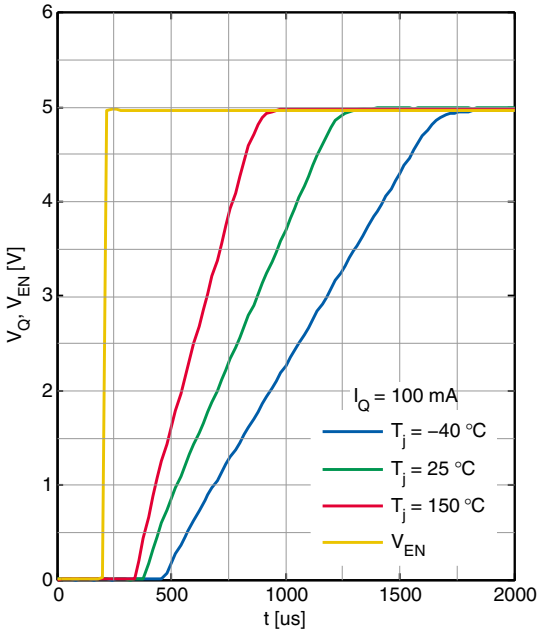
Input current I_{IN} versus input voltage V_{IN} (condition: V_{EN} = 0 V)



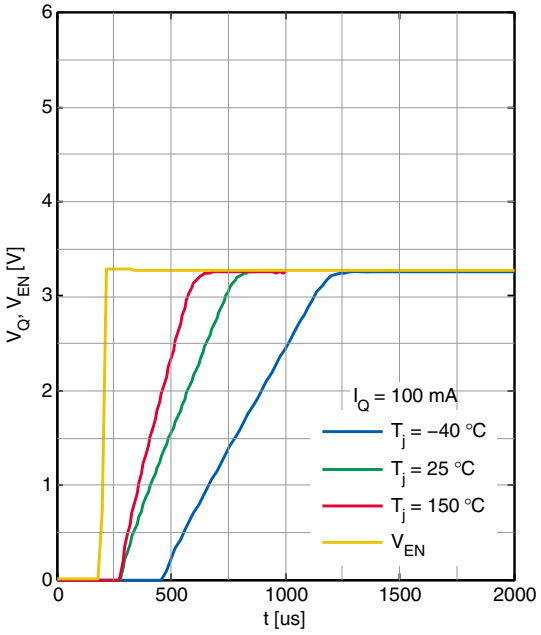
Enable input current I_{EN} versus enable input voltage V_{EN}



Output voltage V_Q versus time (EN switched ON, 5 V version)



Output voltage V_Q versus time (EN switched ON, 3.3 V version)



4.7 Reset

The TLS820F0's output voltage is supervised by the reset feature, including undervoltage reset, delayed reset at power-on and an adjustable reset threshold.

The undervoltage reset function sets the pin RO to LOW, in case V_Q is falling for any reason below the reset threshold $V_{RT,low}$.

When the regulator is powered on, the pin RO is held at LOW for the duration of the power-on reset delay time t_{rd}.

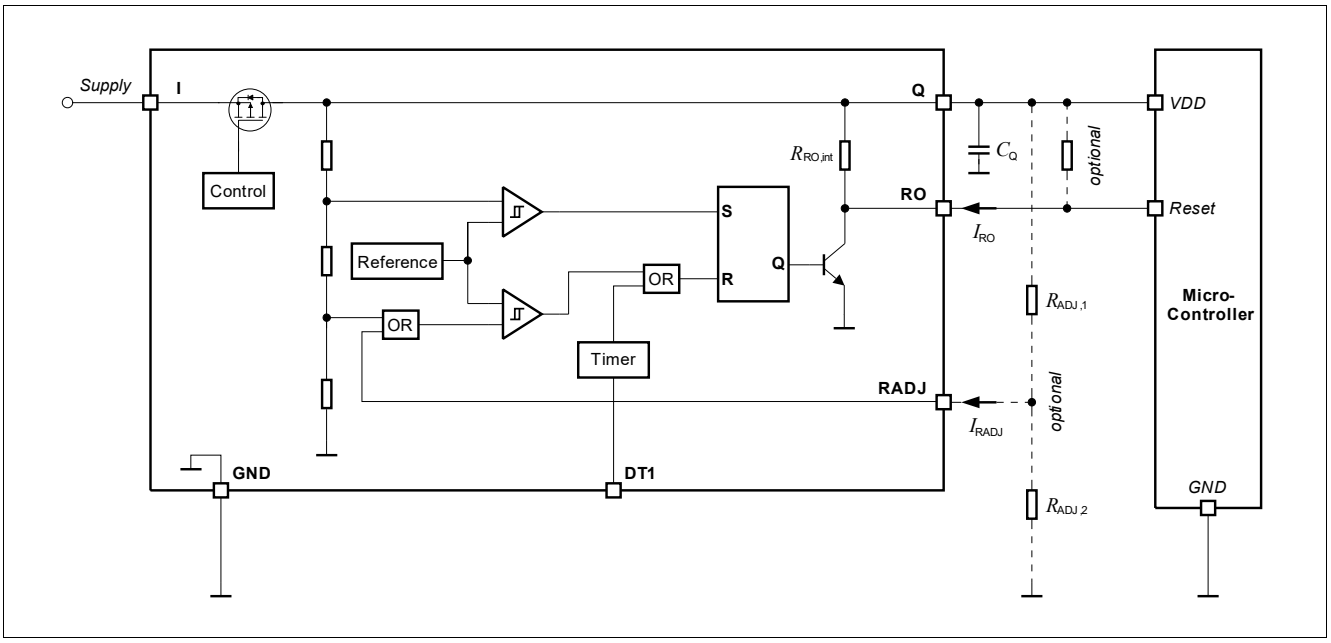


Figure 5 Block diagram reset circuit

Reset delay time

The pin DT1 is used to set the desired reset delay time t_{rd}. Connect this pin either to GND or Q to select the timing according to **Table 8**.

Table 8 Reset delay time selection

DT1 connected to	t_{rd}
GND	16.5 ms
Q	8.5 ms

Power-on reset delay time

The power-on reset delay time is defined by the parameter t_{rd} and allows a microcontroller and oscillator to start up. This delay time is the time period from exceeding the upper reset switching threshold $V_{RT,high}$ until the reset is released by switching the reset output "RO" from "LOW" to "HIGH".

Undervoltage reset delay time

The undervoltage reset delay time is defined by the parameter t_{rd}. It is the time interval from exceeding the reset switching threshold $V_{RT,high}$ until the reset is released by switching the reset output from low to high.

Reset blanking time

The reset blanking time $t_{rr,blank}$ avoids that short undervoltage spikes trigger an unwanted reset "low" signal.

Reset reaction time

In case the output voltage of the regulator drops below the output undervoltage lower reset threshold $V_{RT,low}$, the reset output “RO” is set to low, after the delay of the internal reset reaction time $t_{rr,int}$. The reset blanking time $t_{rr,blank}$ is part of the reset reaction time $t_{rr,int}$.

Reset output “RO”

The reset output “RO” is an open collector output with an integrated pull-up resistor. In case a lower-ohmic “RO” signal is desired, an external pull-up resistor can be connected to the output “Q”. Since the maximum “RO” sink current is limited, the minimum value of the optional external resistor “$R_{RO,ext}$” is given in **Table “Reset output RO” on Page 23**.

Reset output “RO” low for VQ ≥ 1 V

In case of an undervoltage reset condition reset output “RO” is held “low” for $V_Q \geq 1$ V, even if the input “I” is not supplied and the voltage V_I drops below 1 V. This is achieved by supplying the reset circuit from the output capacitor.

Reset adjust function

The undervoltage reset switching threshold can be adjusted according to the application’s needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin “RADJ”. For selecting the default threshold connect pin “RADJ” to GND. The reset adjustment range for the TLS820F0ELV50 is given in **Reset threshold adjustment range**. The reset adjustment range for the TLS820F0ELV33 is given in **Reset threshold adjustment range**.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows (neglecting the Reset adjust pin current I_{RADJ}):

$$V_{RT,lo,new} = V_{RADJ,th} \times (R_{ADJ,1} + R_{ADJ,2}) / R_{ADJ,2} \quad (4.1)$$

with

- $V_{RT,lo,new}$: Desired undervoltage reset switching threshold.
- $R_{ADJ,1}$, $R_{ADJ,2}$: Resistors of the external voltage divider, see **Figure 5**.
- $V_{RADJ,th}$: Reset adjust switching threshold given in **Reset adjustment switching threshold**.

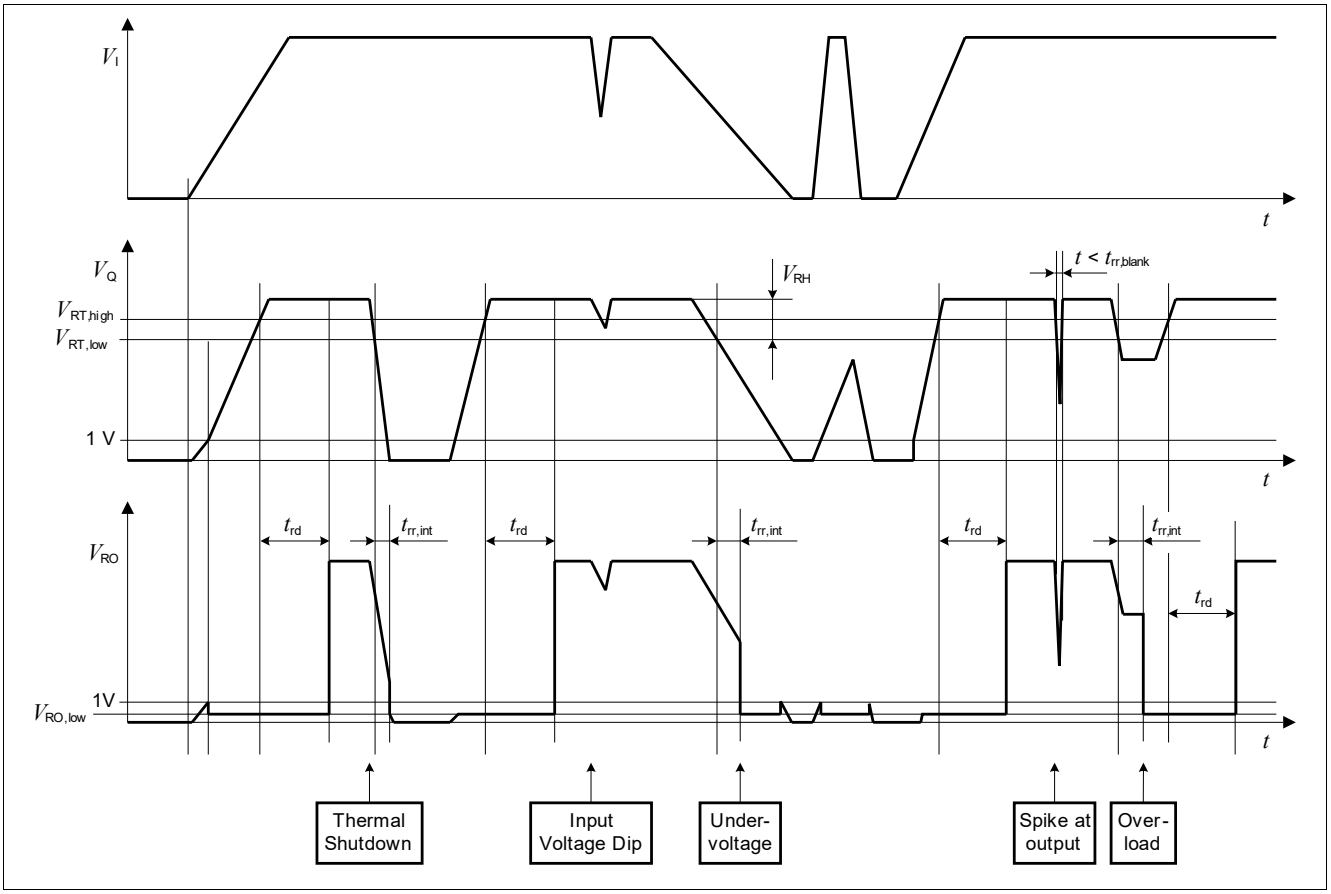


Figure 6 Typical timing diagram reset

Table 9 Electrical characteristics reset

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output undervoltage reset 5V version only							
Output undervoltage reset upper switching threshold	$V_{RT,high}$	4.6	4.7	4.8	V	V_Q increasing	P_5.7.1
Output undervoltage reset lower switching threshold - default	$V_{RT,low}$	4.5	4.6	4.7	V	V_Q decreasing RADJ = GND	P_5.7.2
Output undervoltage reset switching hysteresis	$V_{RT,hy}$	60	100	–	mV	RADJ connected to GND	P_5.7.3
Output undervoltage reset headroom V_Q - V_{RT}	V_{RH}	200	400	–	mV	RADJ = GND	P_5.7.4
Output undervoltage reset 3V3 version only							
Output undervoltage reset upper switching threshold	$V_{RT,high}$	3.08	3.15	3.22	V	V_Q increasing	P_5.7.5
Output undervoltage reset lower switching threshold - default	$V_{RT,low}$	3.0	3.05	3.13	V	V_Q decreasing RADJ = GND	P_5.7.6
Output undervoltage reset switching hysteresis	$V_{RT,hy}$	60	100	–	mV	RADJ connected to GND	P_5.7.7
Output undervoltage reset headroom V_Q - V_{RT}	V_{RH}	100	250	–	mV	RADJ = GND	P_5.7.8
Reset threshold adjustment							
Reset adjustment switching threshold	$V_{RADJ,th}$	1.15	1.20	1.25	V	–	P_5.7.9
Reset threshold adjustment range	$V_{RT,range}$	2.5	–	4.4	V	for $V_{Q,nom}$ = 5 V	P_5.7.10
Reset threshold adjustment range	$V_{RT,range}$	2.5	–	2.9	V	for $V_{Q,nom}$ = 3.3 V	P_5.7.11
Reset output RO							
Reset output low voltage	$V_{RO,low}$	–	0.2	0.4	V	1 V ≤ V_Q ≤ V_{RT}; R_{RO} ≥ 5.1 kΩ	P_5.7.12
Reset output internal pull-up resistor	$R_{RO,int}$	13	20	36	kΩ	internally connected to Q	P_5.7.13
Reset output external pull-up resistor to V_Q	$R_{RO,ext}$	5.1	–	–	kΩ	1 V ≤ V_Q ≤ V_{RT}; V_{RO} ≤ 0.4 V	P_5.7.14
Reset delay timing							
Reset delay time	$t_{rd,slow}$	13.2	16.5	19.8	ms	DT1 connected to GND	P_5.7.20
Reset delay time	$t_{rd,fast}$	6.8	8.5	10.2	ms	DT1 connected to Q	P_5.7.21
Reset blanking time	$t_{rr,blank}$	–	6	–	µs	[1] for $V_{Q,nom}$ = 3.3 V	P_5.7.22
Reset blanking time	$t_{rr,blank}$	–	7	–	µs	[2] for $V_{Q,nom}$ = 5 V	P_5.7.46
Internal reset reaction time	$t_{rr,int}$	–	7	20	µs	for $V_{Q,nom}$ = 3.3 V	P_5.7.23
Internal reset reaction time	$t_{rr,int}$	–	10	33	µs	for $V_{Q,nom}$ = 5 V	P_5.7.36

Table 9 Electrical characteristics reset (cont'd)

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

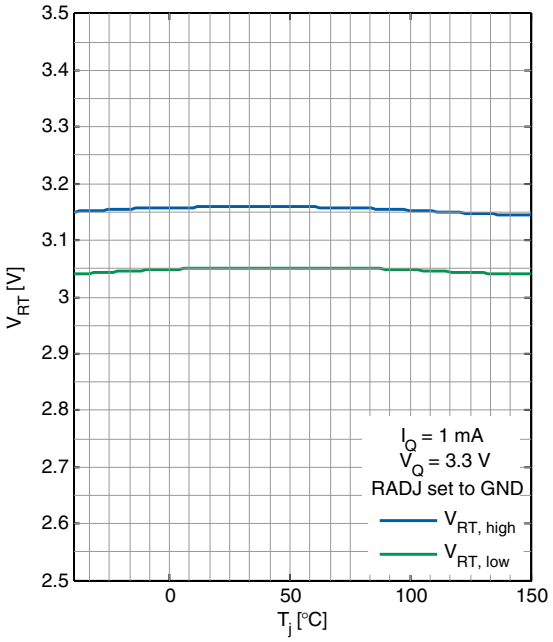
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset delay input DT1							
Delay input DT1 high signal valid	$V_{DT1,H}$	2.0	–	–	V	–	P_5.7.24
Delay input DT1 low signal valid	$V_{DT1,L}$	–	–	0.80	V	–	P_5.7.25
Delay input DT1 signal slew rate	dV_{DT1}/dt	1	–	–	V/µs	$V_{DT1,L} < V_{DT1} < V_{DT1,H}$	P_5.7.34
High level input current	$I_{DT1,H}$	–	–	3.5	µA	V_{DT1} = 3.3 V	P_5.7.27
Delay input DT1 internal pull-down resistor	R_{DT1}	0.9	1.5	2.6	MΩ	–	P_5.7.28

1) Not subject to production test, specified by design.
2) Not subject to production test, specified by design.

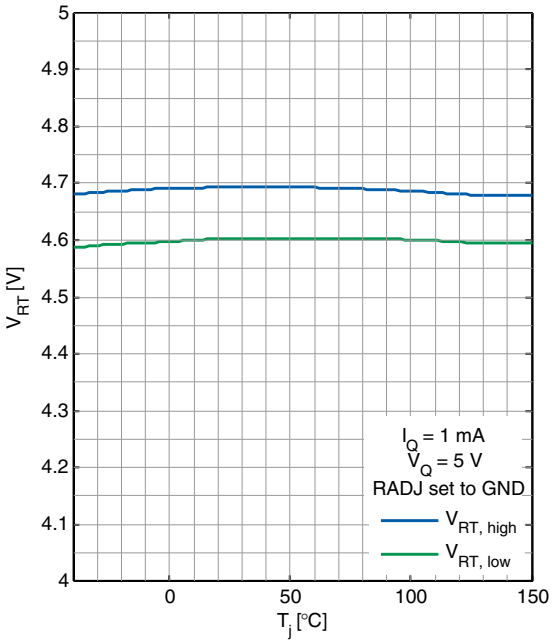
4.8 Typical performance characteristics reset

Typical performance characteristics

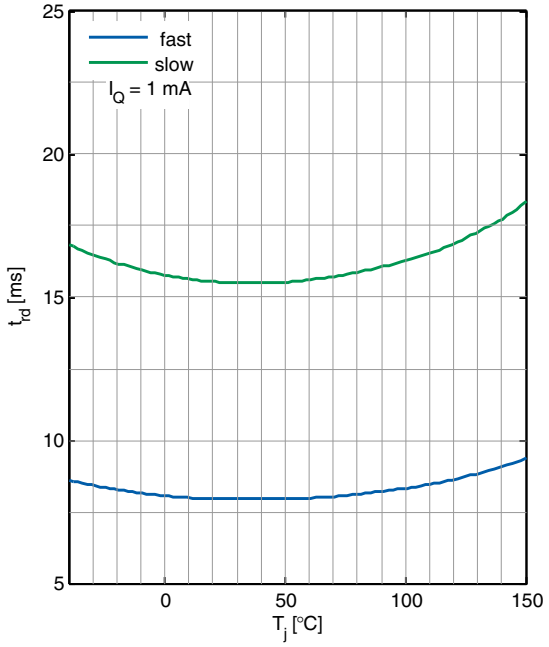
Undervoltage reset threshold V_{RT} versus junction temperature T_j (3.3 V version)



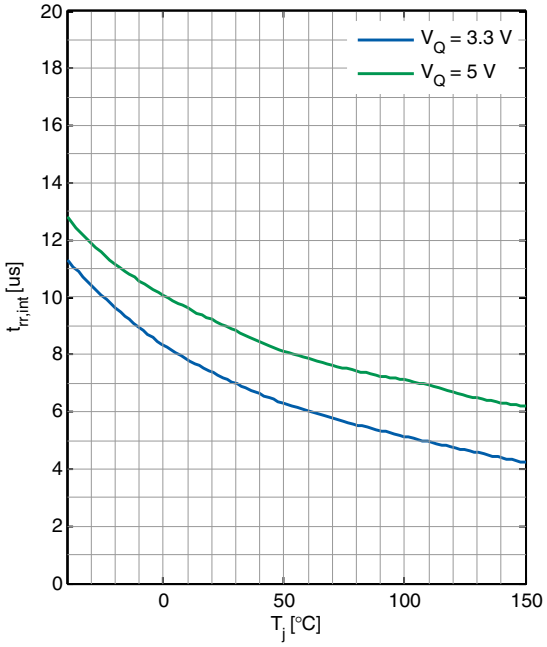
Undervoltage reset threshold V_{RT} versus junction temperature T_j (5 V version)



Power-on reset delay time t_{rd} versus junction temperature T_j



Internal reset reaction time $t_{rr,int}$ versus junction temperature T_j



4.9 Standard watchdog

The TLS820F0 features a load dependent watchdog function with a programmable watchdog timing. The watchdog function monitors a microcontroller, including time base failures. In case of a missing falling edge within a certain pulse repetition time, the watchdog output “WO” is set to “low”.

The watchdog uses an internal oscillator as timebase. The effective trigger window is derived from the watchdog timebase and can be adjusted by using the pins DT1 and DT2.

The watchdog output “WO” is separated from the reset output “RO”. Hence, the watchdog output might be used as an interrupt signal for the microcontroller independent from the reset signal. It is possible to interconnect pin “WO” and pin “RO” in order to establish a wire-or function with a dominant low signal.

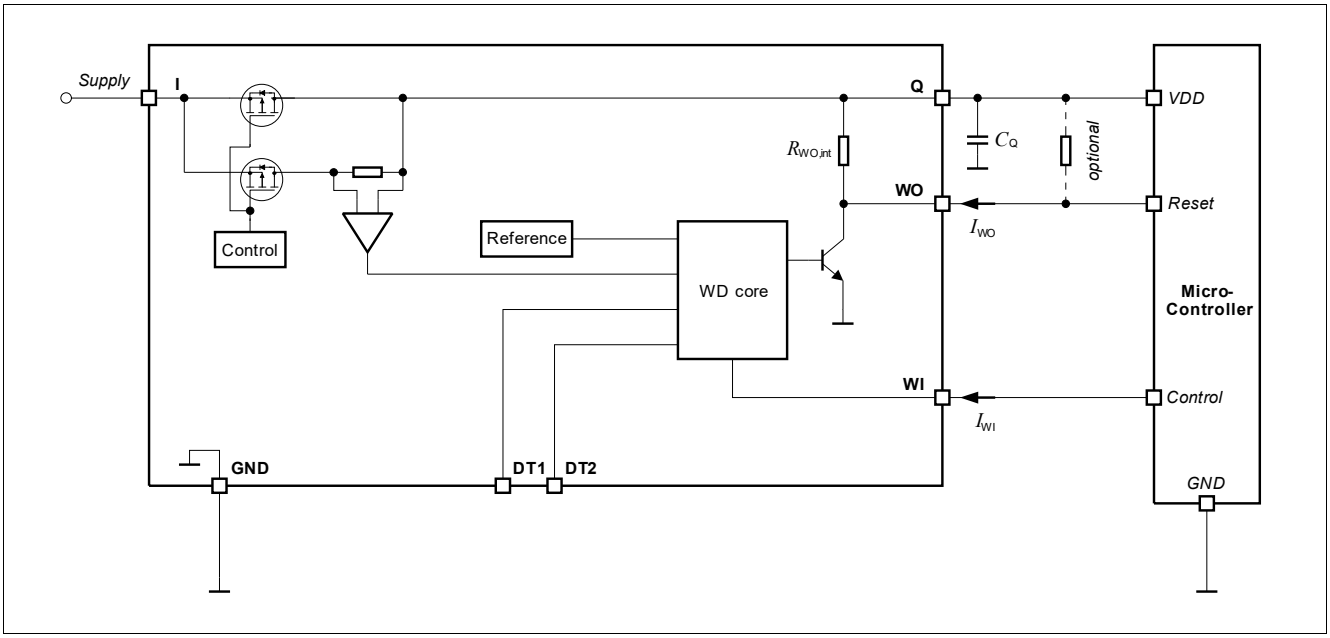


Figure 7 Block diagram watchdog circuit

Watchdog timing

By changing the condition on the “DT” pins, the new timing is valid from the beginning of next period. From this time on, the frequency of the WI signal must be adapted (see also **“Typical watchdog timing diagram, watchdog and reset modes” on Page 27**).

Figure 8 shows the state diagram of the watchdog (WD) and the mode selection. After power-on, the reset output signal at the “RO” pin (microcontroller reset) is kept LOW for the reset delay time t_{rd}. With the LOW to HIGH transition of the signal at “WO” the device starts the watchdog ignore time $t_{WI,i}$. Next, the WD starts the watchdog trigger time (time frame within a trigger at WI must occur).

From now on, the timing of the signal on WI from the microcontroller must fit to the WD-trigger time $t_{WI,tr}$, based on the setting of the “DT” pins. A re-trigger of the WD-trigger time is done with a HIGH-to-LOW transient at the WI-pin within the active $t_{WI,tr}$.

Watchdog output “WO”

The watchdog output “WO” is an open collector output with an integrated pull-up resistor. In case a lower-ohmic “WO” signal is desired, an external pull-up resistor can be connected to the output “Q”. Since the maximum “WO” sink current is limited, the minimum value of the optional external resistor “$R_{WO,ext}$” is given in **Table “Watchdog output WO” on Page 30**. A HIGH to LOW transition of the watchdog trigger signal on pin WI is taken as a trigger. A watchdog signal is generated (“WO” goes LOW), if there is no trigger pulse during the watchdog trigger time.

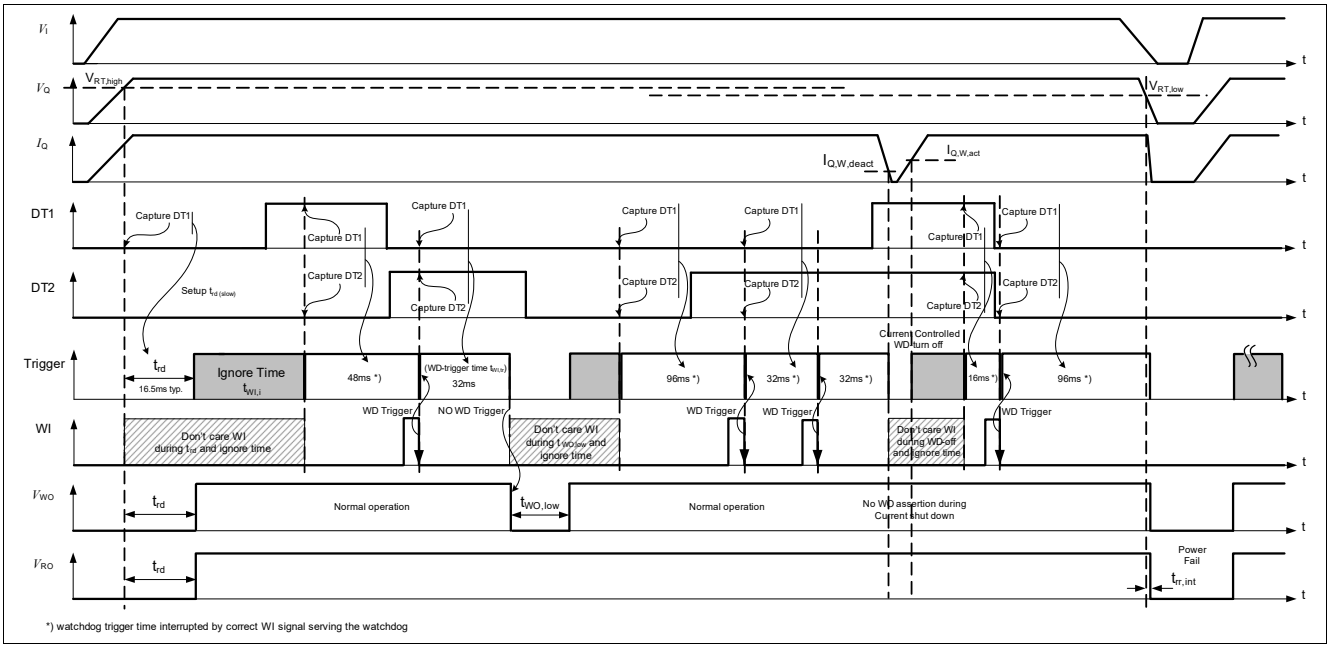


Figure 8 Typical watchdog timing diagram, watchdog and reset modes

Watchdog input “WI”

The watchdog is triggered by a falling edge at the watchdog input pin “WI”. The amplitude and slope of this signal has to comply with the specification (**Table “Watchdog input WI” on Page 29**). For details regarding test pulses, see **Figure 9 “Test pulses watchdog input WI” on Page 27**.

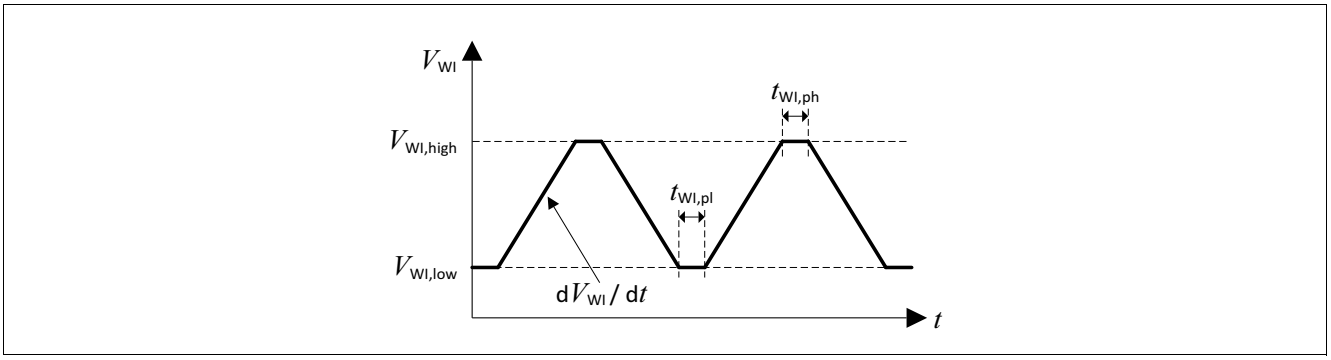


Figure 9 Test pulses watchdog input WI

Table 10 Electrical characteristics watchdog

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Watchdog timing							
Watchdog ignore time	$t_{WI,i}$	12.8	16	19.2	ms	–	P_5.9.1
Watchdog trigger time	$t_{WI,tr,1}$	76.8	96	115.2	ms	DT1 connected to GND; DT2 connected to GND	P_5.9.2
Watchdog trigger time	$t_{WI,tr,2}$	38.4	48	57.6	ms	DT1 connected to Q; DT2 connected to GND	P_5.9.3
Watchdog trigger time	$t_{WI,tr,3}$	25.6	32	38.4	ms	DT1 connected to GND; DT2 connected to Q	P_5.9.4
Watchdog trigger time	$t_{WI,tr,4}$	12.8	16	19.2	ms	DT1 connected to Q; DT2 connected to Q	P_5.9.5
Watchdog output low time	$t_{WO,low}$	6.4	8	9.6	ms	–	P_5.9.6
Load dependent watchdog activation							
Watchdog activation current threshold	$I_{Q,W,act}$	–	–	5.5	mA	for $V_{Q,nom}$ = 5 V: V_I > 5.44 V; high current condition must be applied at least for the time of $t_{W,filter,max}$	P_5.9.11
Watchdog deactivation current threshold	$I_{Q,W,deact}$	1	–	–	mA	for $V_{Q,nom}$ = 5 V: V_I > 5.44 V; low current condition must be applied at least for the time of $t_{W,filter,max}$	P_5.9.12
Watchdog deactivation current hysteresis	$I_{Q,W,hy}$	0.35	–	–	mA	for $V_{Q,nom}$ = 5 V: V_I > 5.44 V;	P_5.9.13
Watchdog activation current threshold	$I_{Q,W,act}$	–	–	5.5	mA	for $V_{Q,nom}$ = 3.3 V: V_I > 3.72 V; high current condition must be applied at least for the time of $t_{W,filter,max}$	P_5.9.39
Watchdog deactivation current threshold	$I_{Q,W,deact}$	1	–	–	mA	for $V_{Q,nom}$ = 3.3 V: V_I > 3.72 V; low current condition must be applied at least for the time of $t_{W,filter,max}$	P_5.9.40
Watchdog deactivation current hysteresis	$I_{Q,W,hy}$	0.35	–	–	mA	for $V_{Q,nom}$ = 3.3 V: V_I > 3.72 V;	P_5.9.41
Watchdog minimum filter time state transition by current	$t_{W,IQ,filter,min}$	100	–	–	µs	[1] – see **Page 30**	P_5.9.14

Table 10 Electrical characteristics watchdog (cont'd)

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Watchdog maximum filter time state transition by current	$t_{W,IQ,filter,max}$	–	–	500	µs	[1] – see **Page 30**	P_5.9.15
Watchdog input WI							
Watchdog input low signal valid	$V_{WI,low}$	–	–	0.8	V	[2] –	P_5.9.16
Watchdog input high signal valid	$V_{WI,high}$	2.0	–	–	V	[2] –	P_5.9.17
Watchdog input high signal pulse length	$t_{WI,ph}$	1	–	–	µs	[2] $V_{WI} \geq V_{WI,high}$	P_5.9.19
Watchdog input low signal pulse length	$t_{WI,pl}$	1	–	–	µs	[2] $V_{WI} \leq V_{WI,low}$	P_5.9.20
Watchdog input signal slew rate	dV_{WI}/dt	1	–	–	V/µs	[2] $V_{WI,low} < V_{WI} < V_{WI,high}$	P_5.9.21
High level input current	$I_{WI,H}$	–	–	3.5	µA	V_{WI} = 3.3 V	P_5.9.22
Watchdog input internal pull-down resistor	R_{WI}	0.9	1.5	2.6	MΩ	–	P_5.9.23
Watchdog disable threshold WI signal value	$V_{WI,dis}$	1.15	–	1.40	V	for $V_{Q,nom}$ = 5 V: V_I > 5.44 V; signal must be applied for > $t_{W,filter,max}$ to deactivate and activate the watchdog	P_5.9.31
Watchdog disable threshold WI signal value	$V_{WI,dis}$	1.15	–	1.40	V	for $V_{Q,nom}$ = 3.3 V: V_I > 4.6 V; signal must be applied for > $t_{W,filter,max}$ to deactivate and activate the watchdog	P_5.9.24
Watchdog minimum filter time state transition by WI	$t_{WI,filter,min}$	100	–	–	µs	[3] – see **Page 32**	P_5.9.25
Watchdog maximum filter time state transition by WI	$t_{WI,filter,max}$	–	–	500	µs	[3] – see **Page 32**	P_5.9.26
Watchdog delay input DT2 (DT1 is defined in chapter Reset delay input DT1)							
Delay input DT2 low signal valid	$V_{DT2,L}$	–	–	0.8	V	–	P_5.9.27
Delay input DT2 high signal valid	$V_{DT2,H}$	2.0	–	–	V	–	P_5.9.28

Table 10 Electrical characteristics watchdog (cont'd)

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay input DT2 Signal Slew Rate	dV_{DT2}/dt	1	–	–	V/µs	$V_{DTx,L} < V_{DTx} < V_{DTx,H}$	P_5.9.38
High level input current DT2	$I_{DT2,H}$	–	–	3.5	µA	V_{DTx} = 3.3 V	P_5.9.30
Delay input DT2 internal pull-down resistor	R_{DT2}	0.9	1.5	2.6	MΩ	–	P_5.9.32
Watchdog setup and hold time (DT1, DT2)	$t_{setup,hold,DT}$	150	–	–	µs	[3] Within the setup and hold time phase, a DTx transition will not be recognized	P_5.9.33
Watchdog output WO							
Watchdog output low voltage	$V_{WO,low}$	–	0.2	0.4	V	R_{WO} > 5.1 kΩ	P_5.9.34
Watchdog output internal pull-up resistor	$R_{WO,int}$	13	20	36	kΩ	internally connected to pin Q	P_5.9.35
Watchdog output external pull-up resistor to V_Q	$R_{WO,ext}$	5.1	–	–	kΩ	V_{WO} ≤ 0.4 V;	P_5.9.36

1) Not subject to production test, specified by design.
2) For details on applied test pulse, see **Figure 9**
3) Not subject to production test, specified by design.

Watchdog trigger time

Two pins, DT1 and DT2, are used to set the desired watchdog trigger time $t_{WI,tr}$. Connect these pins either to GND or to high level (e.g. Q) to select the timing according to **Table 11**.

Table 11 Watchdog trigger time selection

DT1 connected to	DT2 connected to	$t_{WI,tr,typ}$
GND	GND	96 ms
Q	GND	48 ms
GND	Q	32 ms
Q	Q	16 ms

Watchdog deactivation by current control

The watchdog is load dependent inactive. This ensures, that if the microcontroller is in a power save mode ($I_Q \le I_{Q,W,deact}$) and not able to provide a correct watchdog trigger signal at pin "WI", no watchdog signal "WO = low" is generated. The transition from an active to an inactive state will be performed after a dead time of $t_{W,IQ,filter,max}$, when output current keeps below the deactivation threshold. This protects against an unintended entering of the watchdog deactivation state caused by short dynamic current drops. In case of very short current drops up to the time of $t_{W,IQ,filter,min}$, the activation state will definitely be kept. These scenarios are also valid for the transition from deactivation to activation state. For details see also **Figure 10**

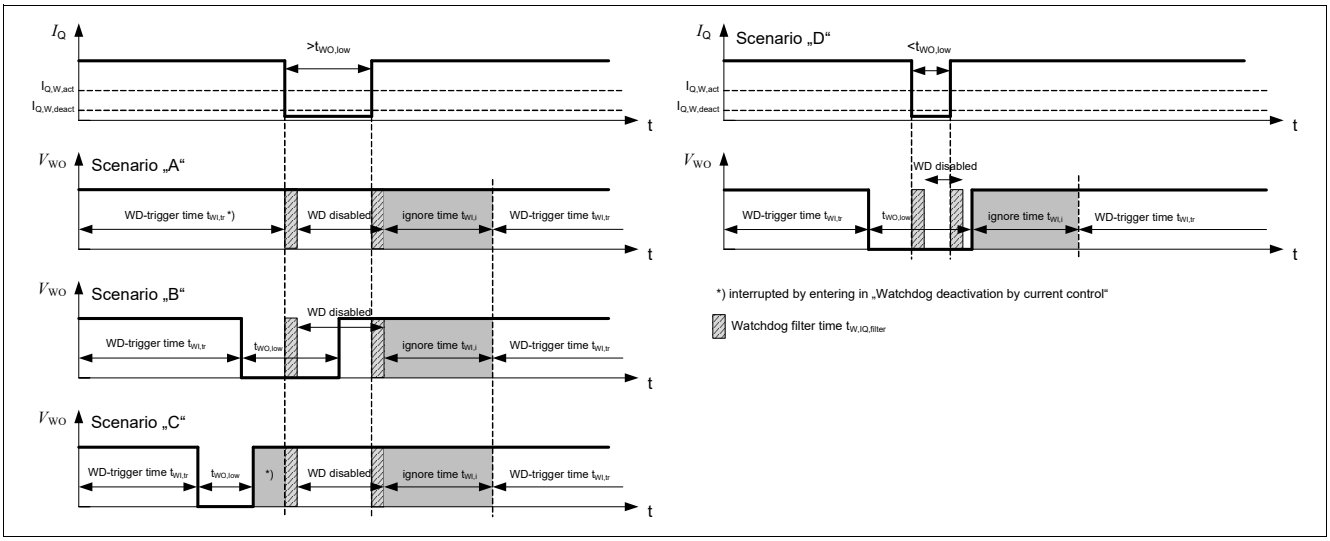


Figure 10 Watchdog output behavior for watchdog deactivation by current control

Scenario “A”

In scenario “A” the watchdog logic expects a next trigger at WI pin within the WD-trigger time $t_{WI,tr}$. This state is interrupted by the low current load state ($I_Q \le I_{Q,W,deact}$). During this state, the watchdog is disabled. The watchdog output signal “WO” will stay high while the watchdog is disabled. After leaving the low current load state ($I_Q \ge I_{Q,W,act}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a low current load time greater than $t_{WO,low}$.

Scenario “B”

In scenario “B” the watchdog is not served within WD-trigger time $t_{WI,tr}$ with an trigger event at WI pin. As a result the “WO” is set to low. This state is interrupted by the low current load state ($I_Q \le I_{Q,W,deact}$). During this state, the watchdog is disabled. The watchdog output signal “WO” is kept in low state for $t_{WO,low}$ and then the “WO” is set to high. After leaving the low current load state ($I_Q \ge I_{Q,W,act}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a low current load time greater than $t_{WO,low}$.

Scenario “C”

In scenario “C” the watchdog is not served within WD-trigger time $t_{WI,tr}$ with an trigger event at WI pin. As a result the “WO” is set to low. After this an ignore window follows. This state is interrupted by the low current load state ($I_Q \le I_{Q,W,deact}$). During this state, the watchdog is disabled. The watchdog output signal “WO” will stay high while the watchdog is disabled. After leaving the low current load state ($I_Q \ge I_{Q,W,act}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a low current load time greater than $t_{WO,low}$.

Scenario “D”

In scenario “D” the watchdog is not served within WD-trigger time $t_{WI,tr}$ with a trigger event at WI pin. As a result the “WO” is set to low. This state is interrupted by the low current load state ($I_Q \le I_{Q,W,deact}$). During this state, the watchdog is disabled. The watchdog output signal “WO” is kept in low state for the time of low current load state. After leaving the low current load state ($I_Q \ge I_{Q,W,act}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a low current load time less than $t_{WO,low}$.

Watchdog deactivation by external signal (pin “WI”)

Note: Disabling the watchdog should only considered when the application is not running in the normal operating conditions as the safe operation is not ensured any more. Example would be the flashing process of the microcontroller.

The Watchdog can be disabled by connecting a voltage level between the range of 1.15 V to 1.40 V to WI. By entering the watchdog deactivation, the “WO” signal behaves like it is described in **Figure 11**. The transition from active to an inactive state will be performed after a dead time of $t_{WI,filter,max}$, when correct level to WI pin is applied. This protects against the unintended entering of watchdog deactivation state. After leaving the deactivation voltage range 1.15 V to 1.40 V, the watchdog is again active and starts with an ignore window. This scenario is also valid for the transition from deactivation to activation state.

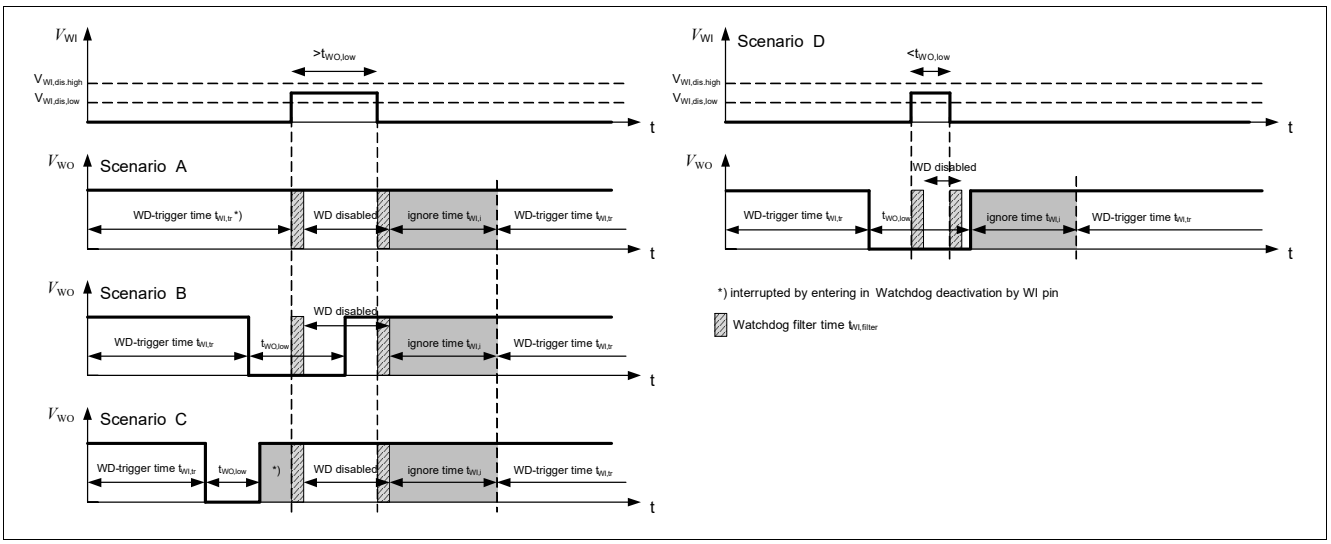


Figure 11 Watchdog output behavior for watchdog deactivation by WI pin

Scenario “A”

In scenario “A” the watchdog logic expects a next trigger at WI pin within the WD-trigger time $t_{WI,tr}$. This state is interrupted by setting V_{WI} to the disable condition ($V_{WI,dis,low} \le V_{WI} \le V_{WI,dis,high}$). During this state, the watchdog is disabled. The watchdog output signal “WO” will stay high while the watchdog is disabled. After leaving the disable condition ($V_{WI} \ge V_{WI,dis,high}$ or $V_{WI} \le V_{WI,dis,low}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a watchdog disabled duration greater than $t_{WO,low}$.

Scenario “B”

In scenario “B” the watchdog is not served within WD-trigger time $t_{WI,tr}$ with an trigger event at WI pin. As a result the “WO” is set to low. This state is interrupted by setting V_{WI} to the disable condition ($V_{WI,dis,low} \le V_{WI} \le V_{WI,dis,high}$). During this state, the watchdog is disabled. The watchdog output signal “WO” is kept in low state for $t_{WO,low}$ and then the “WO” is set to high. After leaving the disable condition ($V_{WI} \ge V_{WI,dis,high}$ or $V_{WI} \le V_{WI,dis,low}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a watchdog disabled duration greater than $t_{WO,low}$.

Scenario “C”

In scenario “C” the watchdog is not served within WD-trigger time $t_{WI,tr}$ with an trigger event at WI pin. As a result the “WO” is set to low. After this an ignore window follows. This state is interrupted by setting V_{WI} to the

disable condition ($V_{WI,dis,low} \leq V_{WI} \leq V_{WI,dis,high}$). During this state, the watchdog is disabled. The watchdog output signal “WO” will stay high while the watchdog is disabled. After leaving the disable condition ($V_{WI} \geq V_{WI,dis,high}$ or $V_{WI} \leq V_{WI,dis,low}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a watchdog disabled duration greater than $t_{WO,low}$.

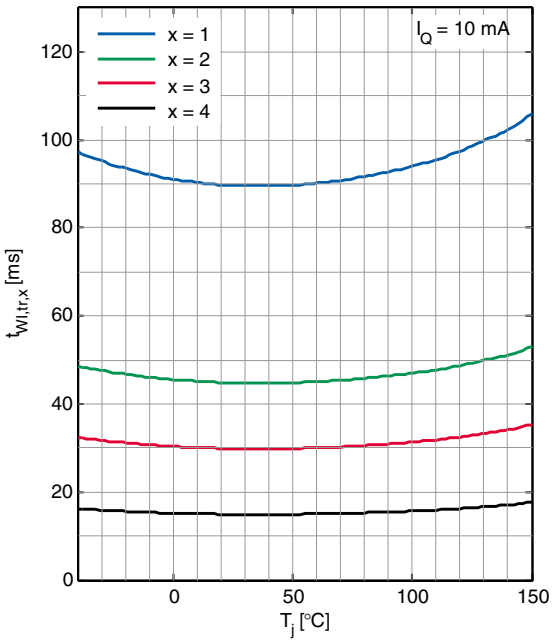
Scenario “D”

In scenario “D” the watchdog is not served within WD-trigger time $t_{WI,tr}$ with a trigger event at WI pin. As a result the “WO” is set to low. This state is interrupted by setting V_{WI} to the disable condition ($V_{WI,dis,low} \leq V_{WI} \leq V_{WI,dis,high}$). During this state, the watchdog is disabled. The watchdog output signal “WO” is kept in low state as long the watchdog is disabled. After leaving the disable condition ($V_{WI} \geq V_{WI,dis,high}$ or $V_{WI} \leq V_{WI,dis,low}$), an ignore window $t_{WI,i}$ follows. After this, the watchdog trigger time $t_{WI,tr}$ starts based on the setting of the DT pins. This behavior is defined for cases with a watchdog disabled duration less than $t_{WO,low}$.

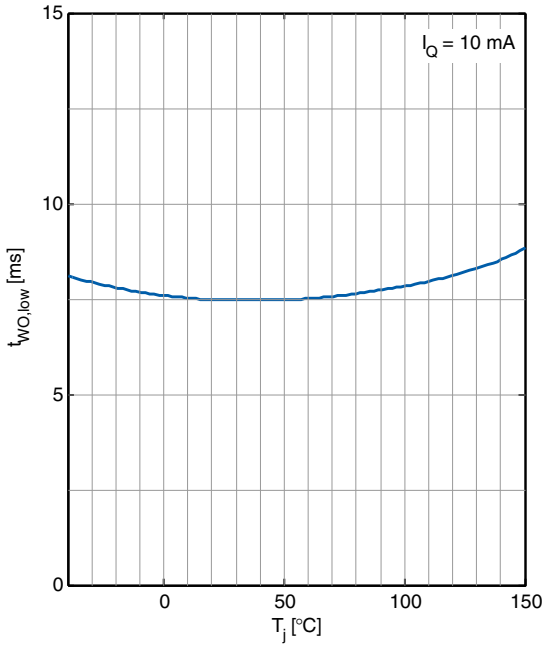
4.10 Typical performance characteristics standard watchdog

Typical performance characteristics

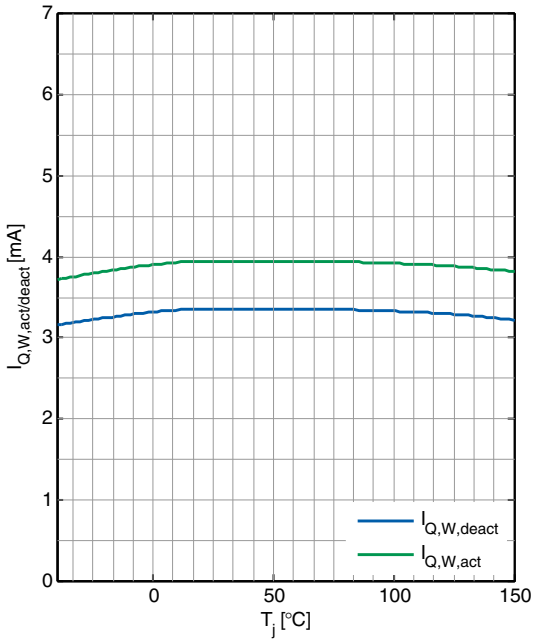
Watchdog trigger time $t_{WI,tr,1,2,3,4}$ versus junction temperature T_j



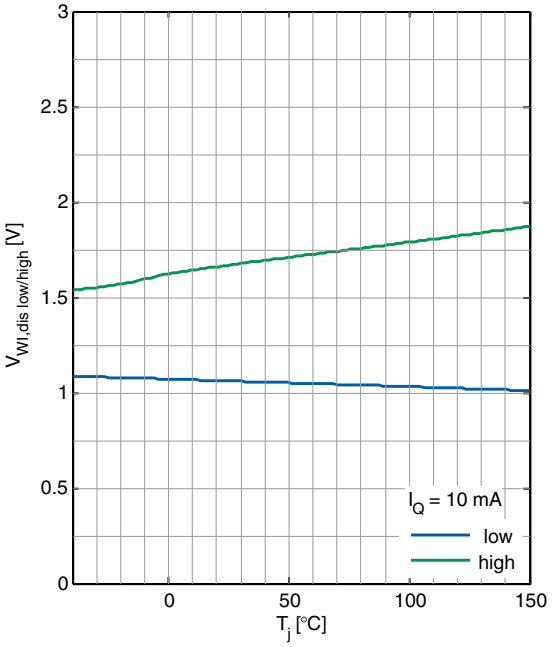
Watchdog output low time $t_{WO,low}$ versus junction temperature T_j



Watchdog activation/deactivation current $I_{Q,W,act}$, $I_{Q,W,deact}$ versus junction temperature T_j



Watchdog disable $V_{WI,dis}$ threshold versus junction temperature T_j



5 Application information

5.1 Application diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

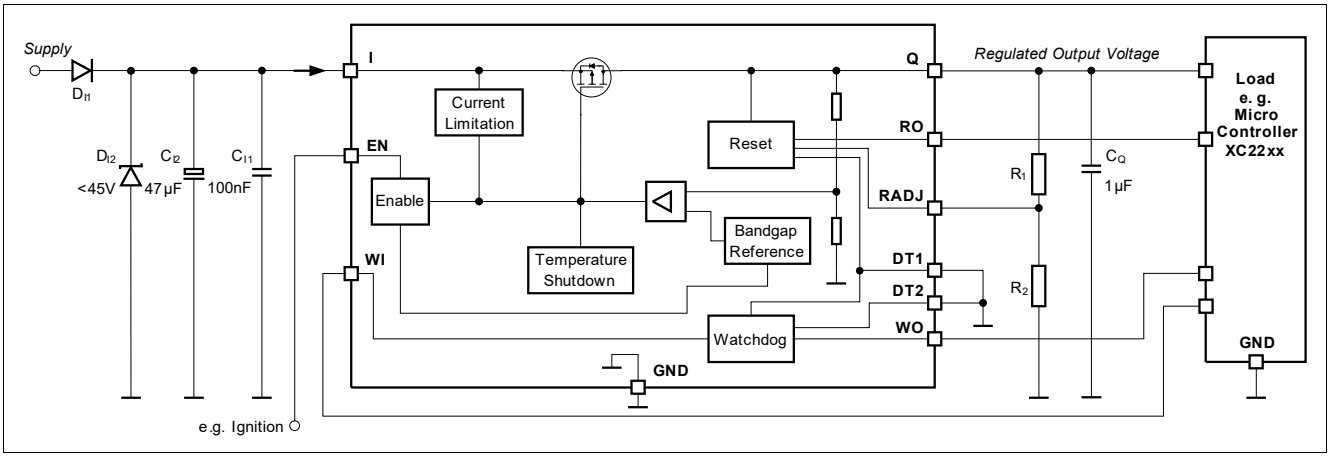


Figure 12 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

5.2 Selection of external components

5.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **"Functional range" on Page 8**. The graph **"Output capacitor series resistor ESR(CQ) versus output current IQ" on Page 15** shows the stable operation range of the device.

TLS820F0 is designed to be also stable with low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (5.1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (5.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **"Thermal resistance" on Page 9**.

Example

Application conditions:

V_I = 13.5 V

V_Q = 5 V

I_Q = 150 mA

T_a = 85 °C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$ ($V_I \times I_q$ can be neglected because of very low I_q)

$= (13.5\ V - 5\ V) \times 150\ mA = 1.275\ W$

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$

$= (150\ °C - 85\ °C) / 1.275\ W = 50.98\ K/W$

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 50.98 K/W. According to **“Thermal resistance” on Page 9**, at least 600 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used to ensure a proper cooling for the TLS820F0 in PG-SSOP-14 package.

5.4 Reverse polarity protection

TLS820F0 is not self protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is needed. The absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 7** must be kept.

5.5 Further application information

- For further information you may contact **http://www.infineon.com/**

6 Package information

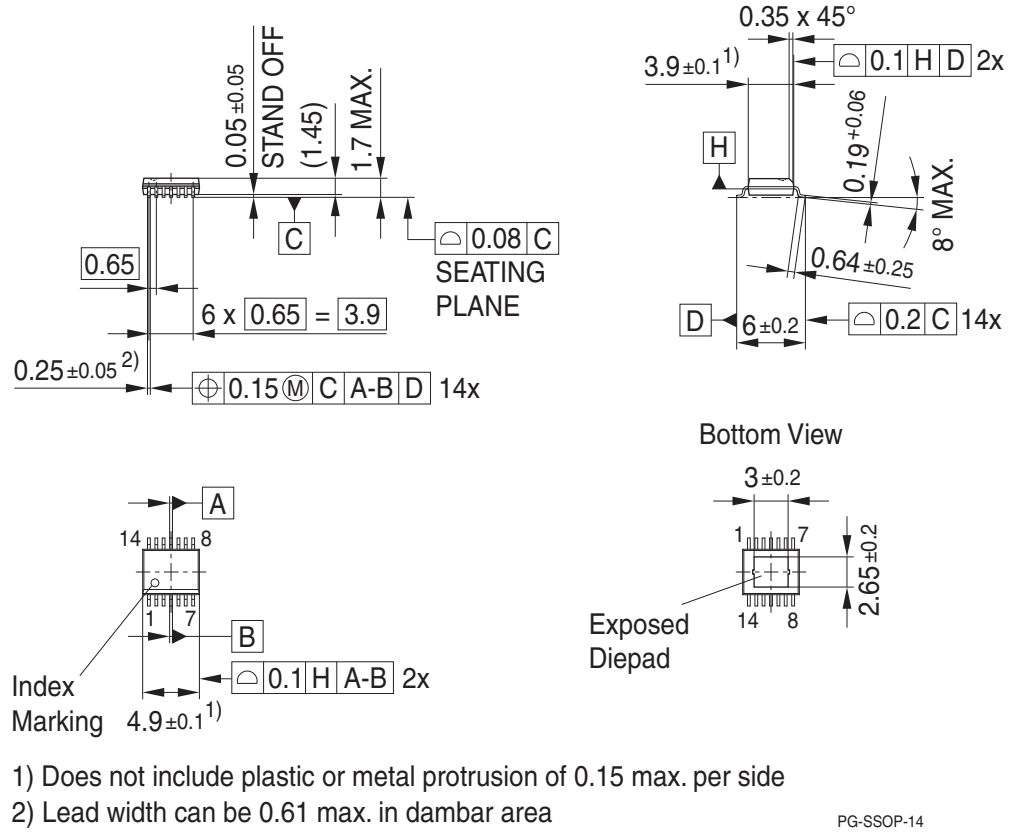


Figure 13 PG-SSOP-14[1)]

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

7 Revision history

Revision	Date	Changes
1.2	2021-04-08	Update layout and structure Parameter P_5.1.12 updated Parameter P_5.1.32 updated Editorial changes applied
1.1	2015-07-24	Additional description added for function “Watchdog deactivation by WI pin” Parameter P_5.7.22 updated New parameter P_5.7.46 added Editorial changes applied
1.0	2015-03-20	Data Sheet - Initial version

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