

# TLE9012AQU

## Li-Ion Battery Monitoring and Balancing IC



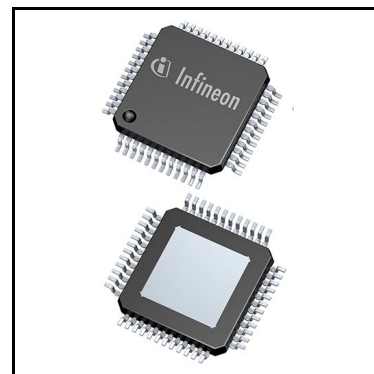
RoHS



ISO26262  
ready

### Features

- General
  - Monitors up to 12 cells connected in series
  - Supports communication of up to 20 devices
  - Supports hot plugging
- Voltage measurement
  - 16 bit high resolution ADC measurement for each cell
  - High accuracy measurement for SoC (State-of-Charge) and SoH (State-of-Health) calculation
  - Temperature compensated measurements
  - Built-in noise filtering
  - Selectable measurement bit length
- Temperature measurement
  - 5 temperature measurement channels for connection to external NTC
  - Internal temperature measurement
- Balancing
  - Integrated balancing switch allowing up to 150 mA balancing current
- Communication Bus (iso UART)
  - Differential robust serial interface for communication between battery blocks
  - High speed communication with 2 Mbps
  - Power balanced communication scheme
- Additional 4 GPIO pins to e.g. connect an external EEPROM
- Green product (RoHS-compliant)
- ISO-26262 ready, supporting ASIL-C BMS safety applications<sup>1)</sup>



### Safety features

- Two independent internal voltage references
- Block voltage measurement based on different ADCs
- Configurable analog OV/UV comparators
- End-to-end CRC secured communication
- CRC secured configuration registers
- Internal open load detection

1) according to ISO 26262-8 clause 13 first edition

- Emergency mode signaling using iso UART lines

## Potential applications

- Multi-cell battery monitoring and balancing system IC designed for Li-Ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as in 12 V Lithium-Ion batteries

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Description

The TLE9012AQU provides the main function of monitoring the temperature of the battery and voltage of each cell as well as the communication to the host controller.

| Type       | Package    | Marking    |
|------------|------------|------------|
| TLE9012AQU | PG-TQFP-48 | TLE9012AQU |

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## Block diagram

### 1 Block diagram

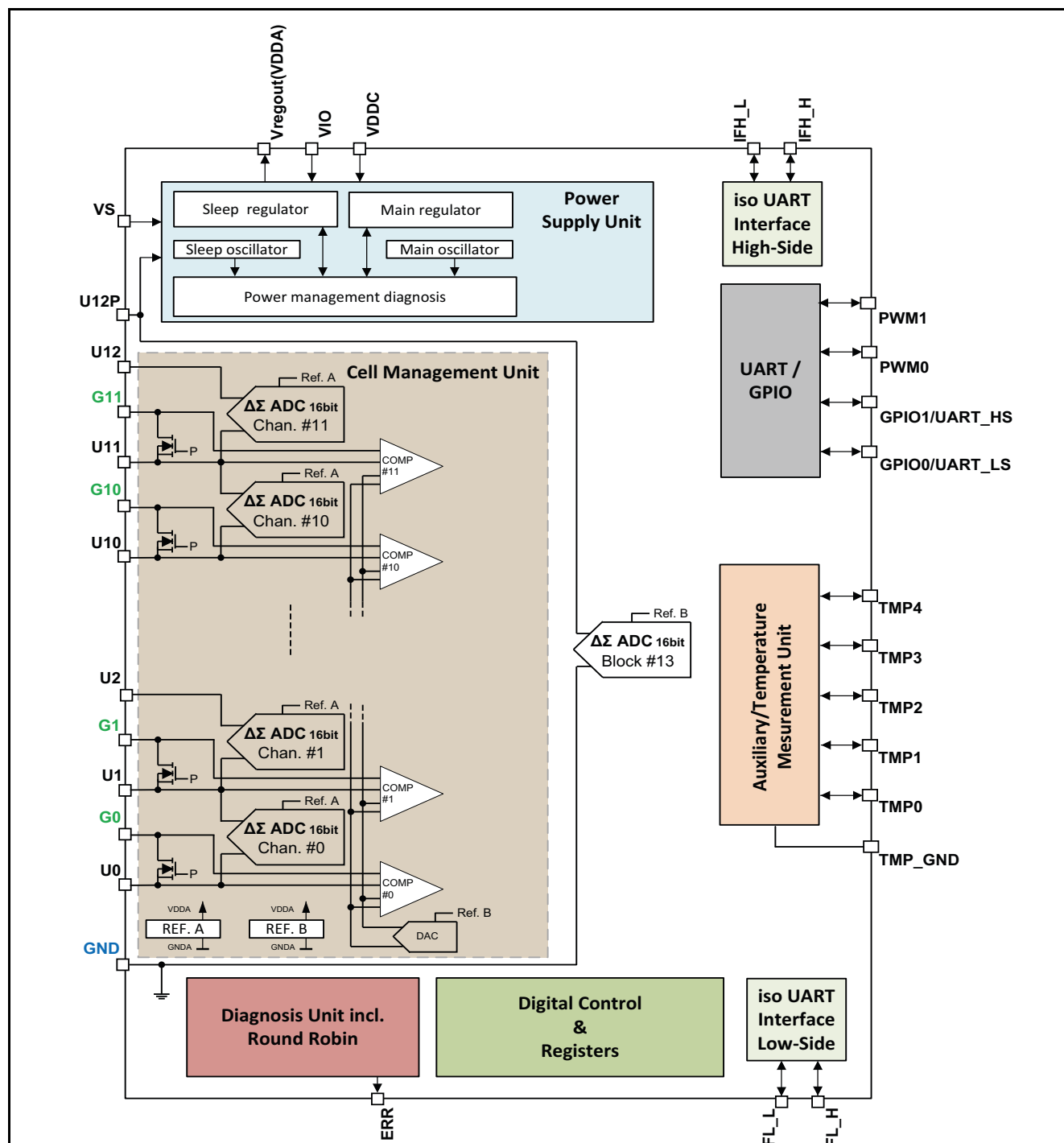


Figure 1 TLE9012AQU block diagram

## Pin configuration

## 2 Pin configuration

### 2.1 Pin assignment

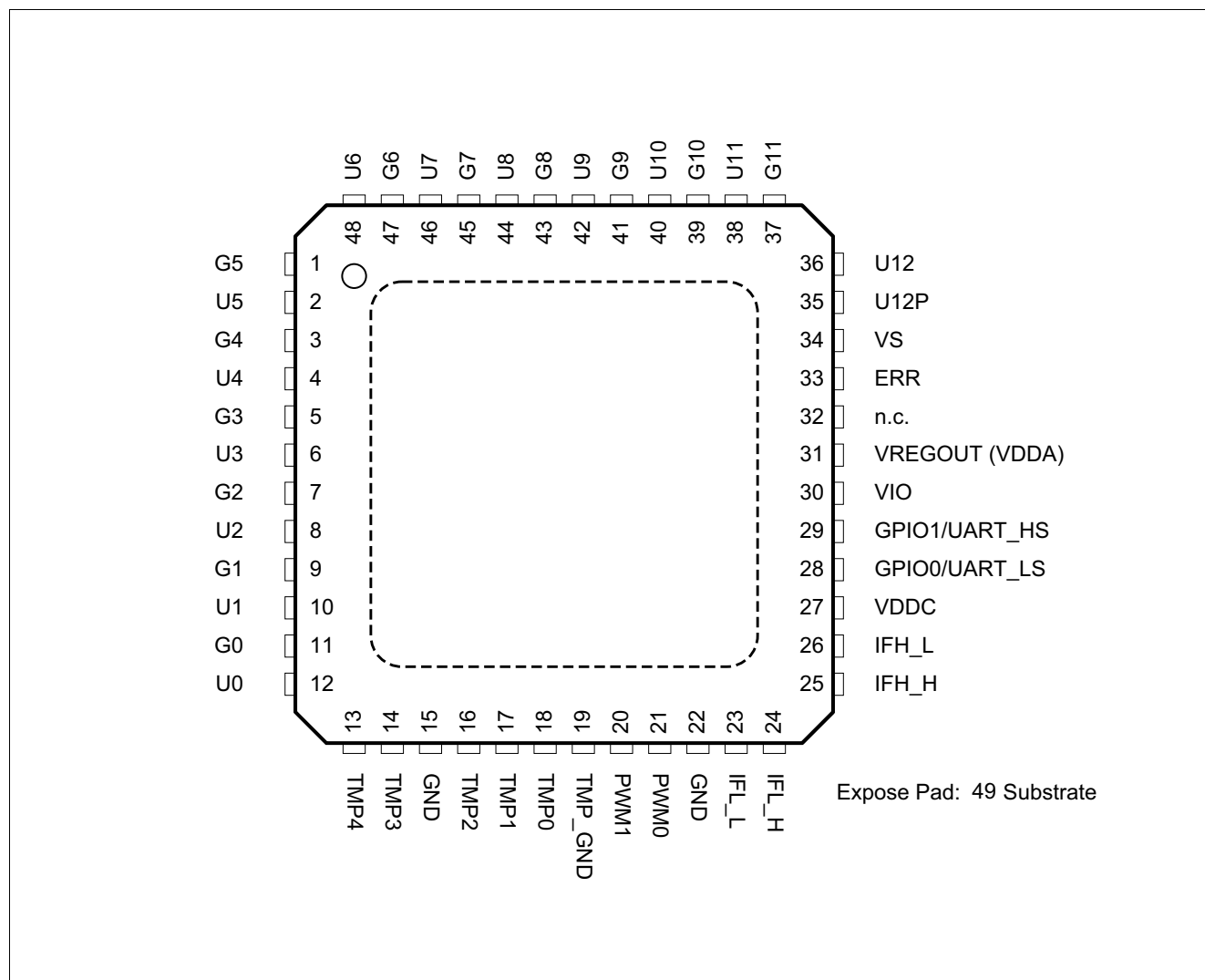


Figure 2 Pin configuration

**Pin configuration**

**2.2 Pin definitions and functions**

**Table 1 Pin assignment**

| Pin | Symbol            | Function  |
|-----|-------------------|---|
| 1   | G5                | Cell balance control channel 5, input of SCVS   |
| 2   | U5                | Cell voltage measurement channel 5 negative terminal (positive terminal of cell 4)  |
| 3   | G4                | Cell balance control channel 4, input of SCVC   |
| 4   | U4                | Cell voltage measurement channel 4 negative terminal (positive terminal of cell 3)  |
| 5   | G3                | Cell balance control channel 3, input of SCVC   |
| 6   | U3                | Cell voltage measurement channel 3 negative terminal (positive terminal of cell 2)  |
| 7   | G2                | Cell balance control channel 2, input of SCVC   |
| 8   | U2                | Cell voltage measurement channel 2 negative terminal (positive terminal of cell 1)  |
| 9   | G1                | Cell balance control channel 1, input of SCVC   |
| 10  | U1                | Cell voltage measurement channel 1 negative terminal (positive terminal of cell 0)  |
| 11  | G0                | Cell balance control channel 0, input of SCVC   |
| 12  | U0                | Cell voltage measurement channel 0 negative terminal (same potential as local GND)  |
| 13  | TMP4              | Temperature sensor 4; If not used, please connect pin to GND. If TMP4 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin. |
| 14  | TMP3              | Temperature sensor 3; If not used, please connect pin to GND. If TMP3 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin. |
| 15  | GND               | Local GND of CSC (Cell Supervision Circuit) device  |
| 16  | TMP2              | Temperature sensor 2; If not used, please connect pin to GND. If TMP2 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin. |
| 17  | TMP1              | Temperature sensor 1; If not used, please connect pin to GND. If TMP1 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin. |
| 18  | TMP0              | Temperature sensor 0; If not used, please connect pin to GND. If TMP0 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin. |
| 19  | TMP_GND           | Temperature sensor reference. This pin can be connected to local GND.   |
| 20  | PWM1              | PWM output channel 1; This pin has also a general purpose input/output function; If not used, please connect pin to GND.                            |
| 21  | PWM0              | PWM output channel 0; This pin has also a general purpose input/output function; If not used, please connect pin to GND.                            |
| 22  | GND               | Local GND of CSC device (Cell Supervision Circuit)  |
| 23  | IFL_L             | Lower Communication Bus (iso UART) L pin  |
| 24  | IFL_H             | Lower Communication Bus (iso UART) H pin  |
| 25  | IFH_H             | Upper Communication Bus (iso UART) H pin  |
| 26  | IFH_L             | Upper Communication Bus (iso UART) L pin  |
| 27  | VDDC              | Buffer capacitor pin for internal Communication Bus (iso UART) supply   |
| 28  | GPIO0/<br>UART_LS | General purpose input/output channel 0. This pin has also the function of UART_LS; If not used, please connect pin to GND.                          |

**Pin configuration**

**Table 1 Pin assignment**

| Pin | Symbol            | Function   |
|-----|-------------------|--|
| 29  | GPIO1/<br>UART_HS | General purpose input/output channel 1. This pin has also the function of UART_HS; if not used, please connect pin to GND. |
| 30  | VIO               | Supply for GPIO interface.   |
| 31  | Vregout           | Output pin of the internal regulator.  |
| 32  | n.c.              | Not connected; this pin shall be connected to GND.   |
| 33  | ERR               | Erroroutput to microcontroller; open drain PMOS connected to VS. If not used, please leave pin open.                       |
| 34  | VS                | Supply pin of internal regulator Vregout.  |
| 35  | U12P              | Positive supply pin; connect to positive terminal of topmost cell in block; supply of the sleep regulator.                 |
| 36  | U12               | Cell voltage measurement channel 11 positive terminal (most upper cell in the block)                                       |
| 37  | G11               | Cell balance control channel 11, input of SCVC   |
| 38  | U11               | Cell voltage measurement channel 11 negative terminal (positive terminal of cell 10)                                       |
| 39  | G10               | Cell balance control channel 10, input of SCVC   |
| 40  | U10               | Cell voltage measurement channel 10 negative terminal (positive terminal of cell 9)  |
| 41  | G9                | Cell balance control channel 9, input of SCVC  |
| 42  | U9                | Cell voltage measurement channel 9 negative terminal (positive terminal of cell 8)   |
| 43  | G8                | Cell balance control channel 8, input of SCVC  |
| 44  | U8                | Cell voltage measurement channel 8 negative terminal (positive terminal of cell 7)   |
| 45  | G7                | Cell balance control channel 7, input of SCVC  |
| 46  | U7                | Cell voltage measurement channel 7 negative terminal (positive terminal of cell 6)   |
| 47  | G6                | Cell balance control channel 6, input of SCVC  |
| 48  | U6                | Cell voltage measurement channel 6 negative terminal (positive terminal of cell 5)   |
| 49  | EPAD              | Cooling tab; should be connected to GND externally.  |



### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to GND, positive current flowing into pin  
(unless otherwise specified)

| Parameter                                      | Symbol                                   | Values                    |      |                          | Unit | Note or Test Condition   | Number |
|--|--|---------------------------|------|--------------------------|------|--|--------|
|  |  | Min.                      | Typ. | Max.                     |      |  |        |
| Voltages                                       |  |                           |      |                          |      |  |        |
| Supply voltage VS                              | V <sub>VS</sub>                          | -0.3                      | –    | 75                       | V    | –  |        |
| Supply voltage U12P                            | V <sub>U12P</sub>                        | -0.3                      | –    | 75                       | V    | –  |        |
| Supply voltage VIO                             | V <sub>VIO</sub>                         | -0.3                      | –    | 5.5                      | V    | –  |        |
| Supply voltage VS rel.                         | V <sub>VS</sub>                          | V <sub>regout</sub> - 0.3 | –    | –                        | –    | –  |        |
| Regulator output VREGOUT                       | V <sub>regout</sub>                      | -0.3                      | –    | 3.6                      | V    | –  |        |
| Regulator output VDDC                          | V <sub>VDDC</sub>                        | -0.3                      | –    | 3.6                      | V    | –  |        |
| Communication Bus (iso UART) interface IFH_x   | V <sub>IFH_L</sub><br>V <sub>IFH_H</sub> | -3                        | –    | 5.5                      | V    | 2)BCI test max. 300 mA injected via twisted pair cable onto iso UART interface (max. pin current 150 mA) |        |
| Communication Bus (iso UART) interface IFL_x   | V <sub>IFL_L</sub><br>V <sub>IFL_H</sub> | -3                        | –    | 5.5                      | V    |  |        |
| Cell sense input voltage abs. Un               | V <sub>Un</sub>                          | -0.3                      | –    | 75                       | V    | 0 ≤ n ≤ 12   |        |
| Cell balancing pin abs. Gn                     | V <sub>Gn</sub>                          | -0.3                      | –    | 75                       | V    | 0 ≤ n ≤ 11   |        |
| Cell sense input voltages rel. Un              | V <sub>Un</sub>                          | V <sub>Un-1</sub> - x     | –    | V <sub>Un-1</sub> + 5.5  | V    | 1 ≤ n ≤ 12;<br>x= -0.0016* <i>T<sub>j</sub></i> + 0.54; e.g.:<br>x=0.5@ <i>T<sub>j</sub></i> =25°C       |        |
| Cell balancing pins rel. Gn                    | V <sub>Gn</sub>                          | V <sub>Un</sub> - 0.3     | –    | V <sub>Un+1</sub> + 0.3  | V    | 0 ≤ n ≤ 11   |        |
| Temperature sensor input voltages abs. TMPn    | V <sub>TMpn</sub>                        | -0.3                      | –    | 2.75                     | V    | 0 ≤ n ≤ 4  |        |
| Temperature sensor input voltages rel. TMPn    | V <sub>TMpn</sub>                        | -0.3                      | –    | V <sub>regout</sub> +0.3 | V    |  |        |
| Temperature sensor input voltages abs. TMP_GND | V <sub>TMp_GND</sub>                     | -0.3                      | –    | 2.75                     | V    | –  |        |
| Temperature sensor input voltages rel. TMP_GND | V <sub>TMp_GND</sub>                     | -0.3                      | –    | V <sub>regout</sub> +0.3 | V    | –  |        |

**General product characteristics**

**Table 2 Absolute maximum ratings<sup>1)</sup>** (cont'd)

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                                     | Symbol             | Values |      |                        | Unit | Note or Test Condition | Number |
|---|--------------------|--------|------|------------------------|------|------------------------|--------|
|   |                    | Min.   | Typ. | Max.                   |      |                        |        |
| General purpose I/O voltages abs. GPION       | $V_{\text{GPION}}$ | -0.3   | –    | 5.5                    | V    | $0 \leq n \leq 1$      |        |
| General purpose I/O voltages rel. GPION       | $V_{\text{GPION}}$ | -0.3   | –    | $V_{\text{VIO}} + 0.3$ | V    |                        |        |
| Pulse width modulation I/O voltages abs. PWMn | $V_{\text{PWMn}}$  | -0.3   | –    | 5.5                    | V    | $0 \leq n \leq 1$      |        |
| Pulse width modulation I/O voltages rel. PWMn | $V_{\text{PWMn}}$  | -0.3   | –    | $V_{\text{VIO}} + 0.3$ | V    |                        |        |
| Open drain output pin abs. ERR                | $V_{\text{ERR}}$   | -0.3   | –    | 75                     | V    | –                      |        |
| Open drain output pin rel. ERR                | $V_{\text{ERR}}$   | -0.3   | –    | $V_{\text{VS}} + 0.3$  | V    | –                      |        |
| Ground pin GND                                | $V_{\text{GND}}$   | 0      | –    | 0                      | V    | Absolute GND           |        |

**Temperatures**

|                                      |                  |     |   |     |                    |   |  |
|--------------------------------------|------------------|-----|---|-----|--------------------|---|--|
| Junction temperature $T_j$           | $T_j$            | -40 | – | 150 | $^{\circ}\text{C}$ | – |  |
| Storage temperature $T_{\text{stg}}$ | $T_{\text{stg}}$ | -55 | – | 150 | $^{\circ}\text{C}$ | – |  |

**ESD robustness**

|                          |                          |      |   |     |    |  |  |
|--------------------------|--------------------------|------|---|-----|----|--|--|
| ESD robustness 2 kV      | $V_{\text{ESD}}$         | -2   | – | 2   | kV | HBM <sup>3)</sup> ; all pins   |  |
| ESD robustness 4 kV      | $V_{\text{ESD}}$         | -4   | – | 4   | kV | HBM <sup>3)</sup> ; Robustness vs. GND for pins: VS, U12P, Un, TMPn, TMP_GND, AUX_MISn, IFH_x, IFL_x, Gn |  |
| ESD robustness CDM 500 V | $V_{\text{ESD}}$         | -500 | – | 500 | V  | CDM <sup>4)</sup> ; all pins   |  |
| ESD robustness CDM 750 V | $V_{\text{ESD\_Corner}}$ | -750 | – | 750 | V  | CDM <sup>4)</sup> ; corner pins  |  |

- 1) Not subject to production test, specified by design.
- 2) Positive and negative transients with a maximum duration of 100ns allowed between +/- 8 V; This should simulate ESD events; however, during normal and steady state condition voltage on these pins must stay inside the maximum ratings specified.
- 3) ESD robustness, according to Human Body Model "HBM" ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)
- 4) ESD robustness, according to Charged Device Model "CDM" JESD22-C101

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**General product characteristics**

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

**General product characteristics**

### 3.2 Functional range

*Note:* Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical characteristics table.

**Table 3 Functional range**

| Parameter            | Symbol     | Values |      |      | Unit | Note or Test Condition            | Number |
|----------------------|------------|--------|------|------|------|-----------------------------------|--------|
|                      |            | Min.   | Typ. | Max. |      |                                   |        |
| Supply voltage $V_S$ | $V_{VS}$   | 4.75   | –    | 60   | V    | when using the internal regulator |        |
| Supply voltage U12P  | $V_{U12P}$ | 4.75   | –    | 60   | V    | –                                 |        |
| Supply voltage VIO   | $V_{VIO}$  | 3      | –    | 5.5  | V    | –                                 |        |

### 3.3 Thermal resistance

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal resistance**

| Parameter                      | Symbol     | Values |      |      | Unit | Note or Test Condition | Number |
|--------------------------------|------------|--------|------|------|------|------------------------|--------|
|                                |            | Min.   | Typ. | Max. |      |                        |        |
| Junction to case $R_{thJC}$    | $R_{thJC}$ | –      | 6    | –    | K/W  | 1)                     |        |
| Junction to ambient $R_{thJA}$ | $R_{thJA}$ | –      | 30   | –    | K/W  | 1)2)                   |        |

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

## **4 Power supply**

### **4.1 Functional description**

The TLE9012AQU has an internal power supply to be able to work completely independent by using the power stored in the cells which it monitors.

### **4.2 Power supply description**

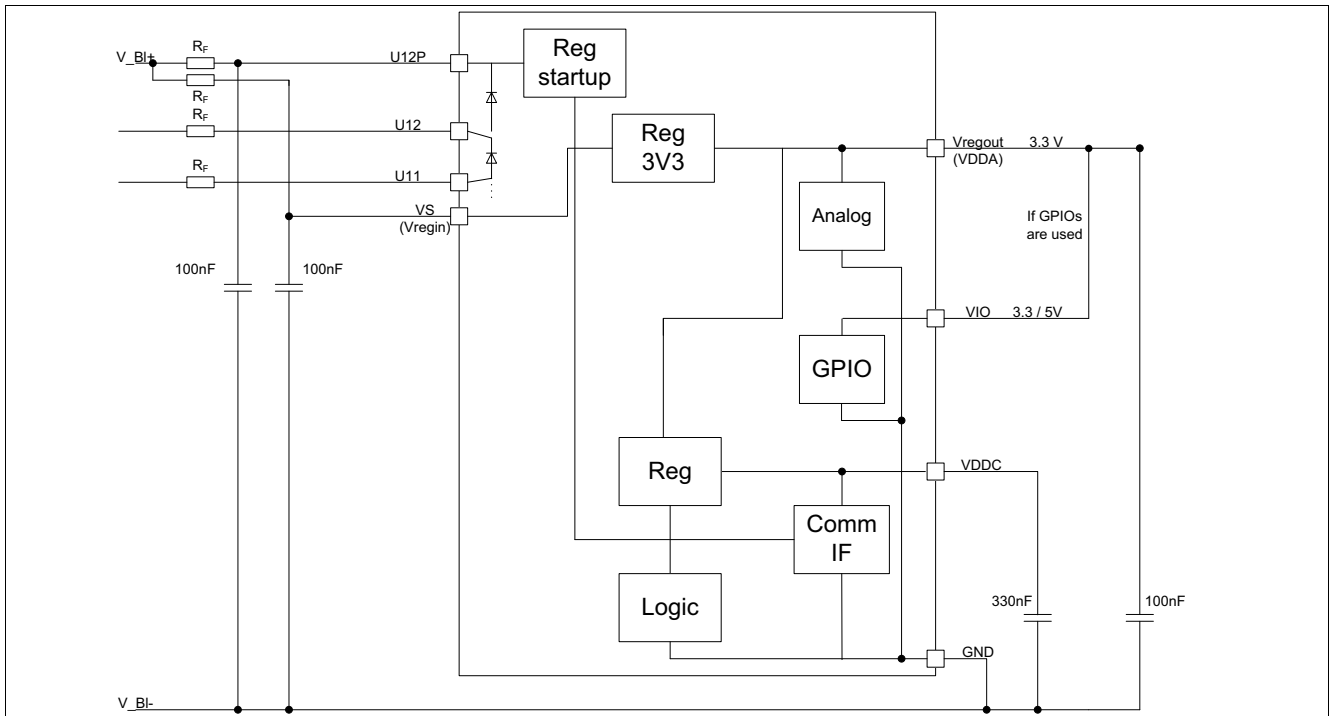
The following table contains a description of the power supply pins of the TLE9012AQU.

**Table 5 Power supply pins**

| <b>Pin name</b> | <b>Function</b>  |
|-----------------|--|
| VS              | VS is the main supply pin. This pin is the input for the internal regulator that is intended to supply the device in normal mode. It should be connected to the highest voltage in the module (usually the positive pole of the top cell). Supplying this pin is necessary to function the device.   |
| U12P            | U12P is the sense pin for the block voltage measurement (BVM); additionally this pin is the input supply pin for the sleep regulator which supplies the wake-up structures. The built-in sleep regulator powers the detection of incoming iso UART and UART wake-up signals in sleep mode which will then trigger the start-up procedure. It should be connected to the highest voltage in the module. Supplying this pin is necessary to function the device. |
| Vregout (VDDA)  | This pin is the output of the internal regulator. Usually this voltage can be used to drive the GPIOs for communication with other devices on board. Please connect this pin to a buffer capacitor.  |
| VIO             | This pin is the supply for the GPIOs. It can be connected either to Vregout or to the output of an external voltage regulator. The voltage available on this pin, will define the GPIO logic output levels as well as the thresholds of the GPIO logic inputs.   |
| VDDC            | VDDC is the output of the internal regulator used for the iso UART communication interface. This pin is used for buffering of the regulator. Please connect this pin to a buffer capacitor to ensure proper and robust communication.  |
| GND             | This is the main reference for the TLE9012AQU on the board.  |

The cell partitioning can be configured in the **PART\_CONFIG** register with the given constraint of starting from the most upper cell (CELL\_11). Please note: Only cells activated in **PART\_CONFIG** are being measured and checked in the round robin scheme (see also **Chapter 8.3.1**).

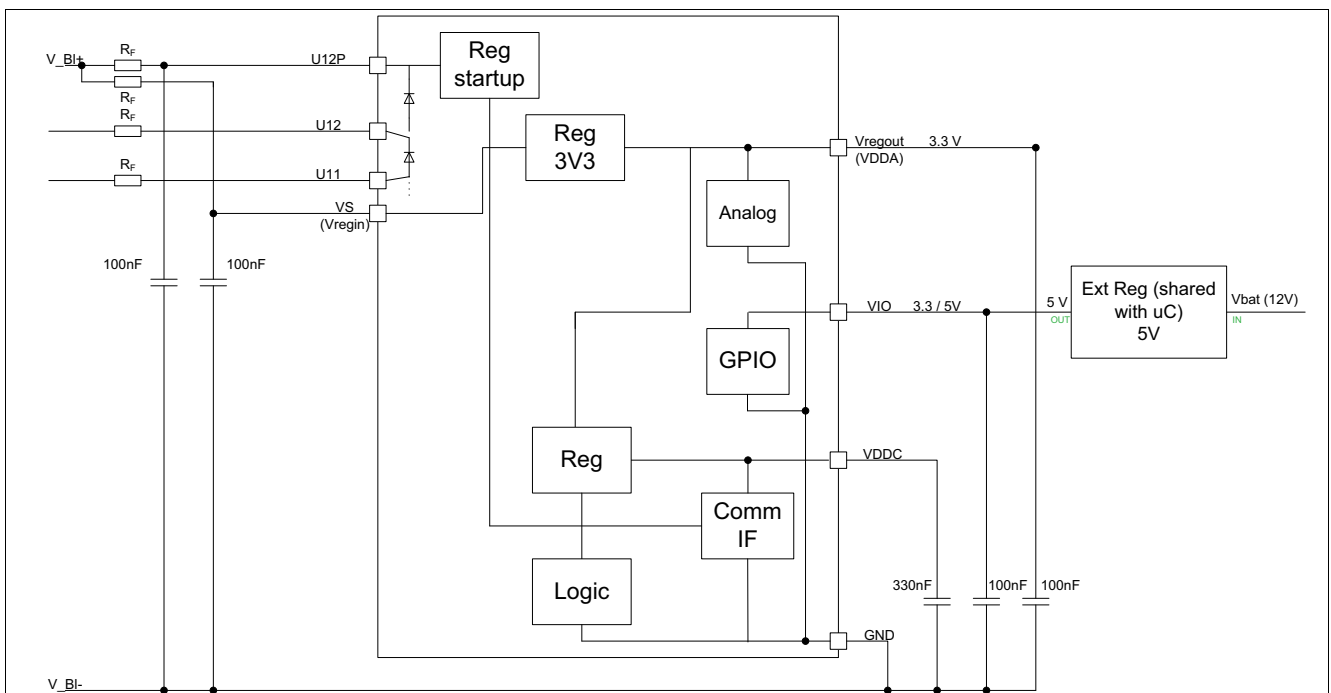
## Power supply



**Figure 3** Typical power supply configuration using the internal voltage regulator

### 4.3 Using an external voltage regulator for the UART/GPIO unit

It is also possible to use an external voltage regulator. This might be desired to have common I/O voltage levels with the host controller in case of systems where no transceiver IC is used and communication is happening directly via UART/GPIO (non-HV application like 12 V/48 V).



**Figure 4** System using an external voltage regulator (non-transceiver application)

## Power supply

### 4.4 Wake-up and sleep mode

The TLE9012AQU is designed to be continuously connected to a battery. Therefore, the physical connection to the cells which powers the device is expected to happen only once in a lifetime. After receiving power on U12P and VS, the part will go into sleep mode and will be monitoring the communication interfaces for a wake-up sequence.

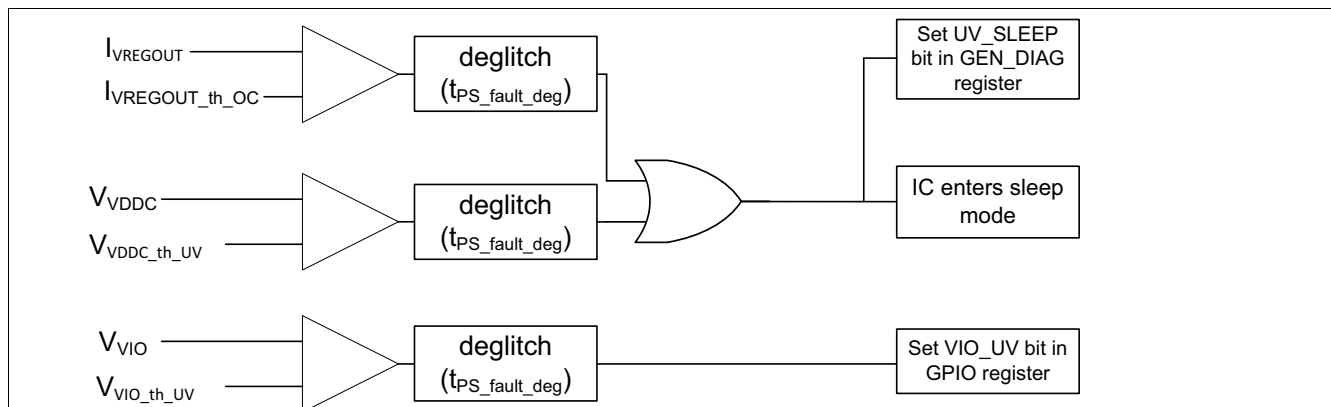
In order to activate the TLE9012AQU a wake-up sequence as described in [Chapter 8.2.2](#) has to be sent via either the iso UART port or the UART interface.

A watchdog is implemented that has to be triggered by regular iso UART/UART communication in order to keep the TLE9012AQU in normal mode. The watchdog timer is programmable (register **WDOG\_CNT**). The device will revert to sleep mode automatically as soon as the watchdog has timed out.

Additionally the TLE9012AQU includes the option to send the device directly to sleep mode, this can be performed by setting the PD bit-field in the **OP\_MODE** register.

### 4.5 Power supply monitoring

To ensure the correct function of the TLE9012AQU, the device is equipped with an internal monitoring unit for the different internal voltages as well as other supply functions. If important supplies go below levels to ensure correct functionality, the IC will enter sleep mode. The fault bit UV\_SLEEP in the **GEN\_DIAG** register indicates sleep mode due to a supply level outside the limits.



**Figure 5 HW monitoring unit**

**Power supply**

**4.6 Electrical characteristics power supply**

**Table 6 Electrical characteristics power supply**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter   | Symbol                      | Values |      |      | Unit | Note or Test Condition   | Number |
|---|-----------------------------|--------|------|------|------|--|--------|
|   |                             | Min.   | Typ. | Max. |      |  |        |
| Internal regulators                               |                             |        |      |      |      |  |        |
| internal regulator output voltage VREGOUT         | V <sub>Vregout</sub>        | 3      | 3.45 | 3.6  | V    | –  |        |
| Overcurrent threshold VREGOUT                     | I <sub>VREGOUT_th_OC</sub>  | 31     | 40   | 60   | mA   | –  |        |
| Undervoltage threshold falling VIO                | V <sub>VIO_th_UV_fall</sub> | 2.2    | –    | 2.76 | V    | –  |        |
| Undervoltage threshold rising VIO                 | V <sub>VIO_th_UV_rise</sub> | 2.24   | –    | 2.8  | V    | –  |        |
| VIO undervoltage hysteresis VIO                   | V <sub>VIO_th_UV_hys</sub>  | 40     | 100  | 160  | mV   | –  |        |
| Output voltage VDDC                               | V <sub>VDDC</sub>           | 2.42   | 2.5  | 2.75 | V    | –  |        |
| Undervoltage threshold VDDC                       | V <sub>VDDC_th_UV</sub>     | 2.15   | –    | 2.42 | V    | –  |        |
| Undervoltage threshold hysteresis VDDC            | V <sub>VDDC_th_UV_hys</sub> | 80     | 100  | 140  | mV   | –  |        |
| Power supply fault deglitch time                  | t <sub>PS_fault_deg</sub>   | 8      | 15   | 24   | μs   | 1)   |        |
| Supply currents                                   |                             |        |      |      |      |  |        |
| Sleep mode current U12P                           | I <sub>U12P_sleep</sub>     | 0      | 3    | 4.9  | μA   | T <sub>j</sub> = 25°C;   |        |
| Sleep mode leakage current VS                     | I <sub>VS_sleep</sub>       | -1     | –    | 1    | μA   | -40°C ≤ T <sub>j</sub> ≤ 85°C  |        |
| Idle current U12P                                 | I <sub>U12P_idle</sub>      | –      | 2.5  | 10   | μA   | IC in idle mode (no sleep mode), but no measurement or communication. VIO connected to Vregout                                       |        |
| Idle current VS                                   | I <sub>VS_idle</sub>        | –      | 4.7  | 9.2  | mA   |  |        |
| Current consumption during GPIO communication VIO | I <sub>VIO_comm</sub>       | –      | –    | 5    | mA   | depending on load on GPIO  |        |
| Current consumption during CVM & BVM VS           | I <sub>VS_meas</sub>        | –      | 21   | 25   | mA   | Parallel measurement of all cells + block voltage measurement. VIO connected to Vregout. Incl. idle consumption I <sub>VS_idle</sub> |        |



**Power supply**

**Table 6 Electrical characteristics power supply (cont'd)**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter   | Symbol              | Values |      |      | Unit | Note or Test Condition  | Number |
|---|---------------------|--------|------|------|------|---|--------|
|   |                     | Min.   | Typ. | Max. |      |   |        |
| Current consumption during round robin scheme running VS                                    | $I_{VS\_RR}$        | –      | 9    | 26   | mA   | Only during round robin scheme is running. VIO connected to Vregout. Incl. idle consumption $I_{VS\_idle}$  |        |
| Current consumption during communication VS   | $I_{VS\_comm}$      | –      | 6.5  | 10.8 | mA   | Valid for GPIO or iso UART communication. Current to charge-up external interface components not included. Incl. idle consumption $I_{VS\_idle}$                                |        |
| Current consumption during communication only for external iso UART interface components VS | $I_{VS\_comm\_ext}$ | –      | –    | 6    | mA   | <sup>1)</sup> $C_{isoUART\_ser} = 1 \text{ nF}$<br>$BR_{isoUART} = 2 \text{ Mbits}$<br>$R_{isoUART\_ser} = 39 \Omega$<br>This consumption needs to be added to $I_{VS\_comm}$ . |        |

1) Not subject to production test, specified by design.

## 5 Cell management unit

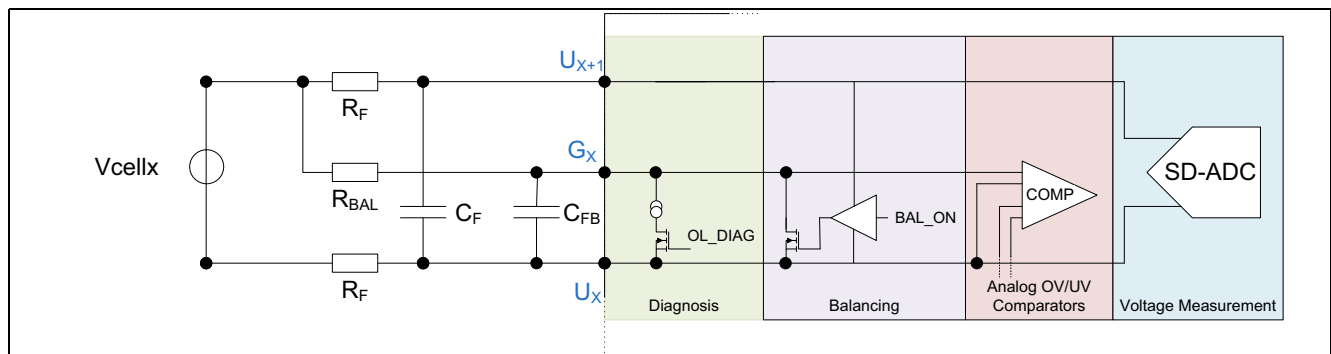
### 5.1 Overview

The TLE9012AQU provides the tools required for managing up to 12 cells stacked in series. It provides the following functions:

- Accurate voltage measurement
- Configurable OV/UV comparators
- Passive cell balancing
- Cell diagnosis

Additionally, other central functions take care of providing the tools to manage the module as a whole. More information can be found in [Chapter 8](#).

Each cell has the same structure as shown in [Figure 6](#). Additionally [Figure 6](#) shows how the unit is connected to the external structure. The cell voltage measurement unit contains a 16-Bit SD-ADC. It is recommend to use similar filter characteristics for the  $U_{x+1}$  -  $U_x$  and  $G_x$  -  $U_x$  input filters to support a synchronous OV/UV check with both units (comparator & SD-ADC).



**Figure 6** Example of internal structure for 1 cell monitoring hardware

### 5.2 Accurate cell voltage measurement

The exact voltage of each cell is necessary to estimate parameters like state of charge of the battery. The TLE9012AQU provides the necessary ADCs to accurately measure the voltage of each cell.

The voltage measurement path consists of 12 individual 16 bit delta sigma analog to digital converters, one for each cell. The use of separate ADC units enables the conversion of all 12 cell voltages simultaneously. The offset and gain errors of the converters are trimmed individually.

The AD conversion for all cells are initiated by writing the CVM\_START bit-field in the [MEAS\\_CTRL](#) register. The IC has the option to enable a programmable timer  $t_{CVM\_del}$ . After receiving a command, which initiates the start of a cell voltage measurement, this timer delays the start of the cell voltage measurement. The IC's cell voltage measurement ADC samples with  $f_s$  and averages the cell voltage measurement result of each cell for the duration of  $t_{CVM}$ . If CVM is started, during the  $t_{CVM}$ , the measurement result is reset. At the end of the conversion, the CVM\_START bit-field is automatically cleared and the RESULT is available. This bit-field can be monitored by reading the respective register. The result registers can be accessed by reading the RESULT bit-field in the [CVM\\_0](#) – [CVM\\_11](#) registers.

Different measurement modes can be selected (this mode will affect all channels at once):

**Table 7 Voltage measurement modes**

| Mode (CVM_BIT_WIDTH [2:0]) | Result resolution | Measuring time ( $t_{CVM}$ ) | ADC bandwidth (cut-off frequency) <sup>1)</sup> | FSR |
|----------------------------|-------------------|------------------------------|---|-----|
| 110                        | 16 Bit            | ~4.68 ms                     | 70 Hz   | 5 V |
| 101                        | 15 Bit            | ~2.34 ms                     | 140 Hz  |     |
| 100                        | 14 Bit            | ~1.17 ms                     | 280 Hz  |     |
| 011                        | 13 Bit            | ~585.1 $\mu$ s               | 560 Hz  |     |
| 010                        | 12 Bit            | ~292.6 $\mu$ s               | 1.12 kHz  |     |
| 001                        | 11 Bit            | ~146.3 $\mu$ s               | 2.24 kHz  |     |
| 000                        | 10 Bit            | ~73.1 $\mu$ s                | 4.48 kHz  |     |

1) The given cut-off frequencies are only theoretical calculations assuming 1st order averaging filter and should be used only for orientation purposes. They will neither be tested nor guaranteed.

The result is always an unsigned value. In case the result is less than 16 bits, the remaining LSBs will be set to "0". The equation to convert the value read from the RESULT bit-fields in the **CVM\_0** – **CVM\_11** registers to the cell voltage is:

$$\text{Cell voltage [mV]} = (\text{FSR} \cdot 1000 \text{ [mV]} / (2^{16})) \cdot \text{RESULT} \quad (5.1)$$

The voltage measurement unit averages the signal automatically over the entire measurement time. So the voltage measurement unit of each cell provides a built-in digital filtering for the cell voltage measurement. The reference for the primary cell voltage measurement ADCs is the internal voltage reference A.

Please note: As soon as a cell voltage measurement start command is received, any ongoing round robin schedule will be cancelled and the measurement will start after  $t_{CVM\_del}$ . After the measurement is finished, the RR task will be restarted. For more information please refer to **Chapter 8.3**.

## 5.2.1 Electrical characteristics

**Table 8 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter   | Symbol              | Values |                         |       | Unit | Note or Test Condition  | Number |
|---|---------------------|--------|-------------------------|-------|------|---|--------|
|   |                     | Min.   | Typ.                    | Max.  |      |   |        |
| Cell sense inputs                                     |                     |        |                         |       |      |   |        |
| CVM differential input current Un                     | $I_{Un\_CVM}$       | 18     | 25                      | 32    | μA   | during CVM<br>$V_{CVM}=5\text{ V}$<br>$0 \leq n \leq 12$<br>typ. value $I_{Un\_CVM} = V_{CVM} / 200\text{ k}\Omega$ |        |
| Input leakage current Un                              | $I_{Un\_leak}$      | -1.0   | 0                       | 1.0   | μA   | $0 \leq n \leq 12$<br>in sleep mode & in idle mode  |        |
| Timing  |                     |        |                         |       |      |   |        |
| CVM propagation delay within IC                       | $t_{CVM\_prop}$     | 0      | –                       | 10    | μs   | <sup>1)</sup> Propagation delay between complete arrival of CVM start message and the actual start of the CVM       |        |
| CVM start delay timer resolution                      | $t_{CVM\_del\_LSB}$ | 35.1   | 36.6                    | 38.1  | μs   | <sup>1)</sup>   |        |
| CVM start delay timer maximum interval                | $t_{CVM\_del\_max}$ | 1.09   | 1.13                    | 1.18  | ms   | <sup>1)</sup>   |        |
| Primary voltage measurement                           |                     |        |                         |       |      |   |        |
| CVM input range                                       | $V_{CVM}$           | 0      | –                       | 5     | V    | <sup>1)</sup> Measuring $V_{cell} = V_{Un+1} - V_{Un}$ ; $0 \leq n \leq 11$   |        |
| CVM resolution  | $V_{CVM\_LSB}$      | –      | $FSR/2^m$               | –     | V    | <sup>1)</sup> $10 \leq m \leq 16$ ; $FSR = 5\text{ V}$  |        |
| CVM ADC sampling frequency                            | $f_{s\_CVM\_ADC}$   | 13.44  | 14                      | 14.56 | MHz  | <sup>1)</sup>   |        |
| CVM time  | $t_{CVM}$           | –      | $2^m / f_{s\_CVM\_ADC}$ | –     | s    | <sup>1)</sup> $10 \leq m \leq 16$   |        |
| Maximum CVM time deviation between channels within IC | $Dev_{CVM\_IC}$     | -0.5   | –                       | 0.5   | %    | <sup>1)</sup> deviation between CVM time $t_{CVM}$ within one IC  |        |
| Maximum CVM time deviation across ICs                 | $Dev_{CVM\_chain}$  | -4     | –                       | 4     | %    | <sup>1)</sup> deviation between CVM time $t_{CVM}$ over all ICs   |        |

## Cell management unit

**Table 8 Electrical characteristics** (cont'd)

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter  | Symbol                  | Values |      |      | Unit | Note or Test Condition   | Number |
|--|-------------------------|--------|------|------|------|--|--------|
|  |                         | Min.   | Typ. | Max. |      |  |        |
| CVM relative accuracy - initial <sup>2)4)</sup>  | $CVM_{ERR\_relative}$   | -0.9   | –    | 0.9  | mV   | 16 bit mode<br>$V_{cell} = 4.3 \text{ V}$<br>$T_j = 25^\circ\text{C}$<br>$\pm 3$ sigma distribution within abs. min/max limits   |        |
| CVM accuracy - initial <sup>2)4)</sup>           | $CVM_{ERR}$             | -2     | –    | 2    | mV   | 14 - 16 bit mode<br>$2.7 \text{ V} \leq V_{cell} \leq 4.3 \text{ V}$<br>$T_j = 25^\circ\text{C}$<br>$\pm 3$ sigma distribution within abs. min/max limits<br>Accuracy at tester in backend |        |
| CVM accuracy EOL <sup>3)4)</sup>                 | $CVM_{ERR\_EOL}$        | -5.8   | –    | 5.8  | mV   | 14 -16 bit mode<br>$2.7 \text{ V} \leq V_{cell} \leq 4.3 \text{ V}$<br>$-40^\circ\text{C} \leq T_j \leq 125^\circ\text{C}$<br>$\pm 3$ sigma distribution within abs. min/max limits        |        |
| CVM accuracy EoL - 10 Bit mode <sup>1)3)4)</sup> | $CVM_{ERR\_EoL\_10Bit}$ | -25    | –    | 25   | mV   | 10 bit mode<br>$0.05 \text{ V} \leq V_{cell} \leq 4.8 \text{ V}$<br>$-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$<br>$\pm 3$ sigma distribution within abs. min/max limits           |        |

1) Not subject to production test, specified by design.

2) Initial accuracy verified by Infineon backend.

3) End-of-Life; according to AEC-Q100 Grade 1 Rev. H automotive qualification.

4) Parameters are verified during the following conditions: no NTC measurement; no iso UART communication; no AUX measurement

### 5.3 Configurable analog overvoltage/undervoltage (OV/UV) comparators

Additionally to the primary measurement path with the SD-ADC the TLE9012AQU includes also a separate analog OV/UV check (see also [Figure 6](#)) via comparators and a Digital-Analog-Converter (DAC). The threshold values of the comparators are configurable. Furthermore the comparator logic is averaging its checks over a time period of  $t_{comp}$ . Similar to the digital comparators used in the round robin scheme to check for OV/UV based on the primary measurement, the analog comparators check the voltage at Gx-Ux against the OV/UV thresholds stored in register [OL\\_OV\\_THR](#) and [OL\\_UV\\_THR](#) as secondary redundant OV/UV path.

This analog unit is connected to the Gx pin which also means the external filter structure is different from the primary path. The approach of the different pins avoids having potential faults violating both OV/UV check paths in the same way.

## **Cell management unit**

The analog OV/UV check against the thresholds happens synchronously to the digital check in every round robin scheme. Please see also round robin scheme description in [Chapter 8.3.1](#).

**Cell management unit**

**5.3.1 Electrical characteristics**

**Table 9 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

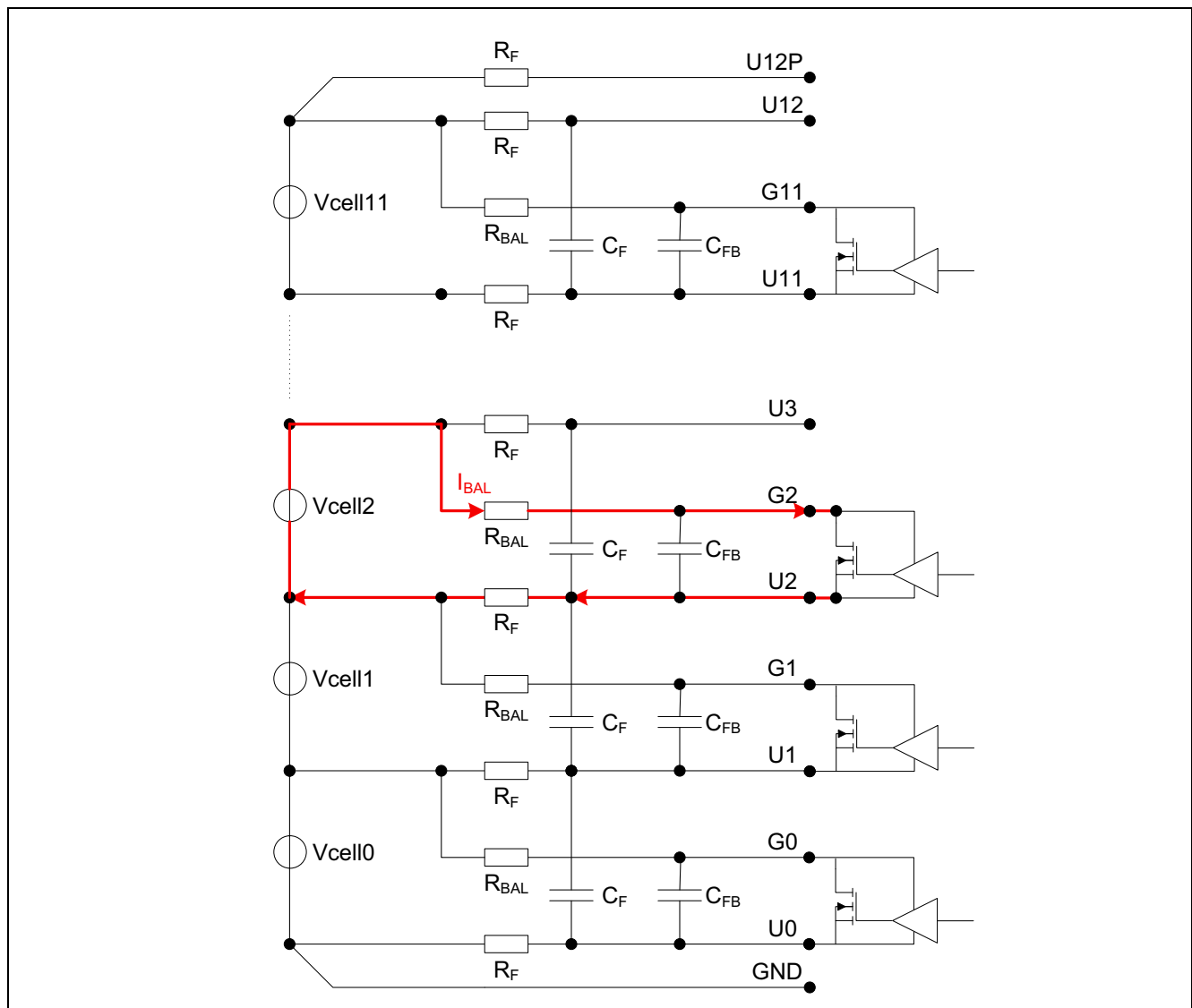
| Parameter                                   | Symbol                    | Values |                                     |      | Unit | Note or Test Condition  | Number |
|---|---------------------------|--------|-------------------------------------|------|------|---|--------|
|   |                           | Min.   | Typ.                                | Max. |      |   |        |
| Cell Gx sense inputs                        |                           |        |                                     |      |      |   |        |
| Comparator differential input current Gn    | $I_{Gn\_comp}$            | –      | 7                                   | 10   | μA   | 0 ≤ n ≤ 11 during comparator check in round robin <sup>1)</sup>                                       |        |
| Analog overvoltage/undervoltage comparators |                           |        |                                     |      |      |   |        |
| Comparator input range                      | $V_{Comp}$                | 0      | –                                   | 5    | V    | <sup>1)</sup> Measuring $V_{cell} = V_{Gn} - V_{Un}$<br>0 ≤ n ≤ 11                                    |        |
| Comparator resolution                       | $V_{Comp\_LSB}$           | –      | FSR/2 <sup>10</sup>                 | –    | V    | <sup>1)</sup> FSR = 5 V   |        |
| Comparator accuracy                         | $COMP_{ERR}$              | -50    | –                                   | 50   | mV   | 1 V < $V_{cell}$ < 4.7 V<br>-40°C ≤ $T_j$ ≤ 150°C<br>±3 sigma distribution within abs. min/max limits |        |
| Relative comparator accuracy                | $COMP_{ERR\_li}$<br>mited | -30    | –                                   | 30   | mV   | $V_{cell}$ = 3.6 V<br>-40°C ≤ $T_j$ ≤ 25°C<br>±3 sigma distribution within abs. min/max limits        |        |
| Comparator sampling frequency               | $f_{COMP}$                | 1      | –                                   | –    | MHz  | <sup>1)</sup>   |        |
| Comparator checking time                    | $t_{comp}$                | –      | 2 <sup>10</sup> / $f_{s\_CVM\_ADC}$ | –    | μs   | <sup>1)</sup>   |        |

1) Not subject to production test, specified by design.

**5.4 Cell balancing**

The TLE9012AQU IC supports passive balancing of up to 12 cells connected in series. The device contains 12 built-in MOSFET switches which can be used together with external resistors to dissipate each cell's energy, see [Figure 7](#).

Balancing can be activated for each cell independently and in any combination, including all 12 channels simultaneously. The internal switches can support balancing currents of  $I_{BAL}$ . For balancing currents higher than  $I_{BAL}$ , external P channel MOSFET transistors can be used as shown in [Figure 9](#).



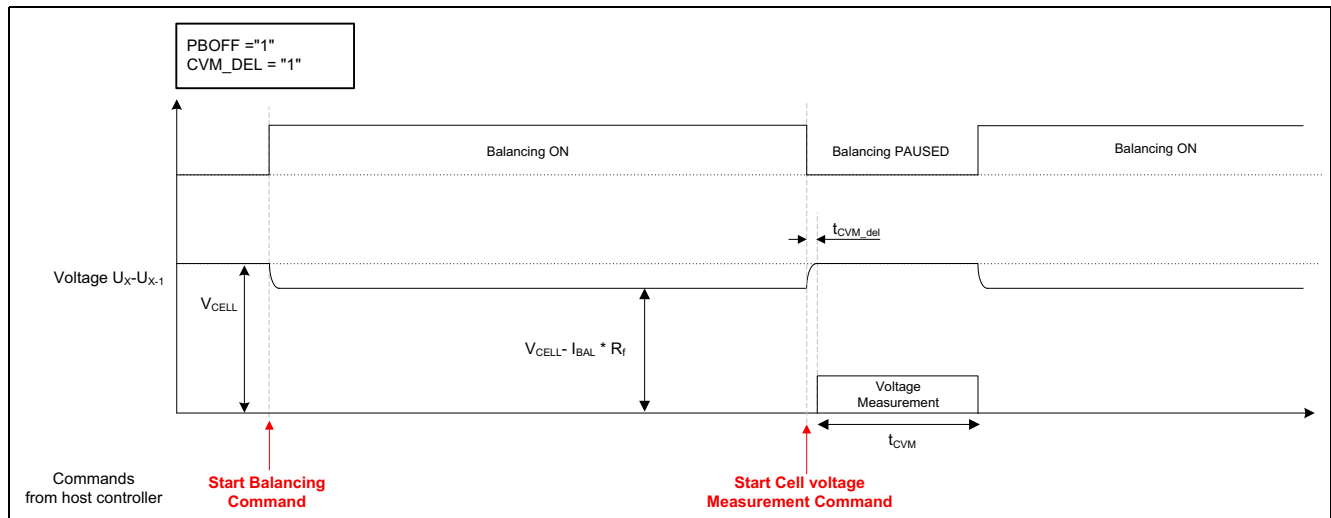
**Figure 7** Passive balancing example of Cell2

Passive balancing is initiated by the host microcontroller by writing to the **BAL\_SETTINGS** register via the UART or the iso UART interface. Writing a “1” to the ON\_1 bit-field, for instance, will turn on the passive balancing switch connected to the G1 pin and the current will start flowing. The switch remains on until a “0” is written to the ON\_1 bit-field, the IC enters the sleep state or a failure occurs (see [Chapter 8.4](#)).

To avoid measurement errors due to passive balancing current, the passive balancing switches can be deactivated automatically during the conversion by setting the PBOFF bit-field in the **MEAS\_CTRL** register.



## Cell management unit



**Figure 8** Timing diagram for balancing & cell voltage measurement with  $t_{CVM\_del}$  (PBOFF Bit = 1)

A programmable settling time  $t_{CVM\_del}$  (bit-field CVM\_DEL) can be programmed in the **MEAS\_CTRL** register; this delays the start of the measurement after the passive balancing transistors are disabled. Please note that for a global synchronization the start of the measurement is always delayed by  $t_{CVM\_del}$  no matter whether balancing was happening or not. Please see **Figure 8** for more details.

The TLE9012AQU includes an extended watchdog mode. In this mode, the watchdog LSB step interval changes to  $t_{WD\_EXT\_LSB}$ . With this extended timing, there is a maximum watchdog duration of  $t_{WD\_EXT\_max}$ .

During the round robin (RR) measurements, the passive balancing switches will be deactivated to avoid false detections during the round robin checks. After the RR scheme is done, the balancing will continue automatically (this is true independent of the PBOFF state). If balancing was activated before the RR starts, the RR will perform a balancing over- and undercurrent check. The balancing fault flag (one for OC and one for UC) is set in the **GEN\_DIAG** register if an overcurrent or undercurrent occurs on any cell.

The balancing function will be deactivated if one of the following errors is detected. The errors are indicated in **GEN\_DIAG**.

- Balancing error overcurrent, bit-field: BAL\_ERR\_OC. Balancing only for affected cell(s) deactivated.
- Balancing error undercurrent, bit-field: BAL\_ERR\_UC. Balancing only for affected cell(s) deactivated.
- Overvoltage error, bit-field: CELL\_OV. Balancing only for affected cell(s) deactivated.
- Undervoltage error, bit-field: CELL\_UV. Balancing only for affected cell(s) deactivated.
- Internal temperature sensor over temperature error, bit-field: INT\_OT. Balancing for all cells deactivated.
- External temperature sensor measurement error, bit-field: EXT\_OT. Balancing for all cells deactivated.
- Configuration register CRC error, bit-field: REG\_CRC\_ERR. Balancing for all cells deactivated.
- Internal IC error, bit-field: INT\_IC\_ERR. Balancing for all cells deactivated.
- Open load error, bit-field: OL\_ERR. Balancing for all cells deactivated.
- ADC error, bit-field: ADC\_ERR. Balancing for all cells deactivated.

### 5.4.1 Using external balancing switches

If the necessary current is higher than the maximum allowed internal balancing current, an external P-MOS can be used to increase the balancing current further. Assuming a proper dimensioning of the external components, all the functions remain unchanged. Please see **Figure 9** for more details. The  $R_{oc/uc}$  resistor is



**Cell management unit**

**Table 10 Electrical characteristics** (cont'd)

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                            | Symbol             | Values |      |               | Unit | Note or Test Condition  | Number |
|--------------------------------------|--------------------|--------|------|---------------|------|---|--------|
|                                      |                    | Min.   | Typ. | Max.          |      |   |        |
| Balancing current                    | $I_{BAL}$          | –      | –    | 150           | mA   | $1.5\text{V} \leq V_{Cell}$   |        |
| Balancing overcurrent detection time | $t_{BAL\_OC\_DET}$ | –      | –    | $t_{RR\_max}$ | ms   | <sup>1)</sup> Time till a balancing over current must be detected. Equivalent to max. round robin cycle time (when the error counter is disabled which is the default value, M_NR_ERR_BAL_OC = 1) |        |

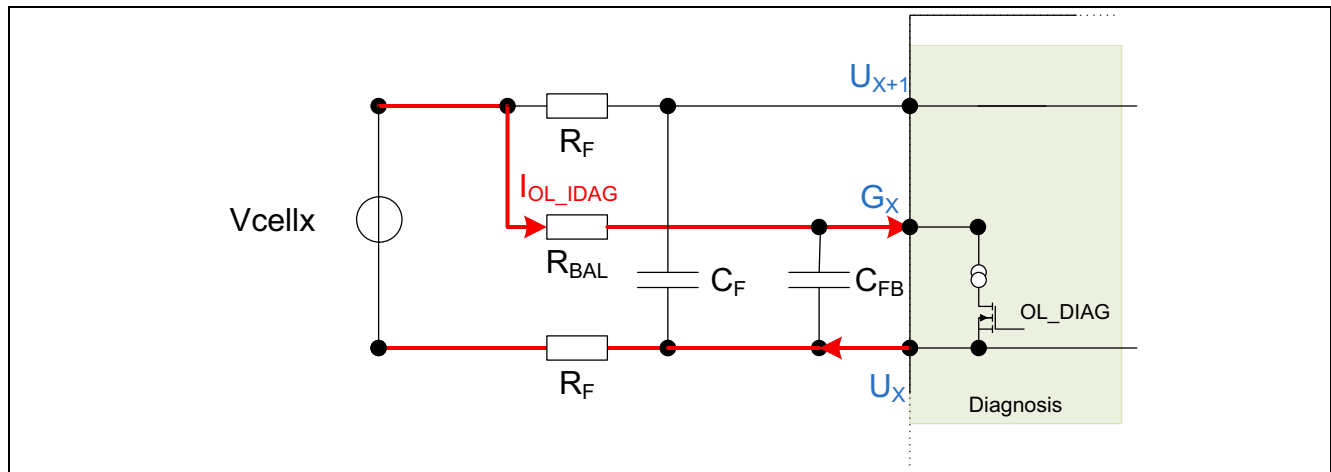
1) Not subject to production test, specified by design.

## 5.5 Cell diagnosis

The cell diagnosis are part of the round robin (see [Chapter 8.3](#)). The TLE9012AQU provides the necessary tools to detect a possible open load/wire of the different cell connections.

In order to help the diagnosis, the following hardware is available:

- 12x cell-specific Sigma-Delta ADC (CVM)
- 1x block measurement ADC (BVM)
- 12x diagnosis current sink (1x for each cell)



**Figure 10** Current path for open load detection

### 5.5.1 Automatic open load detection

The TLE9012AQU offers the possibility to automatically detect open wires in the following pins:  $U_x$ ,  $G_x$ , VS/U12P and GND.

The following steps are executed in the automatic open load detection:

- Turn off diagnosis current sinks and balancing switches (just to be sure that they are off).
- Wait for the duration set in the CVM\_DEL (register [MEAS\\_CTRL](#)).
- Voltage measurement with all CVM in fast acquisition mode (10 bits in 75  $\mu$ s).
- Measure block voltage with BVM. This step is done simultaneously with the previous one.
- Store all 13 intermediate values (12x CVM + 1x BVM) and perform ADC check.
- Turn ON all ODD diagnosis current sinks.
- Wait for the duration set in the CVM\_DEL (register [MEAS\\_CTRL](#)).
- Voltage measurement with all ODD SD-ADC.
- Turn OFF all ODD diagnosis current sinks.
- Compare ODD results.
- Turn ON all EVEN diagnosis current sinks.
- Wait for the duration set in the CVM\_DEL (register [MEAS\\_CTRL](#)).
- Voltage measurement with all EVEN SD-ADC.
- Turn OFF all EVEN diagnosis current sinks.
- Store all 12 intermediate values (6x odd cell specific values + 6x even cell specific values).
- Compare EVEN results.

## Cell management unit

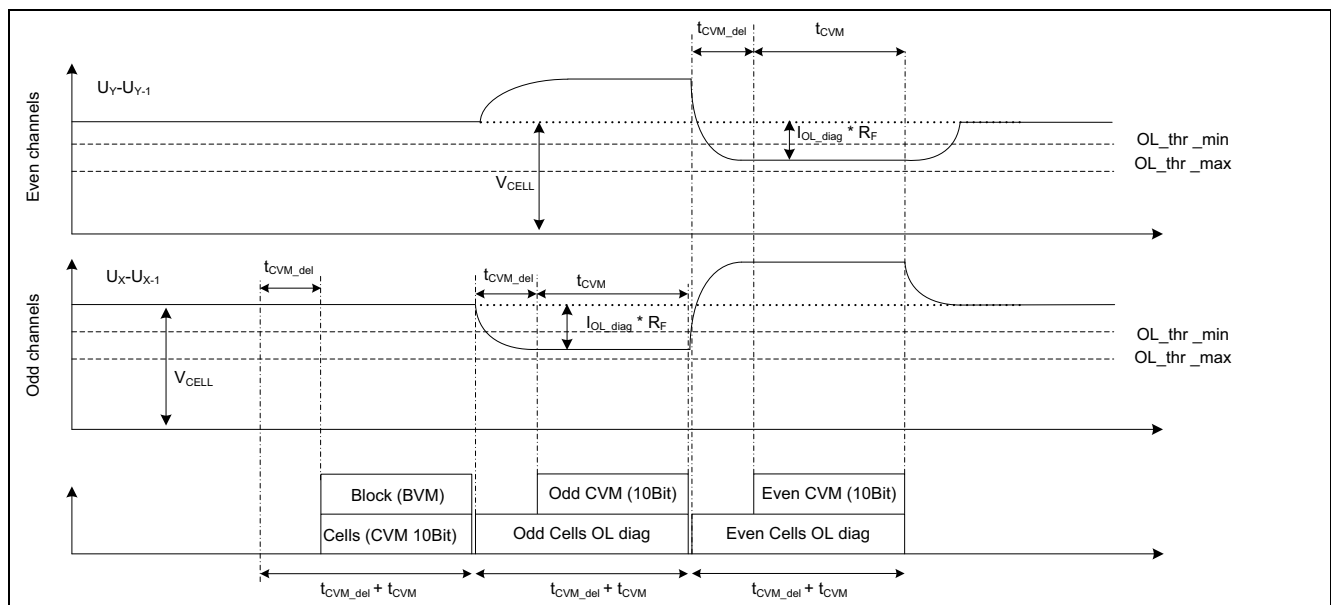
This test will detect an open wire in the path marked in red on **Figure 10**. The sequence above happens automatically within every RR (see also **Chapter 8**). Once the results are available the following conclusions can be derived:

- If the wire is intact, the voltage measurements before turning on the diagnosis current sinks and after turning off again shall have only a small difference (by  $I_{OL\_DIAG} \cdot R_F$ ). If the OL thresholds are set properly to the voltage difference, no OL fault will be indicated.
- If the wire is not connected at the cell (so an open connection between cell + / cell - and the respective  $R_F$  or the  $R_F$  itself at  $U_x$  is broken as open), the measurement comparison will result in a higher delta voltage and an OL fault will be indicated if the OL\_max threshold exceeded.
- if  $R_F$  at  $U_x$  is broken as a short or  $R_{BAL}$  is broken open, the result will be a lower delta voltage and an OL fault will be indicated if OL\_min threshold exceeded.

Furthermore in order to detect an open wire on the corner wire connecting pins U12P/U12/VS or GND/U0 (or the lowest  $U_x$  if less than 12 cells are connected) with the respective cell, all CVM values retrieved during the first CVM measurement need to be added up and the sum should be compared to the BVM (ADC check). This happens automatically in RR in the CVM vs BVM check:

- If the wire connecting U12P/U12/VS or GND/U0 is open, a CVM vs BVM check fault will occur.
- Further distinction between U12P/U12/VS and GND/U0 happens via a cell voltage check (similar to UV but with hard programmed 50 mV threshold). If the lowest cell voltage result is close to zero, the fault happened at GND/U0, and if the highest cell voltage result is close to zero, the fault happened at U12P/U12/VS.
- If both errors which are described above occur (CVM vs. BVM &  $V_{cell} < 50$  mV) at the same time, the TLE9012AQU also increments the respective OL error counter.

The following diagram shows the full process and the expected voltage variations:



**Figure 11 Open load detection timing diagram (no faults)**

### 5.5.2 Overcurrent and undercurrent

The TLE9012AQU offers the possibility to detect over- and undercurrent during balancing. This check will be done during the round robin diagnosis for each cell were balancing was active at the start of the round robin. The check principle is similar to the open load check described in the chapter above.

During balancing, the round robin function will read the cell voltage and compare the value to the expected value (voltage difference =  $I_{BAL} \cdot R_F$ ):

- If the difference is lower than the threshold UC\_THR (register **BAL\_CURR\_THR**), the undercurrent error counter will be incremented.
- If the difference is higher than the threshold OC\_THR (register **BAL\_CURR\_THR**), the overcurrent error counter will be incremented.

As soon as a balancing error is set in **GEN\_DIAG**, the balancing function will be disabled for the given channel. If an external PMOS is used see chapter 5.4.1.

### 5.5.3 Electrical characteristics

**Table 11 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter  | Symbol            | Values |              |      | Unit | Note or Test Condition   | Number |
|--|-------------------|--------|--------------|------|------|--|--------|
|  |                   | Min.   | Typ.         | Max. |      |  |        |
| Sink current for open load diagnosis                 | $I_{OL\_DIAG}$    | 10     | 15           | 18.3 | mA   | $0.75 \text{ V} \leq V_{cell}$   |        |
| <b>Open load</b>                                     |                   |        |              |      |      |  |        |
| Open load threshold maximum value                    | $OL_{thr\_range}$ | –      | 307.6        | –    | mV   | <sup>1)</sup> bit-field with 6 bits                                    |        |
| Open load threshold resolution                       | $OL_{thr\_res}$   | –      | $FSR/2^{10}$ | –    | mV   | <sup>1)</sup> $FSR = 5 \text{ V}$                                      |        |
| <b>Balancing overcurrent &amp; undercurrent</b>      |                   |        |              |      |      |  |        |
| Balancing overcurrent error threshold maximum value  | $OC_{thr\_range}$ | –      | 1.245        | –    | V    | <sup>1)</sup> bit-field with 8 bits. $I_{OC\_thr} = OC\_THR [V] / R_f$ |        |
| Balancing undercurrent error threshold maximum value | $UC_{thr\_range}$ | –      | 1.245        | –    | V    | <sup>1)</sup> bit-field with 8 bits. $I_{UC\_thr} = UC\_THR [V] / R_f$ |        |
| Balancing overcurrent error threshold resolution     | $OC_{thr\_res}$   | –      | $FSR/2^{10}$ | –    | mV   | <sup>1)</sup> $FSR = 5 \text{ V}$                                      |        |
| Balancing undercurrent error threshold resolution    | $UC_{thr\_res}$   | –      | $FSR/2^{10}$ | –    | mV   | <sup>1)</sup> $FSR = 5 \text{ V}$                                      |        |

1) Not subject to production test, specified by design.

## 6 Cell block voltage and auxiliary measurements

Additionally to the 12 dedicated cell voltage measurement ADCs (CVM), a 13th ADC is available to perform different auxiliary voltage measurements including a block voltage measurement (BVM) from U12P to GND. This ADC has a different reference (Reference B) than the CVM ADCs (Reference A). **Figure 12** shows how the 13th ADC is connected within the device.

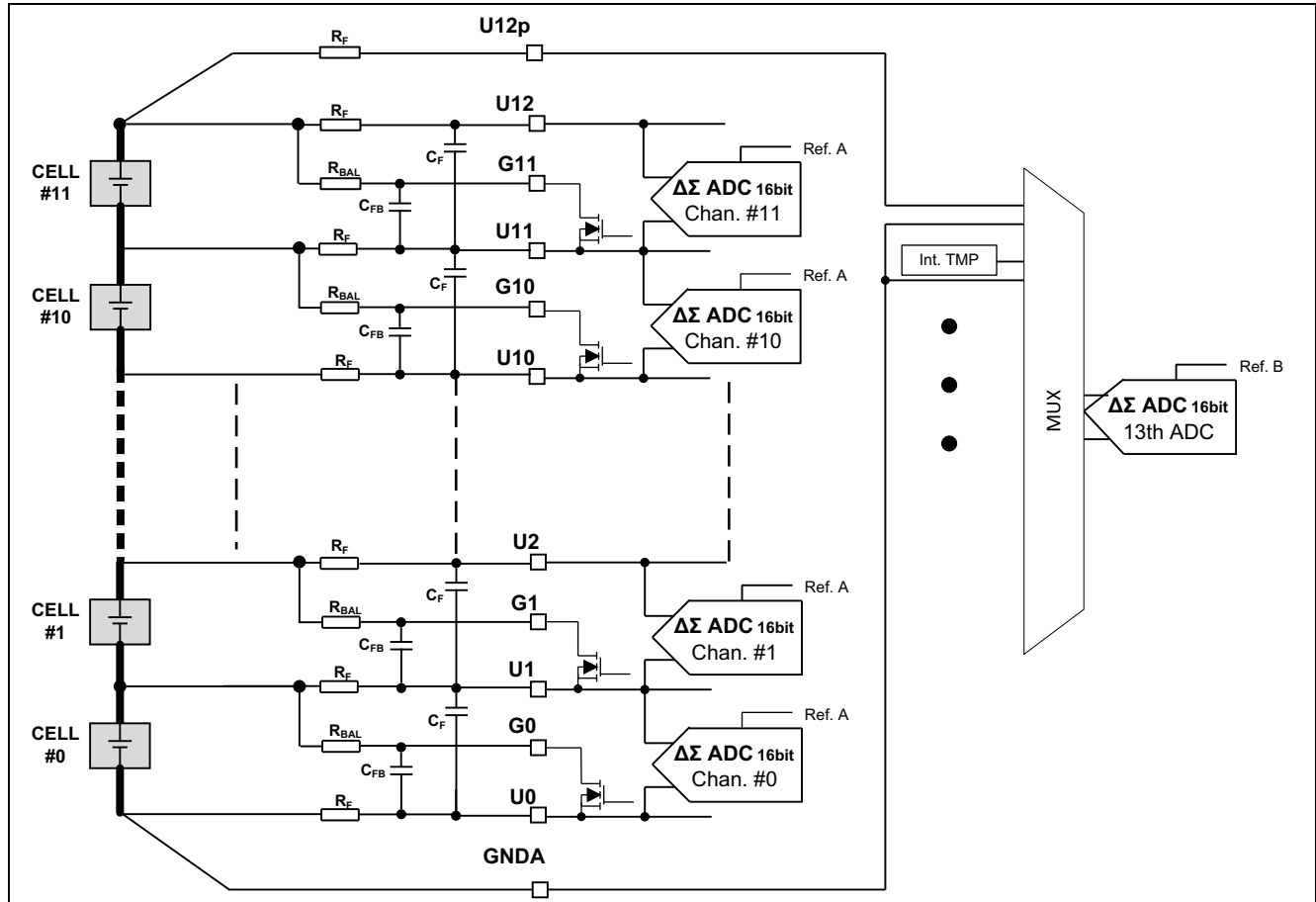


Figure 12 BVM/AVM block diagram

### 6.1 Cell block voltage measurement (BVM) description

The 13th ADC can perform a block voltage measurement (BVM). This measurement can be used as ADC check of the 12 cell specific voltage measurements by comparing the sum with the BVM result. The block measurement is initiated by setting the BVM\_START bit-field in the **MEAS\_CTRL** register and starts after  $t_{BVM\_prop}$ . During the conversion time the BVM\_START bit is set ("1") and the RESULT bit-field in the **BVM** register is cleared ("0").

Please note: As soon as a block voltage measurement start command is received, any ongoing round robin schedule will be cancelled and the measurement will start immediately after  $t_{BVM\_prop}$ . After the measurement is finished, the RR task will be restarted. For more information please refer to **Chapter 8.3**.

By setting the bit-fields BVM\_START and CVM\_START (register **MEAS\_CTRL**) with the same write command, both measurements will happen simultaneously which can be useful for a plausibility comparison in the microcontroller. The conversion time can be selected similar to the CVM:

## Cell block voltage and auxiliary measurements

**Table 12 BVM modes**

| Mode (BVM_BIT_WIDTH [2:0]) | Result resolution | Measuring time ( $t_{BVM}$ ) | ADC bandwidth (cut-off frequency) <sup>1)</sup> | FSR  |
|----------------------------|-------------------|------------------------------|---|------|
| 110                        | 16 Bit            | ~4.68 ms                     | 70 Hz   | 60 V |
| 101                        | 15 Bit            | ~2.34 ms                     | 140 Hz  |      |
| 100                        | 14 Bit            | ~1.17 ms                     | 280 Hz  |      |
| 011                        | 13 Bit            | ~585.1 $\mu$ s               | 560 Hz  |      |
| 010                        | 12 Bit            | ~292.6 $\mu$ s               | 1.12 kHz  |      |
| 001                        | 11 Bit            | ~146.3 $\mu$ s               | 2.24 kHz  |      |
| 000                        | 10 Bit            | ~73.1 $\mu$ s                | 4.48 kHz  |      |

1) The given cut-off frequencies are only theoretical calculations assuming 1st order averaging filter and should be used only for orientation purposes. They will neither be tested nor guaranteed.

When the conversion is complete, the result can be read out via RESULT bit-field in the **BVM** register. The result is always an unsigned value. In case the result is less than 16 bits, only the MSBs are useful. The remaining LSBs will be set to “0” automatically.

The equation to convert the value read from the RESULT bit-field in the **BVM** register to the cell voltage is:

$$\text{Block voltage [mV]} = (\text{FSR} \cdot 1000 \text{ [mV]} / (2^{16})) \cdot \text{RESULT} \quad (6.1)$$

## 6.2 Auxiliary voltage measurement (AVM) description

The 13th SD-ADC can also be used to measure other internal and external voltages as shown in **Figure 12**. The following AVMs are available:

- external temperature measurement of TMP 0
- external temperature measurement of TMP 1
- external temperature measurement of TMP 2
- external temperature measurement of TMP 3
- external temperature measurement of TMP 4
- miscellaneous auxiliary measurement via TMP0 pin if TMP 0 is inactive in **TEMP\_CONF**
- miscellaneous auxiliary measurement via TMP1 pin if TMP 1 is inactive in **TEMP\_CONF**
- miscellaneous auxiliary measurement via TMP2 pin if TMP 2 is inactive in **TEMP\_CONF**
- miscellaneous auxiliary measurement via TMP3 pin if TMP 3 is inactive in **TEMP\_CONF**
- miscellaneous auxiliary measurement via TMP4 pin if TMP 4 is inactive in **TEMP\_CONF**
- diagnosis resistor  $R_{DIAG}$  of external measurement unit

The TMP measurements happen on a cyclical basis within the round robin scheduler (see also **Chapter 8.3** and **Chapter 7**). So the measurement data will be periodically refreshed and is accessible in the corresponding result registers. Furthermore, the miscellaneous auxiliary measurements (in case the corresponding TMP is inactive) as well as the diagnosis resistor measurement must be triggered manually.

The measurement start of a manual triggered AVM happens by setting AVM\_START in the **MEAS\_CTRL** register. Which of the AVM measurements are performed can be set by the bit-field AVM\_xxxx\_MASK or R\_DIAG bit-field (register **AVM\_CONFIG**).



**Cell block voltage and auxiliary measurements**

**6.3 Electrical characteristics**

**Table 13 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                                   | Symbol               | Values |                                       |       | Unit | Note or Test Condition   | Number |
|---|----------------------|--------|---------------------------------------|-------|------|--|--------|
|   |                      | Min.   | Typ.                                  | Max.  |      |  |        |
| Cell sense inputs                           |                      |        |                                       |       |      |  |        |
| BVM input current U12P                      | $I_{U12P\_BVM}$      | –      | 280                                   | 400   | μA   | <sup>1)</sup> during BVM   |        |
| Synchronization timing                      |                      |        |                                       |       |      |  |        |
| BVM propagation delay within IC             | $t_{BVM\_prop}$      | 0      | –                                     | 10    | μs   | <sup>1)</sup> Propagation delay between complete arrival of BVM start message and the actual start of the BVM                            |        |
| Block voltage measurement                   |                      |        |                                       |       |      |  |        |
| BVM input range                             | $V_{BVM}$            | 4.75   | –                                     | 60    | V    | <sup>1)</sup> $V_{BVM} = V_{U12P} - V_{GND}$   |        |
| BVM resolution                              | $V_{BVM\_LSB}$       | –      | FSR/2 <sup>m</sup>                    | –     | V    | <sup>1)</sup> 10 ≤ m ≤ 16; FSR = 60 V  |        |
| BVM ADC sampling frequency                  | $f_{s\_BVM\_ADC}$    | 13.44  | 14                                    | 14.56 | MHz  | <sup>1)</sup>  |        |
| BVM time                                    | $t_{BVM}$            | –      | 2 <sup>m</sup> /<br>$f_{s\_BVM\_ADC}$ | –     | s    | <sup>1)</sup> m bits 10 ≤ m ≤ 16   |        |
| Maximum BVM to CVM time deviation within IC | $Dev_{BVM\_CVM\_IC}$ | -0.5   | –                                     | 0.5   | %    | <sup>1)</sup> deviation between BVM time $t_{BVM}$ and CVM time $t_{CVM}$ within one IC  |        |
| Maximum BVM time deviation across ICs       | $Dev_{BVM\_chain}$   | -4     | –                                     | 4     | %    | <sup>1)</sup> deviation between BVM time $t_{BVM}$ over all ICs  |        |
| BVM accuracy EoL <sup>2)</sup>              | $BVM_{ERR}$          | -70    | –                                     | 70    | mV   | <sup>3)</sup> 14 - 16 Bit mode<br>4.75 V ≤ $V_{BVM}$ ≤ 60 V<br>-40°C ≤ $T_j$ ≤ 150°C<br>±3 sigma distribution within abs. min/max limits |        |

**Cell block voltage and auxiliary measurements**

**Table 13 Electrical characteristics** (cont'd)

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                              | Symbol             | Values |      |      | Unit | Note or Test Condition   | Number |
|--|--------------------|--------|------|------|------|--|--------|
|  |                    | Min.   | Typ. | Max. |      |  |        |
| BVM accuracy EoL <sup>2)</sup> - 10Bit | $BVM_{ERR\_10Bit}$ | -250   | –    | 110  | mV   | <sup>1)3)</sup> 10 Bit mode<br>$4.75 \text{ V} \leq V_{BVM} \leq 60 \text{ V}$<br>$-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$<br>$\pm 3$ sigma distribution within abs. min/max limits |        |

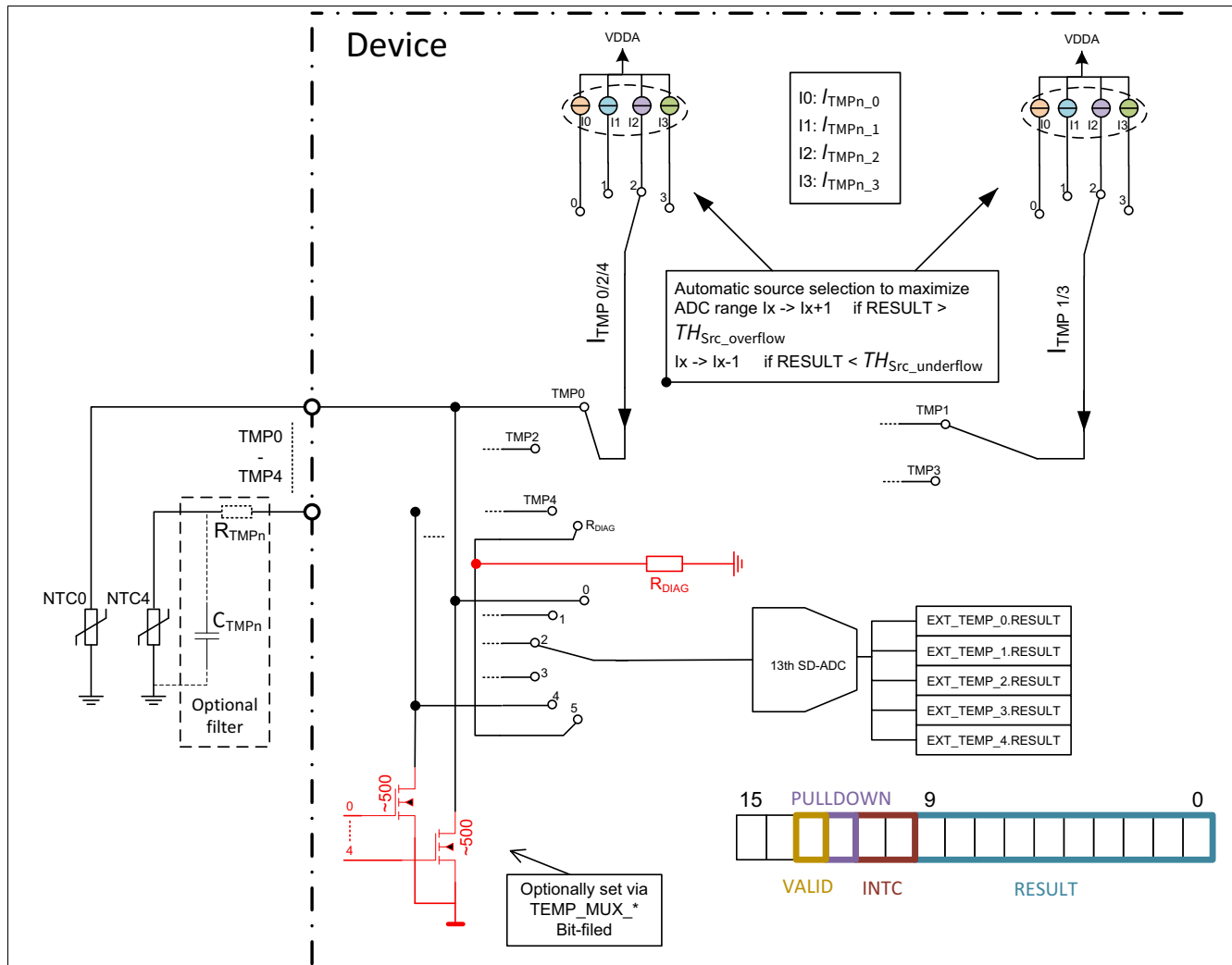
**Auxiliary voltage measurement**

|                                    |                           |     |                          |    |    |   |  |
|------------------------------------|---------------------------|-----|--------------------------|----|----|---|--|
| AUX input range                    | $V_{AUXn} - V_{TMP\_GND}$ | 0   | –                        | 2  | V  | $0 \leq n \leq 4$   |  |
| AUX resolution                     | $V_{AUX\_LSB}$            | –   | $FSR/2^{10}$             | –  | V  | <sup>1)</sup> $FSR = 2 \text{ V}$   |  |
| AUX measurement time               | $t_{AUX}$                 | –   | $2^{10}/f_{s\_BVM\_ADC}$ | –  | s  | <sup>1)</sup>   |  |
| AUX ADC accuracy EoL <sup>2)</sup> | $AUX_{ERR}$               | -45 | –                        | 45 | mV | 10 Bit mode<br>$0.05 \text{ V} \leq V_{AUX} \leq 1.95 \text{ V}$<br>$-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$ |  |

- 1) Not subject to production test, specified by design.
- 2) End-of-Life; according to AEC-Q100 Grade 1 Rev. H automotive qualification.
- 3) Parameters are verified during the following conditions: no NTC measurement; no iso UART communication; no AUX measurement

## 7 Temperature measurement

The TLE9012AQU has 5 inputs for measuring external temperature sensors (NTC's). To measure the resistance a current is forced through the NTC, the resulting voltage drop is measured by the 13th ADC (see [Chapter 6](#)).



**Figure 13 External temperature measurement overview**

In order to get a sufficient resistance measurement resolution independent of the resistance range, the TLE9012AQU will – as part of the round robin scheme – automatically identify which one of the four sources is the best one to use.

The measurement will be performed as part of the round robin scheme. Up to two temperature measurements can be performed in every round robin scheme. It is recommended to use the RR\_SYNC feature to trigger the round robin manually (see [Chapter 8.3.2](#)) in case the NTC measurement is actively used as part of it. Goal is to avoid a clash of the round robin and the CVM/BVM/AVM which would delay the round robin execution (see [Chapter 8.3.4](#)). Reason is that the current sources which power the NTCs are deactivated in case the round robin gets delayed due to a clash with CVM/BVM/AVM.

Results are stored in the respective registers including the information of which current source was chosen for this particular measurement. Based on this information the NTC resistance can be calculated as follows:

$$R_{NTC} [Ohm] = (RESULT [LSB10] * FSR [V] * 4^{INTC}) / (2^{10} * 320 \mu A) - R_{TMP}; INTC = 0 \dots 3 \text{ (used current source)}$$

For testing the correct functionality of the temperature sensor multiplexer, pull down switches are implemented to pull each TMP input to ground. These switches can be activated by setting

## Temperature measurement

TEMP\_MUX\_DIAG\_SEL bit-fields (register [AVM\\_CONFIG](#)). If the pull down was active during the measurement, this will be shown by setting the respective pull-down\_x bit-field in the result register. The VALID\_x bit-fields in the same register indicate a valid (new) measurement. They are cleared after readout.

### External temperature sensor diagnostics

Overtemperature, shorted NTC, and open NTC faults are detected automatically as part of the round robin scheme of the TLE9012AQU. The short and open detection works in the following manner:

- open detected:  $RESULT \geq 1023$  [LSB10] &  $I_{TMPn\_3}$  used
- short detected:  $RESULT \leq 64$  [LSB10] &  $I_{TMPn\_0}$  used

The faults are indicated by the fault flag bits in the [EXT\\_TEMP\\_DIAG](#) register. An overtemperature, short, or open fault on any of the NTC inputs will set the EXT\_OT fault bit-field in the [GEN\\_DIAG](#) register. The EXT\_OT fault bit-field is cleared by writing a “0” to this bit-field, which will also trigger a reset of the value of the [EXT\\_TEMP\\_DIAG](#) register to the reset value. The overtemperature threshold and the NTC bias current used for the overtemperature measurement can be selected in the [TEMP\\_CONF](#) register.

Furthermore the correct functionality of the measurement unit can be checked by measuring against an internal diagnosis resistor as part of the manual AVI. The diagnosis resistor measurement will be done only via current  $I_{TMP0\_2}$ .

### Internal chip temperature

An on-chip temperature sensor provides information about the internal temperature of the TLE9012AQU near the bandgap references. The value is stored in the [INT\\_TEMP](#) register. The junction temperature  $T_j$  can be calculated using the formula:

$$\text{Temperature } [^{\circ}\text{C}] = -T_{\text{int\_LSB}} * \text{RESULT} + 547.3 \quad (7.1)$$

## 7.1 Electrical characteristics

**Table 14 Electrical characteristics**

$V_{\text{VS}} = 4.75 \text{ V}$  to  $60 \text{ V}$ ,  $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                                  | Symbol                | Values |            |      | Unit | Note or Test Condition  | Number |
|--|-----------------------|--------|------------|------|------|---|--------|
|  |                       | Min.   | Typ.       | Max. |      |   |        |
| Internal temperature sensors               |                       |        |            |      |      |   |        |
| internal temperature resolution            | $T_{\text{int\_LSB}}$ | -      | 0.66<br>24 | -    | K    | 1)  |        |
| External temperature sensors               |                       |        |            |      |      |   |        |
| External NTC resistor measurement accuracy | $NTC_{\text{ERR}}$    | -2     | –          | 2    | %    | Accuracy of measured NTC resistance value in the range of 1.22 kΩ to 390 kΩ |        |
| External NTC resistor measurement accuracy | $NTC_{\text{ERR}}$    | -3     | –          | 3    | %    | Accuracy of measured NTC resistance value in the range of 1.22 kΩ to 610 Ω  |        |

**Temperature measurement**

**Table 14 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                                  | Symbol                    | Values |          |       | Unit          | Note or Test Condition   | Number |
|--|---------------------------|--------|----------|-------|---------------|--|--------|
|  |                           | Min.   | Typ.     | Max.  |               |  |        |
| External NTC resistor measurement accuracy | $NTC_{ERR}$               | -4.8   | –        | 4.8   | %             | Accuracy of measured NTC resistance value in the range of 610 $\Omega$ to 400 $\Omega$ |        |
| Temperature ADC voltage input range        | $V_{TMPn} - V_{TMP\_GND}$ | 0      | –        | 2     | V             | <sup>1)</sup> $0 \leq n \leq 4$  |        |
| Measurement current                        | $I_{TMPn\_0}$             | 307.2  | 320      | 332.8 | $\mu\text{A}$ | $0 \leq n \leq 4$  |        |
| Measurement current                        | $I_{TMPn\_1}$             | 76.8   | 80       | 83.2  | $\mu\text{A}$ | $0 \leq n \leq 4$  |        |
| Measurement current                        | $I_{TMPn\_2}$             | 19.2   | 20       | 20.8  | $\mu\text{A}$ | $0 \leq n \leq 4$  |        |
| Measurement current                        | $I_{TMPn\_3}$             | 4.5    | 5        | 5.5   | $\mu\text{A}$ | $0 \leq n \leq 4$  |        |
| Internal TMP diagnosis resistor RDIAG      | $R_{DIAG}$                | 19.9   | –        | 31.9  | k $\Omega$    |  |        |
| Pull-down switch on-state resistance       | $R_{PD\_DSON}$            | –      | –        | 400   | $\Omega$      |  |        |
| Source selection overflow threshold        | $TH_{Src\_overflow}$      |        | 100<br>0 |       |               | <sup>1)</sup>  |        |
| Source selection underflow threshold       | $TH_{Src\_underflow}$     |        | 200      |       |               | <sup>1)</sup>  |        |

**External components**

|                      |            |   |   |    |    |                                 |  |
|----------------------|------------|---|---|----|----|---------------------------------|--|
| NTC filter capacitor | $C_{TMPn}$ | – | – | 10 | nF | <sup>1)</sup> $0 \leq n \leq 4$ |  |
|----------------------|------------|---|---|----|----|---------------------------------|--|

1) Not subject to production test, specified by design.

## 8 Housekeeping functions

### 8.1 Functional description

This chapter describes several functions required to function the TLE9012AQU.

These functions are:

- watchdog and wake-up function
- round robin scheme triggering diagnosis checks cyclically
- Emergency Mode (EMM) & ERR pin function

### 8.2 Watchdog and wake-up function

The TLE9012AQU has a watchdog implemented that if not triggered correctly will transfer the part to sleep mode. If the device is in sleep mode, it needs to receive a wake-up signal in order to trigger the wake-up procedure to enter normal operation.

In the following these two functions will be detailed.

#### 8.2.1 Watchdog counter

A watchdog counter is implemented that must be exercised by regular iso UART or UART communication in order to keep the TLE9012AQU in normal mode. If the watchdog expires, the device will enter sleep mode. The watchdog counter is a 7 bit unsigned down counter. The value of the counter (WD\_CNT, register **WDOG\_CNT**) after a reset is 0x7Fh. The counter is decremented with a clock of either  $t_{WD}$  or  $t_{EXT\_WD}$  depending on the setting of the EXT\_WD bit-field (register **OP\_MODE**) (see [Chapter 5.4](#)).

The WD\_CNT value must be written to a value  $> 0$  by either the UART or iso UART interface before the watchdog counter reaches 0. Otherwise the device will revert to sleep mode which includes disabling balancing as soon as the watchdog has timed out.

Additionally the **WDOG\_CNT** register contains a main counter (MAIN\_CNT) which is a free-running 9 bit up counter clocked with a  $t_{MAIN\_CNT}$ . This signal is derived from the main oscillator of the TLE9012AQU. The content of this counter can be checked by the host microcontroller in order to verify the value of the main oscillator frequency.

#### 8.2.2 Sleep mode and wake-up function

In sleep mode the power dissipation of the receiver logic is very low. However, the TLE9012AQU will continue to monitor all the communication interfaces (iso UART and UART) waiting for a wake-up sequence. Please note that a wake-up via UART/GPIO is possible if voltage at VIO pin  $> V_{VIO\_th\_UV\_rise}$ .

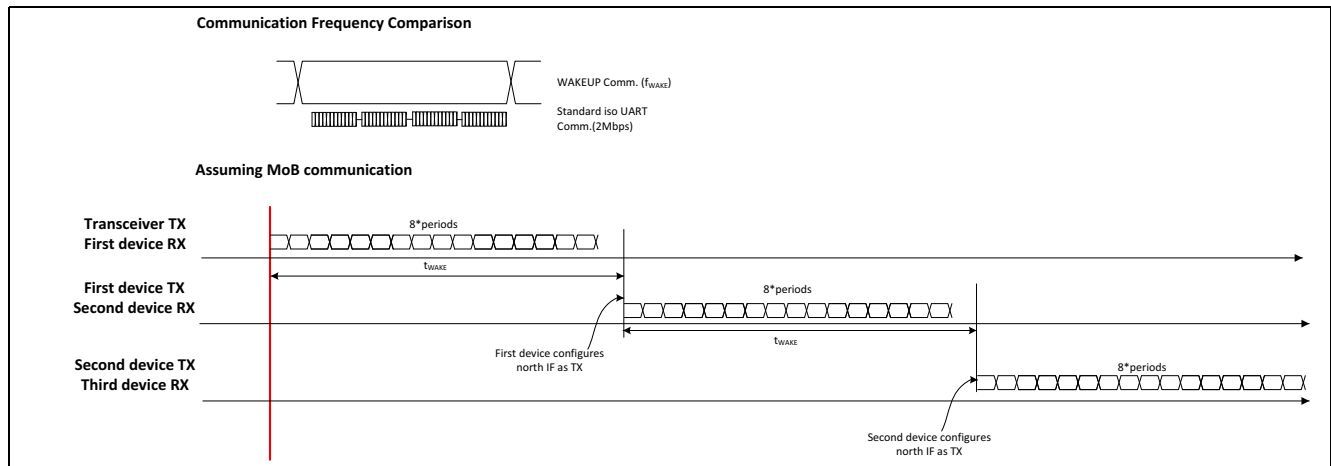
The wake-up sequence is a alternating sequence (with frequency  $f_{WAKEUP}$ ) to be sent by the bus master's iso UART/UART interface.

After  $n_{WAKE\_det}$  complete periods are detected, the device will trigger a wake-up and will require a wake-up time  $t_{WAKE}$  before standard datagrams can be processed. The default direction of the interface where the wake-up signal was detected will be configured as RX (receive) until the device enters sleep mode again. The default direction of the other interface will be configured as TX (transmit) until the device enters sleep mode again.

After  $t_{WAKE}$  the device will start generating a wake-up signal at the TX interface to wake up the next device.

Please keep in mind that the wake-up signal will be propagated through the entire network.

## Housekeeping functions



**Figure 14** Wake-up signals

Approximately 1 ms after the cells are being connected to the device it will be able to detect a wake-up signal and trigger a wake-up.

### 8.2.3 Wake-up procedure

After the wake up following default settings will be used:

- The watchdog counter will be set to the max. value: 0x7F.
- The iso UART node ID will be set to 0.
- The internal checks will be started to be ready for measurements.
- Depending what triggered the wake-up:
  - Round robin sleep time-out: Round robin will be restarted. After RR is finished, the part will go immediately into sleep mode.
  - EMM signal received: Signal will also be generated. After the signal has been sent, the part will go immediately into sleep mode.
  - Wake-up signal received: Signal will also be generated.

If the wake-up reason is a wake-up signal, the device will stay awake and wait for enumeration.

The enumeration procedure is started by the microcontroller. After a wake-up signal has been sent through the chain, all the devices are numbered as “#0”, and in this status the devices will not forward any iso UART messages except for EMM signals.

The microcontroller will send (from either the IFH or IFL interfaces) a write command to device ID#0 changing the ID from #0 to #1. With this, the first device in the chain is already numbered as #1. Since it is no longer #0, the first device in the chain will forward the messages further in the chain; therefore the microcontroller can again send a write command to device ID#0 changing the ID from #0 to #2. Now the second device is already numbered as #2. This task must be continued until the message is received by the opposite interface on the microcontroller side (Ring mode: if the first message was sent from IFL that will be IFH or vice versa). The last device in the chain must be marked as final node.

Please note that the numbering in the chain must always be consecutive, starting with the lowest number next to the master of the chain. Otherwise there is a potential risk of clash in the communication bus.

### 8.2.4 Electrical characteristics

## Housekeeping functions

**Table 15 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                            | Symbol                    | Values |            |        | Unit    | Note or Test Condition  | Number |
|--------------------------------------|---------------------------|--------|------------|--------|---------|---|--------|
|                                      |                           | Min.   | Typ.       | Max.   |         |   |        |
| Wake-up function                     |                           |        |            |        |         |   |        |
| Wake-up signal frequency             | $f_{\text{WAKEUP}}$       | 48     | 50         | 1040   | kHz     | –   |        |
| Device wake-up time                  | $t_{\text{WAKE}}$         | 200    | 370        | 500    | μs      | 48 kHz wake-up frequency from first falling edge of the input pattern to the first edge of the propagated wake-up sequence. |        |
| Wake-up - number of detected periods | $n_{\text{WAKE\_det}}$    | 4      | –          | 8      | periods | –   |        |
| Wake-up - length in periods          | $n_{\text{WAKE}}$         | 8      | –          | 8      | periods | –   |        |
| Watchdog counter                     |                           |        |            |        |         |   |        |
| Watchdog interval step               | $t_{\text{WD\_LSB}}$      | 14.5   | 16         | 17.8   | ms      | <sup>1)</sup> EXT_WD = 0  |        |
| Watchdog interval step - extended    | $t_{\text{WD\_EXT\_LSB}}$ | 13.5   | 15.07      | 17     | min     | <sup>1)</sup> EXT_WD = 1  |        |
| Watchdog maximum interval            | $t_{\text{WD\_max}}$      | 1.8    | 2.03       | 2.3    | s       | <sup>1)</sup> EXT_WD = 0  |        |
| Watchdog maximum interval - extended | $t_{\text{WD\_EXT\_max}}$ | 28.9   | 31.9       | 35.5   | h       | <sup>1)</sup> EXT_WD = 1  |        |
| Main counter                         |                           |        |            |        |         |   |        |
| Main counter interval step           | $t_{\text{count\_LSB}}$   | 281    | 292.5<br>7 | 305    | μs      | <sup>1)</sup>   |        |
| Main counter maximum interval        | $t_{\text{count\_max}}$   | 144.03 | 149.8      | 156.03 | ms      | <sup>1)</sup>   |        |

1) Not subject to production test, specified by design.

## 8.3 Round robin

The TLE9012AQU provides the necessary logic to perform a round robin scheduling scheme to trigger internal diagnostics to check for possible faults. Furthermore the round robin (RR) scheduling triggers the external (via connected NTC) and internal temperature measurement.

In normal mode the device will run the round robin schedule cyclically. The next chapters discussing the RR scheduler and its tasks. During sleep mode, the device has the possibility to wake-up periodically for a short time to apply one RR scheme. RR during sleep mode is described in [Chapter 8.3.3](#).

### 8.3.1 Round robin tasks

The round robin performs the following tasks:

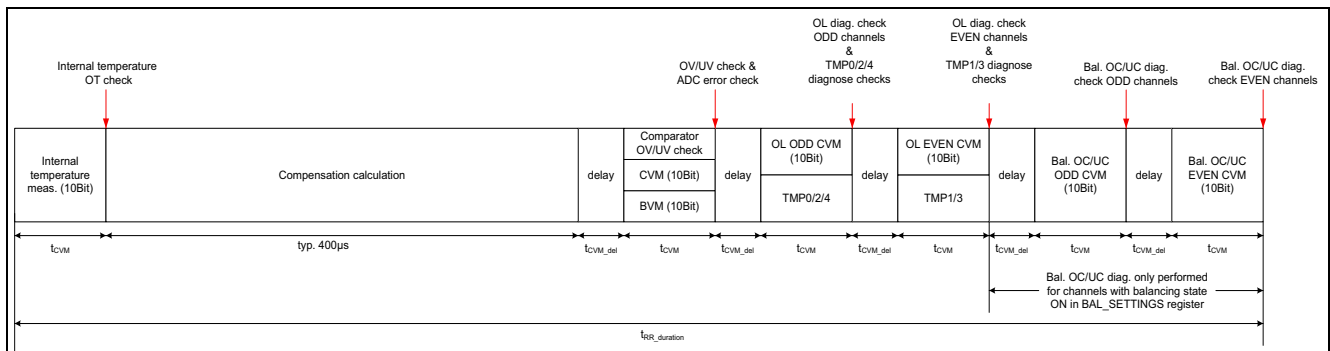
- Internal temperature measurement & overtemperature check



## Housekeeping functions

- Compensation calculations
- Check of block voltage (BVM) vs. sum of all cell voltages (CVM) including needed measurements
- Check of all cells overvoltage
- Check of all cells undervoltage
- Open load detection
- External NTC resistance measurement (2 channels at each RR)
- Balancing diagnosis via over- & undercurrent check (if balancing was activated at start of RR scheme)

The **Figure 15** shows the different tasks and the timing of the round robin in more detail.



**Figure 15 RR task timing diagram**

The following sections will describe the tasks in more detail:

### Internal temperature measurement

During this check, the internal temperature will be measured with the 13th ADC (10 bit mode), and the result will be compared to the configured threshold (INT\_OT\_THR, register **INT\_OT\_WARN\_CONF**). Furthermore, the result will be copied into the related **INT\_TEMP** register.

### Compensation calculation

During this phase the necessary compensation measurements for the compensation are performed and the compensation is calculated.

### ADC error check

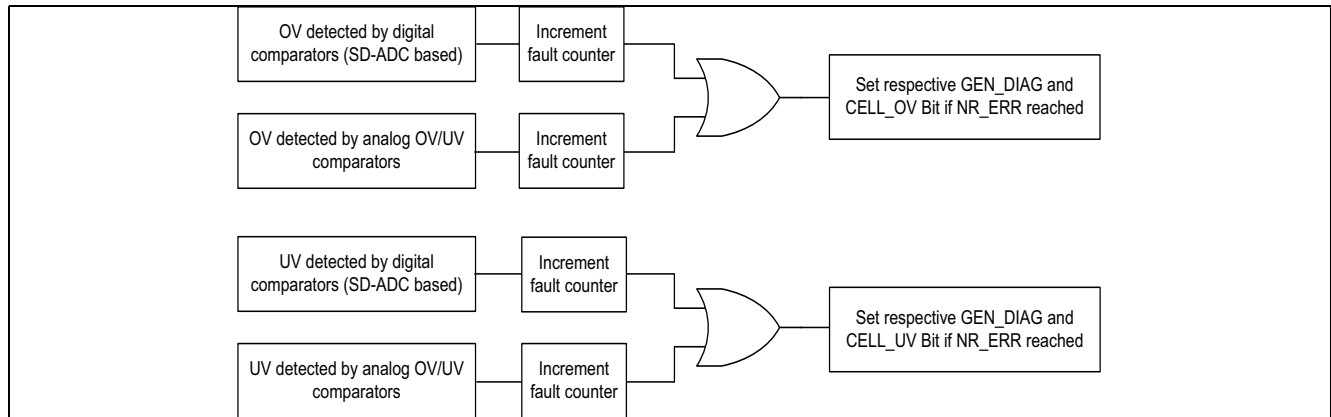
A cell voltage measurement will be performed for each cell. Furthermore a block voltage measurement will be performed with the 13th ADC simultaneously to the cell voltage measurement. Both results will be compared for a plausibility check. If the comparison fails, the fault counter for the ADC error will be incremented. After NR\_ERR (register **RR\_ERR\_CNT**) consecutively fails, the ADC\_ERR bit will be set in the **GEN\_DIAG** register. Please note: The results of the measurements are not stored in the CVM and BVM results register to avoid overriding valid and more precise (e.g. 16 bit measured) results.

### Cell overvoltage and undervoltage check

The results from above (measured as part of the ADC error check) will also be used to check for over- and undervoltage with a digital comparator. Simultaneously also the analog comparators (described in **Chapter 5.3**) will check the voltage from Gx - Ux for over- and undervoltage. If the voltage of any cell is above the programmed threshold on the **OL\_OV\_THR** register, identified either by the digital or the analog comparator, the fault counter will be incremented. Consecutive errors > NR\_ERR (register **RR\_ERR\_CNT**) will set the fault bit in the **GEN\_DIAG** register and the affected cell will be displayed in the corresponding **CELL\_OV**

## Housekeeping functions

register. The same applies for any detected undervoltage (measurement result lower than programmed threshold on **OL\_UV\_THR** register).



**Figure 16 OR function of over- & undervoltage detection check**

### Pin fine open load diagnosis

The open load detection check is also part of the round robin scheme, please see [Chapter 5.5.1](#) for more details. If the check fails, the fault counter for the individual open load diagnosis will be incremented. After NR\_ERR (register **RR\_ERR\_CNT**) consecutively fails, the respective open load error bit will be set in the **GEN\_DIAG** register.

### External resistance measurement via NTC

During this check, the external resistance will be measured with the 13th ADC (10 bit mode) and the result will be compared to the configured threshold (EXT\_OT\_THR, register **TEMP\_CONF**). Furthermore the result will be copied into the related **EXT\_TEMP\_0** – **EXT\_TEMP\_4** registers and the valid bit will be set to “1” after a new result is available.

### Balancing diagnosis via overcurrent and undercurrent check

The TLE9012AQU performs also a balancing overcurrent and undercurrent check as part of the round robin for each cell were the balancing function was active at the start of OV/UV check. Please see [Chapter 5.5](#) for more details. If the checks fails, the fault counter for the individual balancing diagnosis will be incremented. After NR\_ERR (register **RR\_ERR\_CNT**) consecutively fails, the respective balancing error bit will be set in the **GEN\_DIAG** register.

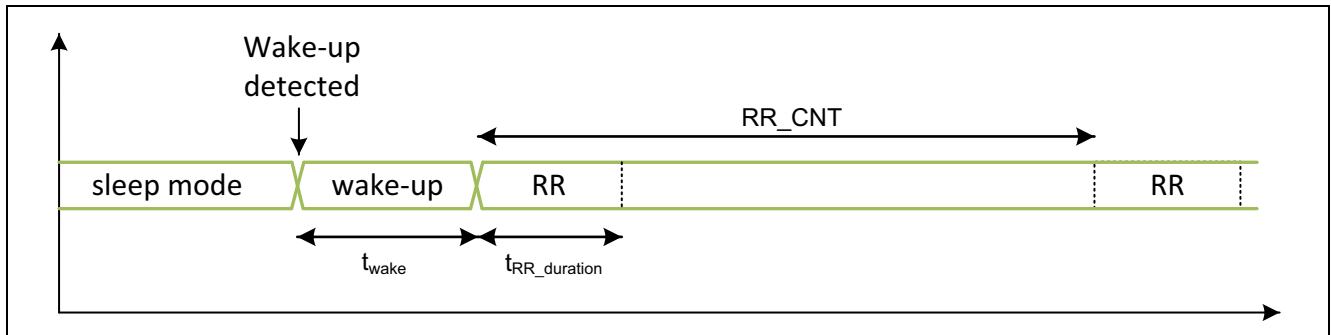
Please note: It is recommend to mask the fault counter for the balancing overcurrent diagnosis in the **RR\_CONFIG** register, so that a balancing diagnosis error gets triggered after the first detection. Reason is the potentially high current in case of an balancing overcurrent. If the fault counter is active (not masked) the individual balancing error counters will be reset as soon as balancing of the corresponding cell gets deactivated. But if balancing gets deactivated for all channels and an individual balancing error counter was already up-counted (but  $\geq$  NR\_ERR) the up-counted error counter value will be kept.

### 8.3.2 Round robin schedule (during normal operation)

The round robin schedule will be executed during normal operation. The task will be executed always directly after the wake-up procedure. [Figure 17](#) shows the RR timing and usual duration after wake-up. After the wake-up the RR is executed cyclically. RR\_CNT (register **RR\_CONFIG**) is available to define the wait time between the RR cycles. The **RR\_CONFIG** can be written by the external microcontroller. The RR\_CNT counter (register **RR\_CONFIG**) has to be between given limits to ensure that internal diagnostics are triggered in a

## Housekeeping functions

reasonable time frame. The RR\_CNT counter will be set back to the value RR\_CNT (register **RR\_CONFIG**) as soon as the RR started.

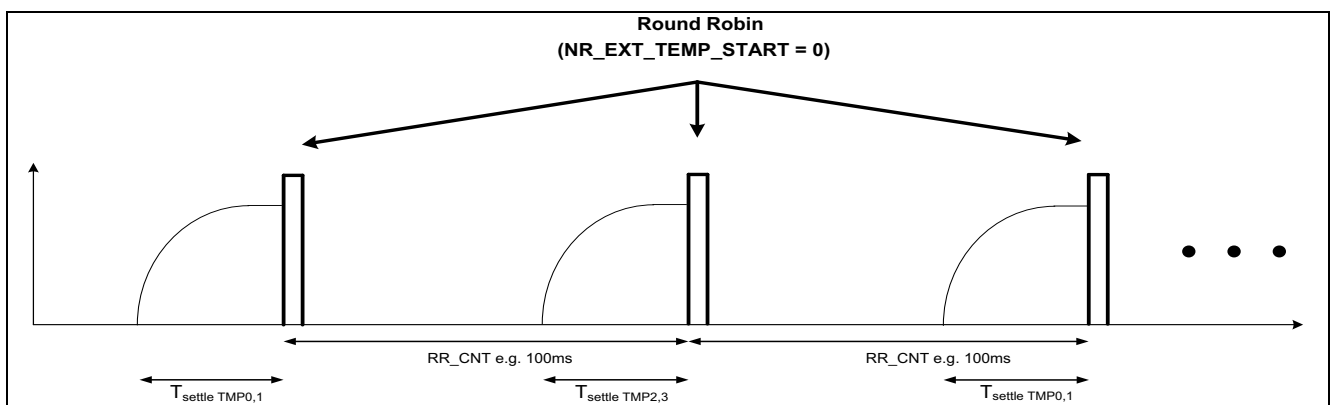


**Figure 17** RR wake-up timing

In order to allow a user configurable filter function before a fault in the **GEN\_DIAG** register is set, certain consecutive number of faults can be allowed by setting the threshold  $n_{\text{ERROR}}$  (bit-field: NR\_ERR, register **RR\_ERR\_CNT**). Each possible fault has a counter  $cnt_{\text{ERROR}_x}$  which is pre-configured to 0. Every time a fault is detected, the counter of the corresponding fault will be incremented. The corresponding fault will be set in the **GEN\_DIAG** register if the counter of that fault is  $> n_{\text{ERROR}}$  (bit-field: NR\_ERR). Furthermore if the fault is not masked out in the **FAULT\_MASK** register, the device will go into emergency mode (and trigger an EMM signal). If no fault is detected during a RR cycle, the corresponding counter will be set back to 0. Alternatively the corresponding counter will also be set back as soon as the corresponding fault bit in the **GEN\_DIAG** register is reset by the host controller.

The counters ( $cnt_{\text{ERROR}_x}$ ) will keep their status while going into sleep mode or coming out of it and will only be reset like described above in normal mode.

In order to reduce power consumption and since the external temperature measurement takes quite a long time, an additional counter  $cnt_{\text{ET}}$  is implemented. The counter is preset to  $n_{\text{ET}}$  (bit-field: NR\_EXT\_TEMP\_START). The counter is decremented with each RR. If the counter reaches zero, an external temperature measurement will be triggered for two channels and the counter will be set to  $n_{\text{ET}}$  again. The time to charge the NTC and its capacitor (optional) is called Tsettle. **Figure 18** shows the round robin timing including Tsettle for the external temperature measurement.

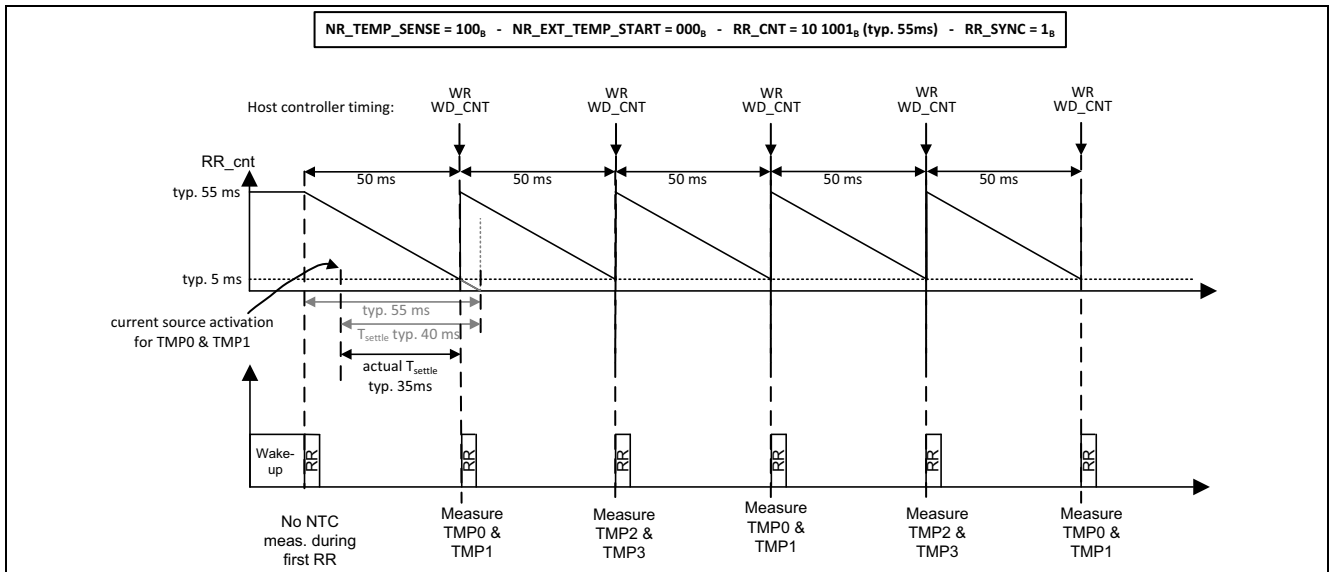


**Figure 18** RR timing (assuming 4 active external temperature sensors)

In order to re-synchronize the RR tasks of all the devices in the system and with other sub-tasks like cell voltage measurement, a RR\_SYNC bit-field (register **RR\_CONFIG**) is available. If this bit-field is set, the round robin scheme will be executed every time the watchdog is reloaded with a write command into the WD\_CNT bit-field; in addition, the internal RR counter will also be set back to RR\_CNT. It is recommended - especially if the

## Housekeeping functions

NTC resistance measurement is used - to use that function to synchronize all temperature measurements. The following **Figure 19** shows how to make sure that the NTCs are charged up correctly when using this function.



**Figure 19** RR\_SYNC in conjunction with  $T_{\text{settle}}$  (assuming 4 active external NTC sensor channels)

The following diagram shows an extract of the typical RR flow to give a better understanding of the fault checking and EMM generation:

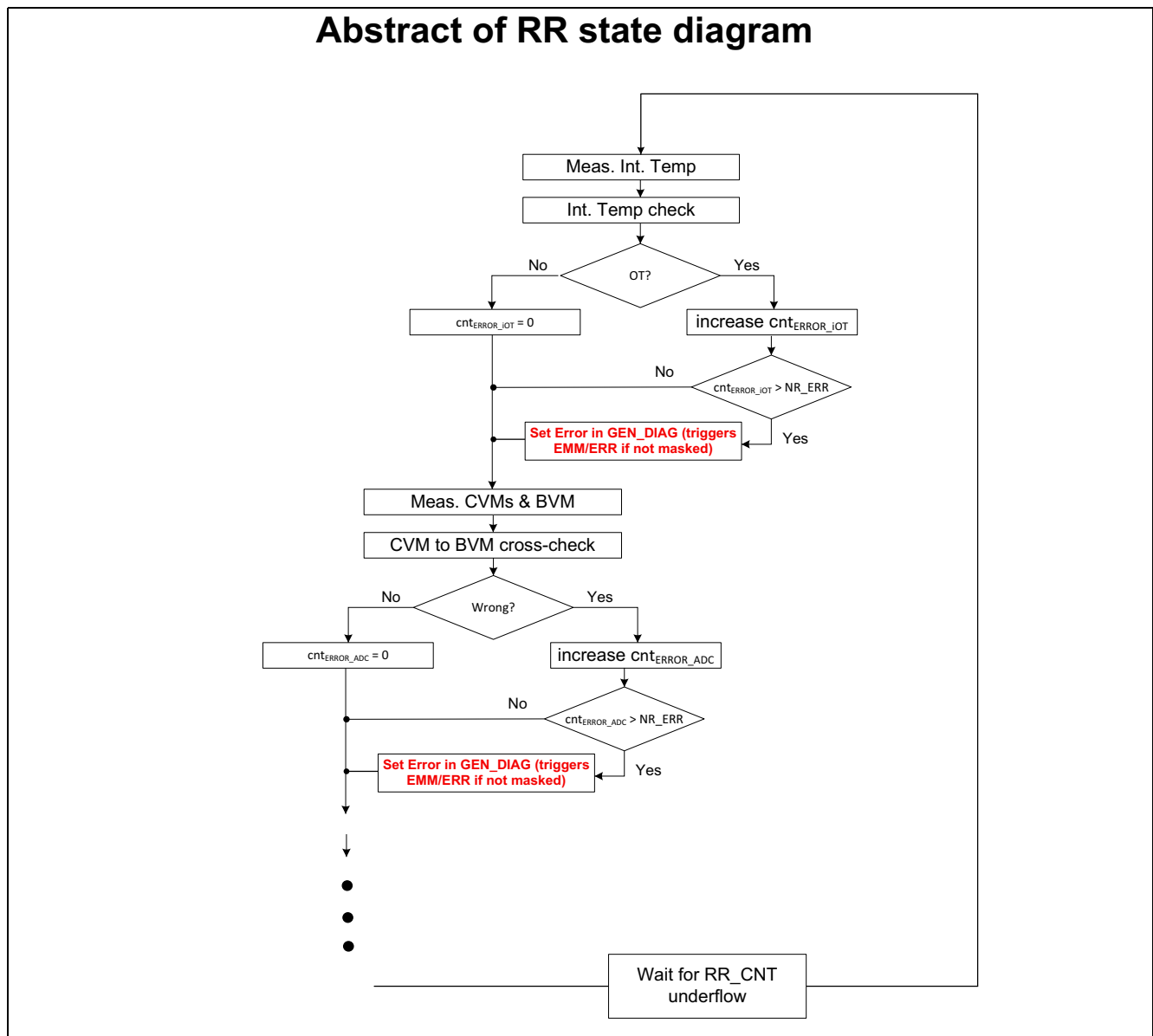


Figure 20 Extract of RR flow to show **GEN\_DIAG** setting and EMM generation

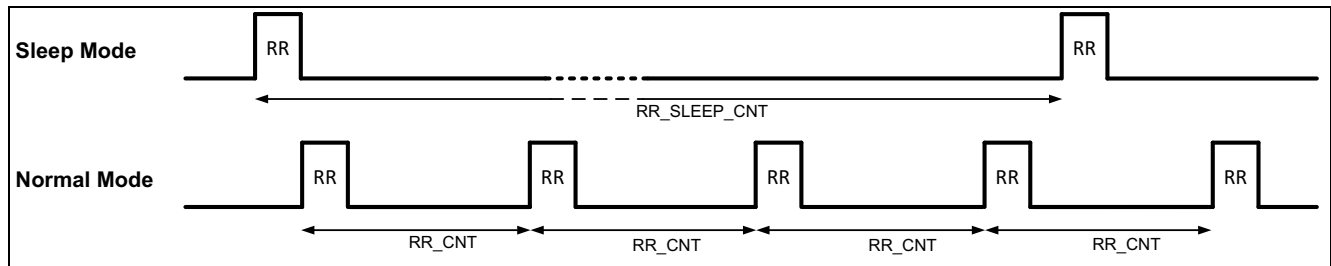
### 8.3.3 Round robin schedule (during sleep mode)

During sleep mode no internal or external checks are performed but the device includes a feature to wake-up periodically from sleep mode to perform one RR scheme. After the RR scheme is performed and no error in the **GEN\_DIAG** is set the device will go back to sleep mode immediately. The function is off by default and can be switched on by setting the RR\_SLEEP\_CNT bit-field (register **RR\_ERR\_CNT**). This bit-field defines the time between two wake-up cycles. If a wake-up signal arrives during the periodical wake-up in sleep mode, the part will go immediately to into normal mode.

**Figure 21** shows the typical timing in sleep mode. Please note: After the RR scheme is performed and an error in the **GEN\_DIAG** is set the device will either send an EMM signal and will go back to sleep mode after the EMM was transmitted or set the ERR pin signal active and go back to sleep mode after  $t_{WD\_max}$

Please note as the RR is the first RR after the wake up no external temperature measurement is performed see Figure 24.

## Housekeeping functions



**Figure 21 Round robin timing**

### 8.3.4 Prioritization of round robin and manual measurement triggering

The manual triggering of a measurement and the measurements which happen cyclically via the round robin scheduler need to be aligned/prioritized since they are partly using the same physical units.

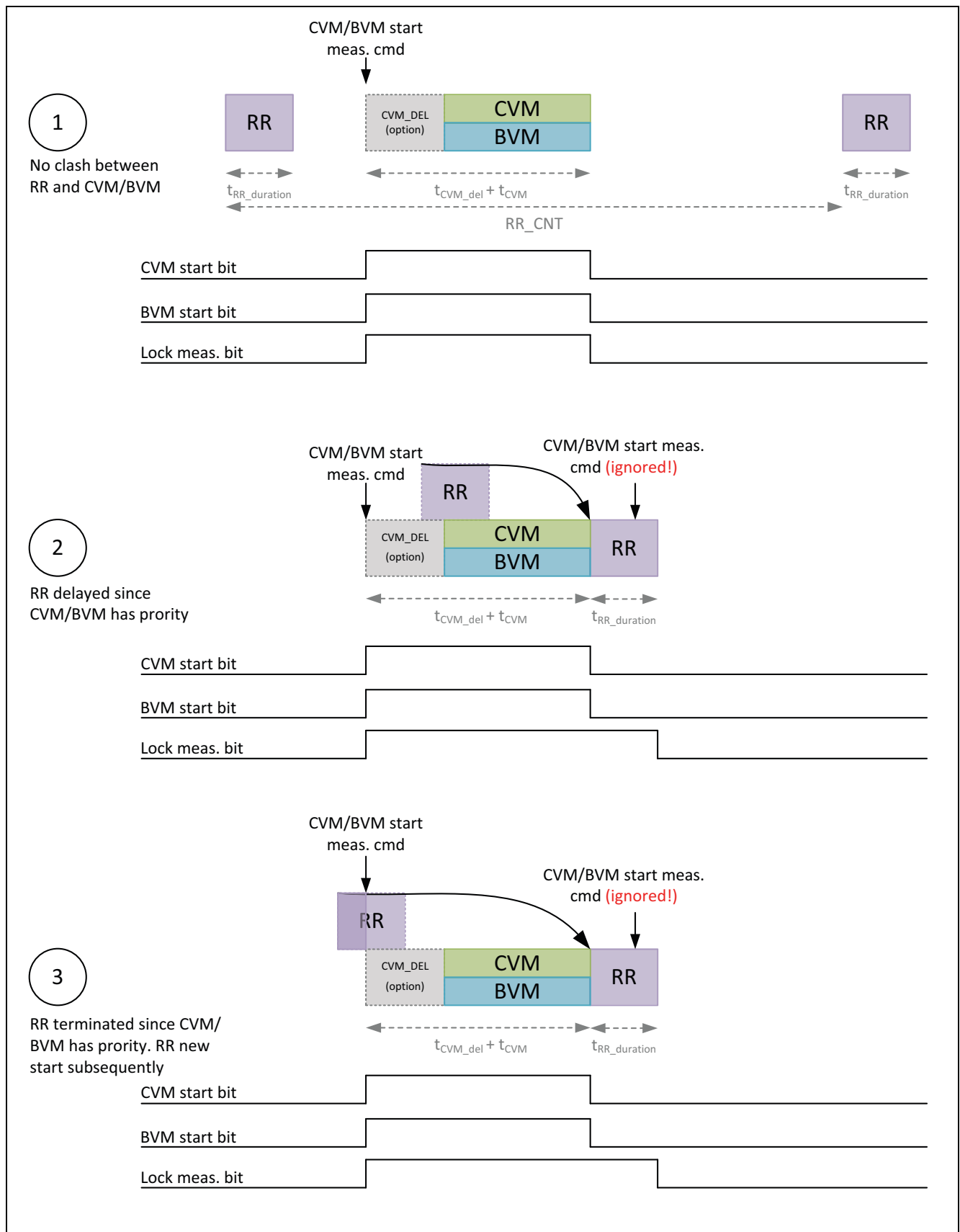
The timing of manually triggered measurements can be critical, especially for the CVM and BVM measurement. The better the measurements are synchronized globally within a battery system, the more accurate are the SoC/SoH models in the microcontroller. Furthermore the synchronization of the CVM and BVM within a device guarantees an accurate measurement comparison. Therefore the manually triggered measurements of CVM and BVM have priority over the RR scheduler and start immediately (see also [Chapter 5.2](#), [Chapter 6.1](#) and [Chapter 8.3](#)). [Figure 22](#) illustrates the various scenarios for the CVM and BVM measurements and how these are processed. Please note that the RR scheduler duration  $t_{RR\_duration}$  depends on the chosen CVM\_DEL configuration.

The manually triggered AVM measurement and the cyclically triggered RR work with the same principle as the CVM/BVM. So the AVM has priority over the RR. The only difference is that the AVM does not include a CVM\_DEL. The AVM measurements are happening sequentially in the same order as defined in the [AVM\\_CONFIG](#) register from LSB to MSB. If BVM and AVM started at the same time only BVM is executed.

As shown in the figures, the lock measurement bit-field (LOCK\_MEAS, register [GEN\\_DIAG](#)) is introduced to prevent multiple triggers by the microcontroller while a measurement is happening and to prevent overriding the RR continuously.

If the temperature measurement within the round robin is used it is recommended to use the RR\_SYNC feature to trigger the round robin manually (see [Chapter 8.3.2](#)). Goal is to avoid a clash of the round robin and the CVM/BVM/AVM which would delay the round robin execution. Reason is that the current sources which power the NTCs are deactivated in case the round robin gets delayed due to a clash with CVM/BVM/AVM.

## Housekeeping functions



**Figure 22** Timing and priority of CVM/BVM and RR measurements

## Housekeeping functions

### 8.3.5 Electrical characteristics

**Table 16 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter  | Symbol                 | Values |              |      | Unit | Note or Test Condition                            | Number |
|--|------------------------|--------|--------------|------|------|---|--------|
|  |                        | Min.   | Typ.         | Max. |      |   |        |
| OV/UV detection                                    |                        |        |              |      |      |   |        |
| OV/UV threshold resolution                         | $V_{OVUV\_thr\_res}$   | –      | $FSR/2^{10}$ | –    | V    | <sup>1)</sup> 10 bit, FSR =5 V                    |        |
| OV/UV threshold range                              | $V_{OVUV\_thr\_range}$ | 0      | –            | 5    | V    | <sup>1)</sup> Cell 0 to Cell 11                   |        |
| Round robin counter                                |                        |        |              |      |      |   |        |
| RR minimum interval                                | $t_{RR\_min}$          | 6.7    | 7.1          | 7.4  | ms   | <sup>1)</sup>                                     |        |
| RR maximum interval                                | $t_{RR\_max}$          | 149    | 155.7        | 163  | ms   | <sup>1)</sup> 7 bit counter                       |        |
| RR interval step                                   | $t_{RR\_LSB}$          | 1.12   | 1.17         | 1.22 | ms   | <sup>1)</sup>                                     |        |
| RR sleep maximum interval                          | $t_{RR\_sleep\_max}$   | 155    | 170.5        | 190  | h    | <sup>1)</sup> 10 bit counter                      |        |
| RR sleep interval step                             | $t_{RR\_sleep\_LSB}$   | 9      | 10           | 11.2 | min  | <sup>1)</sup>                                     |        |
| RR scheme duration                                 | $t_{RR\_duration}$     | –      | 1            | 2    | ms   | <sup>1)</sup> default setting for PBOFF & CVM_DEL |        |
| CRC check cyclic interval                          | $t_{CRC\_check}$       | 47     | 49.15        | 52   | ms   | <sup>1)</sup>                                     |        |
| Error counter                                      | $n_{ERROR}$            | 0      | –            | 7    | –    | <sup>1)</sup> 3 bit counter                       |        |
| current source activation for NTC before RR starts | $T_{settle}$           | 38.4   | 40           | 41.6 | ms   | <sup>1)</sup>                                     |        |

1) Not subject to production test, specified by design.

### 8.4 Emergency mode (EMM) and ERR pin function

Two functions are implemented in TLE9012AQU to signal that an fault occurred:

- Emergency mode (EMM)
- ERR pin function

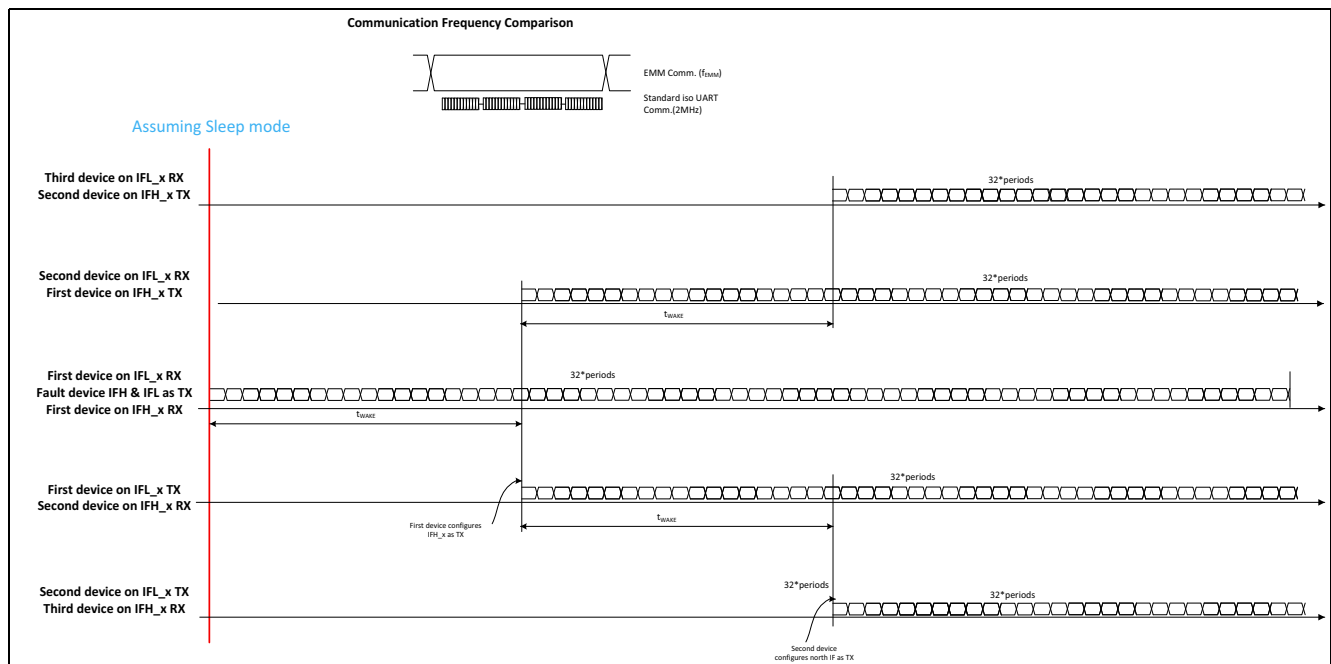
#### 8.4.1 Emergency mode (EMM)

In case of an detected error, the TLE9012AQU can go into emergency mode (EMM). In this mode, all communication interfaces (IFH, IFL) will generate an emergency signal that can be detected by the transceiver device so that the transceiver can enable its ERRQ pin to forward the error detection to the host controller. The following chapters describe this procedure in more detail.

If the chain is in sleep mode, the devices contiguous to the affected one will first recognize the EMM signal as wake-up signal and will trigger a standard wake-up procedure. After the device is awake, the EMM signal will still be present. Therefore, if  $n_{EMM\_dect\_wake-up}$  are detected after wake-up, it will interpret it as an EMM signal (no standard wake-up anymore) and trigger EMM transmitting mode (by extending the signal to  $n_{EMM}$ ).

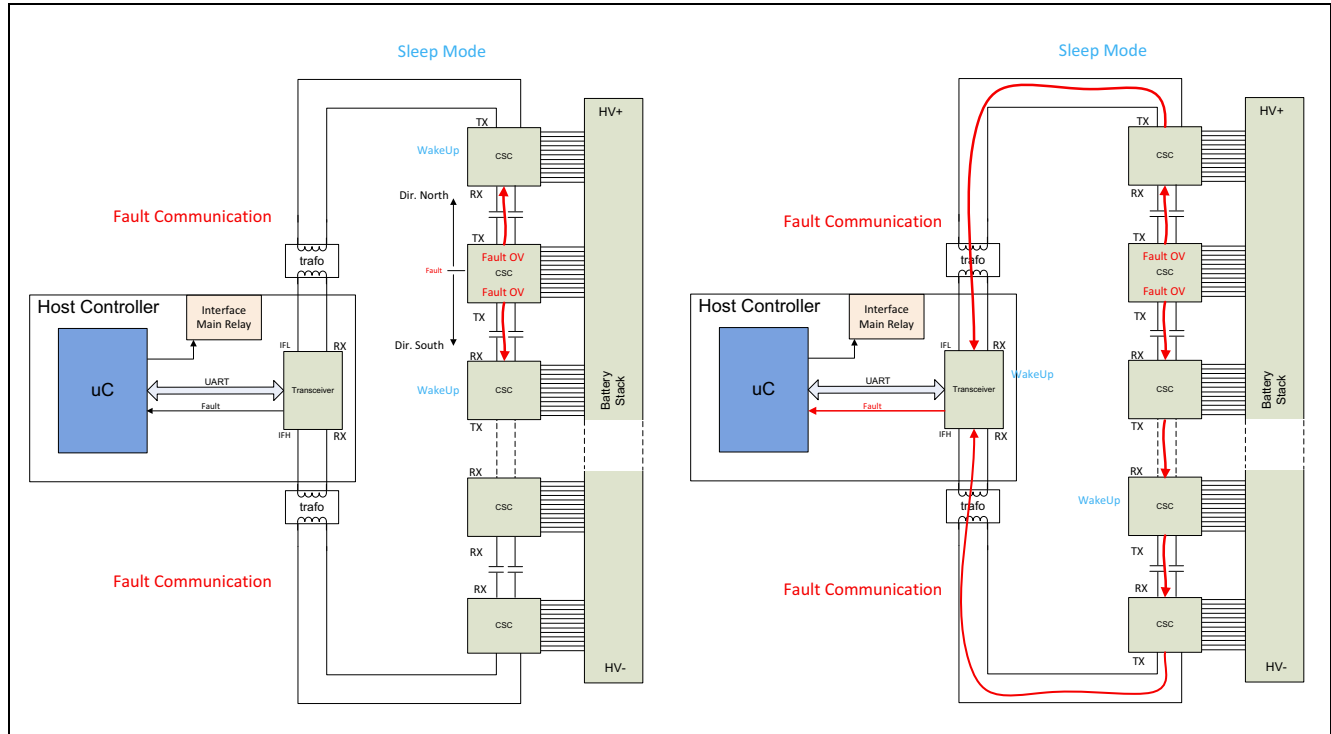


## Housekeeping functions



**Figure 23** EMM signals during sleep mode

The EMM signal will arrive at the transceiver from both sides (top and bottom) in case of a chain being in sleep mode. After the EMM signal is transmitted, the devices will go back into sleep mode.



**Figure 24** EMM during sleep mode

If the chain is in normal operation (i.e. communicating, measuring, etc.), a communication mode (MoT or MoB) is already defined. The affected device will also start transmitting the EMM signal. However, since the chain is already configured for either MoT or MoB communication, the contiguous devices will show either a TX interface or a RX interface. If the contiguous device shows a TX interface, the EMM will not be forwarded.

Housekeeping functions

Therefore, the EMM signal will follow the path that shows the RX interface back to the microcontroller. The following figure shows an EMM communication in case of MoB/MoT configuration:

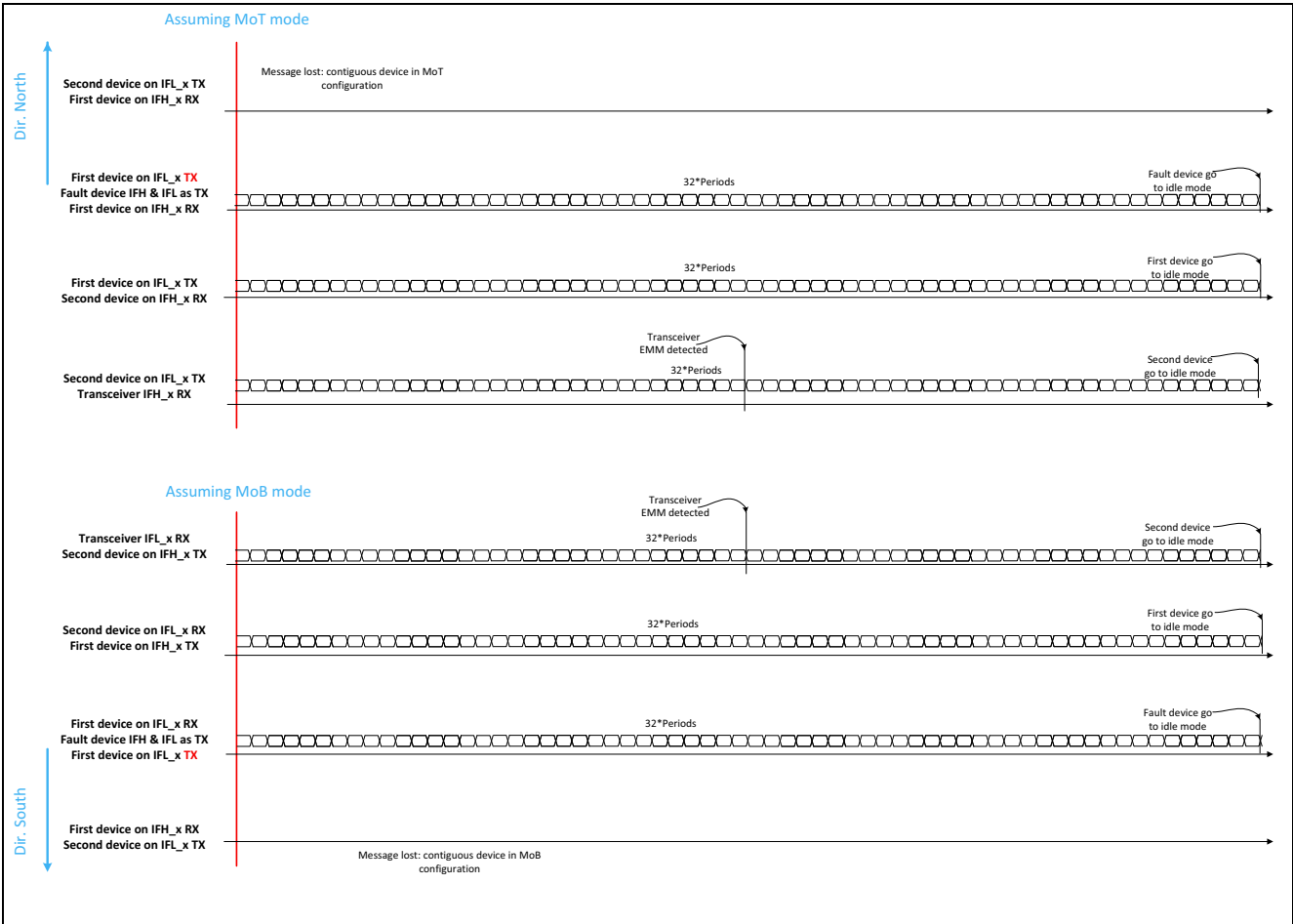
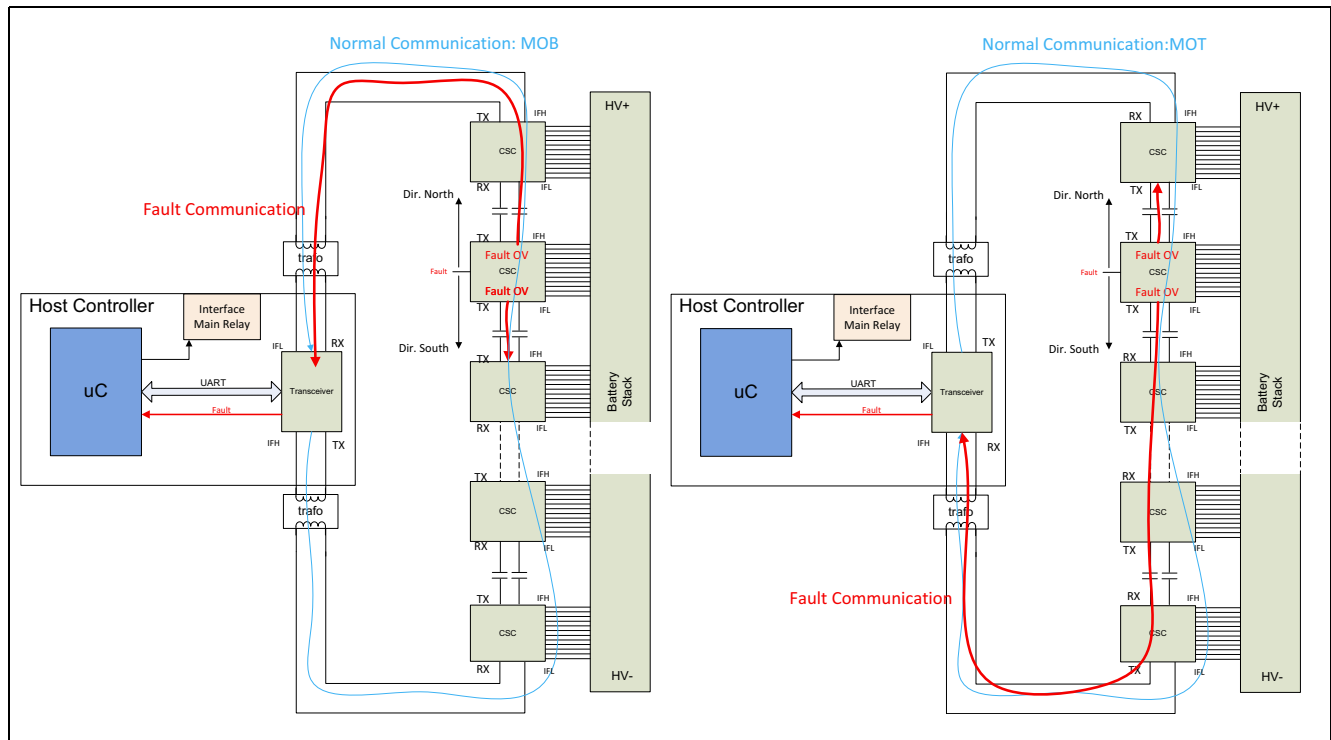


Figure 25 EMM signals during normal operation

## Housekeeping functions



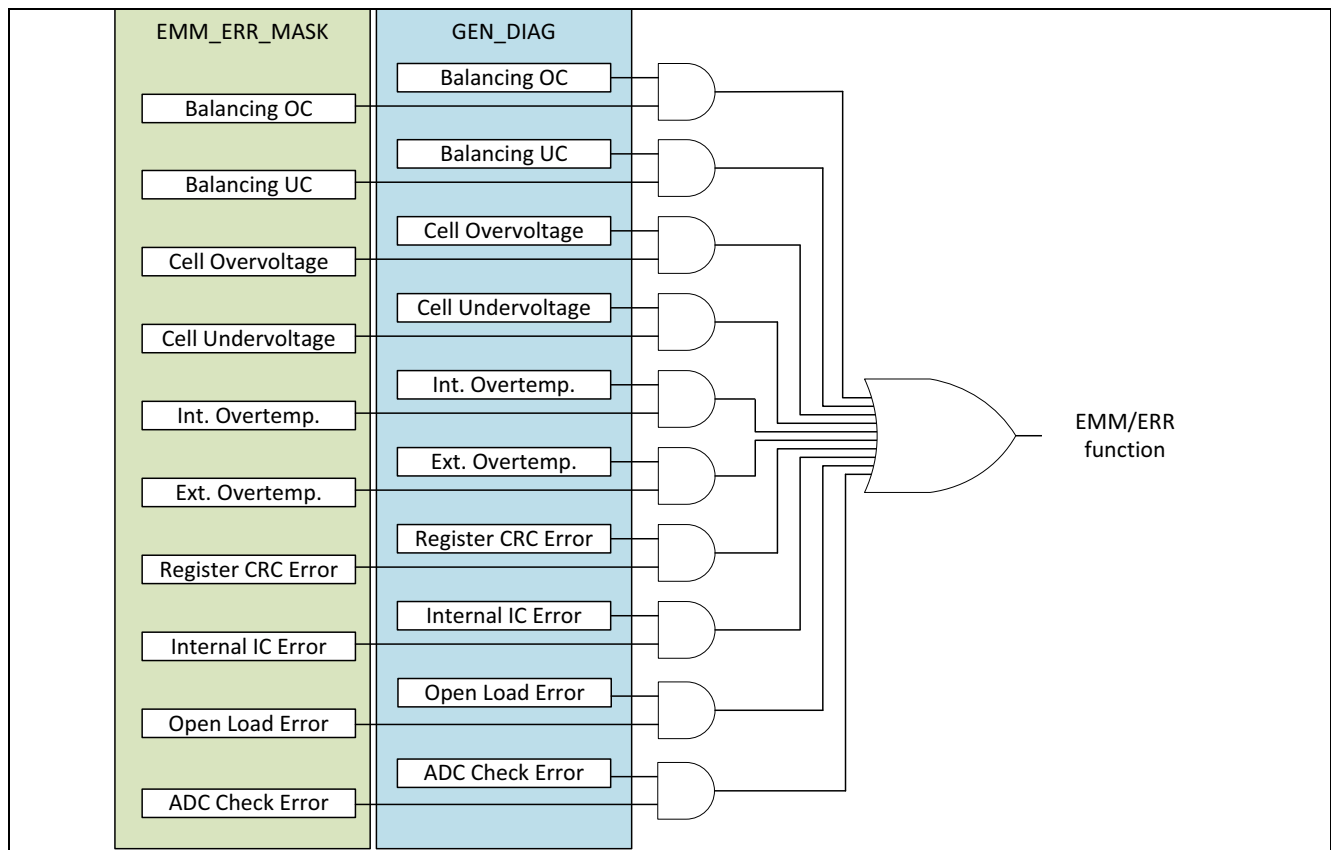
**Figure 26 EMM during MoB/MoT configuration**

The following possible faults can trigger the EMM mode:

- Overvoltage in 1 or more cells detected
- Undervoltage in 1 or more cells detected
- External temperature fault in 1 or more channels detected
- Open load in any Ux/Gx detected
- Overcurrent balancing error detected
- Undercurrent balancing error detected
- ADC cross-check error
- Internal temperature fault detected
- Register CRC check fault detected
- Internal IC error

All the faults above can trigger the EMM, however there is the possibility to mask any of them out by using the **FAULT\_MASK** register. The faults still show up in the **GEN\_DIAG** register and are therefore accessible even if they are masked out for an EMM trigger. **Figure 27** shows how the masking and EMM triggering works.

## Housekeeping functions



**Figure 27 Masking function for EMM and ERR**

After the EMM signal is transmitted, the part will go into sleep mode or back to normal mode again depending on which mode it was in before the EMM signal was transmitted.

The fault information in the **GEN\_DIAG** register will not be lost by going into sleep mode. Only if the battery is disconnection, the information will be lost. Please note that the **GEN\_DIAG** fault bits are latching and can only be reset by the microcontroller or if U12P is not supplied.

During the next round robin cycle after a fault was detected, the device will go again into EMM if the microcontroller did not reset the fault bit in the **GEN\_DIAG** register or masked the EMM via the **FAULT\_MASK** register in the meantime.

Please note: In case the internal IC error check (bit-field: INT\_IC\_ERR) routine detects an error during wake-up the LOCK\_MEAS bit remains set and there is no round robin execution hence there is no EMM triggering happening at all.

### 8.4.2 ERR pin function

Additionally to the EMM mode, the TLE9012AQU has an ERR pin available. This pin is intended to be used in non-transceiver based setups (e.g. for only a few number of cells).

- ERR function as counterpart to the EMM signal with a similar functionality

Please note the pin levels are either GND (low) or VS (high).

#### ERR function

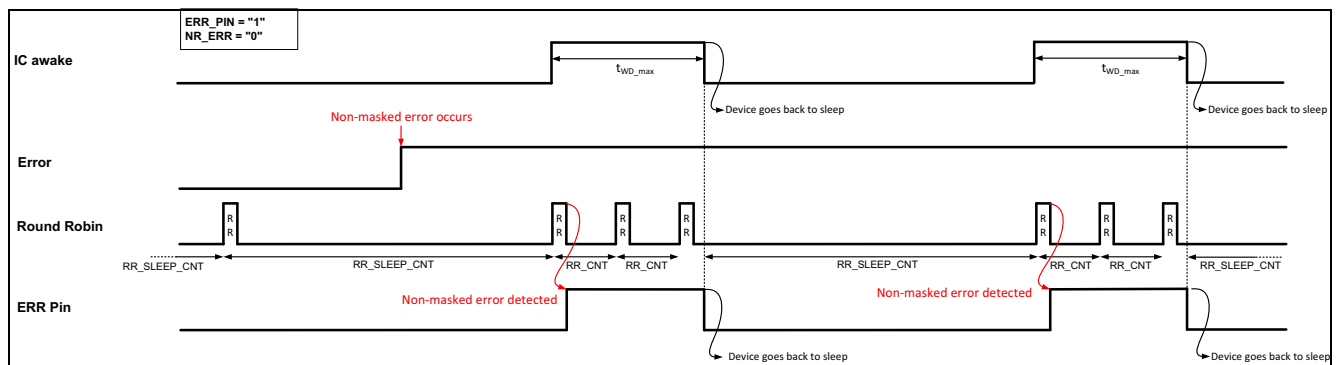
The ERR pin function can be enabled by setting the ERR\_PIN bit-field. Enabling the ERR pin function disables the EMM signal via iso UART. After detecting a fault that leads to an emergency signal (see also **Figure 27**), the pin will go high. The following possible faults can trigger the ERR pin function (same as in EMM mode):

## Housekeeping functions

- Overvoltage in 1 or more cells detected
- Undervoltage in 1 or more cells detected
- External temperature fault in 1 or more channels detected
- Open load in any Ux/Gx detected
- Overcurrent balancing error detected
- Undercurrent balancing error detected
- ADC cross-check error
- Internal temperature fault detected
- Register CRC check fault detected
- Internal IC error

All the faults above can trigger the ERR pin function, there is the possibility to mask any of them out by using the **FAULT\_MASK** register similar to the EMM signal. The faults still show up in the **GEN\_DIAG** register and are therefore accessible even if they are masked out for an ERR/EMM trigger. **Figure 27** shows how the masking and ERR/EMM triggering works.

Once the ERR pin function has been triggered, the pin will stay high until all the faults above are cleared by clearing the faults in the **GEN\_DIAG** register actively by the microcontroller. The microcontroller can stop this behavior by masking out the detected fault in the **FAULT\_MASK** register. During sleep mode the ERR pin is set to low. Please note that the error information in the **GEN\_DIAG** register will still be available after sleep mode, hence if the device exits sleep mode, the ERR pin will go high again if the non-masked error is still existing. Please see **Figure 28** for more details.



**Figure 28** ERR pin function

## 8.4.3 Electrical characteristics

**Table 17** Electrical characteristics

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter            | Symbol           | Values |      |      | Unit | Note or Test Condition | Number |
|----------------------|------------------|--------|------|------|------|------------------------|--------|
|                      |                  | Min.   | Typ. | Max. |      |                        |        |
| Emergency mode EMM   |                  |        |      |      |      |                        |        |
| EMM signal frequency | $f_{\text{EMM}}$ | 48     | 50   | 52   | kHz  | 1)                     |        |

**Housekeeping functions**

**Table 17 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter   | Symbol                          | Values |      |      | Unit    | Note or Test Condition  | Number |
|---|---------------------------------|--------|------|------|---------|---|--------|
|   |                                 | Min.   | Typ. | Max. |         |   |        |
| Number of periods to detect EMM signal - straight after wake-up | $n_{\text{EMM\_dect\_wake-up}}$ | 4      | –    | 4    | periods | <sup>1)</sup> number of periods; valid while IC is forwarding wake-up signal                |        |
| Number of periods to detect EMM signal - idle mode              | $n_{\text{EMM\_dect}}$          | 16     | –    | 16   | periods | <sup>1)</sup> number of periods; valid while IC is in idle mode and not enumerated (ID = 0) |        |
| Length in periods of EMM signal                                 | $n_{\text{EMM}}$                | 32     | –    | 32   | periods | <sup>1)</sup>   |        |

**ERR pin function**

|                                      |                     |                 |   |          |    |  |  |
|--------------------------------------|---------------------|-----------------|---|----------|----|--|--|
| Functional range of ERR pin function | $V_{\text{ERR}}$    | 4.75            | – | $V_{VS}$ | V  | $V_{VS} \leq 20 \text{ V}$   |  |
| Source current                       | $I_{\text{SOURCE}}$ | –               | – | 1        | mA | current capability of pin additionally to R_pull-down (= 100 kΩ) current |  |
| Activated output voltage             | $V_{\text{ERR}}$    | $V_{VS} - 0.25$ | – | –        | V  | current capability 1 mA + current for R_pulldown = 100 kΩ                |  |

1) Not subject to production test, specified by design.

## **9 General Purpose Input / Output (GPIO)**

The TLE9012AQU has 4 GPIO pins (GPIO0/1, PWM0/1) which provide a versatile input/output interface. The GPIO0/1 pins have a double function and can be used as UART interface; if the UART is used, the GPIO functionality is deactivated. If the GPIO0/1 pins are not used as UART interface (wake-up received via iso UART interface), they can be configured as a digital input or a digital output. The setting as well as the monitoring of the data can be handled in the GPIO register.

Furthermore, the PWM0/1 can either be configured as standard GPIO (digital in/out) interface or as PWM output. The configuration of PWM0/1 must also be performed in the **GPIO** register. The PWM functionality can be configured via the **GPIO\_PWM** register.

For the electrical characteristics of the GPIO please see the electrical characteristics of UART in **Table 18** since UART and GPIO is the same physical pin.

## 10 Communication interfaces

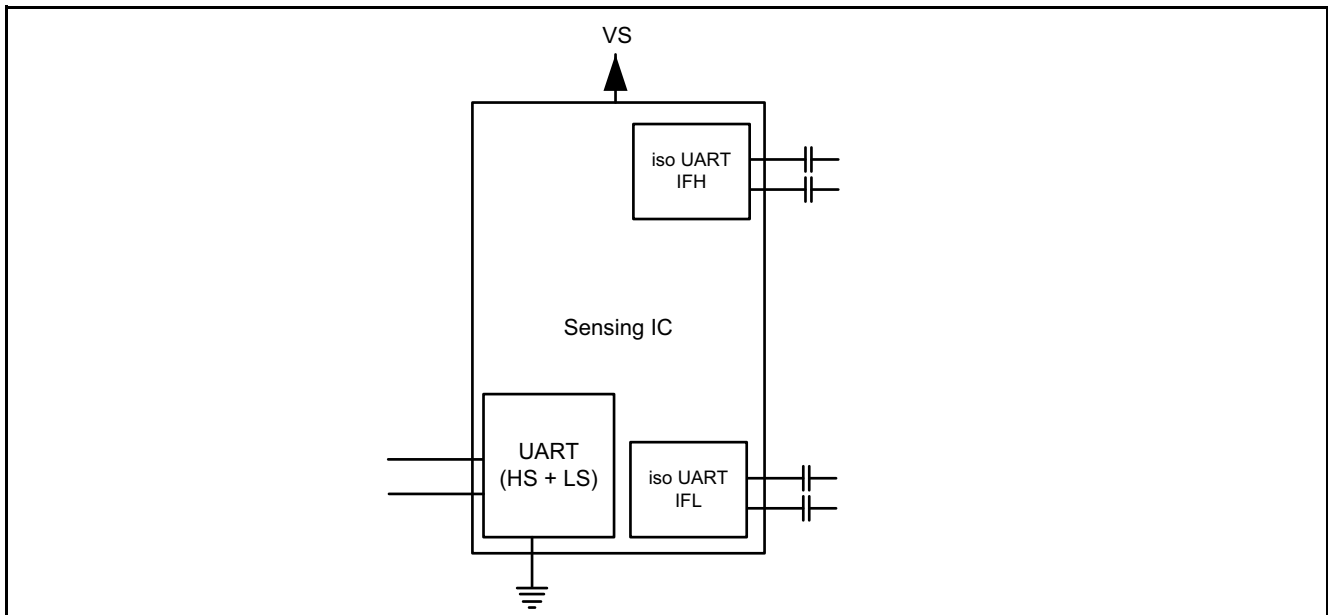
### 10.1 Physical layer

The TLE9012AQU supports two types of physical layers: UART-based and iso UART-based. Both are point-to-point communication protocols and can be used to communicate between the microcontroller in the system and the different slaves.

Each TLE9012AQU contains four different units:

- iso UART IFH
- iso UART IFL
- UART HS
- UART LS

In the following chapters each of these units will be described.



**Figure 29** Typical communication block for TLE9012AQU

#### 10.1.1 UART communication unit

The UART communication is logic-voltage-based. The voltage level for this communication is defined by the voltage between VIO to GND.

Due to the necessary GND connection the UART interface cannot be used for interblock communication if the devices are stacked (not galvanically isolated). Therefore the UART unit is intended to be used in systems where a few number of cells need to be controlled (no sensing IC stacking) as direct sensing IC to microcontroller communication interface. UART supports a communication speed of  $BR_{GPIO}$

UART communication needs only 1 pin on the TLE9012AQU side since it has already integrated a logic controller which fulfills the function of switching between Tx and Rx mode. In a typical UART connection can be seen with 2 pins on the microcontroller side.

The UART LS unit is connected to the GPIO0 pin, and the UART HS unit is connected to the GPIO1 pin. These pins have a double function. During sleep mode, these pins will stay in low power RX mode. If a wake-up signal is detected through the GPIOx pins and the voltage at VIO is higher than the  $V_{VIO\_th\_UV\_rise}$ , the TLE9012AQU will



## Communication interfaces

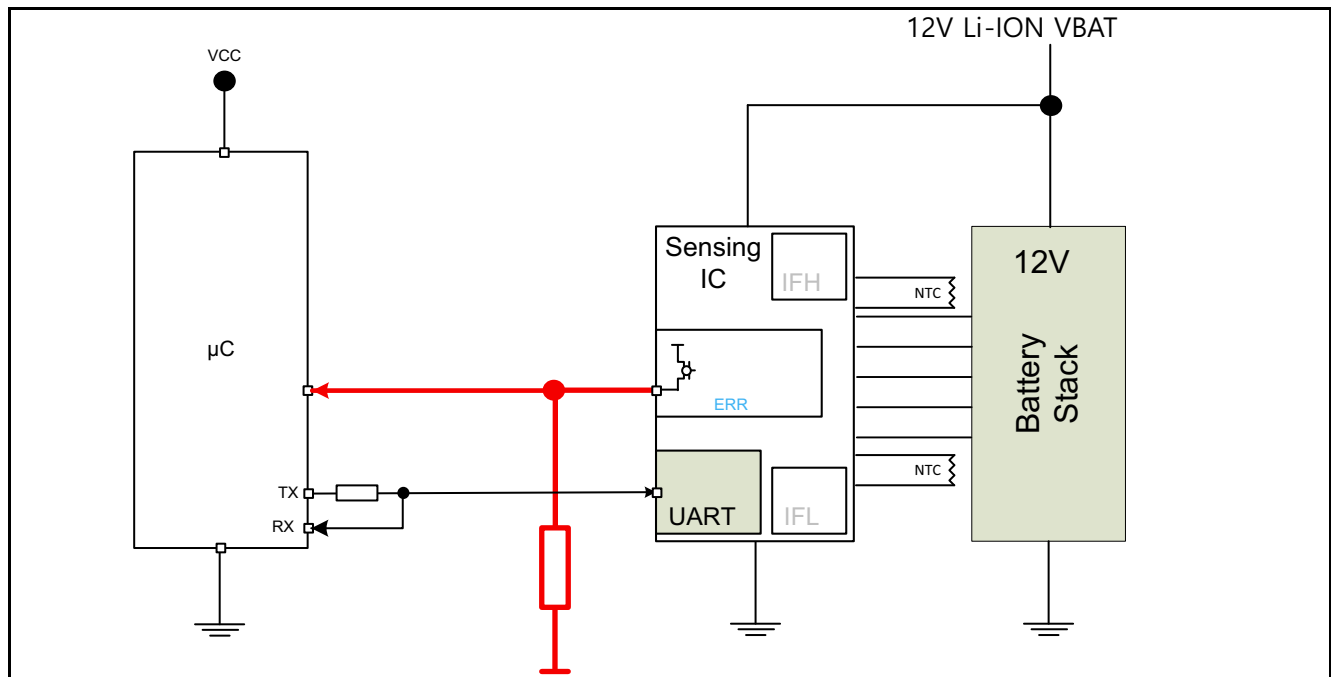
configure the GPIO pin as UART. Furthermore it starts a wake-up procedure (as shown in [Chapter 8.2.3](#)) configured as MoB (see also [Chapter 10.2.1](#)) if the wake-up signal came through GPIO0 (UART LS) or MoT if the wake-up signal came through GPIO1 (UART HS). The GPIOx function will be disabled until the next wake-up cycle. On the other side, if the wake-up signal is detected through an iso UART pin, GPIOx will remain as standard IO and the UART function will be disabled until the next wake-up cycle.

If a wake-up signal is detected at the UART LS, the wake-up signal will be generated at the iso UART IFLH interface as soon as the device enters the idle mode. If a wake-up signal is detected at the UART HS, the wake-up signal will be generated at iso UART IFL interface as soon as the device enters the idle mode.

Please note: In case of communication via UART the logic level of the UART pin in default state shall be static "1".

The only difference between UART and iso UART communication is the physical layer. On higher levels (OSI model), UART and iso UART are equal.

In low voltage systems the ERR pin function is recommended for fault communication to the microcontroller. [Figure 30](#) shows a typical low voltage application including the ERR pin functionality.



**Figure 30** Typical 12 V application including ERR function

### 10.1.2 Communication Bus (iso UART) unit

The iso UART is an Infineon-proprietary point-to-point communication bus with a dedicated protocol. Every TLE9012AQU node, except the first and the last node in the chain, is connected to two neighboring TLE9012AQU devices via two physical links: high side interface (IFH) and low side interface (IFL).

The iso UART is based on differential bus lines. Both the high and low side interfaces are able to drive the differential lines (TX mode), and both have a differential receiver circuit (RX mode). The bus timing protocol determines which of the interface modules is allowed to drive the bus lines.

The iso UART physical layer is a  $\pm V_{DDC}$  edge detection based interface suitable for capacitive coupling as well as inductive coupling. This interface can offer the required galvanic isolation as well as the robustness to guarantee error free communication between the different CSCs in the battery system.

The iso UART physical layer will forward all messages (except if ID is #0 or the device is in sleep mode) coming in to the opposite side; i.e. if a device was woken up through the IFL, any message coming from the IFL will be forwarded through to the IFH. Also the message will be analyzed by the internal logic. Once the message CRC

## **Communication interfaces**

has been checked, the IC compares the NODE\_ID with the message ID and processes the message if the IDs are matching.

The iso UART communication physical layer supports wake-up and EMM communication as described in [Chapter 8](#).

The TLE9012AQU can also support a mixed system where the first interface is UART and the rest are iso UART. In this mode, the first IC needs to be woken-up by UART (see [Chapter 10.2](#)).

### 10.1.3 Electrical characteristics

**Table 18 Electrical characteristics**

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter                                 | Symbol                          | Values                     |      |                            | Unit     | Note or Test Condition   | Number |
|---|---------------------------------|----------------------------|------|----------------------------|----------|--|--------|
|   |                                 | Min.                       | Typ. | Max.                       |          |  |        |
| GPIO physical layer                       |                                 |                            |      |                            |          |  |        |
| GPIO input threshold voltage LOW          | $V_{\text{GPIO\_th\_LOW}}$      | –                          | –    | $V_{\text{VIO}} \cdot 0.3$ | V        | –  |        |
| GPIO input threshold voltage HIGH         | $V_{\text{GPIO\_th\_HIGH}}$     | $V_{\text{VIO}} \cdot 0.7$ | –    | –                          | V        | –  |        |
| GPIO output voltage LOW                   | $V_{\text{GPIO\_LOW}}$          | 0                          | –    | 0.45                       | V        | $I_{\text{GPIO}} \leq 5 \text{ mA}$                            |        |
| GPIO output voltage HIGH                  | $V_{\text{GPIO\_HIGH}}$         | $V_{\text{VIO}} - 0.45$    | –    | $V_{\text{VIO}}$           | V        | $I_{\text{GPIO}} \geq -5 \text{ mA}$                           |        |
| UART to iso UART propagation delay        | $t_{\text{UART\_isoUART\_del}}$ | –                          | 25   | 100                        | ns       | propagation delay from UART to iso UART                        |        |
| GPIO <sub>n</sub> output current          | $I_{\text{GPIO}_n}$             | -5                         | –    | 5                          | mA       | current capability of GPIO output; $0 \leq n \leq 1$           |        |
| External capacitance on GPIO <sub>n</sub> | $C_{\text{GPIO}_n}$             | –                          | –    | 30                         | pF       | <sup>1)</sup> $0 \leq n \leq 1$                                |        |
| GPIO bitrate                              | $BR_{\text{GPIO}}$              | 1.45                       | 2    | 2.1                        | Mbit/s   | –  |        |
| iso UART physical layer                   |                                 |                            |      |                            |          |  |        |
| iso UART current threshold LOW            | $I_{\text{isoUART\_th\_LOW}}$   | -6.75                      | -4.5 | -2.25                      | mA       | $(I_{\text{IFX\_H}} - I_{\text{IFX\_L}}) / 2$                  |        |
| iso UART current threshold HIGH           | $I_{\text{isoUART\_th\_HIGH}}$  | 2.25                       | 4.5  | 6.75                       | mA       | $(I_{\text{IFX\_H}} - I_{\text{IFX\_L}}) / 2$                  |        |
| Transceiver $R_{\text{ON}}$ @100 mA       | $R_{\text{ON}}$                 | –                          | 22   | –                          | $\Omega$ | –  |        |
| iso UART propagation delay                | $t_{\text{isoUART\_prop\_del}}$ | –                          | 25   | 100                        | ns       | <sup>2)</sup> propagation delay from IFH to IFL and IFL to IFH |        |
| iso UART bitrate                          | $BR_{\text{isoUART}}$           | 1.45                       | 2    | 2.1                        | Mbit/s   | –  |        |
| External series capacitor value           | $C_{\text{SER}}$                | 0.95                       | 1    | 1.05                       | nF       | <sup>1)3)</sup>  |        |
| External series resistor value            | $R_{\text{SER}}$                | 37.05                      | 39   | 40.95                      | $\Omega$ | <sup>1)3)</sup>  |        |

1) Not subject to production test, specified by design.

2) Tested with our standard external circuit ( $C_{\text{SER}}$ ,  $R_{\text{SER}}$ )

3) External RC network needs to be adjusted depending on the application constraints (i.e. cable length)

## Communication interfaces

### 10.2 Bus topology

The TLE9012AQU offers the possibility to work in different configurations:

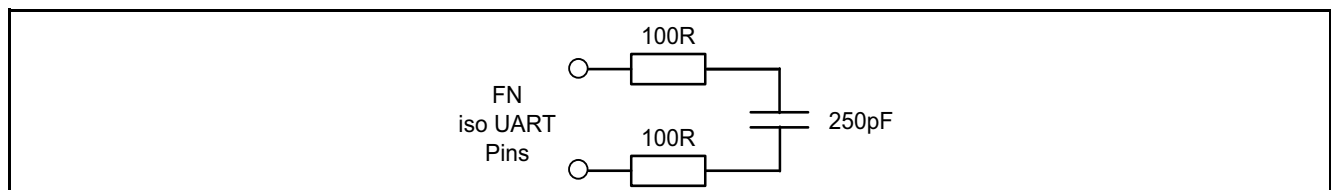
- Master on Top/Master on Bottom
- Ring mode

#### 10.2.1 Master on Top/Master on Bottom (MoT/MoB)

In this mode, the master ( $\mu$ C) is always on the top or bottom of the chain; the TLE9012AQU will be connected on one side to the master (using the transceiver IC) and on the other side to the next TLE9012AQU in the chain. The next node will also have two connections to the previous neighbor and the next neighbor.

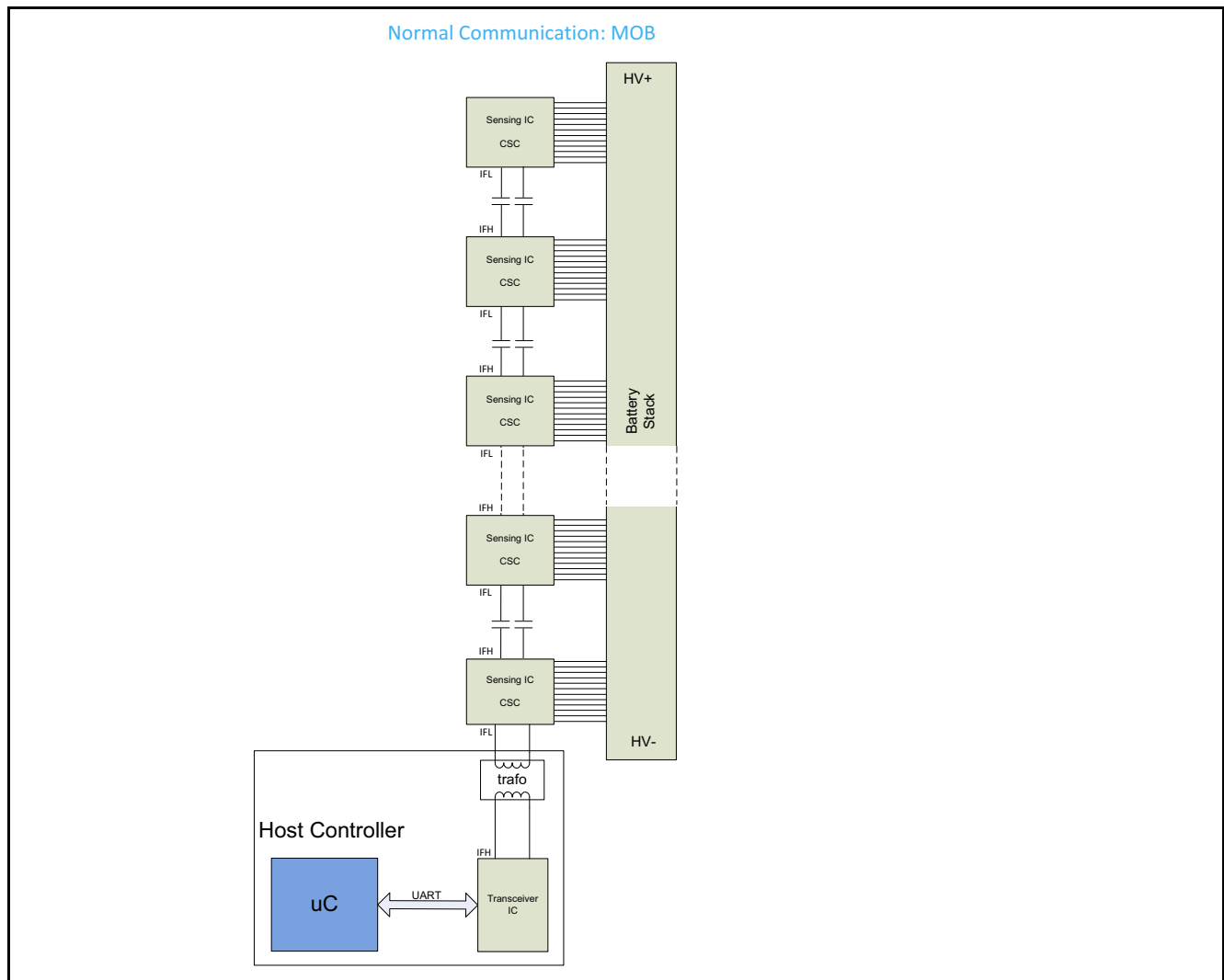
For an MoT topology, the requests will always be forwarded from the IFH to the IFL through the chain. Also for the MoB the requests will be forwarded from the IFL to the IFH. For the response message, the responding device will set both interfaces as TX. Further on, the rest of the chain will forward the message. Some nodes will need to switch their interfaces from TX to RX and RX to TX (this change in the iso UART interfaces is automatically controlled by the internal logic).

For power-balanced communication, the final node needs a termination network. **Figure 31** shows the termination network. The termination network is not required for proper functionality of the device itself.



**Figure 31** iso UART termination network

## Communication interfaces



**Figure 32 Network architecture for Master on Bottom configuration (simplified)**

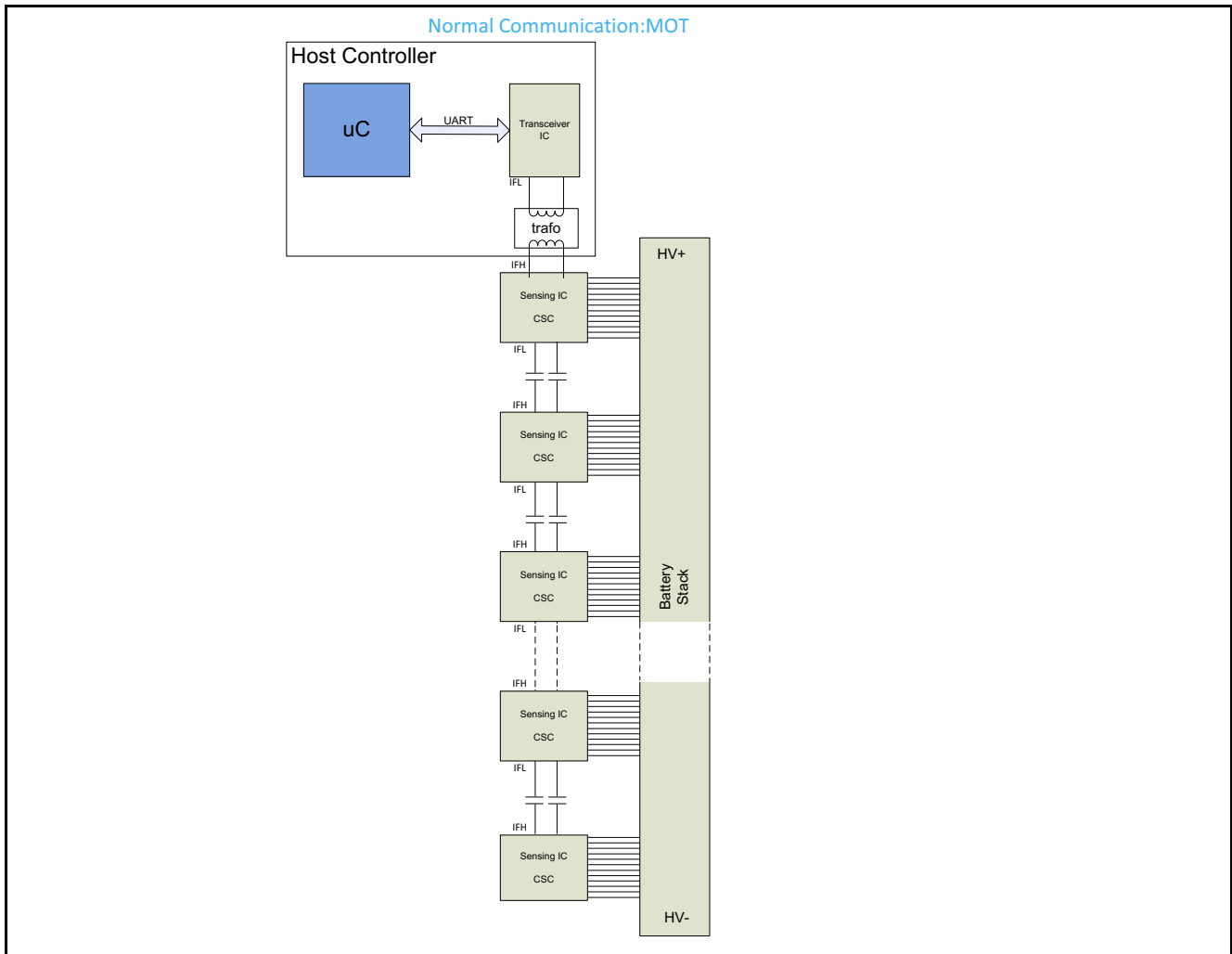
In case of a Master on Top configuration, the master of the chain will send the wake-up signal through the IFL, and the first device in the chain will receive it through the IFH. For a Master on Bottom topology, the master is sending messages through the IFH and the devices in the chain are receiving them through the IFL.

The topology MoT or MoB can be selected depending on which interface is used for receiving the wake-up signal. After a wake-up procedure is completed, a bit will be set in the **GEN\_DIAG** register showing an MoT or MoB topology and this bit will remain fixed until the next wake-up cycle.

The MoT or MoB topology defines the main function (RX or TX mode) of each interface as follows:

**Table 19 Interfaces**

| Topology         | iso UART interface | Sleep mode   | Idle interface status | EMM mode or response mode |
|------------------|--------------------|--------------|-----------------------|---------------------------|
| Master on Bottom | IFH                | Low power RX | TX                    | TX                        |
|                  | IFL                | Low power RX | RX                    | TX                        |
| Master on Top    | IFH                | Low power RX | RX                    | TX                        |
|                  | IFL                | Low power RX | TX                    | TX                        |



**Figure 33 Network architecture for Master on Top configuration (simplified)**

### 10.2.2 Ring topology

The TLE9012AQU offers the possibility to connect all the devices in a system by using the so called ring topology. This topology is very similar to MoB or MoT, but the last node in the chain is as well connected to the master through a second transceiver iso UART interface. In this case no termination network is required.

When using a ring topology the host controller may wake-up the chain by using either UART HS or UART LS. Once the wake-up signal is sent, the direction must be kept until the next wake-up cycle.

The requests will be forwarded through the chain respecting the direction set by wake-up. The master (microcontroller) will receive again the request from the opposite interface confirming that the full chain has no connections problem.

On the other side, the responses will be forwarded in both directions from the responding node. In this case, if the chain has no connection problems, the master will receive the same response from both interfaces.

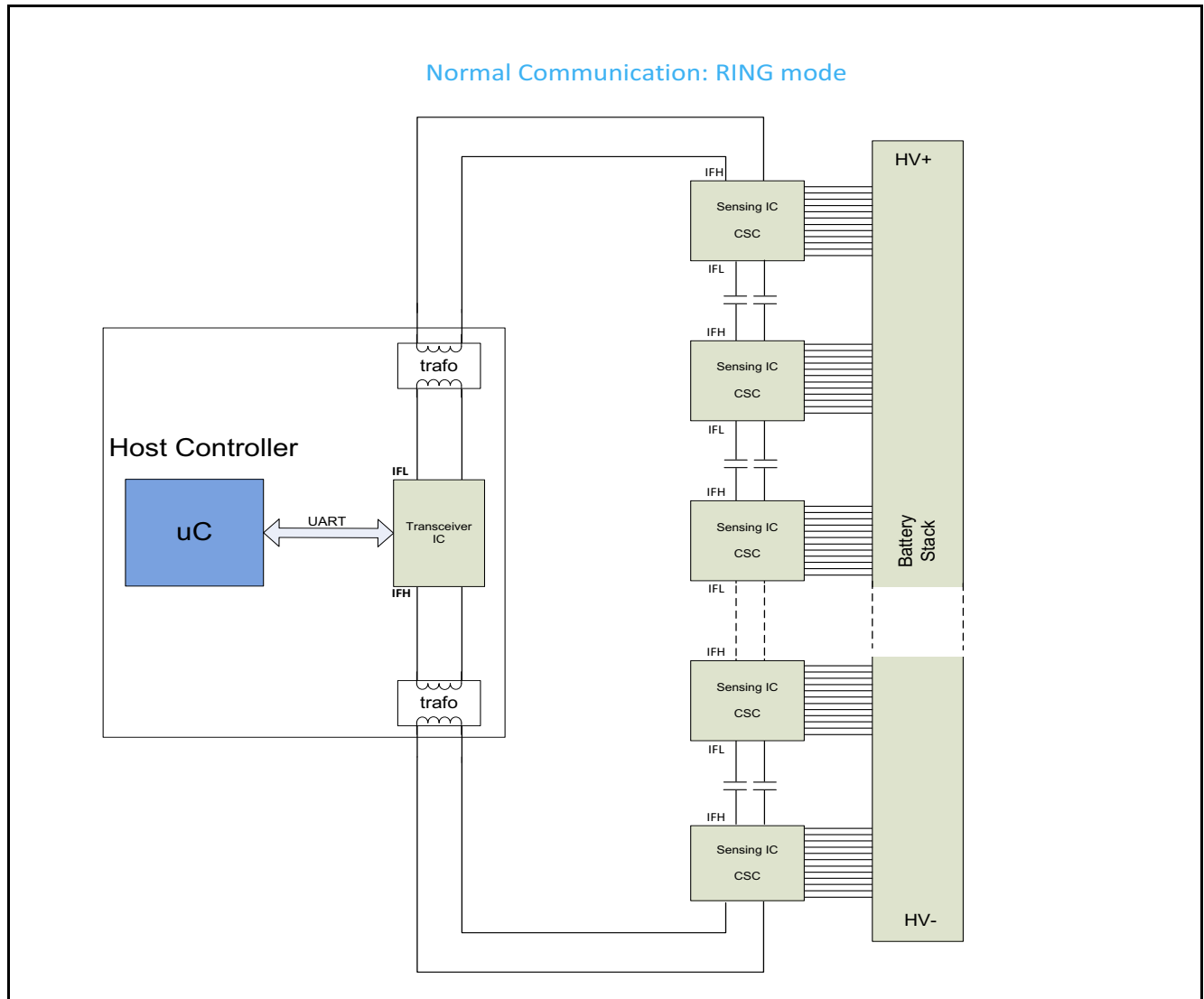
The ring topology has significant advantages in terms of system availability under fault conditions.

If one of the connections is lost inside the chain, all the parts after this open wire will be separated from the master. In this case, the microcontroller will recognize that there is a problem if after the open wire no response from any node is received. Communication can be still achieved if following steps are considered. The microcontroller has to wait until the watchdog of the lost devices reaches underflow and go into sleep mode. The microcontroller needs to set the transceiver IC into sleep mode. Afterwards, the master can start a new wake-up procedure from the opposite interface to contact the lost devices. This would mean the BMS has

## Communication interfaces

then two sub-chains (MoT and MoB) which need to be alternately accessed (Transceiver IC needs to send into sleep mode to switch between MoT and MoB configuration). Please remember that in this case the numbering of the nodes in each of the sub-chains needs to be consecutive again to avoid any clashes in the communication.

Please note that since in this case the network is changed, balanced communication power consumption can not be guaranteed anymore.



**Figure 34 Network architecture for Ring mode configuration (simplified)**

## 10.3 Frame description

The communication (UART or iso UART) frame structure is different for read and write operations. This is due to the fact that a data read request contains less information than a write request. Every request and response contains always a CRC that is checked on the TLE9012AQU on every incoming message. In addition, for every outgoing message a CRC is calculated and sent along with the response. A CRC is calculated over the full message length.

### 10.3.1 Request frames

There are 5 type of requests from the master:

## Communication interfaces

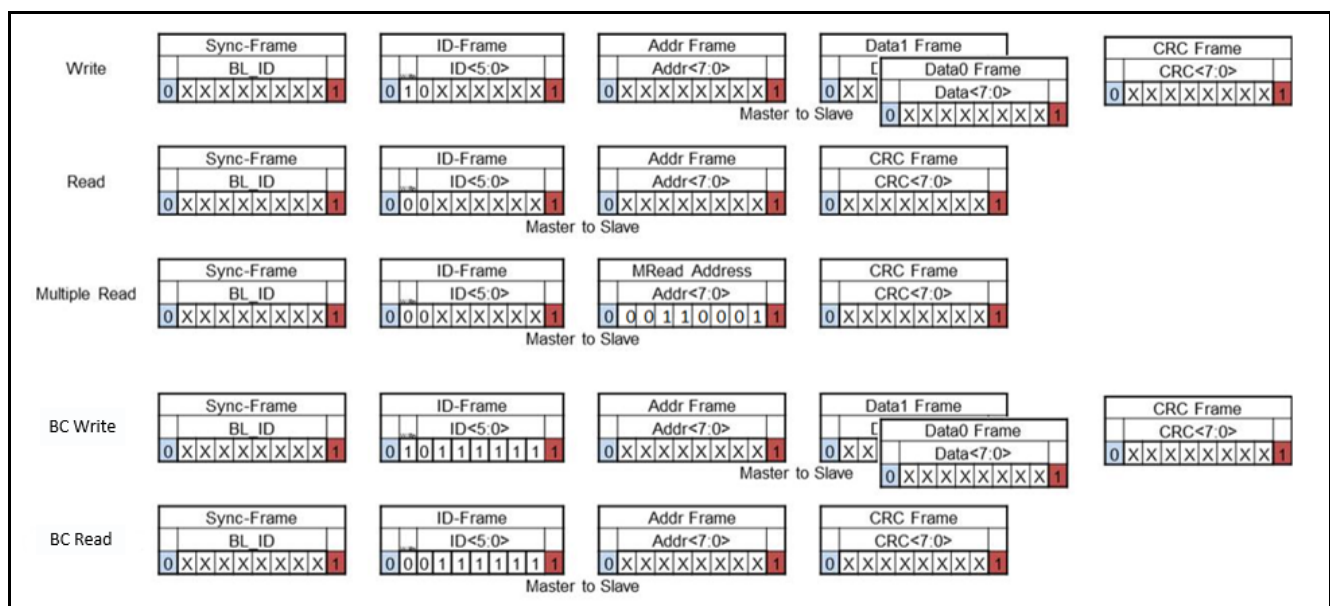
- Write single register command
- Read single register command
- Read multiple registers command
- Broadcast write command
- Broadcast (BC) read single register command

The write single register command fulfills the function of writing data in one 16 bit register of one device while the read single register command is used to read the data of one 16 bit register of one device e.g. the voltage measurement result of one cell. The reading multiple registers command makes it possible to read multiple registers of one device, e.g. all 12 voltage measurement results of one device. Please see [Chapter 12](#) for more information.

Additionally a broadcast (BC) command can be used to communicate with all ICs in the chain – either with a BC read single register command to read data from the same register of all ICs, or with a BC write single register command to write data to the same register of all ICs in the chain. A typical command could be setting or reading a timer for all devices with one single command. By using ID=63 the master can initiate a broadcast command.

Please note: Please use only BC write commands to write into the **MULTI\_READ\_CFG** register if more than one device is connected in a chain.

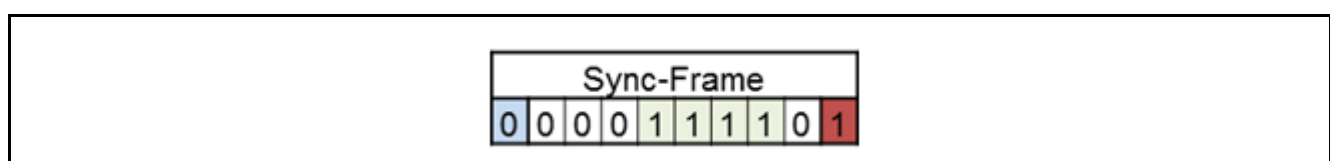
**Figure 35** shows the typical incoming requests from the master:



**Figure 35** Communication master's possible requests

## Synchronization frame

The sync frame is necessary to start the communication with a defined scheme. The sync recognition is edge triggered and recognizes the 0 -> 1 -> 0 -> 1 scheme. **Figure 36** shows the required fixed synchronization frame.



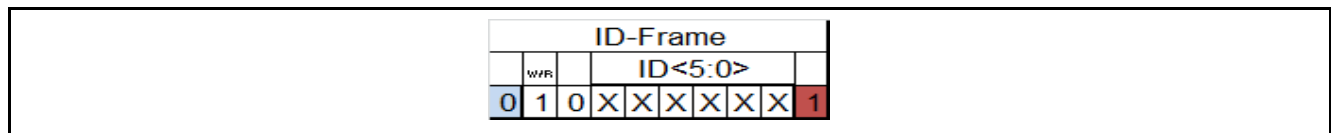
**Figure 36** Synchronization frame



## Communication interfaces

### ID frame

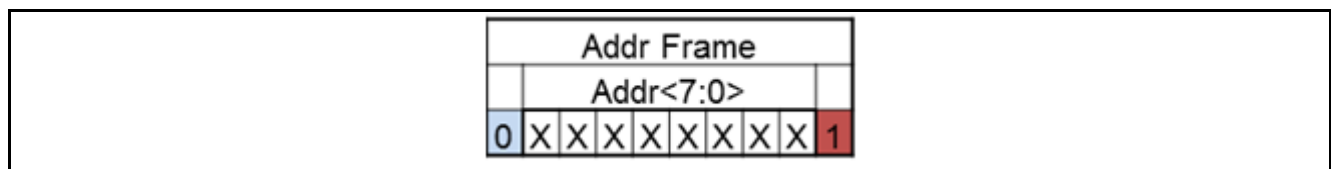
The ID frame fulfills two functions. The MSB defines the kind of command: 1 means it is a write command while 0 means it is a read command. The next six bits represent the ID of the device the master wants to address. On the other side, all bits 1 in a row in the ID-Frame indicate a broadcast command. Furthermore the ID #0 is a special ID where no frames are forwarded to the next IC (see [Chapter 8.2](#)). Theoretically this means a maximum of 62 devices can be connected to one master; however only 20 devices are tested and guaranteed.



**Figure 37 ID frame**

### Address frame

The address frame represents the register that the master wants to either write or read data. Please see [Chapter 12](#) for more information on read multiple registers with one command.

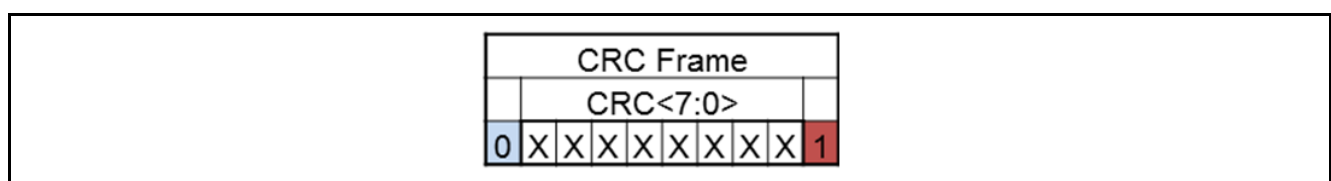


**Figure 38 Address frame**

### CRC frame

As shown in [Figure 35](#), cyclic redundancy check (CRC) status is evaluated by the TLE9012AQU.

For both the read and write request frames, a 8-bit CRC is calculated over the complete message length. The CRC code is based on an 8-bit polynomial  $G(z) = z^8 + z^5 + z^3 + z^2 + z + 1$ . The TLE9012AQU calculates the CRC for incoming requests and compares it with the one included in the message. If the calculated CRC and the one in the message do not match, the device refuses to answer. Therefore the master would then run into a time-out and realize that the communication failed.



**Figure 39 CRC frame**

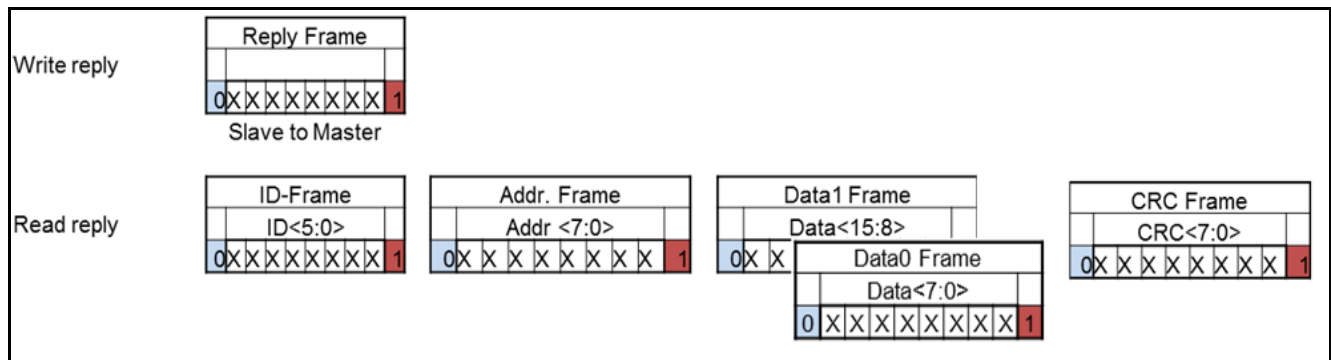
## 10.3.2 Reply frames

There are 6 different types of reply frames:

- Write reply frame single register
- Read reply frame single register
- Read reply frame multiple registers
- Broadcast write reply frame
- Broadcast read single register reply frame

Nevertheless the different reply frames contain only two different frame structures. One register writing reply frame or different types of reading reply frames.

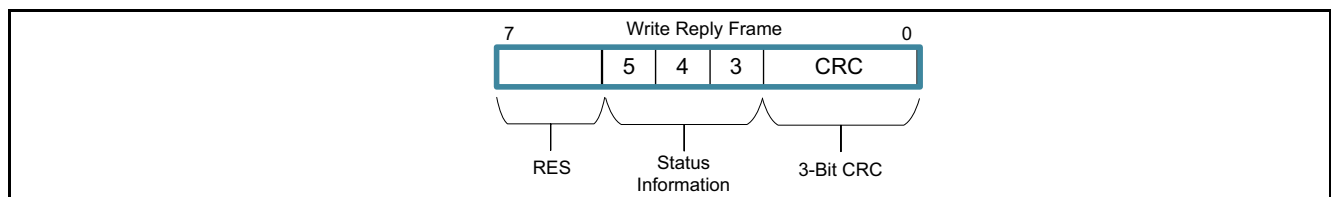
## Communication interfaces



**Figure 40** Slave's reply frames structures

### Write reply frame

Since the entire register writing process is CRC-protected, there is no need for a detailed acknowledge frame. Therefore the writing reply frame is kept as short as possible to minimize communication-based power consumption and time. In case there is no message CRC error detected by the addressed device, it will send a write reply frame back. This means if the master does not get a write reply frame back after sending a write command, either the addressed device detected a CRC error or the connection is lost completely. The write reply frame contains the information shown in [Figure 41](#) and [Table 20](#). Please see also [Chapter 12](#) for more information what needs to be considered when writing to registers.



**Figure 41** Slave's write reply frame

**Table 20** Write reply frame status information

| Bit | Data | Status Information   |
|-----|------|--|
| 3   | 0    | No fault indicated in <a href="#">GEN_DIAG</a> register  |
|     | 1    | At least one fault is indicated in <a href="#">GEN_DIAG</a> register   |
| 4   | 0    | Register address for write command valid   |
|     | 1    | Register address for write command NOT valid   |
| 5   | 0    | Write command was successful   |
|     | 1    | Write command was NOT successful (only checked for CRC protected registers, see also <a href="#">Chapter 8.3.1</a> ) |

In case of a BC write command, each device in the chain will switch RX and TX units after successful writing. Then the last device in the chain (identified by setting the FN-Bit in the [CONFIG](#) register) sends a reply frame after successful register writing. That frame will be transported through the full chain back to the master if all device in between did switch RX and TX due to a successful writing. If the master receives the reply frame, it is confirmed that the BC write request was successful.

The CRC code is based on an 3-bit polynomial  $G(z) = z^3 + z + 1$

## Communication interfaces

### Read reply frame

There are three different read requests. Depending on the request the reply frames sent by the CSC devices are different. A single register read reply frame looks exactly like shown in [Figure 40](#). A multiple registers read reply frame looks like the one shown in [Figure 40](#) but the CSC device sends such a frame once for each register which is part of the multiple register reading command. The ID will stay constant while the address, the data and the CRC will be different for each message frame.

The BC command reply messages working in the same manner. A BC read for a single register will generate a reply message frame like in [Figure 40](#) transmitted from the device in the chain with ID #1, followed by the device with the ID #2 with a similar frame and so on. Each response frame will have the corresponding ID of the device which is answering, plus the register address (which will be the same for all Nodes).

### 10.4 Chain timing

The chain timing is shown in [Figure 42](#). The pass through time for each node is  $t_{\text{isoUART\_prop\_del}}$ . This means the microcontroller is still sending while the beginning of the message is already back at the microcontroller in ring mode.

There is a reply delay  $t_{\text{reply\_delay}}$  implemented to make sure that all nodes can change their TX/RX direction properly before their reply frame is send.

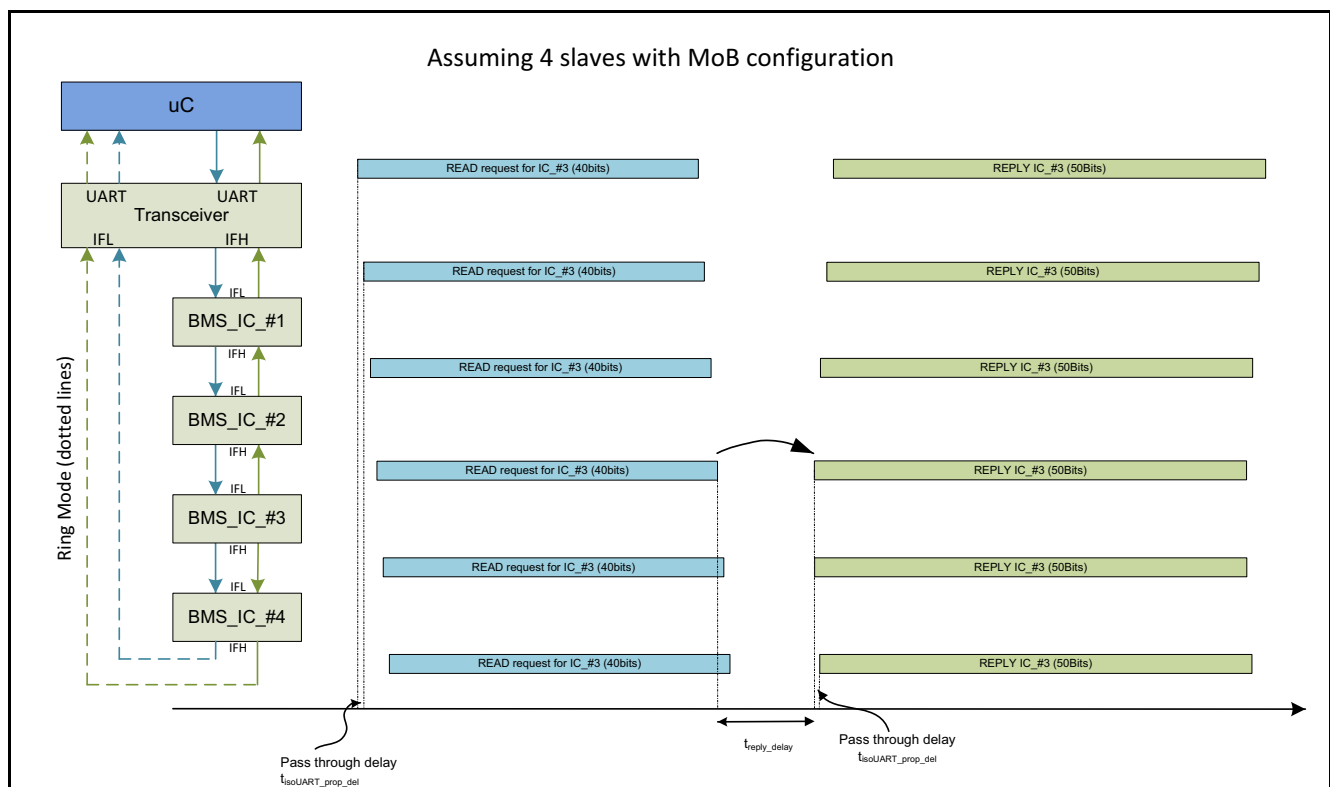


Figure 42 Timing

## Communication interfaces

### 10.4.1 Electrical characteristics

**Table 21** Electrical characteristics

$V_{VS} = 4.75 \text{ V to } 60 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ , all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values |      |      | Unit | Note or Test Condition | Number |
|-----------|--------|--------|------|------|------|------------------------|--------|
|           |        | Min.   | Typ. | Max. |      |                        |        |

#### Delay timing

|                  |                           |   |     |   |               |               |  |
|------------------|---------------------------|---|-----|---|---------------|---------------|--|
| Reply delay time | $t_{\text{reply\_delay}}$ | 0 | 1.7 | 3 | $\mu\text{s}$ | <sup>1)</sup> |  |
|------------------|---------------------------|---|-----|---|---------------|---------------|--|

1) Not subject to production test, specified by design.

**Built-in diagnosis features**

## 11 Built-in diagnosis features

This chapter provides a summary of the built-in diagnosis features of the TLE9012AQU. Furthermore it references to the related registers and bit-fields. There are four different types of diagnosis mechanisms implemented in the TLE9012AQU:

- Periodically triggered diagnosis mechanisms via round robin (please see also chapter [Chapter 8.3](#))
- Periodically triggered diagnosis mechanisms with a fixed hardware cycle (please see below)
- Continuous hardware monitoring diagnosis (please see also chapter [Chapter 4.5](#) and [Chapter 10.3](#))
- Manually triggerable diagnosis mechanisms (please see also chapter [Chapter 7](#))

The following [Table 22](#) gives an overview of each built-in diagnosis mechanism mapped to one of the four types from above.

**Table 22 Summary of built-in diagnosis mechanisms**

| Error   | Register                 | Bit-field   | State  |
|---|--------------------------|-------------|--|
| <b>Periodically triggered mechanism via round robin</b>           |                          |             |  |
| Balancing overcurrent   | <a href="#">GEN_DIAG</a> | BAL_ERR_OC  | IC remains in normal mode. Balancing for affected cell(s) deactivated. |
| Balancing undercurrent  | <a href="#">GEN_DIAG</a> | BAL_ERR_UC  | IC remains in normal mode. Balancing for affected cell(s) deactivated. |
| Cell overvoltage  | <a href="#">GEN_DIAG</a> | CELL_OV     | IC remains in normal mode. Balancing for affected cell(s) deactivated. |
| Cell undervoltage   | <a href="#">GEN_DIAG</a> | CELL_UV     | IC remains in normal mode. Balancing for affected cell(s) deactivated. |
| Internal overtemperature error                                    | <a href="#">GEN_DIAG</a> | INT_OT      | IC remains in normal mode. Balancing deactivated                       |
| External temperature sensor error                                 | <a href="#">GEN_DIAG</a> | EXT_OT      | IC remains in normal mode. Balancing deactivated                       |
| Open load detection (for all Ux/Gx)                               | <a href="#">GEN_DIAG</a> | OL_ERR      | IC remains in normal mode. Balancing deactivated                       |
| ADC result (CVM vs. BVM) comparison error                         | <a href="#">GEN_DIAG</a> | ADC_ERR     | IC remains in normal mode. Balancing deactivated                       |
| <b>Periodically triggered mechanism with fixed hardware cycle</b> |                          |             |  |
| Register CRC error  | <a href="#">GEN_DIAG</a> | REG_CRC_ERR | IC remains in normal mode. Balancing deactivated                       |
| Internal IC error   | <a href="#">GEN_DIAG</a> | INT_IC_ERR  | IC remains in normal mode. Balancing deactivated.                      |
| <b>Continuous hardware monitoring diagnosis</b>                   |                          |             |  |
| VREGOUT overcurrent   | <a href="#">GEN_DIAG</a> | UV_SLEEP    | IC goes to sleep mode  |
| Internal supply undervoltage                                      | <a href="#">GEN_DIAG</a> | UV_SLEEP    | IC goes to sleep mode  |
| VIO undervoltage  | <a href="#">GPIO</a>     | VIO_UV      | IC remains in normal mode  |

**Built-in diagnosis features**

**Table 22 Summary of built-in diagnosis mechanisms**

| Error                            | Register | Bit-field | State   |
|----------------------------------|----------|-----------|---|
| Incoming communication CRC error |          |           | IC remains in normal mode.<br>Interfaces changed to default direction |
| Oscillator drift error detection |          |           | IC goes to sleep mode   |

**Manually triggerable diagnosis mechanisms**

|  |                   |                       |  |
|--|-------------------|-----------------------|--|
| NTC source error check via $R_{DIAG}$ measurement                      |                   | RESULT                |  |
| Internal temperature MUX error via internal pull down switches         | <b>AVM_CONFIG</b> | TEMP_MUX_DI<br>AG_SEL |  |
| External short of neighboring TMP pins via internal pull down switches | <b>AVM_CONFIG</b> | TEMP_MUX_DI<br>AG_SEL |  |

**Built-in diagnosis with fixed hardware cycle**

There are additional internal checks implemented in the TLE9012AQU. First of all the registers with the following addresses are CRC protected: 01<sub>H</sub>, 02<sub>H</sub>, 03<sub>H</sub>, 04<sub>H</sub>, 05<sub>H</sub>, 08<sub>H</sub>, 09<sub>H</sub>, 0A<sub>H</sub>, 14<sub>H</sub>, 15<sub>H</sub>, 17<sub>H</sub>, 36<sub>H</sub>, 38<sub>H</sub>, 3A<sub>H</sub>. Additionally the internal IC data (e.g. ADC trimming values) is also ECC protected. The register CRC check as well as the internal data check is executed with a fixed hardware cycle time  $t_{CRC\_check}$  independent of the round robin scheme interval time.

Please note: The register CRC error as well as the internal IC error do not have an error counter.

## 12 Registers

### 12.1 Registers overview

**Table 23** gives an overview over all registers of the TLE9012AQU. Register fields labelled “RES” (reserved for future use) are as the name indicates reserved for potential future use. When writing into a register, the “RES” part of the register must always be written with “0”. The same applies for read only bit-fields. When reading, the contents of the “RES” fields should be masked out since the value is not defined.

- r = read access
- w = write access
- wo = write access only one time
- h = the IC hardware can change the contents of the field
- rocw = read only, clear bit by writing a “0” to the respective bit position
- roawl = read only, clear bit by writing a “0”, linked register is reset to default state
- rocr = read only, clearing bit by reading

**Table 23 Register Overview**

| Register Short Name                              | Register Long Name   | Offset Address  | Reset Value       |
|--|--|-----------------|-------------------|
| <b>Registers overview, Registers description</b> |  |                 |                   |
| <b>PART_CONFIG</b>                               | Partitioning config (supplied in sleep)                            | 01 <sub>H</sub> | 0800 <sub>H</sub> |
| <b>OL_OV_THR</b>                                 | Cell voltage thresholds (supplied in sleep)                        | 02 <sub>H</sub> | FFFF <sub>H</sub> |
| <b>OL_UV_THR</b>                                 | Cell voltage thresholds (supplied in sleep)                        | 03 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>TEMP_CONF</b>                                 | Temperature measurement configuration (supplied in sleep)          | 04 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>INT_OT_WARN_CONF</b>                          | Internal temperature measurement configuration (supplied in sleep) | 05 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>RR_ERR_CNT</b>                                | Round Robin ERR counters (supplied in sleep)                       | 08 <sub>H</sub> | 0002 <sub>H</sub> |
| <b>RR_CONFIG</b>                                 | Round Robin configuration (supplied in sleep)                      | 09 <sub>H</sub> | 8024 <sub>H</sub> |
| <b>FAULT_MASK</b>                                | ERR pin / EMM mask (supplied in sleep)                             | 0A <sub>H</sub> | 3400 <sub>H</sub> |
| <b>GEN_DIAG</b>                                  | General diagnosis (supplied in sleep)                              | 0B <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CELL_UV</b>                                   | Cell voltage supervision warning flags UV (supplied in sleep)      | 0C <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CELL_OV</b>                                   | Cell voltage supervision warning flags OV (supplied in sleep)      | 0D <sub>H</sub> | 0000 <sub>H</sub> |
| <b>EXT_TEMP_DIAG</b>                             | External overtemperature warning flags (supplied in sleep)         | 0E <sub>H</sub> | 0000 <sub>H</sub> |
| <b>DIAG_OL</b>                                   | Diagnosis OPENLOAD (supplied in sleep)                             | 10 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>REG_CRC_ERR</b>                               | REG_CRC_ERR (supplied in sleep)                                    | 11 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>OP_MODE</b>                                   | Operation mode   | 14 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>BAL_CURR_THR</b>                              | Balancing current thresholds                                       | 15 <sub>H</sub> | 00AC <sub>H</sub> |
| <b>BAL_SETTINGS</b>                              | Balance settings   | 16 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>AVM_CONFIG</b>                                | Auxiliary Voltage Measurement Configuration                        | 17 <sub>H</sub> | 001C <sub>H</sub> |

## Registers

**Table 23 Register Overview** (cont'd)

| Register Short Name    | Register Long Name                  | Offset Address  | Reset Value       |
|------------------------|-------------------------------------|-----------------|-------------------|
| <b>MEAS_CTRL</b>       | Measurement control                 | 18 <sub>H</sub> | 0021 <sub>H</sub> |
| <b>CVM_0</b>           | Cell voltage measurement 0          | 19 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_1</b>           | Cell voltage measurement 1          | 1A <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_2</b>           | Cell voltage measurement 2          | 1B <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_3</b>           | Cell voltage measurement 3          | 1C <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_4</b>           | Cell voltage measurement 4          | 1D <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_5</b>           | Cell voltage measurement 5          | 1E <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_6</b>           | Cell voltage measurement 6          | 1F <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_7</b>           | Cell voltage measurement 3          | 20 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_8</b>           | Cell voltage measurement 8          | 21 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_9</b>           | Cell voltage measurement 9          | 22 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_10</b>          | Cell voltage measurement 10         | 23 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CVM_11</b>          | Cell voltage measurement 11         | 24 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>BVM</b>             | Block voltage measurement           | 28 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>EXT_TEMP_0</b>      | Temp result 0                       | 29 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>EXT_TEMP_1</b>      | Temp result 1                       | 2A <sub>H</sub> | 0000 <sub>H</sub> |
| <b>EXT_TEMP_2</b>      | Temp result 2                       | 2B <sub>H</sub> | 0000 <sub>H</sub> |
| <b>EXT_TEMP_3</b>      | Temp result 3                       | 2C <sub>H</sub> | 0000 <sub>H</sub> |
| <b>EXT_TEMP_4</b>      | Temp result 4                       | 2D <sub>H</sub> | 0000 <sub>H</sub> |
| <b>EXT_TEMP_R_DIAG</b> | Temp result R Diagnose              | 2F <sub>H</sub> | 0000 <sub>H</sub> |
| <b>INT_TEMP</b>        | Chip temperature                    | 30 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>MULTI_READ</b>      | Multiread command                   | 31 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>MULTI_READ_CFG</b>  | Multiread Configuration             | 32 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>BAL_DIAG_OC</b>     | Passive bal. diagnosis OVERCURRENT  | 33 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>BAL_DIAG_UC</b>     | Passive bal. diagnosis UNDERCURRENT | 34 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CONFIG</b>          | Configuration                       | 36 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>GPIO</b>            | General purpose input / output      | 37 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>GPIO_PWM</b>        | PWM settings                        | 38 <sub>H</sub> | 0000 <sub>H</sub> |
| <b>ICVID</b>           | IC version and manufacturing ID     | 39 <sub>H</sub> | C101 <sub>H</sub> |
| <b>MAILBOX</b>         | Mailbox register                    | 3A <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CUSTOMER_ID_0</b>   | Customer ID                         | 3B <sub>H</sub> | 0000 <sub>H</sub> |
| <b>CUSTOMER_ID_1</b>   | Customer ID                         | 3C <sub>H</sub> | 0000 <sub>H</sub> |
| <b>WD OG_CNT</b>       | Watchdog counter                    | 3D <sub>H</sub> | 007F <sub>H</sub> |



## Registers

### 12.1.1 Registers description

#### PART\_CONFIG

| PART_CONFIG                             | Offset          | Reset Value       |
|---|-----------------|-------------------|
| Partitioning config (supplied in sleep) | 01 <sub>H</sub> | 0800 <sub>H</sub> |

| 15  | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|
| RES | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* | EN_* |
| rwh | r    | rw   | rw   | rw   | rw   | rw   | rw   | rw   | rw   | rw   | rw   | rw   | rw   |

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| RES       | 15:12 | rwh  | <b>Reserved for future use</b><br>00000 <sub>B</sub> , not defined (default)   |
| EN_CELL11 | 11    | r    | <b>Enable cell monitoring for cell 11</b><br>Please note: Cell 11 must be connected<br>1 <sub>B</sub> , cell attached (default)  |
| EN_CELL10 | 10    | rw   | <b>Enable cell monitoring for cell 10</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached |
| EN_CELL9  | 9     | rw   | <b>Enable cell monitoring for cell 9</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached  |
| EN_CELL8  | 8     | rw   | <b>Enable cell monitoring for cell 8</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached  |
| EN_CELL7  | 7     | rw   | <b>Enable cell monitoring for cell 7</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached  |
| EN_CELL6  | 6     | rw   | <b>Enable cell monitoring for cell 6</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached  |
| EN_CELL5  | 5     | rw   | <b>Enable cell monitoring for cell 5</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached  |

## Registers

| Field    | Bits | Type | Description   |
|----------|------|------|---|
| EN_CELL4 | 4    | rw   | <b>Enable cell monitoring for cell 4</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached |
| EN_CELL3 | 3    | rw   | <b>Enable cell monitoring for cell 3</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached |
| EN_CELL2 | 2    | rw   | <b>Enable cell monitoring for cell 2</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached |
| EN_CELL1 | 1    | rw   | <b>Enable cell monitoring for cell 1</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached |
| EN_CELLO | 0    | rw   | <b>Enable cell monitoring for cell 0</b><br>Please note: Cells must be connected consecutively starting from cell 11<br>0 <sub>B</sub> , no cell attached (default)<br>1 <sub>B</sub> , cell attached |

## OL\_OV\_THR

| OL_OV_THR  | Offset          | Reset Value       |
|--|-----------------|-------------------|
| Cell voltage thresholds (supplied in sleep)  | 02 <sub>H</sub> | FFFF <sub>H</sub> |
| <div> <div>15</div> <div>10</div> <div>9</div> <div>0</div> </div> <div> <div>OL_THR_MAX</div> <div>OV_THR</div> </div> <div> <div>rw</div> <div>rw</div> </div> |                 |                   |

| Field      | Bits  | Type | Description   |
|------------|-------|------|---|
| OL_THR_MAX | 15:10 | rw   | <b>Openload maximum voltage drop threshold (LSB10)</b><br>6 bit (LSB10) to define the maximum threshold for the voltage drop while OL-diagnosis ( $I_{OL\_DIAG} \cdot R_f$ ). If drop voltage > OL_thr_max, the OLx bit of channel x is set.<br>11 1111 <sub>B</sub> , threshold (default)                                      |
| OV_THR     | 9:0   | rw   | <b>Overvoltage fault threshold (LSB10)</b><br>10 bit overvoltage fault threshold. Battery input voltages (U0 to U11) are tested for overvoltage with given value. OV Error is detected and indicated in GEN_DIAG register if cell voltage is HIGHER than OV fault threshold.<br>11 1111 1111 <sub>B</sub> , threshold (default) |

## Registers

### OL\_UV\_THR

| OL_UV_THR                                   | Offset          | Reset Value       |
|---|-----------------|-------------------|
| Cell voltage thresholds (supplied in sleep) | 03 <sub>H</sub> | 0000 <sub>H</sub> |

|            |    |        |   |
|------------|----|--------|---|
| 15         | 10 | 9      | 0 |
| OL_THR_MIN |    | UV_THR |   |
| rw         |    | rw     |   |

| Field      | Bits  | Type | Description   |
|------------|-------|------|---|
| OL_THR_MIN | 15:10 | rw   | <b>Openload minimum voltage drop threshold (LSB10)</b><br>6 bit (LSB10) to define the minimum threshold for the voltage drop while OL-diagnosis ( $I_{OL\_DIAG} \cdot R_f$ ). If voltage drop < OL_thr_min, the OLx bit of channel x is set.<br>00 0000 <sub>B</sub> , threshold (default)  |
| UV_THR     | 9:0   | rw   | <b>Undervoltage fault threshold (LSB10)</b><br>10 bit undervoltage fault threshold. Battery input voltages (U0 to U11) are tested for undervoltage with given value. UV Error is detected and indicated in GEN_DIAG register if cell voltage is LOWER than UV fault threshold.<br>00 0000 0000 <sub>B</sub> , threshold (default) |

### TEMP\_CONF

| TEMP_CONF   | Offset          | Reset Value       |
|---|-----------------|-------------------|
| Temperature measurement configuration (supplied in sleep) | 04 <sub>H</sub> | 0000 <sub>H</sub> |

|     |            |       |            |    |   |   |
|-----|------------|-------|------------|----|---|---|
| 15  | 14         | 12    | 11         | 10 | 9 | 0 |
| RES | NR_TEMP_S* | I_NTC | EXT_OT_THR |    |   |   |
| rwh | rw         | rw    | rw         |    |   |   |

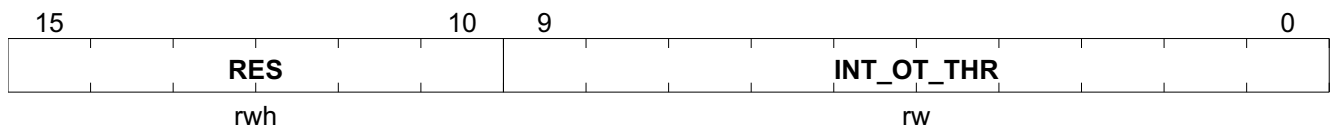
| Field         | Bits  | Type | Description  |
|---------------|-------|------|--|
| RES           | 15    | rwh  | <b>Reserved for future use</b><br>0 <sub>B</sub> , not defined (default)   |
| NR_TEMP_SENSE | 14:12 | rw   | <b>Number of external temperature sensors</b><br>000 <sub>B</sub> , no external TMP sensor (default)<br>001 <sub>B</sub> , TMP0 active<br>010 <sub>B</sub> , TMP0 + TMP1 active<br>011 <sub>B</sub> , TMP0 + TMP1 + TMP 2 active<br>100 <sub>B</sub> , TMP0 + TMP1 + TMP 2 + TMP 3 active<br>101 <sub>B</sub> , TMP0 + TMP1 + TMP 2 + TMP 3 + TMP 4 active |

## Registers

| Field             | Bits  | Type | Description   |
|-------------------|-------|------|---|
| <b>I_NTC</b>      | 11:10 | rw   | <b>Current source used for OT fault</b><br>00 <sub>B</sub> , $I_{TMPn\_0}$ used (default)<br>01 <sub>B</sub> , $I_{TMPn\_1}$ used<br>10 <sub>B</sub> , $I_{TMPn\_2}$ used<br>11 <sub>B</sub> , $I_{TMPn\_3}$ used   |
| <b>EXT_OT_THR</b> | 9:0   | rw   | <b>External temperature overtemperature threshold</b><br>10 bit overtemperature fault threshold. Overtemperature error is detected and indicated in GEN_DIAG register if the RESULT is < EXT_OT_THR. Balancing is deactivated.<br>00 0000 0000 <sub>B</sub> , threshold (default) |

## INT\_OT\_WARN\_CONF

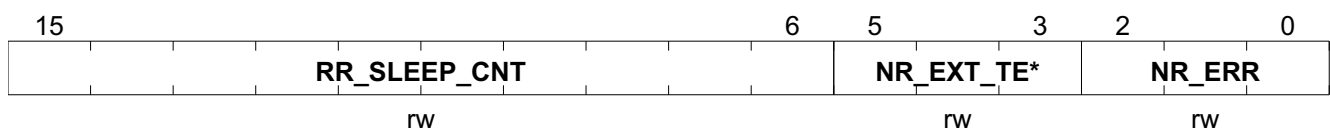
|  |                 |                    |
|--|-----------------|--------------------|
| <b>INT_OT_WARN_CONF</b>  | <b>Offset</b>   | <b>Reset Value</b> |
| Internal temperature measurement configuration (supplied in sleep) | 05 <sub>H</sub> | 0000 <sub>H</sub>  |



| Field             | Bits  | Type | Description  |
|-------------------|-------|------|--|
| <b>RES</b>        | 15:10 | rwh  | <b>Reserved for future use</b><br>0000 00 <sub>B</sub> , not defined (default)   |
| <b>INT_OT_THR</b> | 9:0   | rw   | <b>Internal temperature overtemperature threshold</b><br>10 bit overtemperature fault threshold. Overtemperature error is detected and indicated in GEN_DIAG register if internal temperature result is LOWER than the fault threshold. Balancing is deactivated.<br>00 0000 0000 <sub>B</sub> , threshold (default) |

## RR\_ERR\_CNT

|  |                 |                    |
|--|-----------------|--------------------|
| <b>RR_ERR_CNT</b>                            | <b>Offset</b>   | <b>Reset Value</b> |
| Round Robin ERR counters (supplied in sleep) | 08 <sub>H</sub> | 0002 <sub>H</sub>  |



## Registers

| Field             | Bits | Type | Description  |
|-------------------|------|------|--|
| RR_SLEEP_CNT      | 15:6 | rw   | <b>Round Robin timing in sleep mode</b><br>$0_B$ , RR in sleep mode is deactivated (default)<br>$1_B$ , $t_{RR\_sleep\_LSB}$<br>$3FF_H$ , $t_{RR\_sleep\_LSB} * 1023$  |
| NR_EXT_TEMP_START | 5:3  | rw   | <b>External temperature triggering in round robin</b><br>$0_B$ , every RR (default)<br>$1_B$ , 1 RR measurement, 1 RR no measurement<br>$10_B$ , 1 RR measurement, 2 RR no measurement<br>$11_B$ , 1 RR measurement, 3 RR no measurement<br>$100_B$ , 1 RR measurement, 4 RR no measurement<br>$101_B$ , 1 RR measurement, 5 RR no measurement<br>$110_B$ , 1 RR measurement, 6 RR no measurement<br>$111_B$ , 1 RR measurement, 7 RR no measurement |
| NR_ERR            | 2:0  | rw   | <b>Number of errors</b><br>Number of consecutive detected errors before error is valid and set in GEN_DIAG and individual fault registers. Only used for faults where counter NR_ERR is active (this can be set in register NR_ERR_MASK). Please note: The register CRC errors as well as the internal IC errors do not have an error counter.<br>$000_B$ , 0<br>$001_B$ , 1<br>$010_B$ , 2 (default)<br>...<br>$111_B$ , 7                          |

## RR\_CONFIG

| RR_CONFIG                                     | Offset | Reset Value |
|---|--------|-------------|
| Round Robin configuration (supplied in sleep) | $09_H$ | $8024_H$    |

|      |      |      |      |      |      |      |      |      |   |  |  |  |  |  |        |   |
|------|------|------|------|------|------|------|------|------|---|--|--|--|--|--|--------|---|
| 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    | 7    | 6 |  |  |  |  |  |        | 0 |
| M_N* | M_N* | M_N* | M_N* | M_N* | M_N* | M_N* | M_N* | RR_* |   |  |  |  |  |  | RR_CNT |   |
| rw   | rw   | rw   | rw   | rw   | rw   | rw   | rw   | rw   |   |  |  |  |  |  | rw     |   |

| Field               | Bits | Type | Description  |
|---------------------|------|------|--|
| M_NR_ERR_B<br>AL_OC | 15   | rw   | <b>mask NR_ERR counter for balancing error overcurrent</b><br>$0_B$ , No masking of NR_ERR. Counter is active<br>$1_B$ , NR_ERR counter masked. Fault valid after first detection (default)  |
| M_NR_ERR_B<br>AL_UC | 14   | rw   | <b>mask NR_ERR counter for balancing error undercurrent</b><br>$0_B$ , No masking of NR_ERR. Counter is active (default)<br>$1_B$ , NR_ERR counter masked. Fault valid after first detection |

## Registers

| Field                        | Bits | Type | Description   |
|------------------------------|------|------|---|
| <b>M_NR_ERR_C<br/>ELL_OV</b> | 13   | rw   | <b>mask NR_ERR counter for overvoltage error</b><br>0 <sub>B</sub> , No masking of NR_ERR. Counter is active (default)<br>1 <sub>B</sub> , NR_ERR counter masked. Fault valid after first detection   |
| <b>M_NR_ERR_C<br/>ELL_UV</b> | 12   | rw   | <b>mask NR_ERR counter for undervoltage error</b><br>0 <sub>B</sub> , No masking of NR_ERR. Counter is active (default)<br>1 <sub>B</sub> , NR_ERR counter masked. Fault valid after first detection  |
| <b>M_NR_ERR_I<br/>NT_OT</b>  | 11   | rw   | <b>mask NR_ERR counter for internal temperature error</b><br>0 <sub>B</sub> , No masking of NR_ERR. Counter is active (default)<br>1 <sub>B</sub> , NR_ERR counter masked. Fault valid after first detection  |
| <b>M_NR_ERR_E<br/>XT_OT</b>  | 10   | rw   | <b>mask NR_ERR counter for external temperature error</b><br>0 <sub>B</sub> , No masking of NR_ERR. Counter is active (default)<br>1 <sub>B</sub> , NR_ERR counter masked. Fault valid after first detection  |
| <b>M_NR_ERR_O<br/>L_ERR</b>  | 9    | rw   | <b>mask NR_ERR counter for open load error</b><br>0 <sub>B</sub> , No masking of NR_ERR. Counter is active (default)<br>1 <sub>B</sub> , NR_ERR counter masked. Fault valid after first detection   |
| <b>M_NR_ERR_A<br/>DC_ERR</b> | 8    | rw   | <b>mask NR_ERR counter for ADC error</b><br>0 <sub>B</sub> , No masking of NR_ERR. Counter is active (default)<br>1 <sub>B</sub> , NR_ERR counter masked. Fault valid after first detection   |
| <b>RR_SYNC</b>               | 7    | rw   | <b>Round Robin synchronization</b><br>0 <sub>B</sub> , no synch with WD_CNT write access (default)<br>1 <sub>B</sub> , synch with WD_CNT write access (RR will be started by write access, if RR is already running the RR will be restarted from beginning again.) |
| <b>RR_CNT</b>                | 6:0  | rw   | <b>Round Robin counter</b><br>Setting round robin counter (default: 010 0100 ~ 50 ms)<br>0 <sub>H</sub> , Round Robin starts every $t_{RR\_min}$<br>7F <sub>H</sub> , Round Robin starts every $t_{RR\_max}$  |

## FAULT\_MASK

**FAULT\_MASK** Offset **Reset Value**  
ERR pin / EMM mask (supplied in sleep) 0A<sub>H</sub> 3400<sub>H</sub>

|             |             |             |             |             |             |             |             |             |             |             |   |            |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|------------|
| 15          | 14          | 13          | 12          | 11          | 10          | 9           | 8           | 7           | 6           | 5           | 4 | 0          |
| <b>M_B*</b> | <b>M_B*</b> | <b>M_C*</b> | <b>M_C*</b> | <b>M_I*</b> | <b>M_E*</b> | <b>M_R*</b> | <b>M_I*</b> | <b>M_O*</b> | <b>M_A*</b> | <b>ERR*</b> |   | <b>RES</b> |
| rw          | rw          | rw          | rw          | rw          | rw          | rw          | rw          | rw          | rw          | rw          |   | rwh        |

| Field               | Bits | Type | Description   |
|---------------------|------|------|---|
| <b>M_BAL_ERR_OC</b> | 15   | rw   | <b>EMM/ERR mask for balancing error overcurrent</b><br>0 <sub>B</sub> , ERR/EMM will NOT be set if this type of error occurs (default)<br>1 <sub>B</sub> , ERR/EMM will be set for this type of error |

## Registers

| Field                | Bits | Type | Description   |
|----------------------|------|------|---|
| <b>M_BAL_ERR_UC</b>  | 14   | rw   | <b>EMM/ERR mask for balancing error undercurrent</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs (default)<br>$1_B$ , ERR/EMM will be set for this type of error  |
| <b>M_CELL_OV</b>     | 13   | rw   | <b>EMM/ERR mask for cell overvoltage error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs<br>$1_B$ , ERR/EMM will be set for this type of error (default)  |
| <b>M_CELL_UV</b>     | 12   | rw   | <b>EMM/ERR mask for cell undervoltage error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs<br>$1_B$ , ERR/EMM will be set for this type of error (default)   |
| <b>M_INT_OT</b>      | 11   | rw   | <b>EMM/ERR mask for internal temperature error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs (default)<br>$1_B$ , ERR/EMM will be set for this type of error  |
| <b>M_EXT_OT</b>      | 10   | rw   | <b>EMM/ERR mask for external temperature error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs<br>$1_B$ , ERR/EMM will be set for this type of error (default)  |
| <b>M_REG_CRC_ERR</b> | 9    | rw   | <b>EMM/ERR mask for register CRC error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs (default)<br>$1_B$ , ERR/EMM will be set for this type of error  |
| <b>M_INT_IC_ERR</b>  | 8    | rw   | <b>EMM/ERR mask for internal IC error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs (default)<br>$1_B$ , ERR/EMM will be set for this type of error   |
| <b>M_OL_ERR</b>      | 7    | rw   | <b>EMM/ERR mask for openload error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs (default)<br>$1_B$ , ERR/EMM will be set for this type of error  |
| <b>M_ADC_ERR</b>     | 6    | rw   | <b>EMM/ERR mask for ADC error</b><br>$0_B$ , ERR/EMM will NOT be set if this type of error occurs (default)<br>$1_B$ , ERR/EMM will be set for this type of error   |
| <b>ERR_PIN</b>       | 5    | rw   | <b>Enable Error PIN functionality</b><br>$0_B$ , ERR pin deactivated, EMM signal over iso UART active. Device goes back to the mode as it was before the EMM. (default)<br>$1_B$ , ERR Pin function enabled. Fault indication only via ERR Pin. EMM signal over iso UART deactivated. If ERR PIN triggered, pin stays high (device is then in normal mode) until watchdog runs out or pin is cleared. |
| <b>RES</b>           | 4:0  | rwh  | <b>Reserved for future use</b><br>$00000_B$ , not defined (default)   |

## GEN\_DIAG

| GEN_DIAG                              | Offset | Reset Value |
|---------------------------------------|--------|-------------|
| General diagnosis (supplied in sleep) | $0B_H$ | $0000_H$    |

## Registers

|       |       |       |       |       |       |       |       |       |       |       |      |      |      |      |      |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|
| 15    | 14    | 13    | 12    | 11    | 10    | 9     | 8     | 7     | 6     | 5     | 4    | 3    | 2    | 1    | 0    |
| BAL*  | BAL*  | CEL*  | CEL*  | INT*  | EXT*  | REG*  | INT*  | OL_*  | ADC*  | UV_*  | RR_* | LOC* | BAL* | MOT* | GPI* |
| rocwl | rocwl | rocwl | rocwl | rocwl | rocwl | rocwl | rocwl | rocwl | rocwl | rocwl | rh   | rh   | rh   | rh   | rh   |

| Field              | Bits | Type  | Description   |
|--------------------|------|-------|---|
| <b>BAL_ERR_OC</b>  | 15   | rocwl | <b>Balancing error overcurrent (will be reset in sleep mode)</b><br>Please Note: Resetting the error here resets also the respective detailed error register<br>0 <sub>B</sub> , no balancing error. (default)<br>1 <sub>B</sub> , balancing error occurred. Detailed information in the respective error register                  |
| <b>BAL_ERR_UC</b>  | 14   | rocwl | <b>Balancing error undercurrent (will be reset in sleep mode)</b><br>Please Note: Resetting the error here resets also the respective detailed error register<br>0 <sub>B</sub> , no balancing error (default)<br>1 <sub>B</sub> , balancing error occurred. Detailed information in the respective error register                  |
| <b>CELL_OV</b>     | 13   | rocwl | <b>Cell overvoltage (OV) error</b><br>Please Note: Resetting the error here resets also the respective detailed error register<br>0 <sub>B</sub> , no OV error (default)<br>1 <sub>B</sub> , OV error occurred. Detailed information in the respective error register   |
| <b>CELL_UV</b>     | 12   | rocwl | <b>Cell undervoltage (UV) error</b><br>Please Note: Resetting the error here resets also the respective detailed error register<br>0 <sub>B</sub> , no UV error (default)<br>1 <sub>B</sub> , UV error occurred. Detailed information in the respective error register  |
| <b>INT_OT</b>      | 11   | rocwl | <b>Internal temperature (OT) error</b><br>0 <sub>B</sub> , no internal OT error (default)<br>1 <sub>B</sub> , internal OT error occurred. Balancing is deactivated.   |
| <b>EXT_OT</b>      | 10   | rocwl | <b>External temperature error</b><br>Please Note: Resetting the error here resets also the respective detailed error register<br>0 <sub>B</sub> , no external OT/OL/Short error (default)<br>1 <sub>B</sub> , external OT/OL/Short error occurred. Detailed information in the respective error register. Balancing is deactivated. |
| <b>REG_CRC_ERR</b> | 9    | rocwl | <b>Register CRC error</b><br>Please Note: Resetting the error here resets also the respective detailed error register<br>0 <sub>B</sub> , no CRC check error (default)<br>1 <sub>B</sub> , CRC check error occurred. Detailed information in the respective error register. Balancing is deactivated.                               |



## Registers

| Field       | Bits | Type  | Description   |
|-------------|------|-------|---|
| INT_IC_ERR  | 8    | rocw  | <b>Internal IC error</b><br>0 <sub>B</sub> , no internal error (default)<br>1 <sub>B</sub> , internal IC check error occurred. Balancing is deactivated.  |
| OL_ERR      | 7    | rocwl | <b>Openload error</b><br>Please Note: Resetting the error here resets also the respective detailed error register<br>0 <sub>B</sub> , no openload error (default)<br>1 <sub>B</sub> , openload error occurred. Detailed information in the respective error register. Balancing is deactivated. |
| ADC_ERR     | 6    | rocw  | <b>ADC Error</b><br>0 <sub>B</sub> , no ADC mismatch between sum of CVM and BVM (default)<br>1 <sub>B</sub> , ERROR of ADC-result comparison. Balancing is deactivated.   |
| UV_SLEEP    | 5    | rocw  | <b>Undervoltage induced sleep</b><br>0 <sub>B</sub> , no UV induced sleep (default)<br>1 <sub>B</sub> , UV induced sleep occurred   |
| RR_ACTIVE   | 4    | rh    | <b>Round Robin active</b><br>This bit indicates if the Round Robin scheduler was active during read.<br>0 <sub>B</sub> , no Round Robin active (default)<br>1 <sub>B</sub> , Round Robin active   |
| LOCK_MEAS   | 3    | rh    | <b>Lock measurement</b><br>This bit indicates an ongoing CVM, BVM or AVM or a delayed RR.<br>0 <sub>B</sub> , no measurement ongoing (default)<br>1 <sub>B</sub> , CVM, BVM or AVM measurement ongoing  |
| BAL_ACTIVE  | 2    | rh    | <b>Balancing active</b><br>0 <sub>B</sub> , no balancing ongoing (default)<br>1 <sub>B</sub> , balancing ongoing, at least one channel is ON  |
| MOT_MOB_N   | 1    | rh    | <b>Master on Top/Bottom configuration</b><br>0 <sub>B</sub> , configured as master on bottom (default)<br>1 <sub>B</sub> , configured as master on top  |
| GPIO_WAKEUP | 0    | rh    | <b>Wake-up via GPIO</b><br>0 <sub>B</sub> , wake-up via iso UART (default)<br>1 <sub>B</sub> , wake-up via GPIO   |

## CELL\_UV

| CELL_UV  | Offset          | Reset Value       |
|--|-----------------|-------------------|
| Cell voltage supervision warning flags UV<br>(supplied in sleep) | 0C <sub>H</sub> | 0000 <sub>H</sub> |

|     |      |      |      |      |      |      |      |      |      |      |      |      |      |
|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 15  | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| RES | UV_* | UV_* | UV_9 | UV_8 | UV_7 | UV_6 | UV_5 | UV_4 | UV_3 | UV_2 | UV_1 | UV_0 |      |
| rwh | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw |

## Registers

| Field        | Bits  | Type | Description   |
|--------------|-------|------|---|
| <b>RES</b>   | 15:12 | rwh  | <b>Reserved for future use</b><br>0000 <sub>B</sub> , not defined (default)   |
| <b>UV_11</b> | 11    | rocw | <b>Undervoltage in cell 11</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 11 (default)<br>1 <sub>B</sub> , undervoltage in cell 11. Balancing is deactivated for this cell. |
| <b>UV_10</b> | 10    | rocw | <b>Undervoltage in cell 10</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 10 (default)<br>1 <sub>B</sub> , undervoltage in cell 10. Balancing is deactivated for this cell. |
| <b>UV_9</b>  | 9     | rocw | <b>Undervoltage in cell 9</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 9 (default)<br>1 <sub>B</sub> , undervoltage in cell 9. Balancing is deactivated for this cell.    |
| <b>UV_8</b>  | 8     | rocw | <b>Undervoltage in cell 8</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 8 (default)<br>1 <sub>B</sub> , undervoltage in cell 8. Balancing is deactivated for this cell.    |
| <b>UV_7</b>  | 7     | rocw | <b>Undervoltage in cell 7</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 7 (default)<br>1 <sub>B</sub> , undervoltage in cell 7. Balancing is deactivated for this cell.    |
| <b>UV_6</b>  | 6     | rocw | <b>Undervoltage in cell 6</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 6 (default)<br>1 <sub>B</sub> , undervoltage in cell 6. Balancing is deactivated for this cell.    |
| <b>UV_5</b>  | 5     | rocw | <b>Undervoltage in cell 5</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 5 (default)<br>1 <sub>B</sub> , undervoltage in cell 5. Balancing is deactivated for this cell.    |
| <b>UV_4</b>  | 4     | rocw | <b>Undervoltage in cell 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 4 (default)<br>1 <sub>B</sub> , undervoltage in cell 4. Balancing is deactivated for this cell.    |
| <b>UV_3</b>  | 3     | rocw | <b>Undervoltage in cell 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 3 (default)<br>1 <sub>B</sub> , undervoltage in cell 3. Balancing is deactivated for this cell.    |
| <b>UV_2</b>  | 2     | rocw | <b>Undervoltage in cell 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no undervoltage in cell 2 (default)<br>1 <sub>B</sub> , undervoltage in cell 2. Balancing is deactivated for this cell.    |

## Registers

| Field       | Bits | Type | Description   |
|-------------|------|------|---|
| <b>UV_1</b> | 1    | rocw | <b>Undervoltage in cell 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit 0 <sub>B</sub> , no undervoltage in cell 1 (default)<br>1 <sub>B</sub> , undervoltage in cell 1. Balancing is deactivated for this cell. |
| <b>UV_0</b> | 0    | rocw | <b>Undervoltage in cell 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit 0 <sub>B</sub> , no undervoltage in cell 0 (default)<br>1 <sub>B</sub> , undervoltage in cell 0. Balancing is deactivated for this cell. |

## CELL\_OV

| CELL_OV  | Offset          | Reset Value       |
|--|-----------------|-------------------|
| Cell voltage supervision warning flags OV<br>(supplied in sleep) | 0D <sub>H</sub> | 0000 <sub>H</sub> |

|     |    |      |      |      |      |      |      |      |      |      |      |      |      |
|-----|----|------|------|------|------|------|------|------|------|------|------|------|------|
| 15  | 12 | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| RES |    | OV_* | OV_* | OV_9 | OV_8 | OV_7 | OV_6 | OV_5 | OV_4 | OV_3 | OV_2 | OV_1 | OV_0 |
| rwh |    | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw |

| Field        | Bits  | Type | Description   |
|--------------|-------|------|---|
| <b>RES</b>   | 15:12 | rwh  | <b>Reserved for future use</b><br>0000 <sub>B</sub> , not defined (default)   |
| <b>OV_11</b> | 11    | rocw | <b>Overvoltage in cell 11</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit 0 <sub>B</sub> , no overvoltage in cell 11 (default)<br>1 <sub>B</sub> , overvoltage in cell 11. Balancing is deactivated for this cell. |
| <b>OV_10</b> | 10    | rocw | <b>Overvoltage in cell 10</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit 0 <sub>B</sub> , no overvoltage in cell 10 (default)<br>1 <sub>B</sub> , overvoltage in cell 10. Balancing is deactivated for this cell. |
| <b>OV_9</b>  | 9     | rocw | <b>Overvoltage in cell 9</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit 0 <sub>B</sub> , no overvoltage in cell 9 (default)<br>1 <sub>B</sub> , overvoltage in cell 9. Balancing is deactivated for this cell.    |
| <b>OV_8</b>  | 8     | rocw | <b>Overvoltage in cell 8</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit 0 <sub>B</sub> , no overvoltage in cell 8 (default)<br>1 <sub>B</sub> , overvoltage in cell 8. Balancing is deactivated for this cell.    |
| <b>OV_7</b>  | 7     | rocw | <b>Overvoltage in cell 7</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit 0 <sub>B</sub> , no overvoltage in cell 7 (default)<br>1 <sub>B</sub> , overvoltage in cell 7. Balancing is deactivated for this cell.    |

## Registers

| Field       | Bits | Type | Description   |
|-------------|------|------|---|
| <b>OV_6</b> | 6    | rocw | <b>Overvoltage in cell 6</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overvoltage in cell 6 (default)<br>1 <sub>B</sub> , overvoltage in cell 6. Balancing is deactivated for this cell. |
| <b>OV_5</b> | 5    | rocw | <b>Overvoltage in cell 5</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overvoltage in cell 5 (default)<br>1 <sub>B</sub> , overvoltage in cell 5. Balancing is deactivated for this cell. |
| <b>OV_4</b> | 4    | rocw | <b>Overvoltage in cell 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overvoltage in cell 4 (default)<br>1 <sub>B</sub> , overvoltage in cell 4. Balancing is deactivated for this cell. |
| <b>OV_3</b> | 3    | rocw | <b>Overvoltage in cell 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overvoltage in cell 3 (default)<br>1 <sub>B</sub> , overvoltage in cell 3. Balancing is deactivated for this cell. |
| <b>OV_2</b> | 2    | rocw | <b>Overvoltage in cell 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overvoltage in cell 2 (default)<br>1 <sub>B</sub> , overvoltage in cell 2. Balancing is deactivated for this cell. |
| <b>OV_1</b> | 1    | rocw | <b>Overvoltage in cell 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overvoltage in cell 1 (default)<br>1 <sub>B</sub> , overvoltage in cell 1. Balancing is deactivated for this cell. |
| <b>OV_0</b> | 0    | rocw | <b>Overvoltage in cell 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overvoltage in cell 0 (default)<br>1 <sub>B</sub> , overvoltage in cell 0. Balancing is deactivated for this cell. |

## EXT\_TEMP\_DIAG

| EXT_TEMP_DIAG   | Offset                | Reset Value             |
|---|-----------------------|-------------------------|
| <b>External overtemperature warning flags<br/>(supplied in sleep)</b> | <b>0E<sub>H</sub></b> | <b>0000<sub>H</sub></b> |

| 15         | 14          | 13          | 12          | 11          | 10          | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| <b>RES</b> | <b>OT_4</b> | <b>SHO*</b> | <b>OPE*</b> | <b>OT_3</b> | <b>SHO*</b> | <b>OPE*</b> | <b>OT_2</b> | <b>SHO*</b> | <b>OPE*</b> | <b>OT_1</b> | <b>SHO*</b> | <b>OPE*</b> | <b>OT_0</b> | <b>SHO*</b> | <b>OPE*</b> |
| rwh        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        | rocw        |

| Field      | Bits | Type | Description   |
|------------|------|------|---|
| <b>RES</b> | 15   | rwh  | <b>Reserved for future use</b><br>0000 <sub>B</sub> , not defined (default) |

## Registers

| Field          | Bits | Type | Description   |
|----------------|------|------|---|
| <b>OT_4</b>    | 14   | rocw | <b>Overtemperature in ext. temp 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overtemperature in ext. temp 4 (default)<br>1 <sub>B</sub> , ADC conversion of ext. temp 4 measurement < overtemperature threshold EXT_OT_THR |
| <b>SHORT_4</b> | 13   | rocw | <b>Short in ext. temp 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no short in ext. temp 4 (default)<br>1 <sub>B</sub> , short in ext. temp 4   |
| <b>OPEN_4</b>  | 12   | rocw | <b>Openload in ext. temp 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload in ext. temp 4 (default)<br>1 <sub>B</sub> , openload in ext. temp 4  |
| <b>OT_3</b>    | 11   | rocw | <b>Overtemperature in ext. temp 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overtemperature in ext. temp 3 (default)<br>1 <sub>B</sub> , ADC conversion of ext. temp 3 measurement < overtemperature threshold EXT_OT_THR |
| <b>SHORT_3</b> | 10   | rocw | <b>Short in ext. temp 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no short in ext. temp 3 (default)<br>1 <sub>B</sub> , short in ext. temp 3   |
| <b>OPEN_3</b>  | 9    | rocw | <b>Openload in ext. temp 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload in ext. temp 3 (default)<br>1 <sub>B</sub> , openload in ext. temp 3  |
| <b>OT_2</b>    | 8    | rocw | <b>Overtemperature in ext. temp 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overtemperature in ext. temp 2 (default)<br>1 <sub>B</sub> , ADC conversion of ext. temp 2 measurement < overtemperature threshold EXT_OT_THR |
| <b>SHORT_2</b> | 7    | rocw | <b>Short in ext. temp 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no short in ext. temp 2 (default)<br>1 <sub>B</sub> , short in ext. temp 2   |
| <b>OPEN_2</b>  | 6    | rocw | <b>Openload in ext. temp 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload in ext. temp 2 (default)<br>1 <sub>B</sub> , openload in ext. temp 2  |
| <b>OT_1</b>    | 5    | rocw | <b>Overtemperature in ext. temp 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overtemperature in ext. temp 1 (default)<br>1 <sub>B</sub> , ADC conversion of ext. temp 1 measurement < overtemperature threshold EXT_OT_THR |

## Registers

| Field          | Bits | Type | Description   |
|----------------|------|------|---|
| <b>SHORT_1</b> | 4    | rocw | <b>Short in ext. temp 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no short in ext. temp 1 (default)<br>1 <sub>B</sub> , short in ext. temp 1   |
| <b>OPEN_1</b>  | 3    | rocw | <b>Openload in ext. temp 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload in ext. temp 1 (default)<br>1 <sub>B</sub> , openload in ext. temp 1  |
| <b>OT_0</b>    | 2    | rocw | <b>Overtemperature in ext. temp 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no overtemperature in ext. temp 0 (default)<br>1 <sub>B</sub> , ADC conversion of ext. temp 0 measurement < overtemperature threshold EXT_OT_THR |
| <b>SHORT_0</b> | 1    | rocw | <b>Short in ext. temp 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no short in ext. temp 0 (default)<br>1 <sub>B</sub> , short in ext. temp 0   |
| <b>OPEN_0</b>  | 0    | rocw | <b>Openload in ext. temp 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload in ext. temp 0 (default)<br>1 <sub>B</sub> , openload in ext. temp 0  |

## DIAG\_OL

| DIAG_OL                                | Offset          | Reset Value       |
|--|-----------------|-------------------|
| Diagnosis OPENLOAD (supplied in sleep) | 10 <sub>H</sub> | 0000 <sub>H</sub> |

|    |     |    |      |      |      |      |      |      |      |      |      |      |      |      |
|----|-----|----|------|------|------|------|------|------|------|------|------|------|------|------|
| 15 |     | 12 | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|    | RES |    | OL_* | OL_* | OL_9 | OL_8 | OL_7 | OL_6 | OL_5 | OL_4 | OL_3 | OL_2 | OL_1 | OL_0 |
|    | rwh |    | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw |

| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| <b>RES</b>   | 15:12 | rwh  | <b>Reserved for future use</b><br>0000 <sub>B</sub> , not defined (default)  |
| <b>OL_11</b> | 11    | rocw | <b>Openload in cell 11</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_10</b> | 10    | rocw | <b>Openload in cell 10</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |

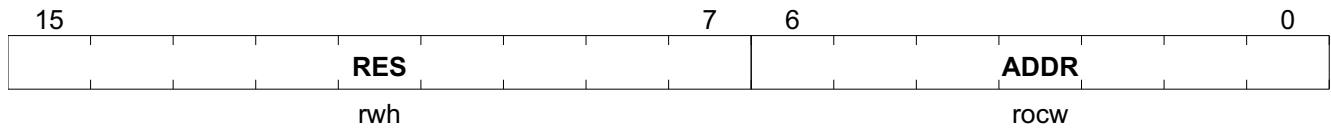
## Registers

| Field       | Bits | Type | Description   |
|-------------|------|------|---|
| <b>OL_9</b> | 9    | rocw | <b>Openload in cell 9</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_8</b> | 8    | rocw | <b>Openload in cell 8</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_7</b> | 7    | rocw | <b>Openload in cell 7</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_6</b> | 6    | rocw | <b>Openload in cell 6</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_5</b> | 5    | rocw | <b>Openload in cell 5</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_4</b> | 4    | rocw | <b>Openload in cell 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_3</b> | 3    | rocw | <b>Openload in cell 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_2</b> | 2    | rocw | <b>Openload in cell 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_1</b> | 1    | rocw | <b>Openload in cell 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |
| <b>OL_0</b> | 0    | rocw | <b>Openload in cell 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no openload detected in respective channel (default)<br>1 <sub>B</sub> , openload detected in respective channel |

## REG\_CRC\_ERR

### Reset Value

0000<sub>H</sub>



| Field       | Bits | Type | Description   |
|-------------|------|------|---|
| <b>RES</b>  | 15:7 | rwh  | <b>Reserved for future use</b><br>0 0000 0000 <sub>B</sub> , not defined (default)  |
| <b>ADDR</b> | 6:0  | rocw | <b>Register Address of register where CRC check failed</b><br>Register address of CRC check fail, Can also be cleared on write '0' to connected GEN_DIAG register bit<br>000 0000 <sub>B</sub> , Register address (default) |

**OP\_MODE**

### Reset Value

0000<sub>H</sub>

| Field  | Bits | Type | Description   |
|--------|------|------|---|
| RES    | 15:2 | rwh  | <b>Reserved for future use</b><br>0000 <sub>H</sub> , not defined (default)   |
| EXT_WD | 1    | rw   | <b>Extended watchdog</b><br>0 <sub>B</sub> , no extended watchdog (default)<br>1 <sub>B</sub> , extended watchdog active  |
| PD     | 0    | rw   | <b>Activate sleep mode</b><br>0 <sub>B</sub> , chip operating in normal mode (default)<br>1 <sub>B</sub> , chip is set to sleep mode. No further communication possible after bit is set to '1' |

**BAL\_CURR\_THR**

### Reset Value

00AC<sub>H</sub>



Diagram illustrating the structure of the UC\_CTL register fields:

- UC\_THR**: 7 bits (bits 15 to 8), read-write (rw).
- OC\_THR**: 8 bits (bits 7 to 0), read-write (rw).

## Registers

| Field       | Bits | Type | Description   |
|-------------|------|------|---|
| <b>ON_6</b> | 6    | rwh  | <b>Switching state of balancing driver 6</b><br>$0_B$ , respective balancing switch off (default)<br>$1_B$ , respective balancing switch on |
| <b>ON_5</b> | 5    | rwh  | <b>Switching state of balancing driver 5</b><br>$0_B$ , respective balancing switch off (default)<br>$1_B$ , respective balancing switch on |
| <b>ON_4</b> | 4    | rwh  | <b>Switching state of balancing driver 4</b><br>$0_B$ , respective balancing switch off (default)<br>$1_B$ , respective balancing switch on |
| <b>ON_3</b> | 3    | rwh  | <b>Switching state of balancing driver 3</b><br>$0_B$ , respective balancing switch off (default)<br>$1_B$ , respective balancing switch on |
| <b>ON_2</b> | 2    | rwh  | <b>Switching state of balancing driver 2</b><br>$0_B$ , respective balancing switch off (default)<br>$1_B$ , respective balancing switch on |
| <b>ON_1</b> | 1    | rwh  | <b>Switching state of balancing driver 1</b><br>$0_B$ , respective balancing switch off (default)<br>$1_B$ , respective balancing switch on |
| <b>ON_0</b> | 0    | rwh  | <b>Switching state of balancing driver 0</b><br>$0_B$ , respective balancing switch off (default)<br>$1_B$ , respective balancing switch on |

## AVM\_CONFIG

| AVM_CONFIG   | Offset                | Reset Value             |
|--|-----------------------|-------------------------|
| <b>Auxiliary Voltage Measurement Configuration</b> | <b>17<sub>H</sub></b> | <b>0007<sub>H</sub></b> |

|    |  |            |  |    |             |            |             |             |             |             |             |                   |  |   |
|----|--|------------|--|----|-------------|------------|-------------|-------------|-------------|-------------|-------------|-------------------|--|---|
| 15 |  |            |  | 10 | 9           | 8          | 7           | 6           | 5           | 4           | 3           | 2                 |  | 0 |
|    |  | <b>RES</b> |  |    | <b>R_D*</b> | <b>RES</b> | <b>AVM*</b> | <b>AVM*</b> | <b>AVM*</b> | <b>AVM*</b> | <b>AVM*</b> | <b>TEMP_MUX_*</b> |  |   |
|    |  | rwh        |  |    | rw          | rwh        | rw          | rw          | rw          | rw          | rw          | rw                |  |   |

| Field         | Bits  | Type | Description   |
|---------------|-------|------|---|
| <b>RES</b>    | 15:10 | rwh  | <b>Reserved for future use</b><br>0000 00 <sub>B</sub> , not defined (default)  |
| <b>R_DIAG</b> | 9     | rw   | <b>Masking diagnosis resistor as part of AVM</b><br>$0_B$ , manual AVM diagnosis resistor measurement masked out when AVM_START bit triggered (default)<br>$1_B$ , manual AVM diagnosis resistor measurement performed when AVM_START bit triggered |
| <b>RES</b>    | 8     | rwh  | <b>Reserved for future use</b><br>$0_B$ , not defined (default)   |

## Registers

| Field                    | Bits | Type | Description  |
|--------------------------|------|------|--|
| <b>AVM_TMP4_MASK</b>     | 7    | rw   | <b>Masking auxiliary measurement via deactive TMP 4 as part of AVM</b><br>$0_B$ , manual AVM TMP4 measurement masked out when AVM_START bit triggered (default)<br>$1_B$ , manual AVM TMP4 measurement performed when AVM_START bit triggered  |
| <b>AVM_TMP3_MASK</b>     | 6    | rw   | <b>Masking auxiliary measurement via deactive TMP 3 as part of AVM</b><br>$0_B$ , manual AVM TMP3 measurement masked out when AVM_START bit triggered (default)<br>$1_B$ , manual AVM TMP3 measurement performed when AVM_START bit triggered  |
| <b>AVM_TMP2_MASK</b>     | 5    | rw   | <b>Masking auxiliary measurement via deactive TMP 2 as part of AVM</b><br>$0_B$ , manual AVM TMP2 measurement masked out when AVM_START bit triggered (default)<br>$1_B$ , manual AVM TMP2 measurement performed when AVM_START bit triggered  |
| <b>AVM_TMP1_MASK</b>     | 4    | rw   | <b>Masking auxiliary measurement via deactive TMP 1 as part of AVM</b><br>$0_B$ , manual AVM TMP1 measurement masked out when AVM_START bit triggered (default)<br>$1_B$ , manual AVM TMP1 measurement performed when AVM_START bit triggered  |
| <b>AVM_TMP0_MASK</b>     | 3    | rw   | <b>Masking auxiliary measurement via deactive TMP 0 as part of AVM</b><br>$0_B$ , manual AVM TMP0 measurement masked out when AVM_START bit triggered (default)<br>$1_B$ , manual AVM TMP0 measurement performed when AVM_START bit triggered  |
| <b>TEMP_MUX_DIAG_SEL</b> | 2:0  | rw   | <b>Selector for ext. temp diagnose</b><br>$000_B$ , pull-down for ext. temp 0 measurement is active<br>$001_B$ , pull-down for ext. temp 1 measurement is active<br>$010_B$ , pull-down for ext. temp 2 measurement is active<br>$011_B$ , pull-down for ext. temp 3 measurement is active<br>$100_B$ , pull-down for ext. temp 4 measurement is active<br>$111_B$ , No pull-down active (default) |

## MEAS\_CTRL

|                            |                       |                         |
|----------------------------|-----------------------|-------------------------|
| <b>MEAS_CTRL</b>           | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Measurement control</b> | <b>18<sub>H</sub></b> | <b>0021<sub>H</sub></b> |

## Registers

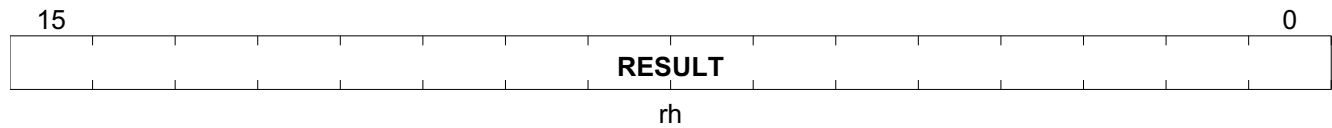
|      |            |      |            |      |     |      |   |   |         |   |
|------|------------|------|------------|------|-----|------|---|---|---------|---|
| 15   | 14         | 12   | 11         | 10   | 8   | 7    | 6 | 5 | 4       | 0 |
| CVM* | CVM_BIT_W* | BVM* | BVM_BIT_W* | AVM* | RES | PBO* |   |   | CVM_DEL |   |
| rwh  | rw         | rwh  | rw         | rwh  | rwh | rw   |   |   | rw      |   |

| Field         | Bits  | Type | Description   |
|---------------|-------|------|---|
| CVM_START     | 15    | rwh  | <b>Start cell voltage measurement</b><br>Bit cleared if conversion done<br>0 <sub>B</sub> , no measurement ongoing (default)<br>1 <sub>B</sub> , trigger measurement  |
| CVM_BIT_WIDTH | 14:12 | rw   | <b>Bit width of cell voltage measurement</b><br>0 <sub>B</sub> , 10 bit (default)<br>1 <sub>B</sub> , 11 bit<br>110 <sub>B</sub> , 16 bit   |
| BVM_START     | 11    | rwh  | <b>Start block voltage measurement</b><br>Bit cleared if conversion done<br>0 <sub>B</sub> , no measurement ongoing (default)<br>1 <sub>B</sub> , trigger measurement   |
| BVM_BIT_WIDTH | 10:8  | rw   | <b>Bit width of block voltage measurement</b><br>0 <sub>B</sub> , 10 bit (default)<br>1 <sub>B</sub> , 11 bit<br>110 <sub>B</sub> , 16 bit  |
| AVM_START     | 7     | rwh  | <b>Start auxiliary voltage measurement</b><br>Bit cleared if conversion done<br>0 <sub>B</sub> , no measurement ongoing (default)<br>1 <sub>B</sub> , trigger measurement, if BVM_START=0                             |
| RES           | 6     | rwh  | <b>Reserved for future use</b><br>0 <sub>B</sub> , not defined (default)  |
| PBOFF         | 5     | rw   | <b>Enable PBOFF time</b><br>0 <sub>B</sub> , keep balancing state for CVM / BVM<br>1 <sub>B</sub> , switch off balancing before conversion starts (default)   |
| CVM_DEL       | 4:0   | rw   | <b>CVM delay timer</b><br>Wait for CVM_DEL before CVM and/or BVM is started<br>0 <sub>B</sub> , no settling time<br>1 <sub>B</sub> , $t_{CVM\_del\_LSB}$ (default)<br>11111 <sub>B</sub> , $\times t_{CVM\_del\_LSB}$ |

## CVM\_0

| CVM_0                      | Offset          | Reset Value       |
|----------------------------|-----------------|-------------------|
| Cell voltage measurement 0 | 19 <sub>H</sub> | 0000 <sub>H</sub> |

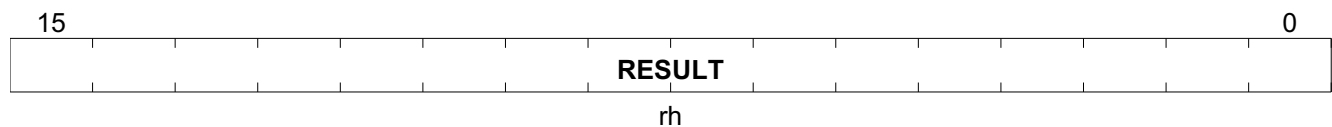
## Registers



| Field         | Bits | Type | Description  |
|---------------|------|------|--|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 0</b><br><br>0000 <sub>H</sub> , default |

### CVM\_1

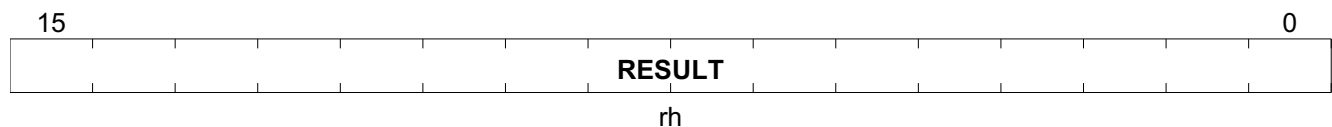
|                                   |                       |                         |
|-----------------------------------|-----------------------|-------------------------|
| <b>CVM_1</b>                      | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Cell voltage measurement 1</b> | <b>1A<sub>H</sub></b> | <b>0000<sub>H</sub></b> |



| Field         | Bits | Type | Description  |
|---------------|------|------|--|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 1</b><br><br>0000 <sub>H</sub> , default |

### CVM\_2

|                                   |                       |                         |
|-----------------------------------|-----------------------|-------------------------|
| <b>CVM_2</b>                      | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Cell voltage measurement 2</b> | <b>1B<sub>H</sub></b> | <b>0000<sub>H</sub></b> |

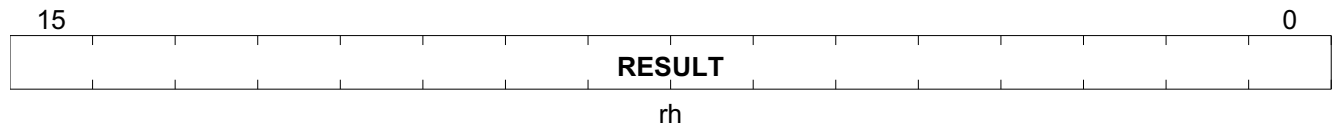


| Field         | Bits | Type | Description  |
|---------------|------|------|--|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 2</b><br><br>0000 <sub>H</sub> , default |

### CVM\_3

## Registers

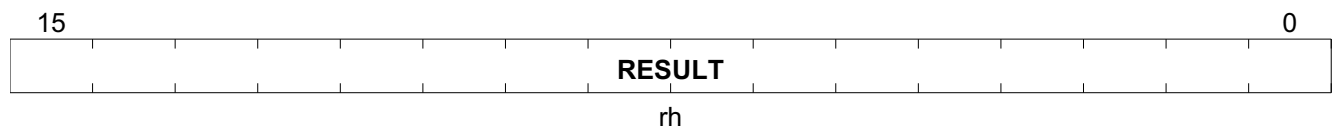
**CVM\_3** **Offset** **Reset Value**  
**Cell voltage measurement 3** **1C<sub>H</sub>** **0000<sub>H</sub>**



| Field  | Bits | Type | Description   |
|--------|------|------|---|
| RESULT | 15:0 | rh   | Result of cell voltage measurement 3<br>0000 <sub>H</sub> , default |

## CVM\_4

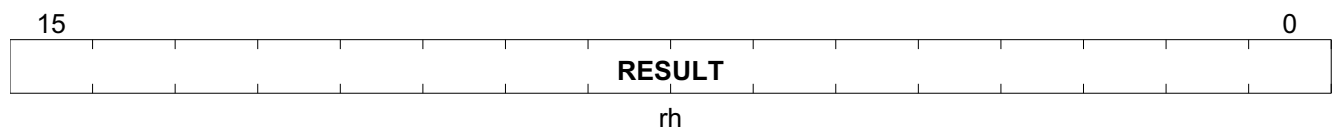
**CVM\_4** **Offset** **Reset Value**  
**Cell voltage measurement 4** **1D<sub>H</sub>** **0000<sub>H</sub>**



| Field  | Bits | Type | Description   |
|--------|------|------|---|
| RESULT | 15:0 | rh   | Result of cell voltage measurement 4<br>0000 <sub>H</sub> , default |

## CVM\_5

**CVM\_5** **Offset** **Reset Value**  
**Cell voltage measurement 5** **1E<sub>H</sub>** **0000<sub>H</sub>**

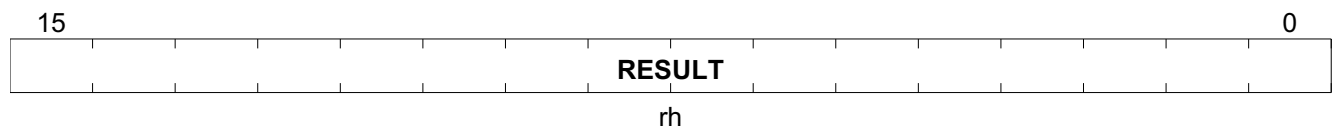


| Field  | Bits | Type | Description   |
|--------|------|------|---|
| RESULT | 15:0 | rh   | Result of cell voltage measurement 5<br>0000 <sub>H</sub> , default |

## Registers

### CVM\_6

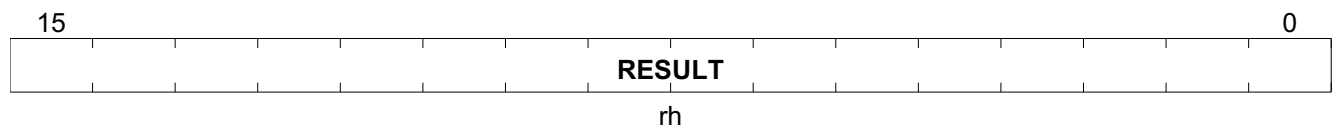
**CVM\_6** **Offset** **Reset Value**  
**Cell voltage measurement 6** **1F<sub>H</sub>** **0000<sub>H</sub>**



| Field         | Bits | Type | Description  |
|---------------|------|------|--|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 6</b><br><br>0000 <sub>H</sub> , default |

### CVM\_7

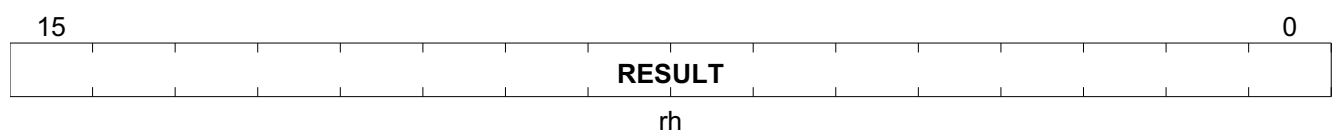
**CVM\_7** **Offset** **Reset Value**  
**Cell voltage measurement 7** **20<sub>H</sub>** **0000<sub>H</sub>**



| Field         | Bits | Type | Description  |
|---------------|------|------|--|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 7</b><br><br>0000 <sub>H</sub> , default |

### CVM\_8

**CVM\_8** **Offset** **Reset Value**  
**Cell voltage measurement 8** **21<sub>H</sub>** **0000<sub>H</sub>**

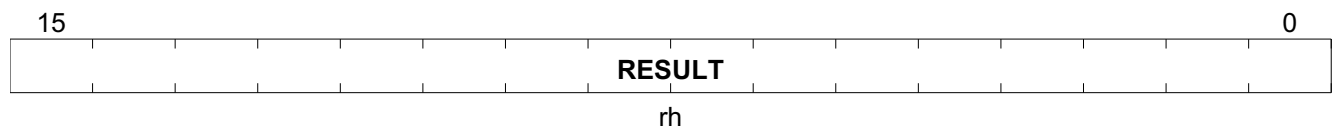


## Registers

| Field         | Bits | Type | Description  |
|---------------|------|------|--|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 8</b><br><br>0000 <sub>H</sub> , default |

### CVM\_9

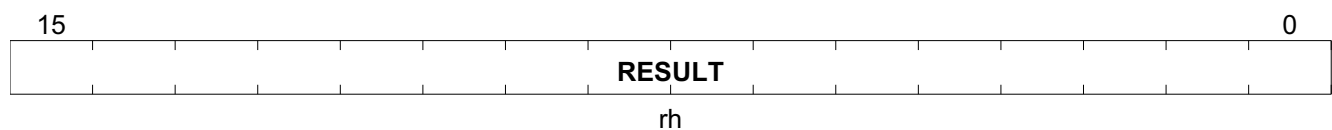
|                                   |                       |                         |
|-----------------------------------|-----------------------|-------------------------|
| <b>CVM_9</b>                      | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Cell voltage measurement 9</b> | <b>22<sub>H</sub></b> | <b>0000<sub>H</sub></b> |



| Field         | Bits | Type | Description  |
|---------------|------|------|--|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 9</b><br><br>0000 <sub>H</sub> , default |

### CVM\_10

|                                    |                       |                         |
|------------------------------------|-----------------------|-------------------------|
| <b>CVM_10</b>                      | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Cell voltage measurement 10</b> | <b>23<sub>H</sub></b> | <b>0000<sub>H</sub></b> |



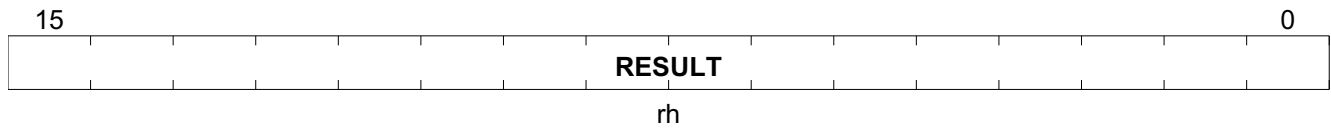
| Field         | Bits | Type | Description   |
|---------------|------|------|---|
| <b>RESULT</b> | 15:0 | rh   | <b>Result of cell voltage measurement 10</b><br><br>0000 <sub>H</sub> , default |

### CVM\_11

|                                    |                       |                         |
|------------------------------------|-----------------------|-------------------------|
| <b>CVM_11</b>                      | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Cell voltage measurement 11</b> | <b>24<sub>H</sub></b> | <b>0000<sub>H</sub></b> |



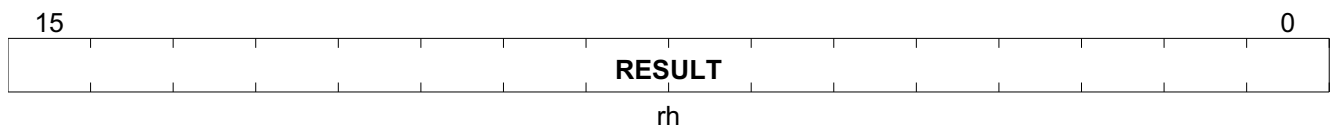
## Registers



| Field  | Bits | Type | Description  |
|--------|------|------|--|
| RESULT | 15:0 | rh   | Result of cell voltage measurement 11<br><br>0000 <sub>H</sub> , default |

### BVM

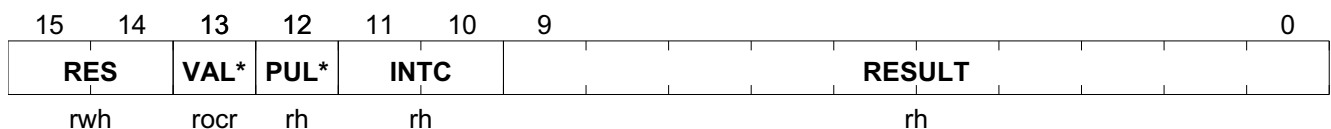
|                           |                 |                    |
|---------------------------|-----------------|--------------------|
| <b>BVM</b>                | <b>Offset</b>   | <b>Reset Value</b> |
| Block voltage measurement | 28 <sub>H</sub> | 0000 <sub>H</sub>  |



| Field  | Bits | Type | Description  |
|--------|------|------|--|
| RESULT | 15:0 | rh   | Result of block voltage measurement<br><br>0000 <sub>H</sub> , default |

### EXT\_TEMP\_0

|                   |                 |                    |
|-------------------|-----------------|--------------------|
| <b>EXT_TEMP_0</b> | <b>Offset</b>   | <b>Reset Value</b> |
| Temp result 0     | 29 <sub>H</sub> | 0000 <sub>H</sub>  |



| Field | Bits  | Type | Description  |
|-------|-------|------|--|
| RES   | 15:14 | rwh  | Reserved for future use<br>00 <sub>B</sub> , not defined (default)   |
| VALID | 13    | rocr | Indicating a valid result<br>0 <sub>B</sub> , no new result available (default)<br>1 <sub>B</sub> , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_0 register |

## Registers

| Field           | Bits  | Type | Description   |
|-----------------|-------|------|---|
| <b>PULLDOWN</b> | 12    | rh   | <b>Indicating pull-down switch state</b><br>0 <sub>B</sub> , normal measurement done (default)<br>1 <sub>B</sub> , pull-down for Mux-test was active during conversion  |
| <b>INTC</b>     | 11:10 | rh   | <b>Indicates which current source was used</b><br>number of current source that was active for latest measurement<br>00 <sub>B</sub> , source $I_{TMP0\_0}$ used (default)<br>01 <sub>B</sub> , source $I_{TMP0\_1}$ used<br>10 <sub>B</sub> , source $I_{TMP0\_2}$ used<br>11 <sub>B</sub> , source $I_{TMP0\_3}$ used |
| <b>RESULT</b>   | 9:0   | rh   | <b>Result of ext. temp 0 measurement</b><br>SD-ADC result of resistance or voltage measurement.<br>000 <sub>H</sub> , (default)   |

## EXT\_TEMP\_1

|                      |                       |                         |
|----------------------|-----------------------|-------------------------|
| <b>EXT_TEMP_1</b>    | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Temp result 1</b> | <b>2A<sub>H</sub></b> | <b>0000<sub>H</sub></b> |

|            |             |             |             |    |    |   |  |  |  |  |  |  |  |  |               |
|------------|-------------|-------------|-------------|----|----|---|--|--|--|--|--|--|--|--|---------------|
| 15         | 14          | 13          | 12          | 11 | 10 | 9 |  |  |  |  |  |  |  |  | 0             |
| <b>RES</b> | <b>VAL*</b> | <b>PUL*</b> | <b>INTC</b> |    |    |   |  |  |  |  |  |  |  |  | <b>RESULT</b> |
| rwh        | rocr        | rh          | rh          |    |    |   |  |  |  |  |  |  |  |  | rh            |

| Field           | Bits  | Type | Description   |
|-----------------|-------|------|---|
| <b>RES</b>      | 15:14 | rwh  | <b>Reserved for future use</b><br>00 <sub>B</sub> , not defined (default)   |
| <b>VALID</b>    | 13    | rocr | <b>Indicating a valid result</b><br>0 <sub>B</sub> , no new result available<br>1 <sub>B</sub> , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_1 register   |
| <b>PULLDOWN</b> | 12    | rh   | <b>Indicating pull-down switch state</b><br>0 <sub>B</sub> , normal measurement done<br>1 <sub>B</sub> , pull-down for Mux-test was active during conversion  |
| <b>INTC</b>     | 11:10 | rh   | <b>Indicates which current source was used</b><br>Number of current source that was active for latest measurement<br>00 <sub>B</sub> , source $I_{TMP1\_0}$ used (default)<br>01 <sub>B</sub> , source $I_{TMP1\_1}$ used<br>10 <sub>B</sub> , source $I_{TMP1\_2}$ used<br>11 <sub>B</sub> , source $I_{TMP1\_3}$ used |
| <b>RESULT</b>   | 9:0   | rh   | <b>Result of ext. temp 1 measurement</b><br>SD-ADC result of resistance or voltage measurement.<br>000 <sub>H</sub> , default   |

## Registers

### EXT\_TEMP\_2

**EXT\_TEMP\_2** **Offset**  
**Temp result 2** **2B<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**

|            |             |             |             |    |    |   |  |  |  |               |  |  |  |  |   |
|------------|-------------|-------------|-------------|----|----|---|--|--|--|---------------|--|--|--|--|---|
| 15         | 14          | 13          | 12          | 11 | 10 | 9 |  |  |  |               |  |  |  |  | 0 |
| <b>RES</b> | <b>VAL*</b> | <b>PUL*</b> | <b>INTC</b> |    |    |   |  |  |  | <b>RESULT</b> |  |  |  |  |   |
| rwh        | rocr        | rh          | rh          |    |    |   |  |  |  | rh            |  |  |  |  |   |

| Field           | Bits  | Type | Description   |
|-----------------|-------|------|---|
| <b>RES</b>      | 15:14 | rwh  | <b>Reserved for future use</b><br>00 <sub>B</sub> , not defined (default)   |
| <b>VALID</b>    | 13    | rocr | <b>Indicating a valid result</b><br>0 <sub>B</sub> , no new result available<br>1 <sub>B</sub> , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_2 register   |
| <b>PULLDOWN</b> | 12    | rh   | <b>Indicating pull-down switch state</b><br>0 <sub>B</sub> , normal measurement done<br>1 <sub>B</sub> , pull-down for Mux-test was active during conversion  |
| <b>INTC</b>     | 11:10 | rh   | <b>Indicates which current source was used</b><br>Number of current source that was active for latest measurement<br>00 <sub>B</sub> , source I <sub>TMP0_0</sub> used (default)<br>01 <sub>B</sub> , source I <sub>TMP0_1</sub> used<br>10 <sub>B</sub> , source I <sub>TMP0_1</sub> used<br>11 <sub>B</sub> , source I <sub>TMP0_3</sub> used |
| <b>RESULT</b>   | 9:0   | rh   | <b>Result of ext. temp 2 measurement</b><br>SD-ADC result of resistance or voltage measurement.<br>000 <sub>H</sub> , default   |

### EXT\_TEMP\_3

**EXT\_TEMP\_3** **Offset**  
**Temp result 3** **2C<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**

|            |             |             |             |    |    |   |  |  |  |               |  |  |  |  |   |
|------------|-------------|-------------|-------------|----|----|---|--|--|--|---------------|--|--|--|--|---|
| 15         | 14          | 13          | 12          | 11 | 10 | 9 |  |  |  |               |  |  |  |  | 0 |
| <b>RES</b> | <b>VAL*</b> | <b>PUL*</b> | <b>INTC</b> |    |    |   |  |  |  | <b>RESULT</b> |  |  |  |  |   |
| rwh        | rocr        | rh          | rh          |    |    |   |  |  |  | rh            |  |  |  |  |   |

| Field      | Bits  | Type | Description   |
|------------|-------|------|---|
| <b>RES</b> | 15:14 | rwh  | <b>Reserved for future use</b><br>00 <sub>B</sub> , not defined (default) |

## Registers

| Field           | Bits  | Type | Description   |
|-----------------|-------|------|---|
| <b>VALID</b>    | 13    | rocr | <b>Indicating a valid result</b><br>0 <sub>B</sub> , no new result available<br>1 <sub>B</sub> , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_3 register   |
| <b>PULLDOWN</b> | 12    | rh   | <b>Indicating pull-down switch state</b><br>0 <sub>B</sub> , normal measurement done<br>1 <sub>B</sub> , pull-down for Mux-test was active during conversion  |
| <b>INTC</b>     | 11:10 | rh   | <b>Indicates which current source was used</b><br>Number of current source that was active for latest measurement<br>00 <sub>B</sub> , source $I_{TMP1\_0}$ used (default)<br>01 <sub>B</sub> , source $I_{TMP1\_1}$ used<br>10 <sub>B</sub> , source $I_{TMP1\_2}$ used<br>11 <sub>B</sub> , source $I_{TMP1\_3}$ used |
| <b>RESULT</b>   | 9:0   | rh   | <b>Result of ext. temp 3 measurement</b><br>SD-ADC result of resistance or voltage measurement.<br>000 <sub>H</sub> , default   |

## EXT\_TEMP\_4

|                      |                       |                         |
|----------------------|-----------------------|-------------------------|
| <b>EXT_TEMP_4</b>    | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Temp result 4</b> | <b>2D<sub>H</sub></b> | <b>0000<sub>H</sub></b> |

|            |             |             |             |    |    |   |  |  |  |  |  |  |  |  |    |
|------------|-------------|-------------|-------------|----|----|---|--|--|--|--|--|--|--|--|----|
| 15         | 14          | 13          | 12          | 11 | 10 | 9 |  |  |  |  |  |  |  |  | 0  |
| <b>RES</b> | <b>VAL*</b> | <b>PUL*</b> | <b>INTC</b> |    |    |   |  |  |  |  |  |  |  |  |    |
| rw         | rocr        | rh          | rh          |    |    |   |  |  |  |  |  |  |  |  | rh |

| Field           | Bits  | Type | Description   |
|-----------------|-------|------|---|
| <b>RES</b>      | 15:14 | rw   | <b>Reserved for future use</b><br>00 <sub>B</sub> , not defined (default)   |
| <b>VALID</b>    | 13    | rocr | <b>Indicating a valid result</b><br>0 <sub>B</sub> , no new result available<br>1 <sub>B</sub> , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_4 register   |
| <b>PULLDOWN</b> | 12    | rh   | <b>Indicating pull-down switch state</b><br>0 <sub>B</sub> , normal measurement done<br>1 <sub>B</sub> , pull-down for Mux-test was active during conversion  |
| <b>INTC</b>     | 11:10 | rh   | <b>Indicates which current source was used</b><br>Number of current source that was active for latest measurement<br>00 <sub>B</sub> , source $I_{TMPn\_0}$ used (default)<br>01 <sub>B</sub> , source $I_{TMPn\_0}$ used<br>10 <sub>B</sub> , source $I_{TMPn\_0}$ used<br>11 <sub>B</sub> , source $I_{TMPn\_0}$ used |

## Registers

| Field  | Bits | Type | Description   |
|--------|------|------|---|
| RESULT | 9:0  | rh   | <b>Result of ext. temp 4 measurement</b><br>SD-ADC result of resistance or voltage measurement.<br>000 <sub>H</sub> , default |

## EXT\_TEMP\_R\_DIAG

|                               |                       |                         |
|-------------------------------|-----------------------|-------------------------|
| <b>EXT_TEMP_R_DIAG</b>        | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Temp result R Diagnose</b> | <b>2F<sub>H</sub></b> | <b>0000<sub>H</sub></b> |

|     |      |     |      |    |    |   |  |  |  |  |  |  |  |  |        |
|-----|------|-----|------|----|----|---|--|--|--|--|--|--|--|--|--------|
| 15  | 14   | 13  | 12   | 11 | 10 | 9 |  |  |  |  |  |  |  |  | 0      |
| RES | VAL* | RES | INTC |    |    |   |  |  |  |  |  |  |  |  | RESULT |
| rwh | rocr | rwh | rh   |    |    |   |  |  |  |  |  |  |  |  | rh     |

| Field  | Bits  | Type | Description   |
|--------|-------|------|---|
| RES    | 15:14 | rwh  | <b>Reserved for future use</b><br>00 <sub>B</sub> , not defined (default)   |
| VALID  | 13    | rocr | <b>Indicating a valid result</b><br>0 <sub>B</sub> , no new result available<br>1 <sub>B</sub> , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_R_DIAG register  |
| RES    | 12    | rwh  | <b>Reserved for future use</b><br>0 <sub>B</sub> , not defined (default)  |
| INTC   | 11:10 | rh   | <b>Indicates which current source was used</b><br>Number of current source that was active for latest measurement<br>00 <sub>B</sub> , source I <sub>TMP0_0</sub> used (default)<br>01 <sub>B</sub> , source I <sub>TMP0_1</sub> used<br>10 <sub>B</sub> , source I <sub>TMP0_2</sub> used<br>11 <sub>B</sub> , source I <sub>TMP0_3</sub> used |
| RESULT | 9:0   | rh   | <b>Result of diagnosis resistor measurement</b><br>SD-ADC result<br>000 <sub>H</sub> , default  |

## INT\_TEMP

|                         |                       |                         |
|-------------------------|-----------------------|-------------------------|
| <b>INT_TEMP</b>         | <b>Offset</b>         | <b>Reset Value</b>      |
| <b>Chip temperature</b> | <b>30<sub>H</sub></b> | <b>0000<sub>H</sub></b> |

|     |      |    |     |    |   |  |  |  |  |  |  |  |  |  |        |
|-----|------|----|-----|----|---|--|--|--|--|--|--|--|--|--|--------|
| 15  | 14   | 13 | 12  | 10 | 9 |  |  |  |  |  |  |  |  |  | 0      |
| RES | VAL* |    | RES |    |   |  |  |  |  |  |  |  |  |  | RESULT |
| rwh | rocr |    | rwh |    |   |  |  |  |  |  |  |  |  |  | rh     |

| Field         | Bits  | Type | Description   |
|---------------|-------|------|---|
| <b>RES</b>    | 15:14 | rwh  | <b>Reserved for future use</b><br>00 <sub>B</sub> , not defined (default)   |
| <b>VALID</b>  | 13    | rocr | <b>Indicating a valid result</b><br>0 <sub>B</sub> , no new result available (default)<br>1 <sub>B</sub> , a new result is stored in the register, cleared automatically after readout of the INT_TEMP register |
| <b>RES</b>    | 12:10 | rwh  | <b>Reserved for future use</b><br>000 <sub>B</sub> , not defined (default)  |
| <b>RESULT</b> | 9:0   | rh   | <b>Result of internal temperature measurement</b><br>SD-ADC result of internal temperature measurement.<br>000 <sub>H</sub> , default   |

| Field | Bits  | Type | Description   |
|-------|-------|------|---|
| RES   | 15:10 | rwh  | <b>Reserved for future use</b><br>00 <sub>H</sub> , not defined (default) |

## Registers

| Field          | Bits | Type | Description   |
|----------------|------|------|---|
| INT_TEMP_SEL   | 9    | rw   | <b>Selects if INT_TEMP result is part of the multiread</b><br>0 <sub>B</sub> , no INT_TEMP result (default)<br>1 <sub>B</sub> , result of INT_TEMP  |
| EXT_TEMP_R_SEL | 8    | rw   | <b>Selects if R_DIAG result is part of the multiread</b><br>0 <sub>B</sub> , no R_DIAG result (default)<br>1 <sub>B</sub> , result of R_DIAG  |
| EXT_TEMP_SEL   | 7:5  | rw   | <b>Selects which TEMP result is part of the multiread</b><br>0 <sub>B</sub> , no TEMP result (default)<br>1 <sub>B</sub> , result of TEMP 0<br>10 <sub>B</sub> , result of TEMP 0 & TEMP 1<br>11 <sub>B</sub> , result of TEMP 0 & TEMP 1 & TEMP 2<br>100 <sub>B</sub> , result of TEMP 0 & TEMP 1 & TEMP 2 & TEMP 3<br>101 <sub>B</sub> , result of TEMP 0 & TEMP 1 & TEMP 2 & TEMP 3 & TEMP 4 |
| BVM_SEL        | 4    | rw   | <b>Selects if BVM result is part of the multiread</b><br>0 <sub>B</sub> , no BVM result (default)<br>1 <sub>B</sub> , result of BVM   |
| CVM_SEL        | 3:0  | rw   | <b>Selects which CVM results are part of the multiread</b><br>0 <sub>B</sub> , no CVM result (default)<br>1 <sub>B</sub> , only result of Cell 11<br>10 <sub>B</sub> , results of Cell 11- 10<br>11 <sub>B</sub> , results of Cell 11- 9<br>1100 <sub>B</sub> , results of cell 11- 0<br>1101...1111 <sub>B</sub> , no CVM result   |

## BAL\_DIAG\_OC

| BAL_DIAG_OC                        | Offset          | Reset Value       |
|------------------------------------|-----------------|-------------------|
| Passive bal. diagnosis OVERCURRENT | 33 <sub>H</sub> | 0000 <sub>H</sub> |

| 15  | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|
| RES | OC_* | OC_* | OC_9 | OC_8 | OC_7 | OC_6 | OC_5 | OC_4 | OC_3 | OC_2 | OC_1 | OC_0 |      |
| rwh | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw | rocw |

| Field | Bits  | Type | Description   |
|-------|-------|------|---|
| RES   | 15:12 | rwh  | <b>Reserved for future use</b><br>0000 <sub>B</sub> , not defined (default)   |
| OC_11 | 11    | rocw | <b>Balancing overcurrent in cell 11</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell. |

## Registers

| Field        | Bits | Type | Description   |
|--------------|------|------|---|
| <b>OC_10</b> | 10   | rocw | <b>Balancing overcurrent in cell 10</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>OC_9</b>  | 9    | rocw | <b>Balancing overcurrent in cell 9</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |
| <b>OC_8</b>  | 8    | rocw | <b>Balancing overcurrent in cell 8</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |
| <b>OC_7</b>  | 7    | rocw | <b>Balancing overcurrent in cell 7</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |
| <b>OC_6</b>  | 6    | rocw | <b>Balancing overcurrent in cell 6</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |
| <b>OC_5</b>  | 5    | rocw | <b>Balancing overcurrent in cell 5</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |



## Registers

| Field       | Bits | Type | Description  |
|-------------|------|------|--|
| <b>OC_4</b> | 4    | roCW | <b>Balancing overcurrent in cell 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>OC_3</b> | 3    | roCW | <b>Balancing overcurrent in cell 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>OC_2</b> | 2    | roCW | <b>Balancing overcurrent in cell 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>OC_1</b> | 1    | roCW | <b>Balancing overcurrent in cell 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>OC_0</b> | 0    | roCW | <b>Balancing overcurrent in cell 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing overcurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing overcurrent detected in respective cell.<br>Balancing is deactivated for this cell. |

## BAL\_DIAG\_UC

| BAL_DIAG_UC                         | Offset          | Reset Value       |
|-------------------------------------|-----------------|-------------------|
| Passive bal. diagnosis UNDERCURRENT | 34 <sub>H</sub> | 0000 <sub>H</sub> |

|     |      |      |      |      |      |      |      |      |      |      |      |      |      |
|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 15  | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| RES | UC_* | UC_* | UC_9 | UC_8 | UC_7 | UC_6 | UC_5 | UC_4 | UC_3 | UC_2 | UC_1 | UC_0 |      |
| rwh | roCW | roCW | roCW | roCW | roCW | roCW | roCW | roCW | roCW | roCW | roCW | roCW | roCW |

**Registers**

| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| <b>RES</b>   | 15:12 | rwh  | <b>Reserved for future use</b><br>0000 <sub>B</sub> , not defined (default)  |
| <b>UC_11</b> | 11    | rocw | <b>Balancing undercurrent in cell 11</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>UC_10</b> | 10    | rocw | <b>Balancing undercurrent in cell 10</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>UC_9</b>  | 9     | rocw | <b>Balancing undercurrent in cell 9</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |
| <b>UC_8</b>  | 8     | rocw | <b>Balancing undercurrent in cell 8</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |
| <b>UC_7</b>  | 7     | rocw | <b>Balancing undercurrent in cell 7</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |
| <b>UC_6</b>  | 6     | rocw | <b>Balancing undercurrent in cell 6</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell.  |

## Registers

| Field       | Bits | Type | Description   |
|-------------|------|------|---|
| <b>UC_5</b> | 5    | rocw | <b>Balancing undercurrent in cell 5</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>UC_4</b> | 4    | rocw | <b>Balancing undercurrent in cell 4</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>UC_3</b> | 3    | rocw | <b>Balancing undercurrent in cell 3</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>UC_2</b> | 2    | rocw | <b>Balancing undercurrent in cell 2</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>UC_1</b> | 1    | rocw | <b>Balancing undercurrent in cell 1</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |
| <b>UC_0</b> | 0    | rocw | <b>Balancing undercurrent in cell 0</b><br>Can also be cleared on write '0' to connected GEN_DIAG register bit<br>0 <sub>B</sub> , no balancing undercurrent detected in respective cell (default)<br>1 <sub>B</sub> , balancing undercurrent detected in respective cell.<br>Balancing is deactivated for this cell. |

## CONFIG

## Registers

**CONFIG** **Offset**  
36<sub>H</sub> **Reset Value**  
0000<sub>H</sub>  
**Configuration**

|    |     |    |     |     |      |   |     |   |   |  |  |         |   |
|----|-----|----|-----|-----|------|---|-----|---|---|--|--|---------|---|
| 15 |     | 12 | 11  | 10  | 9    | 8 |     | 6 | 5 |  |  |         | 0 |
|    | RES |    | FN  | RES | EN_* |   | RES |   |   |  |  | NODE_ID |   |
|    | rwh |    | rwo | rwh | rwo  |   | rwh |   |   |  |  | rwo     |   |

| Field      | Bits  | Type | Description  |
|------------|-------|------|--|
| RES        | 15:12 | rwh  | <b>Reserved for future use</b><br>0000 <sub>B</sub> , not defined (default)  |
| FN         | 11    | rwo  | <b>Final Node</b><br>The final node in stack must have this bit set. If the final node does not have FN set, no reply frame on broadcast will be sent -> iso UART time-out.<br>0 <sub>B</sub> , not the final node (default)<br>1 <sub>B</sub> , final node  |
| RES        | 10    | rwh  | <b>Reserved for future use</b><br>0 <sub>B</sub> , not defined (default)   |
| EN_ALL_ADC | 9     | rwo  | <b>Enable all ADCs</b><br>If this bit is set CVM is done for each channel independent of PART_CONFIG setup. But the results are only available for the cells activated in PART_CONFIG<br>0 <sub>B</sub> , only ADCs enabled which are defined in PART_CONFIG as active cell<br>1 <sub>B</sub> , all ADCs enabled |
| RES        | 8:6   | rwh  | <b>Reserved for future use</b><br>000 <sub>B</sub> , not defined (default)   |
| NODE_ID    | 5:0   | rwo  | <b>Address (ID) of the node, distributed during enumeration</b><br>NODE_ID = 0 --> iso UART signals are not forwarded<br>NODE_ID = 63 --> reserved for broadcast commands<br>000000 <sub>B</sub> , (default)   |

## GPIO

**GPIO** **Offset**  
37<sub>H</sub> **Reset Value**  
0000<sub>H</sub>  
**General purpose input / output**

|      |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 15   | 14  | 13   | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| VIO* | RES | DIR* | OUT* | PWM* | IN_* | DIR* | OUT* | PWM* | IN_* | DIR* | OUT* | IN_* | DIR* | OUT* | IN_* |
| rocw | rwh | rw   | rw   | rw   | rh   | rw   | rw   | rw   | rh   | rw   | rw   | rh   | rw   | rw   | rh   |

## Registers

| Field            | Bits | Type | Description   |
|------------------|------|------|---|
| <b>VIO_UV</b>    | 15   | rocw | <b>VIO undervoltage error (supplied in sleep)</b><br>$0_B$ , no VIO undervoltage error (default)<br>$1_B$ , VIO undervoltage error occurred   |
| <b>RES</b>       | 14   | rwh  | <b>Reserved for future use</b><br>$0_B$ , not defined (default)   |
| <b>DIR_PWM0</b>  | 13   | rw   | <b>PWM 0 direction</b><br>$0_B$ , input (output stage = HiZ) (default)<br>$1_B$ , output (output stage enabled)   |
| <b>OUT_PWM0</b>  | 12   | rw   | <b>PWM 0 output setting</b><br>$0_B$ , drive L (default)<br>$1_B$ , drive H   |
| <b>PWM_PWM0</b>  | 11   | rw   | <b>PWM 0 enable PWM function</b><br>$0_B$ , no PWM function (default)<br>$1_B$ , if DIR_PWM0 = 1, then PWM output regarding PWM_GPIO register and OUT_PWM0 is ignored. If DIR_PWM0 = 0, GPIO input and no PWM function. |
| <b>IN_PWM0</b>   | 10   | rh   | <b>PWM 0 input state</b><br>$0_B$ , pin reads L (default)<br>$1_B$ , pin reads H<br>Also active for DIR_PWM0 = 1 (reading back driven value)  |
| <b>DIR_PWM1</b>  | 9    | rw   | <b>PWM 1 direction</b><br>$0_B$ , input (output stage = HiZ) (default)<br>$1_B$ , output (output stage enabled)   |
| <b>OUT_PWM1</b>  | 8    | rw   | <b>PWM 1 output setting</b><br>$0_B$ , drive L (default)<br>$1_B$ , drive H   |
| <b>PWM_PWM1</b>  | 7    | rw   | <b>PWM 1 enable PWM function</b><br>$0_B$ , no PWM function (default)<br>$1_B$ , if DIR_PWM1 = 1, then PWM output regarding PWM_GPIO register and OUT_PWM1 is ignored. If DIR_PWM1 = 0, GPIO input and no PWM function. |
| <b>IN_PWM1</b>   | 6    | rh   | <b>PWM 1 input state</b><br>$0_B$ , pin reads L (default)<br>$1_B$ , pin reads H<br>Also active for DIR_PWM1 = 1 (reading back driven value)  |
| <b>DIR_GPIO1</b> | 5    | rw   | <b>GPIO 1 direction (ignored if communication over GPIO pins)</b><br>$0_B$ , input (output stage = HiZ) (default)<br>$1_B$ , output (output stage enabled)  |
| <b>OUT_GPIO1</b> | 4    | rw   | <b>GPIO 1 output setting (ignored if communication over GPIO pins)</b><br>$0_B$ , drive L (default)<br>$1_B$ , drive H  |

## Registers

| Field            | Bits | Type | Description  |
|------------------|------|------|--|
| <b>IN_GPIO1</b>  | 3    | rh   | <b>GPIO 1 input state (ignored if communication over GPIO pins)</b><br>$0_B$ , pin reads L (default)<br>$1_B$ , pin reads H<br>Also active for DIR_GPIO1 = 1 (reading back driven value) |
| <b>DIR_GPIO0</b> | 2    | rw   | <b>GPIO 0 direction (ignored if communication over GPIO pins)</b><br>$0_B$ , input (output stage = HiZ) (default)<br>$1_B$ , output (output stage enabled)                               |
| <b>OUT_GPIO0</b> | 1    | rw   | <b>GPIO 0 output setting (ignored if communication over GPIO pins)</b><br>$0_B$ , drive L (default)<br>$1_B$ , drive H   |
| <b>IN_GPIO0</b>  | 0    | rh   | <b>GPIO 0 input state (ignored if communication over GPIO pins)</b><br>$0_B$ , pin reads L (default)<br>$1_B$ , pin reads H<br>Also active for DIR_GPIO0 = 1 (reading back driven value) |

## GPIO\_PWM

| GPIO_PWM  | Offset                | Reset Value             |
|---|-----------------------|-------------------------|
| <b>PWM settings</b>   | <b>38<sub>H</sub></b> | <b>0000<sub>H</sub></b> |
| <div> <div>15</div> <div>13</div> <div>12</div> <div>8</div> <div>7</div> <div>5</div> <div>4</div> <div>0</div> </div> <div> <div>RES</div> <div>PWM_PERIOD</div> <div>RES</div> <div>PWM_DUTY_CYCLE</div> </div> <div> <div>rwh</div> <div>rw</div> <div>rwh</div> <div>rw</div> </div> |                       |                         |

| Field             | Bits  | Type | Description   |
|-------------------|-------|------|---|
| <b>RES</b>        | 15:13 | rwh  | <b>Reserved for future use</b><br>$000_B$ , not defined (default)   |
| <b>PWM_PERIOD</b> | 12:8  | rw   | <b>PWM period time setting</b><br>2 $\mu$ s - 62 $\mu$ s<br>$00000_B$ , no PWM (default)<br>$00001_B$ , 2 $\mu$ s<br>$00010_B$ , 4 $\mu$ s<br>...<br>$11111_B$ , 62 $\mu$ s |
| <b>RES</b>        | 7:5   | rwh  | <b>Reserved for future use</b><br>$000_B$ , not defined (default)   |

## Registers

| Field                 | Bits | Type | Description  |
|-----------------------|------|------|--|
| <b>PWM_DUTY_CYCLE</b> | 4:0  | rw   | <b>PWM duty cycle</b><br>0 - 100%<br>00000 <sub>B</sub> , no PWM (default)<br>00001 <sub>B</sub> , 3.57%<br>00010 <sub>B</sub> , 7.14%<br>...<br>11100 <sub>B</sub> , 100%<br>...<br>11111 <sub>B</sub> , 100% |

## ICVID

| ICVID                           | Offset          | Reset Value       |
|---------------------------------|-----------------|-------------------|
| IC version and manufacturing ID | 39 <sub>H</sub> | C110 <sub>H</sub> |

|                 |   |            |   |
|-----------------|---|------------|---|
| 15              | 8 | 7          | 0 |
| MANUFACTURER_ID |   | VERSION_ID |   |
| rh              |   | rh         |   |

| Field                  | Bits | Type | Description   |
|------------------------|------|------|---|
| <b>MANUFACTURER_ID</b> | 15:8 | rh   | <b>Manufacturer ID</b><br>Read only manufacture ID<br>11000001 <sub>B</sub> , default |
| <b>VERSION_ID</b>      | 7:0  | rh   | <b>Version ID</b><br>Read only version ID<br>00010000 <sub>B</sub> , default          |

## MAILBOX

| MAILBOX          | Offset          | Reset Value       |
|------------------|-----------------|-------------------|
| Mailbox register | 3A <sub>H</sub> | 0000 <sub>H</sub> |

|      |   |
|------|---|
| 15   | 0 |
| DATA |   |
| rw   |   |

| Field       | Bits | Type | Description   |
|-------------|------|------|---|
| <b>DATA</b> | 15:0 | rw   | <b>Data storage register</b><br>2 data byte data storage<br>0000 <sub>H</sub> , (default) |



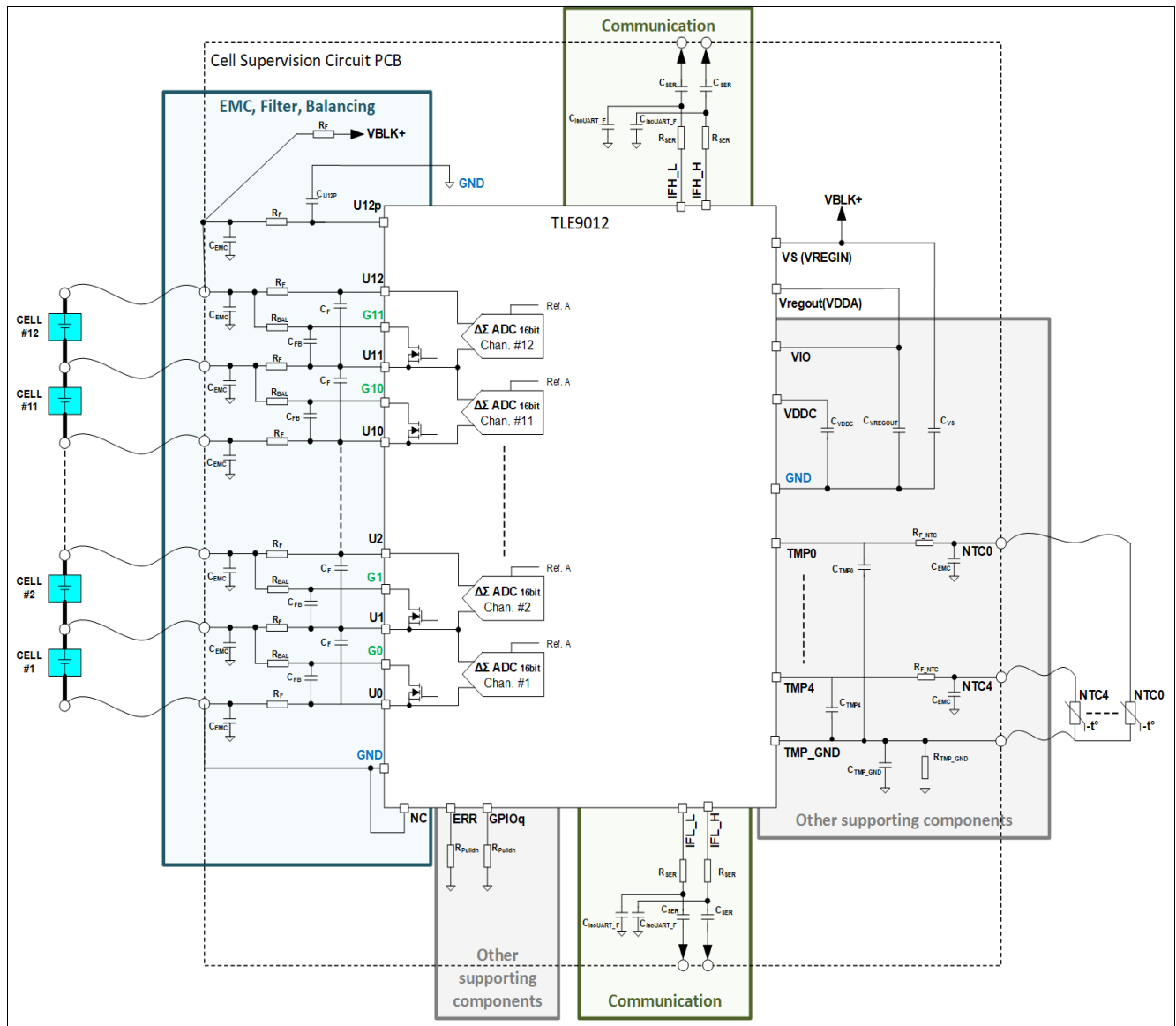


## Registers

| Field           | Bits | Type | Description  |
|-----------------|------|------|--|
| <b>MAIN_CNT</b> | 15:7 | rh   | <b>Main counter</b><br>Used to enable $\mu$ C to measure main oscillator frequency. LSB = $t_{\text{count\_LSB}}$<br>0 0000 0000 <sub>B</sub> , (default)  |
| <b>WD_CNT</b>   | 6:0  | rwh  | <b>Watchdog counter (LP oscillator)</b><br>0 <sub>B</sub> , device goes to sleep<br>1 <sub>B</sub> , $t_{\text{WD\_LSB}}$ (EXT_WD = 0)<br>1 <sub>B</sub> , $t_{\text{WD\_EXT\_LSB}}$ (EXT_WD = 1)<br>111 1111 <sub>B</sub> , $t_{\text{WD\_LSB}} * 127$ (EXT_WD = 0) (default)<br>111 1111 <sub>B</sub> , $t_{\text{WD\_EXT\_LSB}} * 127$ (EXT_WD = 1) |

## 13 Application information

**Note:** The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the circuit must be verified in the real application. Please ask for the Application Note regarding Application Information for more details.



**Figure 43** Application circuitry example

**Note:** Hot-plug and EMC robustness is dependent on used PCB components and PCB routing.

**Figure 44** Package outlines and footprint PG-TQFP-48

## 15 Revision history

| Revision | Date       | Changes   |
|----------|------------|---|
| 1.1      | 2020-06-09 | Editorial changes<br><a href="#">Table 2</a> Cell sense input voltages rel. Un: max. limit increased<br><a href="#">Table 8</a> Minor parameter adjustment<br><a href="#">Table 11</a> Sink current for open load diagnosis: max. limit decreased |
| 1.0      | 2019-12-13 | Initial Datasheet   |
|          |            |   |

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**Edition 2020-06-09**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

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**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

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