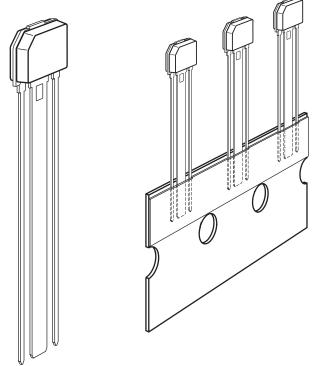


### Data Sheet Supplement Version 1.0

## Dynamic Differential Hall Effect Sensor

TLE4928

For all parameters not specified in this document the TLE4926C-HT E6947 data sheet is valid.



PG-SSO-3-6

Туре	Marking	Ordering Code	Package	
TLE4928	28	SP000700818	PG-SSO-3-6	



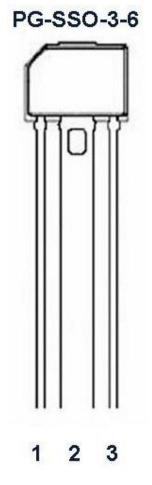


Figure 1: Pin configuration in PG-SSO-3-6

<b>Pin definition</b>	and Function
-----------------------	--------------

Pin No.	Symbol	Function
1	Vs	Supply Voltage
2	GND	Ground
3	Q	Open Drain Output



#### 1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	min.	typ.	max.	Unit	Conditions
1.1.1	Junction temperature	Tj	-40			°C	-
					155	°C	2000 h (not additive)
					165	°C	1000 h (not additive)
					175	°C	168 h (not additive)
					195	°C	3x1 h (additive to the other life times).
1.1.2	Thermal resistance junction-air for PG-SSO-3-6	R <sub>th JA</sub>			190	K/W	Lower values are possible with overmoulded devices.

#### 1.2 ESD Protection

No.	Parameter	Symbol	max	Unit	Remarks
1.2.1	ESD – protection PG-SSO-3-6	V <sub>ESD</sub>	± 6	kV	According to standard EIA/JESD22-A114-B Human Body Model (HBM 1500 Ohm/100pF)

#### 1.3 Operating Range

No.	Parameter	Symbol	min.	typ.	max.	Unit	Conditions
1.3.1	Operating junction	Tj	-40			°C	-
	temperature				155	°C	2000 h (not additive)
					165	°C	1000 h (not additive)
					175	°C	168 h (not additive) reduced signal quality permittable (e.g. jitter).
1.3.2	Power on time	t <sub>on</sub>			1	ms	Time to achieve specified accuracy After power on the output of the IC is always in high-state. After internal resets output is locked <sup>1</sup> .

<sup>&</sup>lt;sup>1</sup> Output of the IC is locked in present state (high-state or low-state) after an internal reset is launched. This reset happens typically every 195ms when there is no output switching in either case. See also 1.4.4. A voltage reset causes a release of the output and output is in high state after power on again. Page 3 of 9



#### 1.4 AC/DC Characteristics

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
1.4.1	Output rise time	t <sub>r</sub> <sup>2</sup>					
			4	12	20	μs	$V_{Load}$ = 4.5 to 24V
							$R_{Load} = 1.2 k\Omega;$
							$C_{Load} = 4.7$ nF external capacitor
1.4.2	Output fall time	t <sub>f</sub> <sup>3</sup>					
			0.5	0.9	1.3	μs	$V_{Load} = 5V$
			0.65	1.15	1.65	μs	$V_{Load} = 12V$
							$R_{Load} = 1.2 k\Omega;$
							$C_{Load} = 4.7$ nF external capacitor
1.4.3	Frequency range <sup>4</sup>	f	0.006		8	kHz	Operation below $6Hz^5$
1.4.4	Offset recalibration time after last output change <sup>4</sup>	t <sub>reset</sub>	165	195	225	ms	Valid for calibrated mode
							Output locked to state
							before recalibration

 $<sup>^2</sup>$  The rise time is defined as the time between the 10 and 90% value.  $^3$  The fall time is defined as the time between the 10 and 90% value.  $^4$  Not part of production testing, verified by design and characterisation  $^5$  Output will switch if magnetic signal is changing more that  $2x |\Delta B_{min}|$  within offset recalibration time even below 6Hz once per magnetic edge, increased phase error is possible. Page 4 of 9



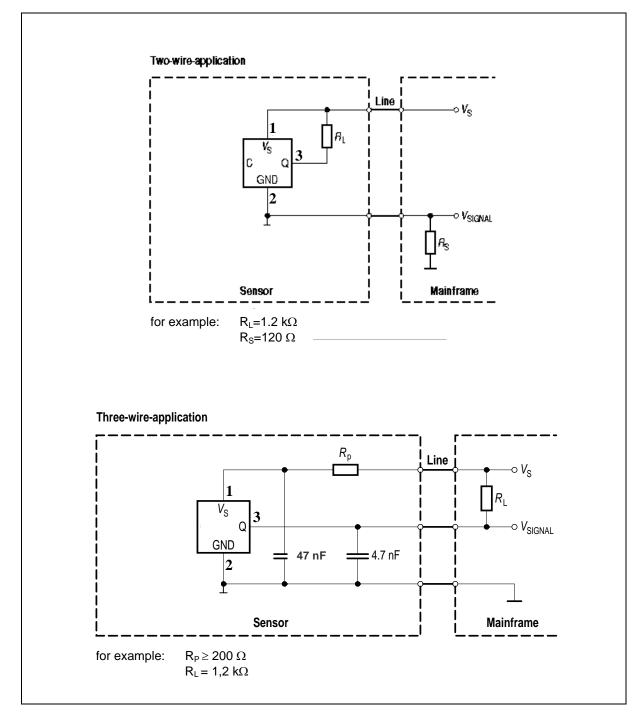


Figure 2: Application Circuits (capacitors to be added externally)



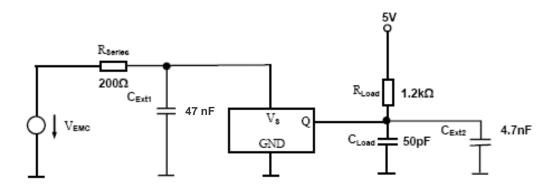
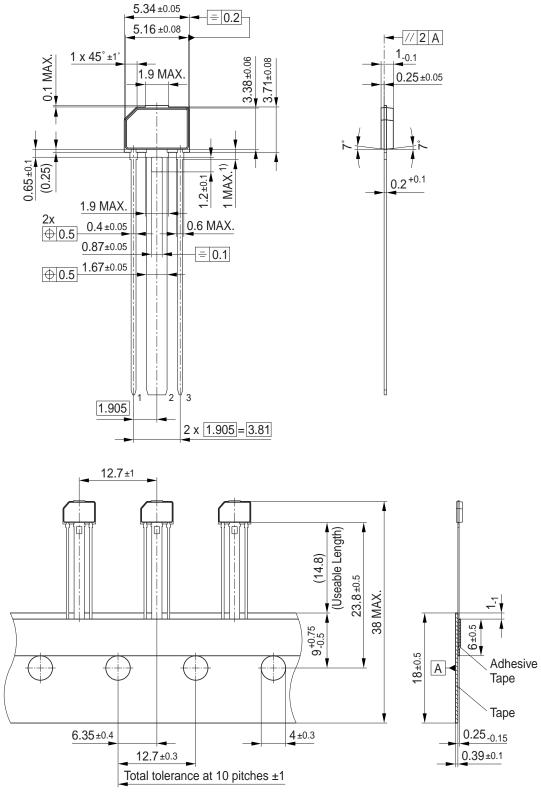


Figure 3: Test Circuit for EMC tests



TLE4928 supplement



1) No solder function area

GPO05960

#### Figure 4: PG-SSO-3-6 package drawing





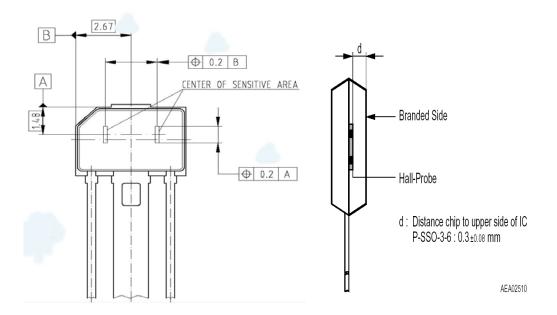


Figure 5: Hall probe spacing in the PG-SSO-3-6 package



Revision History:		November 2009	Version 1.0
Previous '	Version: 0.9		
Page	Subjects (majo	or changes since last revision)	
-	Change to Fi	nal Data Sheet	

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