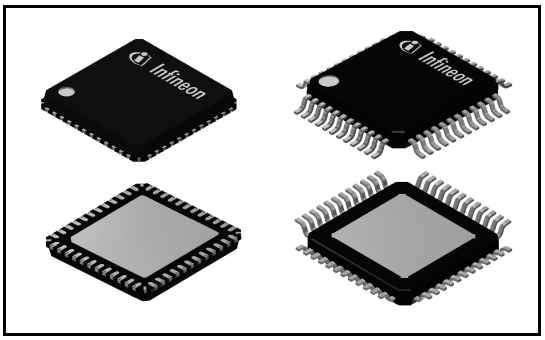
TLD5190

H-Bridge DC/DC Controller

Infineon® LITIX™ Power

Package	PG-VQFN-48-31	PG-TQFP-48-9
Marking	TLD5190QV	TLD5190QU
Sales Name	TLD5190QV	TLD5190QU



1 Overview

Features

- Single Inductor high power Buck-Boost controller
- Wide LED forward voltage Range (2 V up to 55 V)
- Wide VIN Range (IC 4.5 V to 40 V, Power 4.5 V to 55 V)
- Switching Frequency Range from 200 kHz to 700 kHz
- Maximum Efficiency in every condition (up to 96%)
- Constant Current (LED) and Constant Voltage Regulation
- EMC optimized device: Features an auto Spread Spectrum
- Open Load, Overvoltages, Shorted LED fault and Overtemperature Diagnostic Outputs
- LED and Input current sense with dedicated monitor Outputs
- Advanced protection features for device and load
- Enhanced Dimming features: Analog and PWM dimming
- LED current accuracy +/- 3%
- Available in a small thermally enhanced PG-VQFN-48-31 or PG-TQFP-48-9 package
- Automotive AEC Qualified

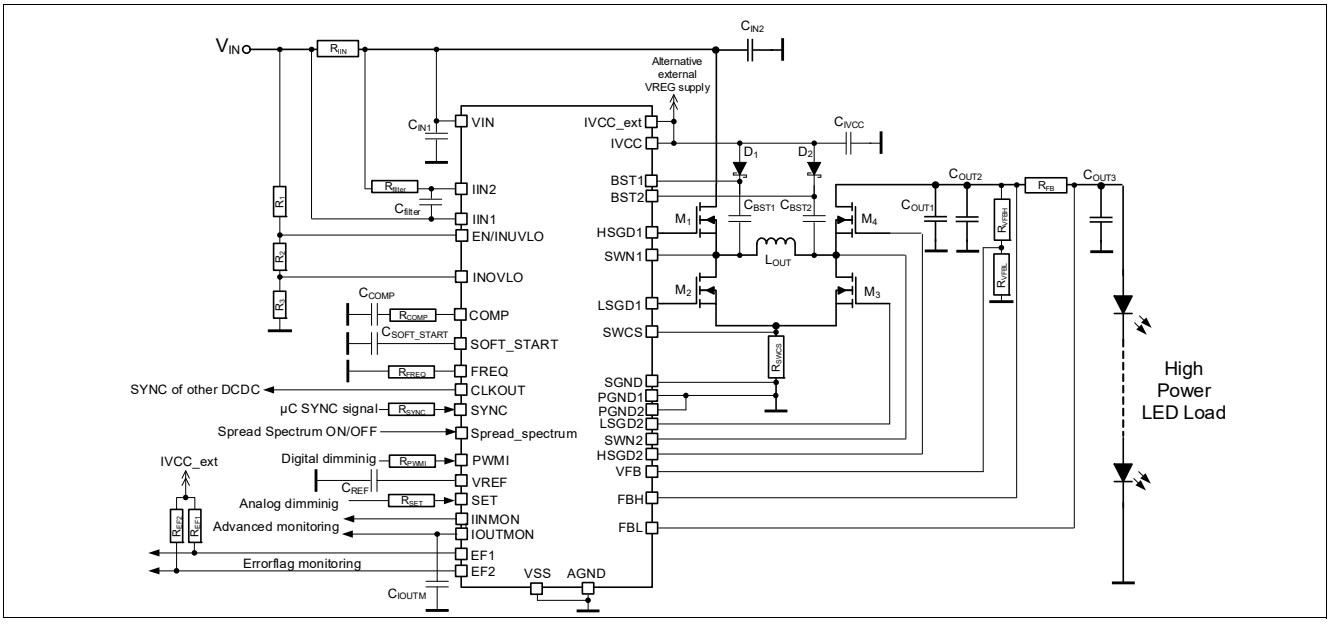


Figure 1 Application Drawing - TLD5190 as current regulator

Overview

Description

The TLD5190 is a synchronous MOSFET H-Bridge DC/DC controller with built in protection features. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5190 offers both analog and digital (PWM) dimming.The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5190 is suitable for use in the harsh automotive environment.

Table 1 Product Summary

Power Stage input voltage range	V_{POW}	4.5 V … 55 V
Device Input supply voltage range	V_{VIN}	4.5 V … 40 V
Maximum output voltage (depending by the application conditions)	$V_{OUT(max)}$	55 V as LED Driver Boost Mode 50 V as LED Driver Buck Mode 50 V as Voltage regulator
Switching Frequency range	f_{SW}	200 kHz... 700 kHz
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Up)	$R_{DS(ON\_PU)}$	2.3 Ω
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Down)	$R_{DS(ON\_PD)}$	1.2 Ω

Protective Functions

- Over load protection of external MOSFETs
- Shorted load, open load, output overvoltage protection
- Input overvoltage and undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Diagnostic information via Error Flags
- Open load detection in ON-state
- Device Overtemperature shutdown
- Advanced diagnostic functions provide I_{LED} and I_{IN} information

Applications

- Especially designed for driving high power LEDs in automotive applications
- Automotive Exterior Lighting: full LED headlamp assemblies (Low Beam, High Beam, Matrix Beam, Pixel Light)
- General purpose current/voltage controlled DC/DC LED driver

2 Block Diagram

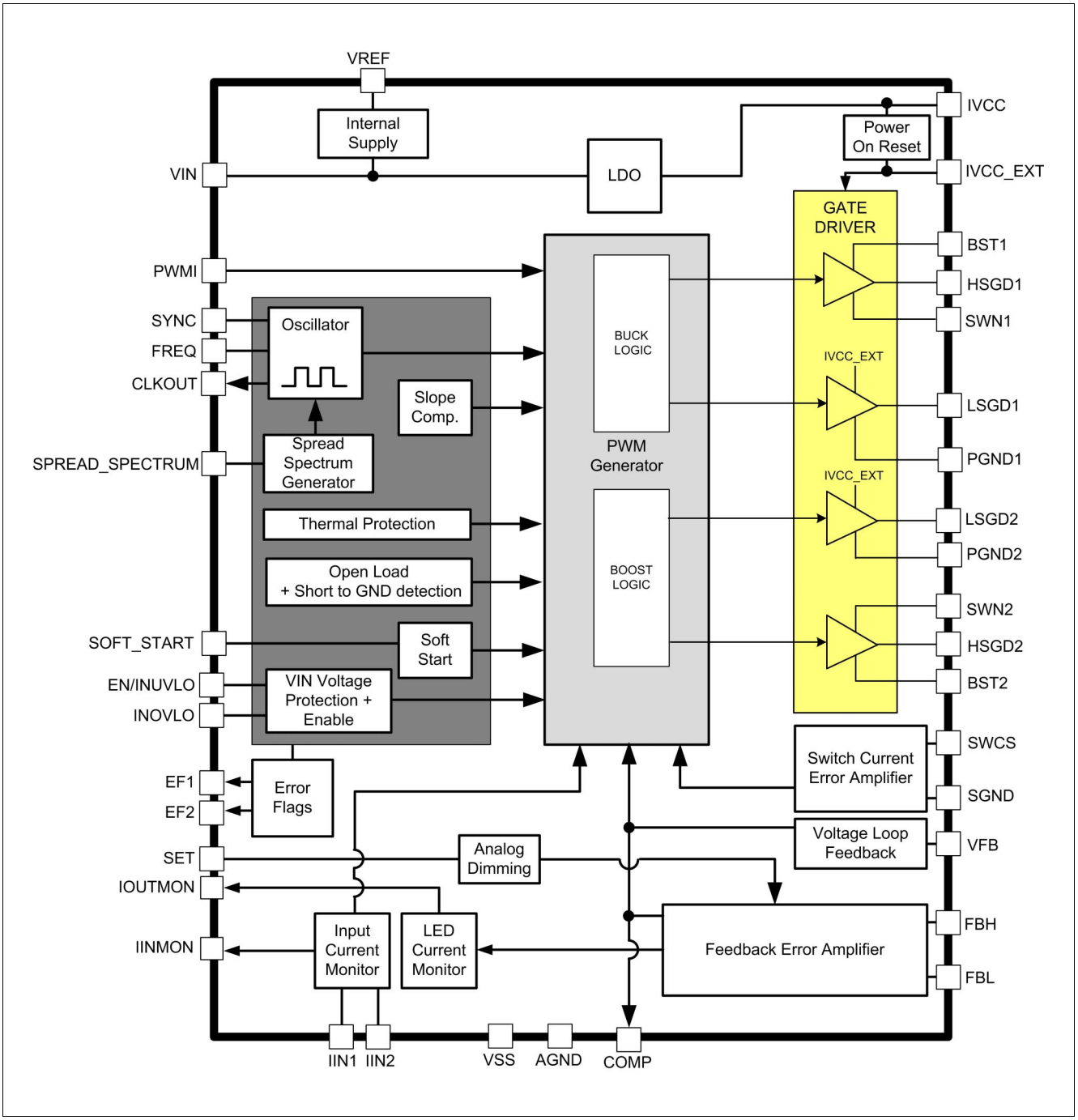


Figure 2 Block Diagram - TLD5190

3 Pin Configuration

3.1 Pin Assignment

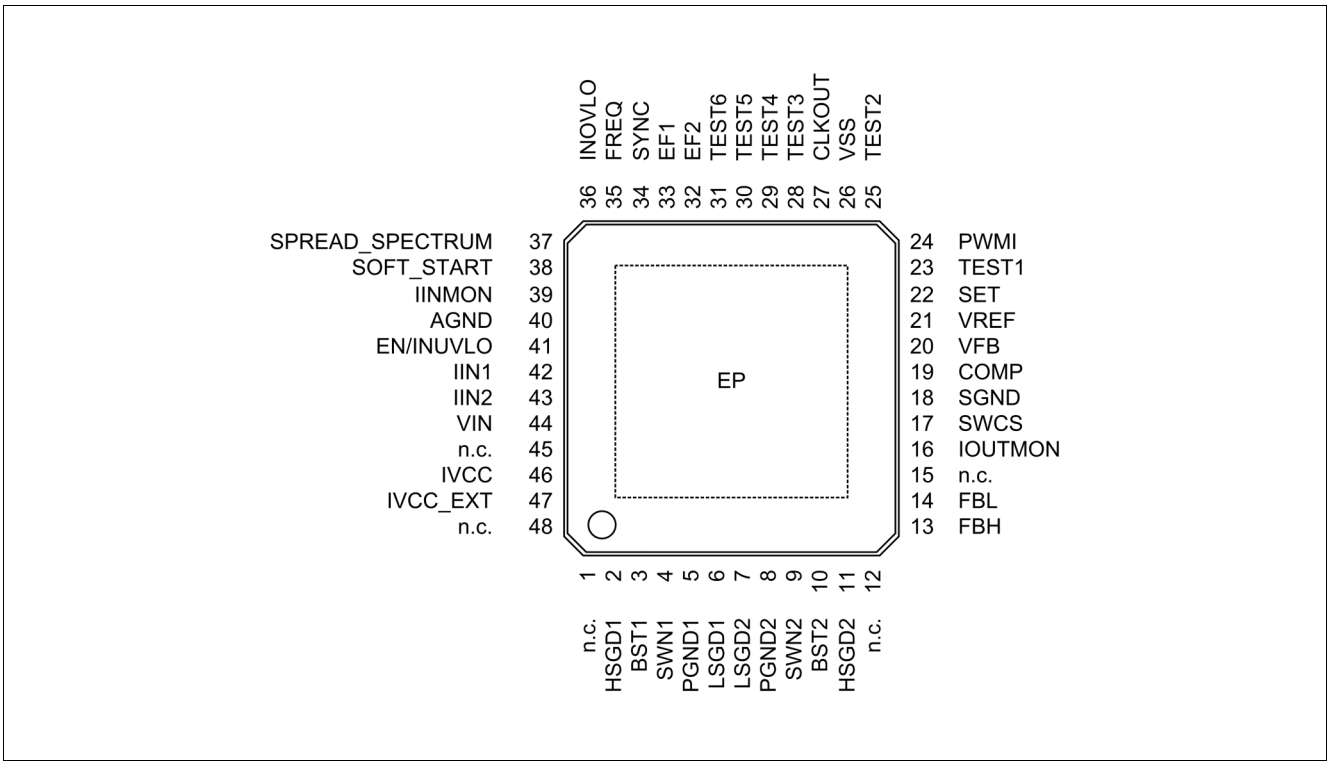


Figure 3 Pin Configuration - TLD5190

3.2 Pin Definitions and Functions

Pin	Symbol	I/O [1]		Function
Power Supply				
1, 12, 15, 45, 48	n.c.	-		**Not connected, tie to AGND on the Layout;**
44	VIN	-		**Power Supply Voltage;** Supply for internal biasing.
47	IVCC_EXT	I	PD	**External LDO input;** Input to alternatively supply internal Gate Drivers via an external LDO. Connect to IVCC pin to use internal LDO to supply gate drivers. Must not be left open.
5, 8	PGND1, 2	-		**Power Ground;** Ground for power potential. Connect externally close to the chip.
26	VSS	-		**Digital GPIO Ground;** Ground for GPIO pins.
40	AGND	-		**Analog Ground;** Ground Reference
-	EP	-		**Exposed Pad;** Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).
Gate Driver Stages				
2	HSGD1	O		**Highside Gate Driver Output 1;** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET.
11	HSGD2	O		**Highside Gate Driver Output 2;** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET.
6	LSGD1	O		**Lowside Gate Driver Output 1;** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET.
7	LSGD2	O		**Lowside Gate Driver Output 2;** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET.
4	SWN1	IO		**Switch Node 1;** SWN1 pin swings from a diode voltage drop below ground up to V_{IN}.
9	SWN2	IO		**Switch Node 2;** SWN2 pin swings from ground up to a diode voltage drop above V_{OUT}.
46	IVCC	O		**Internal LDO output;** Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open.

Pin Configuration

Pin	Symbol	I/O [1]		Function
Inputs and Outputs				
23	TEST1	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
25	TEST2	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
28	TEST3	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
29	TEST4	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
30	TEST5	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
31	TEST6	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
41	EN/INUVLO	I	PD	**Enable/Input Under Voltage Lock Out;** Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open.
35	FREQ	I		**Frequency Select Input;** Connect external resistor to GND to set frequency.
34	SYNC	I	PD	**Synchronization Input;** Apply external clock signal for synchronization.
24	PWMI	I	PD	**Control Input;** Digital input 5 V or 3.3 V.
13	FBH	I		**Output current Feedback Positive;** Non inverting Input (+).
14	FBL	I		**Output current Feedback Negative;** Inverting Input (-).
3	BST1	IO		**Bootstrap capacitor;** Used for internal biasing and to drive the Highside Switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open.
10	BST2	IO		**Bootstrap capacitor;** Used for internal biasing and to drive the Highside Switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open.
17	SWCS	I		**Current Sense Input;** Inductor current measurement - Non Inverting Input (+).
18	SGND	I		**Current Sense Ground;** Inductor current sense - Inverting Input (-). Route as Differential net with SWCS on the Layout.
42	IIN1	I		**Input Current Monitor Positive;** Non Inverting Input (+), connect to VIN if input current monitor is not needed.
43	IIN2	I		**Input Current Monitor Negative;** Inverting Input (-), connect to VIN if input current monitor is not needed.

Pin Configuration

Pin	Symbol	I/O [1]		Function
19	COMP	O		**Compensation Network Pin;** Connect R and C network to pin for stability phase margin adjustment.
38	SOFT_START	O		**Softstart configuration Pin;** Connect a capacitor C_{SOFT_START} to GND to fix a soft start ramp default time.
36	INOVLO	I		**Input Overvoltage Protection Pin;** Define an upper voltage threshold and switches OFF the device in case of overvoltages on the VIN supply. Must not be left open.
20	VFB	I		**Voltage Loop Feedback Pin;** VFB is intended to set output protection functions.
22	SET	I		**Analog current sense adjustment Pin;** A voltage V_{SET} between 0.2 V and 1.5 V will adjust the I_{LED} or V_{OUT} in a linear relation.
37	SPREAD_SPECTRUM	I	PD	**Spread Spectrum Pin;** This pin is enabling and disabling the SPREAD SPECTRUM function. This feature is beneficial to improve the EMC performance.
39	IINMON	O		**Input current monitor output;** Monitor pin that produces a voltage that is 20 times the voltage $V_{IN1-IN2}$. IINMON will be equal 1 V when V_{IIN1}-V_{IIN2} = 50 mV.
16	IOUTMON	O		**Output current monitor output;** Monitor pin that produces a voltage that is 200 mV + 8 times the voltage $V_{FBH-FBL}$. IOUTMON will be equal 1.4 V when $V_{FBH-FBL}$ = 150 mV.
21	VREF	O	PD	**Voltage Reference Output Pin;** Supplies an accurate 2 V output voltage for standalone analog dimming and LED temperature compensation via external resistors. Bypass with an external 100nF capacitor close to the pin. Pin must not be left open.
Logic Outputs				
27	CLKOUT	O		**Clock Output Pin;** Switching Oscillator output signal to supply additional SYNC Inputs of other DCDC devices (beneficial for standalone operations without µC).
33	EF1	O		**Error Flag 1;** An open drain output which is pulled to LOW when an output Short to GND or Overtemperature occurs.
32	EF2	O		**Error Flag 2;** An open drain output which is pulled to LOW when an OPEN load, Overvoltages or Overtemperature occurs.

1) O: Output, I: Input,
PD: pull-down circuit integrated,
PU: pull-up circuit integrated

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1)]
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
VIN Supply Input	V_{VIN}	-0.3	–	60	V	–	P_4.1.1
IVCC Internal Linear Voltage Regulator Output voltage	V_{IVCC}	-0.3	–	6	V	–	P_4.1.3
IVCC_EXT External Linear Voltage Regulator Input voltage	V_{IVCC_EXT}	-0.3	–	6	V	–	P_4.1.4
VREF Voltage reference output	V_{REF}	-0.3	–	3.6	V	–	P_4.1.5
Gate Driver Stages							
LSGD1,2 - PGND1,2 Lowside Gatedriver voltage	$V_{LSGD1,2-PGND1,2}$	-0.3	–	5.5	V	–	P_4.1.54
HSGD1,2 - SWN1,2 Highside Gatedriver voltage	$V_{HSGD1,2-SWN1,2}$	-0.3	–	5.5	V	–	P_4.1.55
SWN1, SWN2 switching node voltage	$V_{SWN1,2}$	-1	–	60	V	–	P_4.1.6
(BST1-SWN1), (BST2-SWN2) Boostrap voltage	$V_{BST1,2-SWN1,2}$	-0.3	–	6	V	–	P_4.1.7
BST1, BST2 Boostrap voltage related to GND	$V_{BST1,2}$	-0.3	–	65	V	–	P_4.1.8
SWCS Switch Current Sense Input voltage	V_{SWCS}	-0.3	–	0.3	V	–	P_4.1.9
SGND Switch Current Sense GND voltage	V_{SGND}	-0.3	–	0.3	V	–	P_4.1.10
SWCS-SGND Switch Current Sense differential voltage	$V_{SWCS-SGND}$	-0.5	–	0.5	V	–	P_4.1.11
PGND1,2 Power GND voltage	$V_{PGND1,2}$	-0.3	–	0.3	V	–	P_4.1.28
High voltage Pins							
IIN1, IIN2 Input Current monitor voltage	$V_{IIN1,2}$	-0.3	–	60	V	–	P_4.1.12

Table 2 Absolute Maximum Ratings[1)] (cont'd)
***T_J* = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IIN1-IIN2 Input Current monitor differential voltage	$V_{IIN1-IIN2}$	-0.5	–	0.5	V	–	P_4.1.13
FBH, FBL Feedback Error Amplifier voltage	$V_{FBH, FBL}$	-0.3	–	60	V	–	P_4.1.14
FBH-FBL Feedback Error Amplifier differential voltage	$V_{FBH-FBL}$	-0.5	–	0.5	V	–	P_4.1.15
EN/INUVLO Device enable/input undervoltage lockout	$V_{EN/INUVLO}$	-0.3	–	60	V	–	P_4.1.16
Digital (I/O) Pins							
PWMI Digital Input voltage	V_{PWMI}	-0.3	–	5.5	V	–	P_4.1.17
SYNC Synchronization Input voltage	V_{SYNC}	-0.3	–	5.5	V	–	P_4.1.22
CLKOUT Clock Output voltage	V_{CLKOUT}	-0.3	–	5.5	V	–	P_4.1.23
SPREAD_SPECTRUM Spread Spectrum Input voltage	$V_{SPREAD\_SPECTRUM}$	-0.3	–	5.5	V	–	P_4.1.24
Analog Pins							
VFB Loop Input voltage	V_{VFB}	-0.3	–	5.5	V	–	P_4.1.25
INOVLO Input overvoltage lockout	V_{INOVLO}	-0.3	–	5.5	V	–	P_4.1.26
EF1, 2 Error Flags output voltage	$V_{EF1,2}$	-0.3	–	5.5	V	–	P_4.1.27
SET Analog dimming Input voltage	V_{SET}	-0.3	–	5.5	V	–	P_4.1.29
COMP Compensation Input voltage	V_{COMP}	-0.3	–	3.6	V	–	P_4.1.30
SOFT_START Softstart Voltage	V_{SOFT_START}	-0.3	–	3.6	V	–	P_4.1.31
FREQ Voltage at frequency selection pin	V_{FREQ}	-0.3	–	3.6	V	–	P_4.1.32
IINMON Voltage at input monitor pin	V_{IINMON}	-0.3	–	3.6	V	–	P_4.1.33
IOUTMON Voltage at output monitor pin	$V_{IOUTMON}$	-0.3	–	5.5	V	–	P_4.1.34
Temperatures							

Table 2 Absolute Maximum Ratings[1)] (cont'd)
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.35
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.36
ESD Susceptibility							
ESD Resistivity of all Pins	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2)]	P_4.1.37
ESD Resistivity to GND	$V_{ESD,CDM}$	-500	–	500	V	CDM[3)]	P_4.1.38
ESD Resistivity of corner Pins to GND	V_{ESD,CDM_corner}	-750	–	750	V	CDM[3)]	P_4.1.39

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Device Extended Supply Voltage Range	V_{VIN}	4.5	–	40	V	1)	P_4.2.1
Device Nominal Supply Voltage Range	V_{VIN}	8	–	36	V	–	P_4.2.2
Power Stage Voltage Range	V_{POW}	4.5	–	55	V	1)	P_4.2.5
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	0.9	–	K/W	1) 2)	P_4.3.1
Junction to Ambient	R_{thJA}	–	25	–	K/W	3) 2s2p	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta = 25°C; The IC is dissipating 1 W.

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta = 25°C; The IC is dissipating 1 W.

5 Power Supply

The TLD5190 is supplied by the following pins:

- VIN (main supply voltage)
- IVCC_EXT (supply for internal gate driver stages)

The VIN supply provides internal supply voltages for the analog and digital blocks.

IVCC_EXT is the supply for the low side driver stages. This supply is used also to charge, through external Schottky diodes, the bootstrap capacitors which provide supply voltages to the high side driver stages. If no external voltage is available this pin must be shorted to IVCC, which is the output of an internal 5 V LDO.

The supply pins VIN and IVCC_EXT have undervoltage detections.

Undervoltage on IVCC_EXT or IVCC voltages forces a deactivation of the driver stages, thus stopping the switching activity.

Moreover the double function pin EN/INUVLO can be used as an input undervoltage protection by placing a resistor divider from VIN to GND (refer to **Chapter 10.3**).

If EN/INUVLO undervoltage is detected, it will turn-off the IVCC voltage regulator and stop switching.

Figure 4 shows a basic concept drawing of the supply domains and interactions among pins VIN and IVCC/IVCC_EXT.

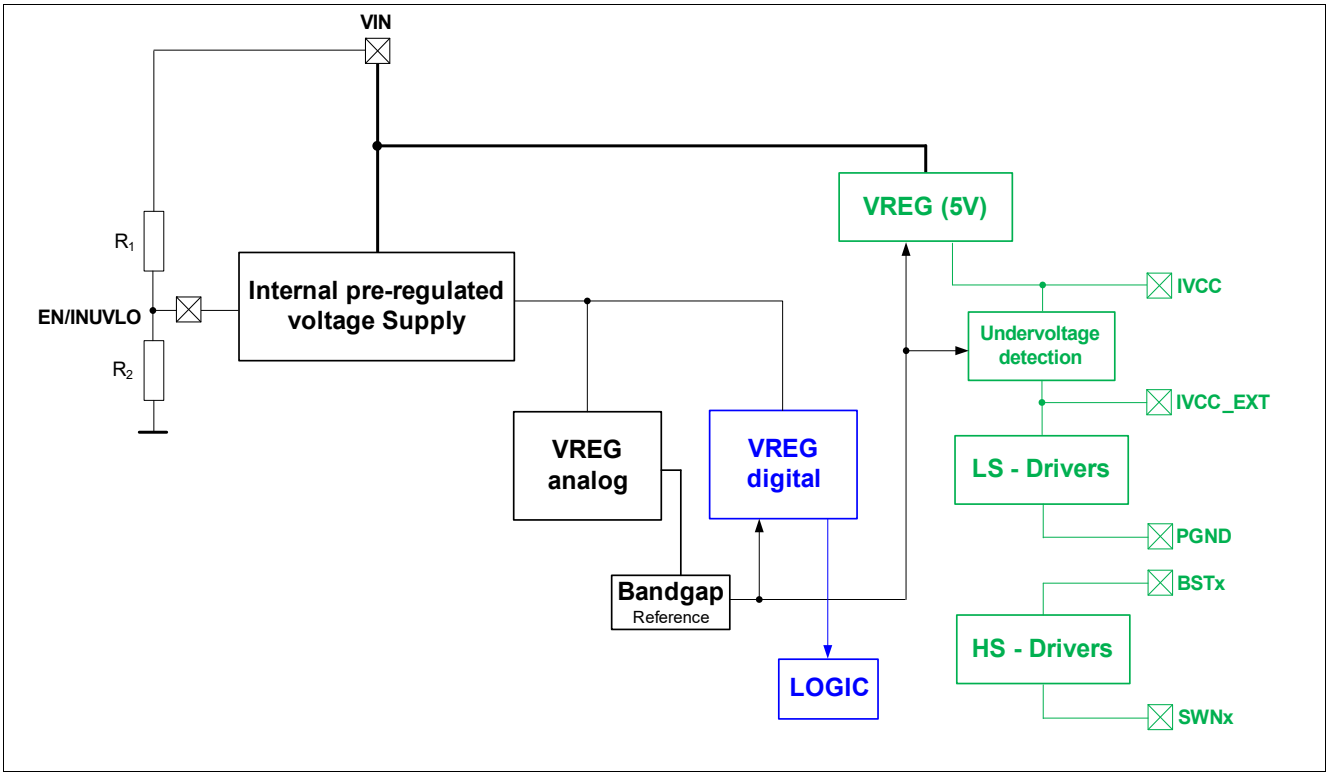


Figure 4 Power Supply Concept Drawing

Usage of EN/INUVLO pin in different applications

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold should be fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a µC-port as shown in (B) .

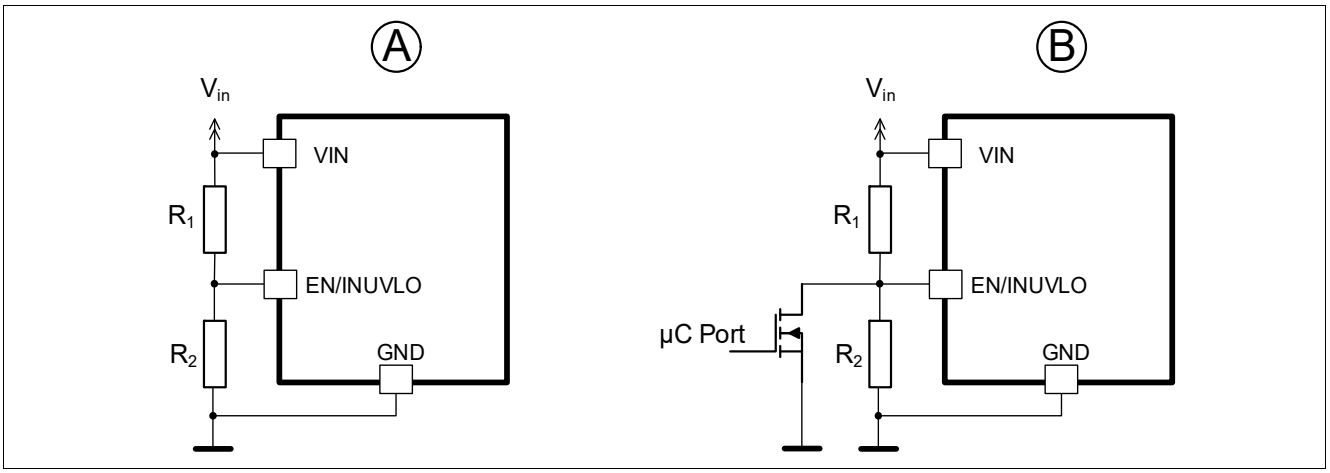


Figure 5 Usage of EN/INUVLO pin in different applications

5.1 Different Power States

TLD5190 has the following power states:

- SLEEP state
- IDLE state
- ACTIVE state

The transition between the power states is determined according to these variables after a filter time of max. 3 clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC_EXT level

The state diagram including the possible transitions is shown in **Figure 6**.

The Power-up condition is entered when the supply voltage V_{VIN} exceeds its minimum supply voltage threshold $V_{VIN(ON)}$.

SLEEP

When the TLD5190 is in the SLEEP state, all outputs are OFF, independently from the supply voltages V_{IN}, IVCC and IVCC_EXT. The current consumption is low. Refer to parameter: $I_{VIN(SLEEP)}$.

The transition from SLEEP to ACTIVE state requires a specified time: t_{ACTIVE}.

IDLE

In IDLE state the internal voltage regulator is working. Diagnosis functions are not available. The output drivers are switched OFF, independently from the supply voltages V_{IN}, IVCC and IVCC_EXT.

ACTIVE

In active state the device will start switching activity to provide power at the output only when PWMI = HIGH. To start the Highside gate drivers HSGD1,2 the voltage level $V_{BST1,2}$ - $V_{SWN1,2}$ needs to be above the threshold $V_{BST1,2}$ - $V_{SWN1,2\_UVth}$. In ACTIVE state the device current consumption via V_{IN} is dependent on the external MOSFET used and the switching frequency f_{SW}.

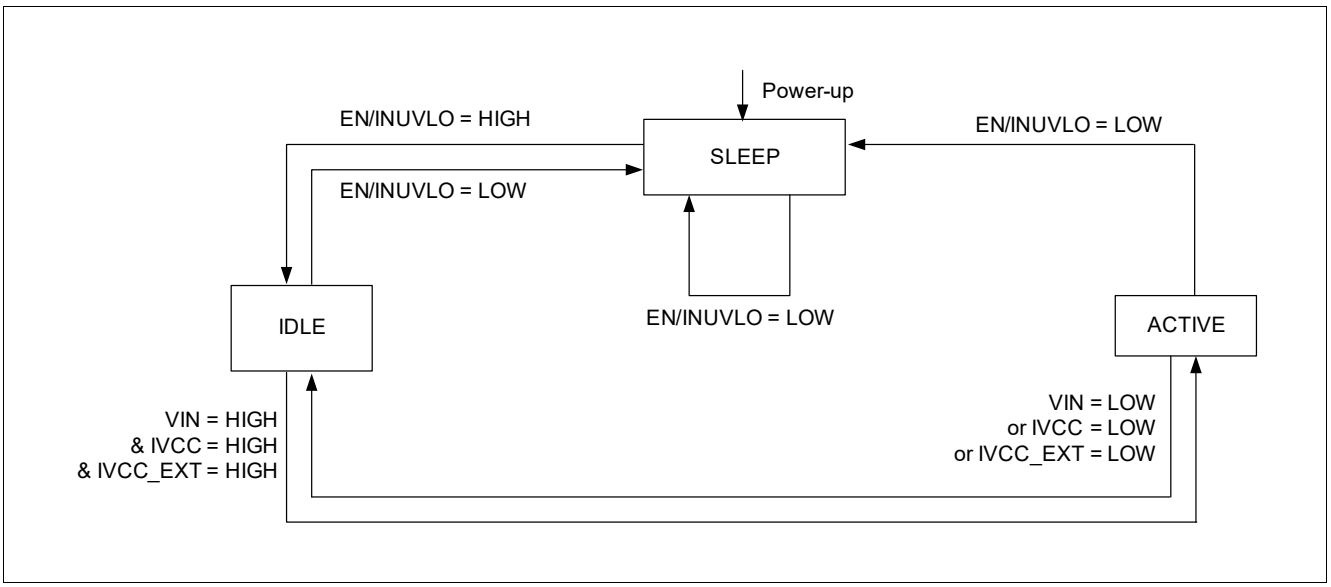


Figure 6 Simplified State Diagram

5.2 Electrical Characteristics

Table 5 EC Power Supply

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply V_{IN}							
Input Voltage Startup	$V_{VIN(ON)}$	–	–	4.7	V	V_{IN} increasing; $V_{EN/INUVLO}$ = HIGH; IVCC = IVCC_EXT = 0 mA;	P_5.3.1
Input Undervoltage switch OFF	$V_{VIN(OFF)}$	–	–	4.5	V	V_{IN} decreasing; $V_{EN/INUVLO}$ = HIGH; IVCC = IVCC_EXT = 10 mA;	P_5.3.14
Device operating current	$I_{VIN(ACTIVE)}$	–	4.4	6	mA	1)ACTIVE mode; CLKOUT freq. 300 KHz; V_{PWMI} = 0 V;	P_5.3.2
V_{IN} Sleep mode supply current	$I_{VIN(SLEEP)}$	–	–	1.5	µA	$V_{EN/INUVLO}$ = 0 V; V_{IN} = 13.5 V; V_{IVCC} = V_{IVCC_EXT} = 0 V;	P_5.3.3
EN/INUVLO Pin characteristics							
Input Undervoltage falling Threshold	$V_{EN/INUVLOth}$	1.6	1.75	1.9	V	–	P_5.3.7
EN/INUVLO Rising Hysteresis	$V_{EN/INUVLO(hyst)}$	–	90	–	mV	1)	P_5.3.8
EN/INUVLO input Current LOW	$I_{EN/INUVLO(LOW)}$	0.45	0.89	1.34	µA	$V_{EN/INUVLO}$ = 0.8 V;	P_5.3.9
EN/INUVLO input Current HIGH	$I_{EN/INUVLO(HIGH)}$	1.1	2.2	3.3	µA	$V_{EN/INUVLO}$ = 2 V;	P_5.3.10
Timings							
SLEEP mode to ACTIVE time	t_{ACTIVE}	–	–	0.7	ms	1) V_{IVCC} = V_{IVCC_EXT}; C_{IVCC} = 10 µF; V_{IN} = 13.5 V;	P_5.3.11

1) Not subject to production test, specified by design.

6 Regulator Description

The TLD5190 includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A voltage mode regulation can also be implemented (Refer to **Chapter 6.6**).

It is designed to control 4 gate driver outputs in a H-Bridge topology by using only one inductor and 4 external MOSFETs. This topology is able to operate in high power BOOST, BUCK-BOOST and BUCK mode applications with maximum efficiency.

The transition between the different regulation modes is done automatically by the device itself, with respect to the application boundary conditions.

The transition phase between modes is seamless.

6.1 Regulator Diagram Description

The TLD5190 includes two analog current control inputs (IIN1, IIN2) to limit the maximum Input current (Block A1 and A7 in **Figure 7**).

A second analog current control loop (A5, A6 with complessive gain = $IFBx_{gm}$) connected to the sensing pins FBL, FBH regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network (R_{COMP}, C_{COMP}) is used to adjust the control loop to various application boundary conditions.

The inductor current for the current mode loop is sensed by the R_{SWCS} resistor.

R_{SWCS} is used also to limit the maximum external switches / inductor current.

If the Voltage across R_{SWCS} exceeds its overcurrent threshold (V_{SWCS_buck} or V_{SWCS_boost} for buck or boost operation respectively) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC) provides a PWM signal to four internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs in an H-Bridge setup . Once the soft start expires a forced CCM regulation mode is performed.

The control loop block diagram displayed in **Figure 7** shows a typical constant current application. The voltage across R_{FB} sets the output current. R_{IN} is used to fix the maximum input current.

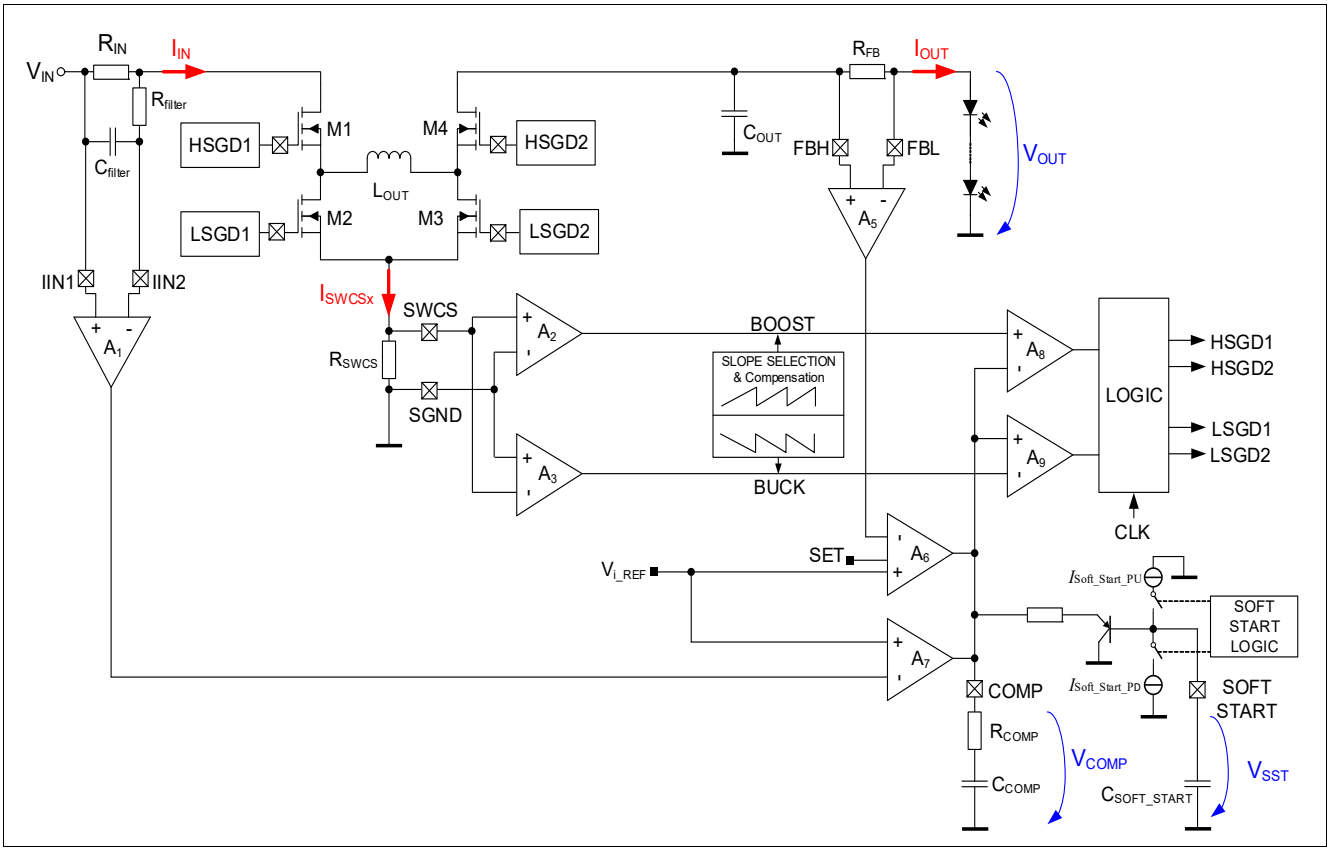


Figure 7 Regulator block diagram with soft start circuitry - TLD5190

6.2 Adjustable Soft Start Ramp

The soft start routine has 2 functionalities:

- Fault management: fault mask and wait-before-retry time (**Figure 8** and chapter **Chapter 10.2**)
- Limit input inrush current and output overshoots by limiting Vcomp (**Figure 7**) in boost mode

The soft start routine is applied:

- At first turn on (first PWM rise after EN = High)
- After Output Short to GND or Open Load detection
- After Input Overvoltage detection

The soft start routine is active during the rising and falling edges of the VSST. The soft start timing is defined by a capacitor placed at the SOFT_START pin and the pull-up and pull down current sources ($I_{Soft\_Start\_PU}$, $I_{Soft\_Start\_PD}$).

Minimum value for soft start capacitor has to be designed such that, at startup, the output voltage exceeds the short to ground threshold (VFB pin exceeds $V_{VFB\_S2G\_INC}$), before the soft start voltage reaches $V_{SOFT\_START\_LOFF}$. Minimum temperature and minimum input voltage shall be considered as worst case condition for previously mentioned dimensioning.

Soft Start rising edge time is approximately:

$$t_{SOFT\_START} = V_{Soft\_Start\_LOFF} \cdot \frac{C_{Soft\_Start}}{I_{Soft\_Start\_PU}} \quad (6.1)$$

The Soft Start routine limits the inrush current by clamping the COMP pin through a buffer as in **Figure 7**. Therefore this functionality is effective only when soft start capacitor is sufficiently larger than the COMP capacitor and its effect is visible mainly in buck-boost and boost regulation mode.

If an open load or a short circuit on the output is detected, a pull-down current source $I_{SOFT\_START\_PD}$ (P_6.4.20) is activated. This current brings down the V_{SOFT_START} until $V_{SOFT\_START\_RESET}$ (P_6.4.22) is reached. Afterwards the pull-up current source $I_{SOFT\_START\_PU}$ (P_6.4.19) turns on again. If the fault condition hasn't been removed until $V_{SOFT\_START\_LOFF}$ (P_6.4.21) is reached, the pull-down current source turns back on again, initiating a new cycle. During the soft start rise time the device is switching, during fall time the device is halted (**Figure 8**).This hiccup mode will continue until the fault is removed.

It is possible to latch the fault condition on the TLD5190 by sourcing a current higher than SOFT_START_PD, through a pull-up resistor connected from VREF to the SOFT START pin. In this condition the device will restart regulating only if EN/INUVLO pin is toggled.

If an input overvoltage is detected the soft start is kept low as long as the overvoltage remains.

At first PWMI rise after EN = High, the internal PWM signal is extended until one of the two following conditions is reached:

- Until V_{SOFT_START} exceeds $V_{Soft\_Start\_LOFF}$
- Until $V_{FBH\text{-}FBL}$ exceeds $V_{FBH\_FBL\_OL}$

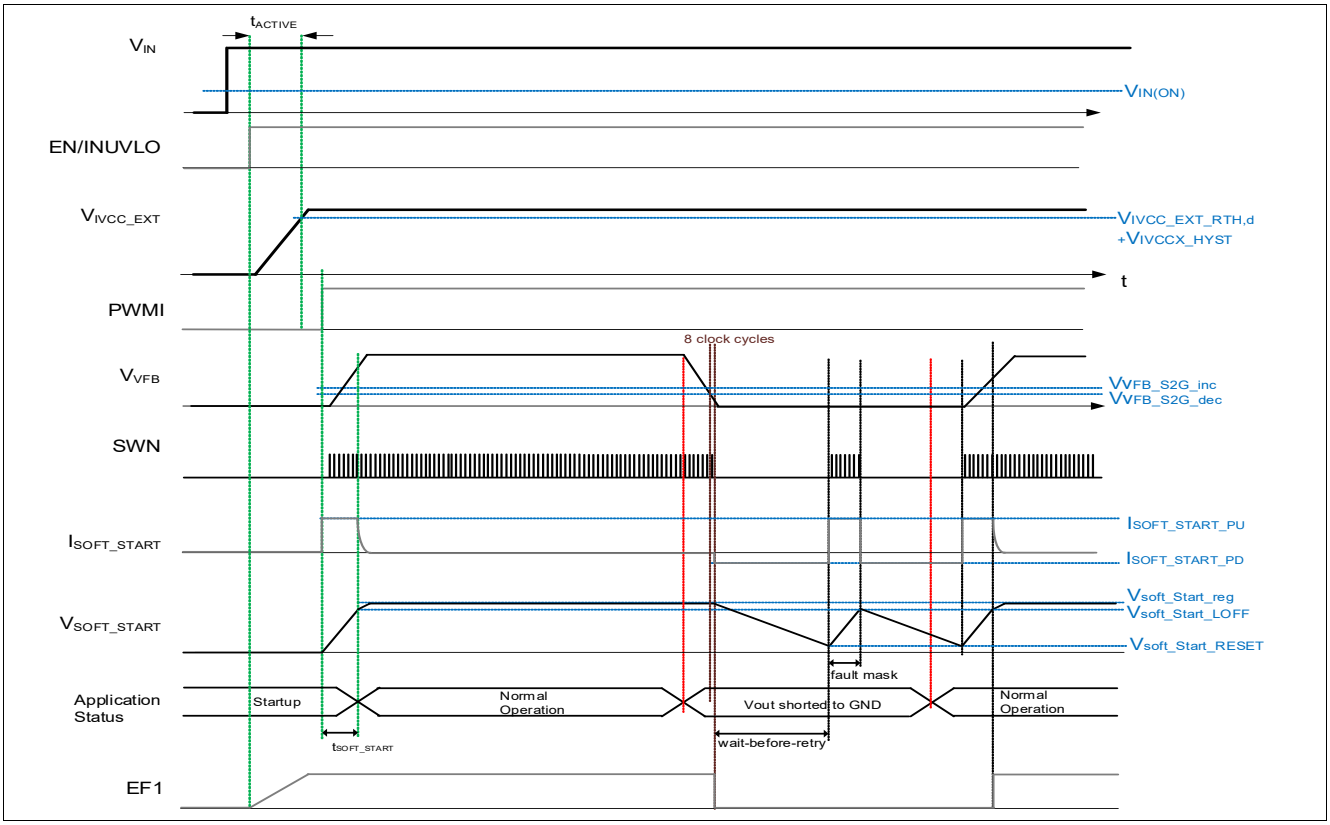


Figure 8 Soft Start timing diagram on a short to ground detected by the VFB pin

6.3 Switching Frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND or by supplying a sync signal as specified in chapter **Chapter 11.2**. Select the switching frequency with an external resistor according to the graph in **Figure 9** or the following approximate formulas.

$$f_{SW}[kHz] = 5375 * (R_{FREQ}[k\Omega])^{-0.8} \quad (6.2)$$

$$R_{FREQ}[k\Omega] = 46023 * (f_{SW}[kHz])^{-1.25} \quad (6.3)$$

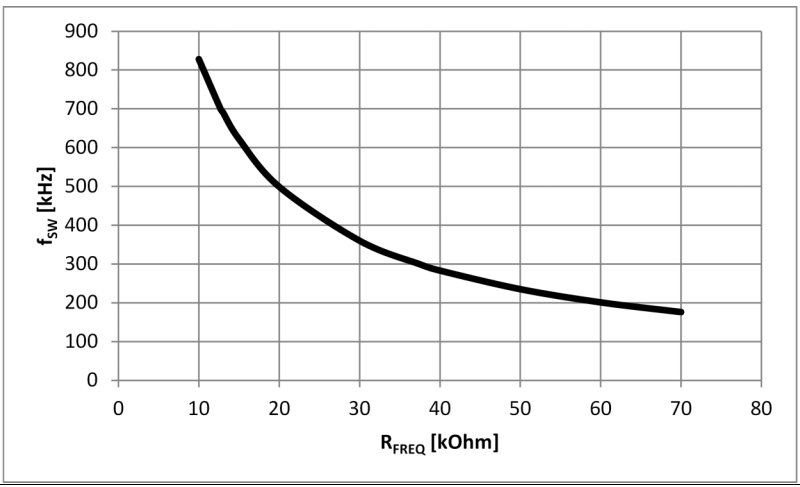


Figure 9 Switching Frequency f_{SW} versus Frequency Select Resistor to GND R_{FREQ}

6.4 Operation of 4 switches H-Bridge architecture

Inductor L_{OUT} connects in an H-Bridge configuration with 4 external N channel MOSFETs (M1, M2, M3 & M4)

- Transistor M1 and M3 provides a path between V_{IN} and ground through L_{OUT} in one direction (Driven by top and bottom gate drivers HSGD1 and LSGD2)
- Transistor M2 and M4 provides a path between VOUT and ground through L_{OUT} in the other direction (Driven by top and bottom gate drivers HSGD2 and LSGD1)
- Nodes SWN1, SWN2, voltage across R_{SWCS}, input and load currents are also monitored by the TLD5190

	BOOST MODE	**BUCK-BOOST** MODE	**BUCK** MODE
M1	ON	PWM	PWM
M2	OFF	PWM	PWM
M3	PWM	PWM	OFF
M4	PWM	PWM	ON

Figure 10 4 switches H-Bridge architecture Transistor Status summary

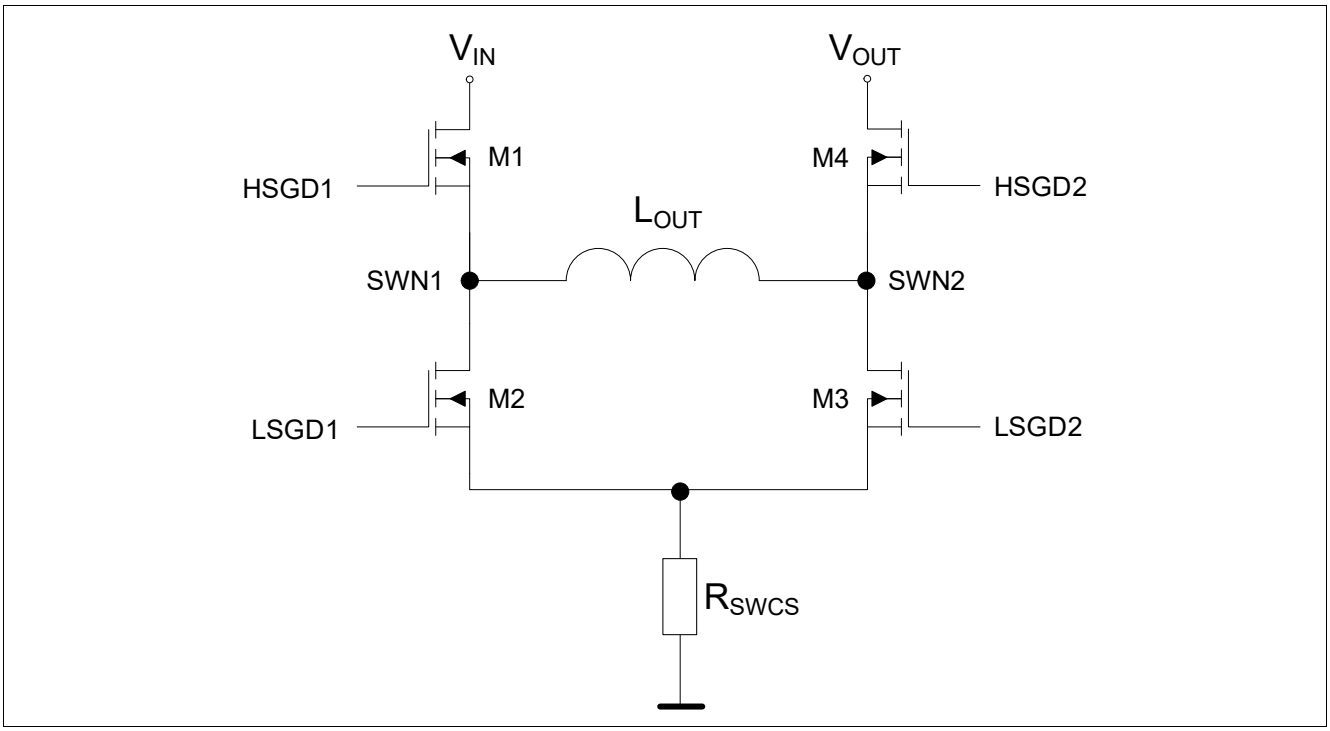


Figure 11 4 switches H-Bridge architecture overview

6.4.1 Boost mode ($V_{IN} < V_{OUT}$)

- M1 is always ON, M2 is always OFF
- Every cycle M3 turns ON first and inductor current is sensed (peak current control)
- M3 stays ON until the upper reference threshold is reached across R_{SWCS} (Energizing)

- M3 turns OFF, M4 turns ON until the end of the cycle (Recirculation)
- Switches M3 and M4 alternate, behaving like a typical synchronous boost Regulator (see **Figure 12**)

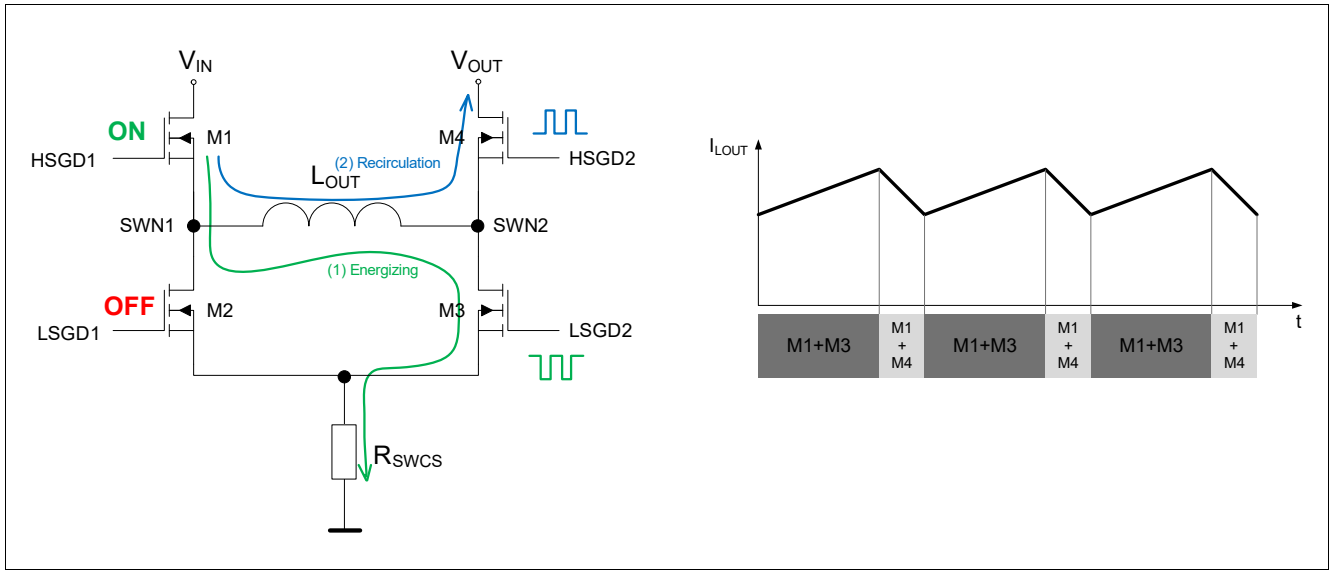


Figure 12 4 switches H-Bridge architecture in BOOST mode

Simplified comparison of 4 switches H-Bridge architecture to traditional asynchronous Boost approach.

- M2 is always OFF in this mode (open)
- M1 is always ON in this mode (closed connection of inductor to V_{IN})
- M4 acts as a synchronous diode, with significantly lower conduction power losses (I^2 x R_{DSON} vs. 0.7 V x I)

Note: Diode is source of losses and lower system efficiency!

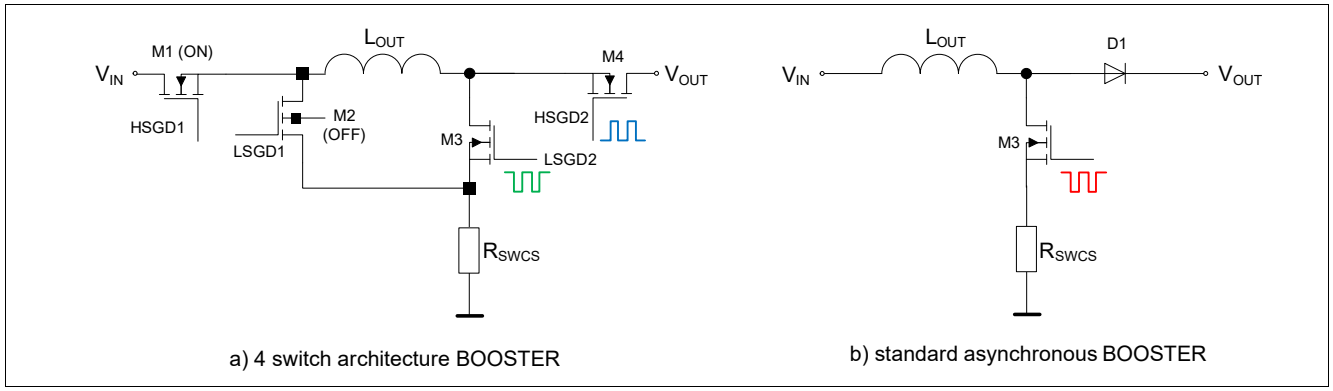


Figure 13 4 switches H-Bridge architecture in BOOST mode compared to standard async Booster

6.4.2 Buck mode (V_{IN} > V_{OUT})

- M4 is always ON, M3 is always OFF
- Every cycle M2 turns ON and inductor current is sensed (valley current control)
- M2 stays ON until the lower reference threshold is reached across R_{SWCS} (Recirculation)

- M2 turns OFF, M1 turns ON until the end of the cycle (Energizing)
- Switches M1 and M2 alternate, behaving like a typical synchronous BUCK Regulator (see **Figure 14**)

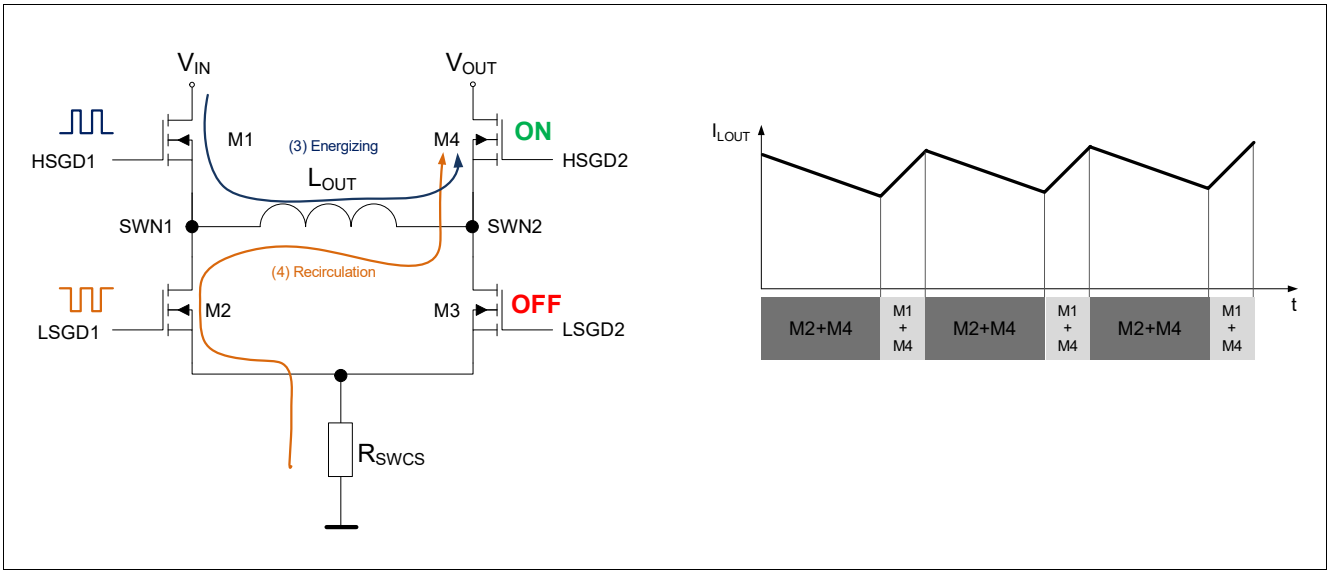


Figure 14 4 switches H-Bridge architecture in BUCK mode

Simplified comparison of 4 switches architecture to traditional asynchronous Buck approach.

- M3 is always OFF in this mode (open).
- M4 is always ON in this mode (closed connection inductor to V_{OUT}).
- M2 acts as a synchronous diode, with significantly lower conduction losses (I^2 x R_{DSON} vs. 0.7 V x I)

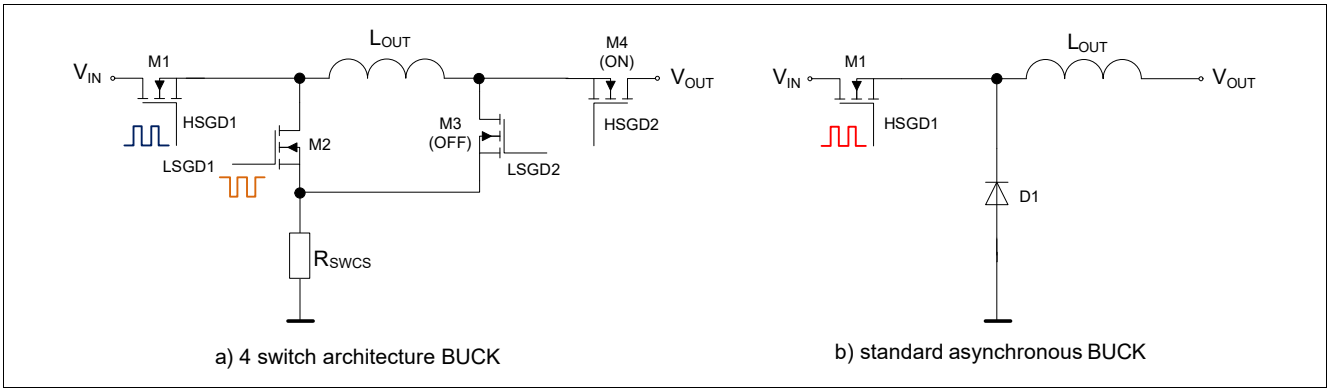


Figure 15 4 switches H-Bridge architecture in BUCK mode compared to standard async BUCK

6.4.3 Buck-Boost mode (V_{IN} ~ V_{OUT})

- When V_{IN} is close to V_{OUT} the controller is in Buck-Boost operation
- All switches are switching in buck-boost operation. The direct energy transfer from the Input to the output (M1+M4 = ON) is beneficial to reduce ripple current and improves the energy efficiency of the Buck-Boost control scheme
- The two buck boost waveforms and switching behaviors are displayed in **Figure 16** below

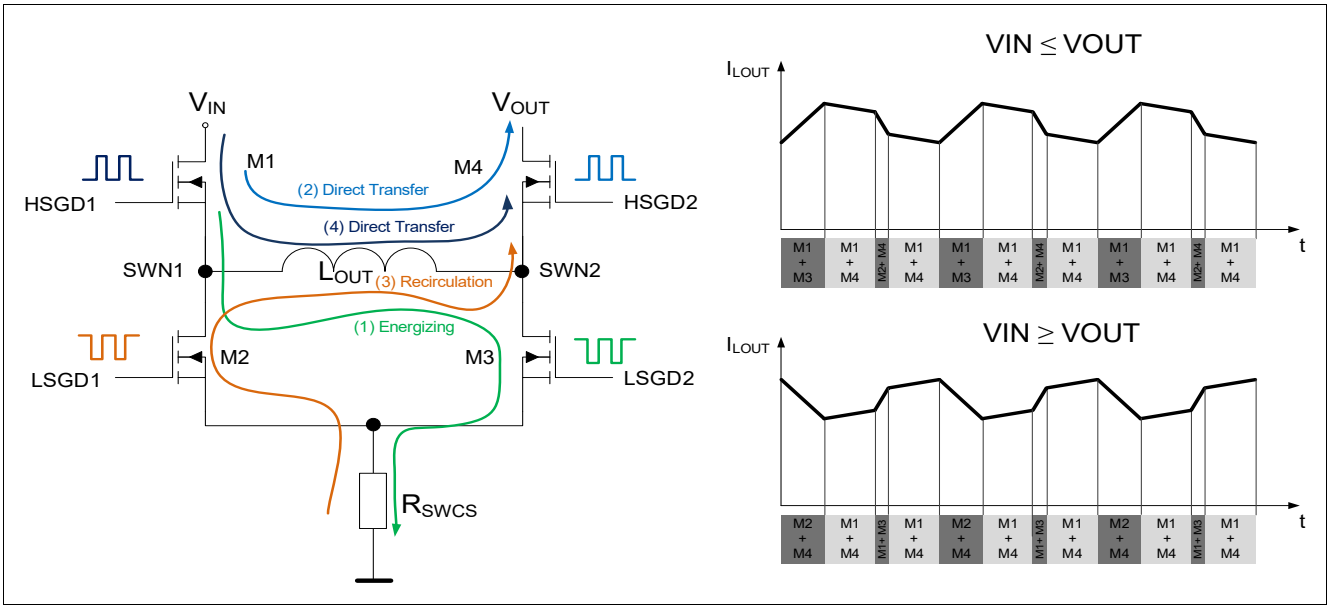


Figure 16 4 switches H-Bridge architecture in BUCK-BOOST mode

6.5 Flexible current sense

The flexible current sense implementation enables highside and lowside current sensing.

The **Figure 17** displays the application examples for the highside and lowside current sense concept.

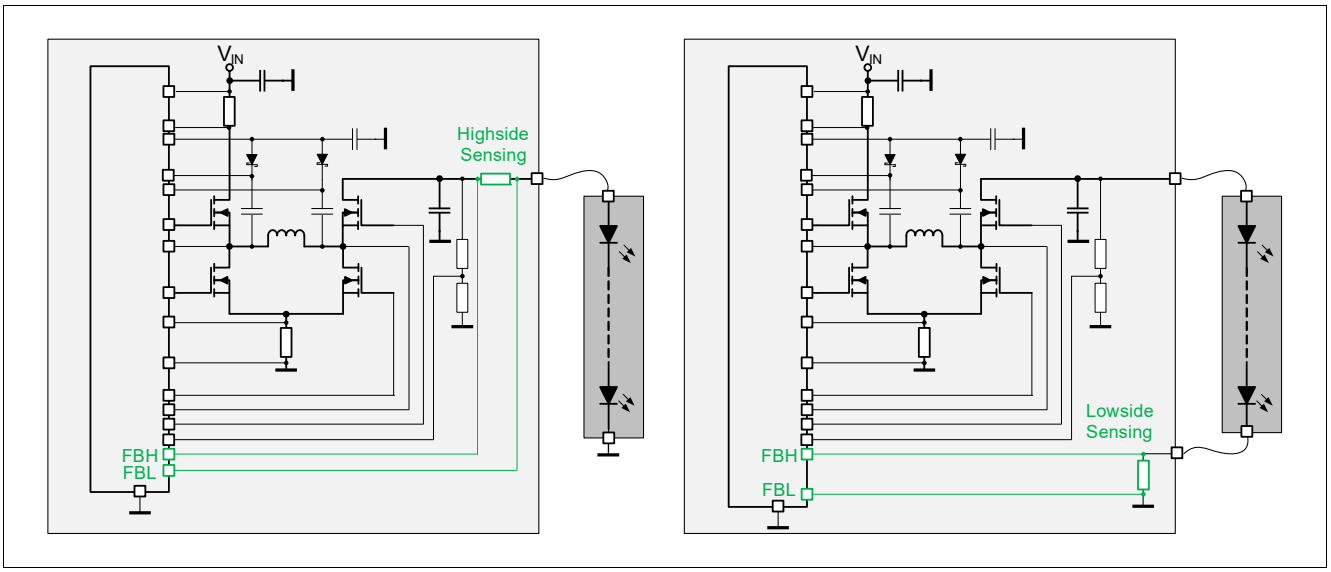


Figure 17 Highside and lowside current sensing - TLD5190

6.6 Programming Output Voltage (Constant Voltage Regulation)

For a voltage regulator, the output voltage can be set by selecting the values R_{FB1}, R_{FB2} and R_{FB3} according to the following **Equation (6.4)**:

$$V_{OUT} = \left(I_{FBH} + \frac{V_{FBH-FBL}}{R_{FB2}} \right) \cdot R_{FB1} + \left(\frac{V_{FBH-FBL}}{R_{FB2}} - I_{FBL} \right) \cdot R_{FB3} + V_{FBH-FBL} \quad (6.4)$$

If Analog dimming is performed, due to the variations on the I_{FBL} (I_{FBL_HSS} (P_6.4.9) and I_{FBL_LSS} (P_6.4.40)) current on the entire voltage spanning, a non linearity on the output voltage may be observed. To minimize this effect RFBx resistors should be properly dimensioned.

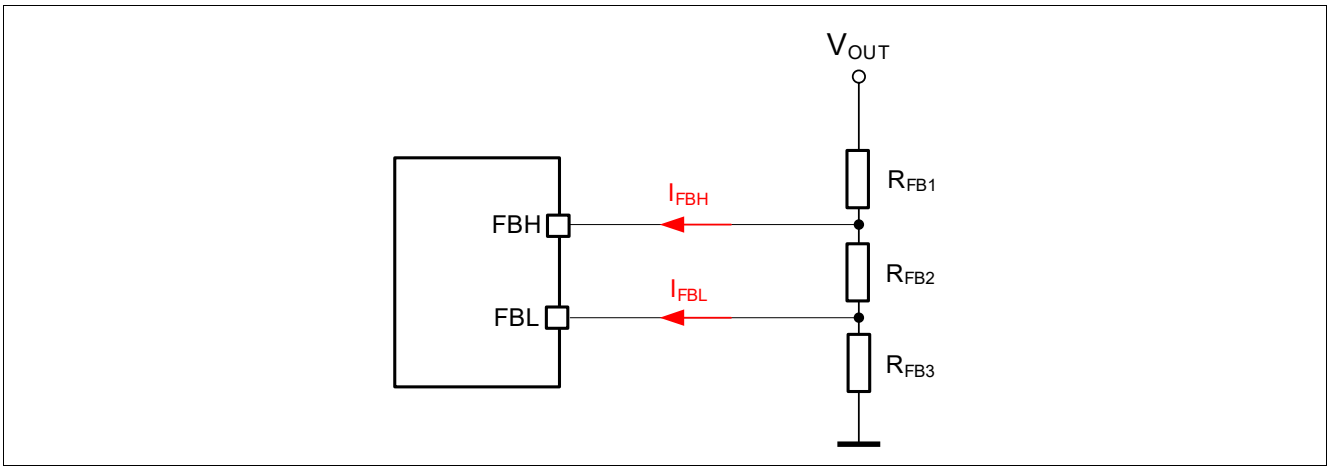


Figure 18 Programming Output Voltage (Constant Voltage Regulation)

6.7 Electrical Characteristics

Table 6 EC Regulator

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator:							
$V_{(FBH-FBL)}$ threshold	$V_{(FBH-FBL)}$	145.5	150	154.5	mV	V_{SET} = 2 V;	P_6.4.1
$V_{(FBH-FBL)}$ threshold @ analog dimming 10%	$V_{(FBH-FBL)\_10}$	10	15	20	mV	V_{SET} = 0.32 V;	P_6.4.6
FBH Bias current @ highside sensing setup	I_{FBH_HSS}	65	110	155	µA	1) V_{FBL} = 7 V; $V_{FBH - FBL}$ = 150 mV;	P_6.4.8
FBL Bias current @ highside sensing setup	I_{FBL_HSS}	17	30	43	µA	1) V_{FBL} = 7 V; $V_{FBH - FBL}$ = 150 mV;	P_6.4.9
FBH Bias current @ lowside sensing setup	I_{FBH_LSS}	-7.5	-4	-2.5	µA	1) V_{FBL} = 0 V; $V_{FBH - FBL}$ = 150 mV;	P_6.4.39
FBL Bias current @ lowside sensing setup	I_{FBL_LSS}	-45	-30	-20	µA	1) V_{FBL} = 0 V; $V_{FBH - FBL}$ = 150 mV;	P_6.4.40
FBH-FBL High Side sensing entry threshold	$V_{FBH\_HSS\_inc}$	-	2	-	V	1) V_{FBH1} increasing;	P_6.9.1
FBH-FBL High Side sensing exit threshold	$V_{FBH\_HSS\_dec}$	-	1.75	-	V	1) V_{FBH} decreasing;	P_6.9.2
OUT Current sense Amplifier g_m	$IFBx_{gm}$	–	890	–	µS	1)	P_6.4.10
Output Monitor Voltage	$V_{IOUTMON}$	1.33	1.4	1.47	V	$V_{FBH - FBL}$ = 150 mV;	P_6.4.11
Maximum BOOST Duty Cycle	D_{BOOST_MAX}	89	91	93	%	1) f_{sw} = 300 kHZ;	P_6.4.12
Input Current Sense threshold $V_{IIN1-IIN2}$	$V_{IIN1-IIN2}$	46	50	54	mV	–	P_6.4.13
Input Current sense Amplifier g_m	I_{IN_gm}	–	2.12	–	mS	1)	P_6.4.14
Input current Monitor Voltage	V_{IINMON}	0.95	1	1.05	V	1) $V_{IIN1 - IIN2}$ = 50 mV; $V_{IIN1} = V_{VIN(ON)}$ to 55 V;	P_6.4.15
Switch Peak Over Current Threshold - BOOST	V_{SWCS_boost}	40	50	60	mV	1)	P_10.8.15
Switch Peak Over Current Threshold - BUCK	V_{SWCS_buck}	-60	-50	-40	mV	1)	P_10.8.16
Soft Start							
Soft Start pull up current	$I_{Soft\_Start\_PU}$	22	26	32	µA	V_{Soft_Start} = 1 V;	P_6.4.19
Soft Start pull down current	$I_{Soft\_Start\_PD}$	2.2	2.6	3.2	µA	V_{Soft_Start} = 1 V;	P_6.4.20

Table 6 EC Regulator (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Soft Start Latch-OFF Threshold	$V_{Soft\_Start\_LOFF}$	1.65	1.75	1.85	V	–	P_6.4.21
Soft Start Reset Threshold	$V_{Soft\_Start\_RESET}$	0.1	0.2	0.3	V	–	P_6.4.22
Soft Start Voltage during regulation	$V_{Soft\_Start\_reg}$	1.9	2	2.1	V	[1] No Faults	P_6.9.3
Oscillator							
Switching Frequency	f_{SW}	285	300	315	kHz	T_j = 25°C; R_{FREQ}= 37.4 kΩ;	P_6.4.23
SYNC Frequency	f_{SYNC}	200	–	700	kHz	–	P_6.4.24
SYNC Turn On Threshold	$V_{SYNC,ON}$	2	–	–	V	–	P_6.4.25
SYNC Turn Off Threshold	$V_{SYNC,OFF}$	–	–	0.8	V	–	P_6.4.26
SYNC High Input Current	$I_{SYNC,H}$	15	30	45	µA	V_{SYNC} = 2.0 V;	P_6.4.62
SYNC Low Input Current	$I_{SYNC,L}$	6	12	18	µA	V_{SYNC} = 0.8 V;	P_6.4.63
Gate Driver for external Switch							
Gate Driver undervoltage threshold VBST1,2-VSWN1,2_UVth	$V_{BST1,2}$-$V_{SWN1,2\_UVth}$	3.4	–	4	V	$V_{BST1,2}$ - $V_{SWN1,2}$ decreasing;	P_6.4.64
HSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)HS}$	1.4	2.3	3.7	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{source} = 100 mA;	P_6.4.28
HSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)HS}$	0.6	1.2	2.2	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{sink} = 100 mA;	P_6.4.29
LSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)LS}$	1.4	2.3	3.7	Ω	V_{IVCC_EXT} = 5 V; I_{source} = 100 mA;	P_6.4.30
LSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)LS}$	0.4	1.2	1.8	Ω	V_{IVCC_EXT} = 5 V; I_{sink} = 100 mA;	P_6.4.31
HSGD1,2 Gate Driver peak sourcing current	$I_{HSGD1,2\_SRC}$	380	–	–	mA	[1] $V_{HSGD1,2}$ - $V_{SWN1,2}$ = 1 V to 4 V; $V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V	P_6.4.32
HSGD1,2 Gate Driver peak sinking current	$I_{HSGD1,2\_SNK}$	410	–	–	mA	[1] $V_{HSGD1,2}$ - $V_{SWN1,2}$ = 4 V to 1 V; $V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V	P_6.4.33

Table 6 EC Regulator (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
LSGD1,2 Gate Driver peak sourcing current	$I_{LSGD1,2\_SRC}$	370	–	–	mA	1) $V_{LSGD1,2}$ = 1 V to 4 V; V_{IVCC_EXT} = 5 V;	P_6.4.34
LSGD1,2 Gate Driver peak sinking current	$I_{LSGD1,2\_SNK}$	550	–	–	mA	1) $V_{LSGD1,2}$ = 4 V to 1 V; V_{IVCC_EXT} = 5 V;	P_6.4.35
LSGD1,2 OFF to HSGD1,2 ON delay	$t_{LSOFF-HSON\_delay}$	15	30	40	ns	1)	P_6.4.36
HSGD1,2 OFF to LSGD1,2 ON delay	$t_{HSOFF-LSON\_delay}$	35	60	75	ns	1)	P_6.4.37

1) Not subject to production test, specified by design

7 Digital Dimming Function

PWM dimming is adopted to vary LEDs brightness with greatly reduced chromaticity shift. PWM dimming achieves brightness reduction by varying the duty cycle of a constant current in the LED string.

7.1 Description

A PWM signal can be transmitted to the TLD5190 as described below.

PWM via direct interface

The PWMI pin can be fed with a pulse width modulated (PWM) signals, this enables when HIGH and disables when LOW the gate drivers of the main switches.

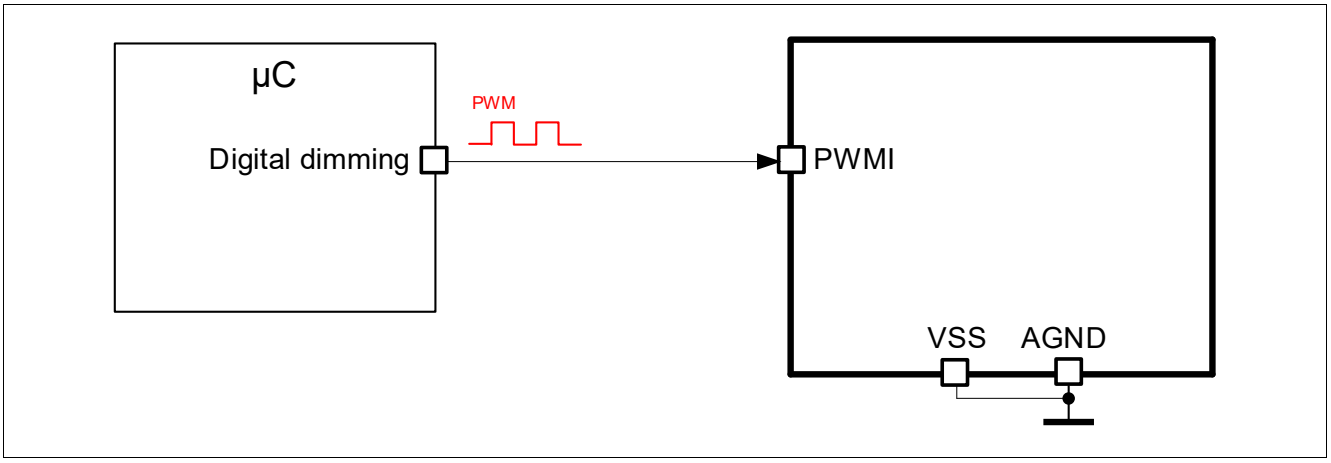


Figure 19 Digital Dimming Overview

To avoid unwanted output overshoots due to not soft start assisted startups, PWM dimming in LOW state should not be used to suspend the output current for long time intervals. To stop in a safe manner EN/INUVLO=LOW can be used.

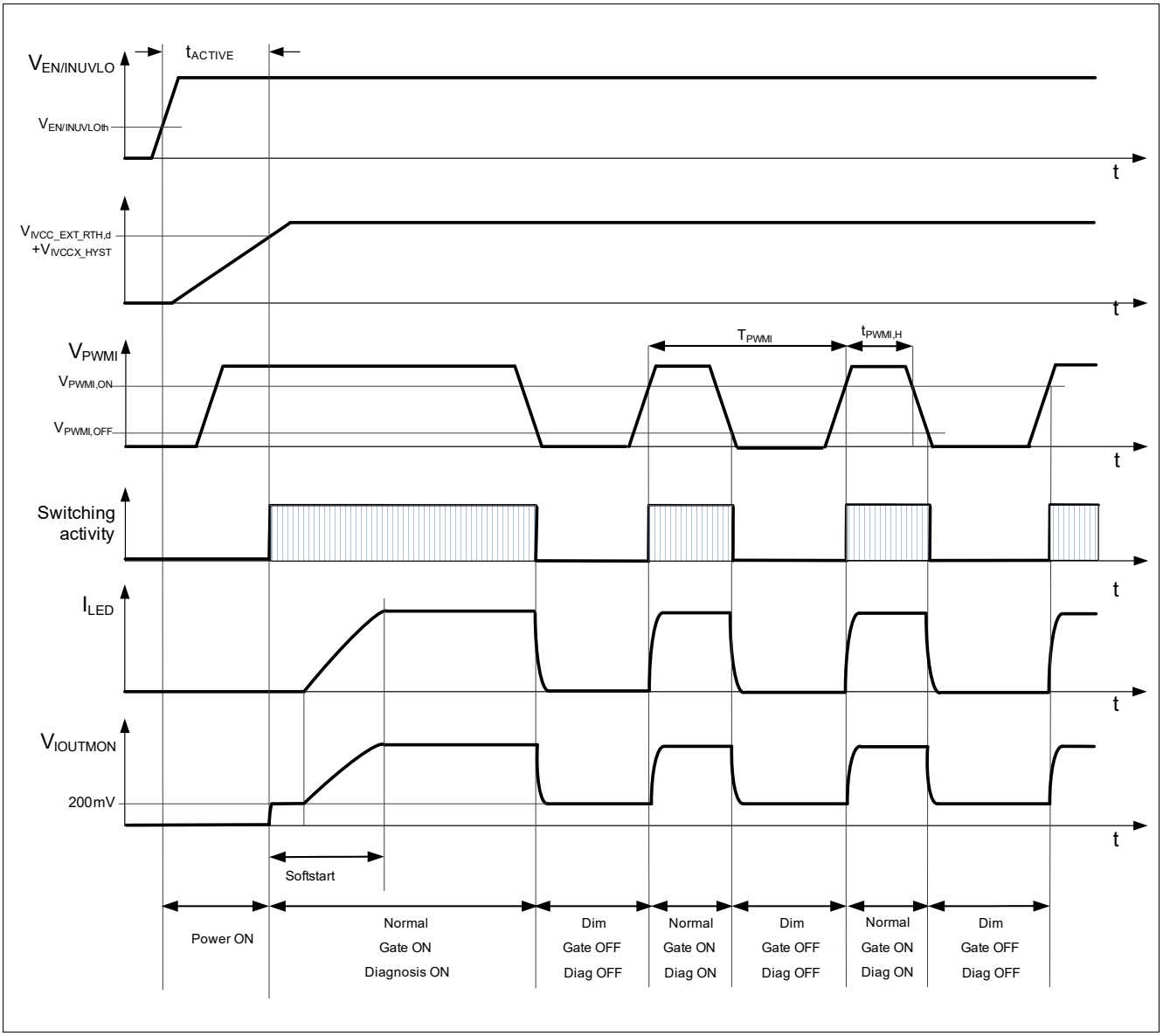


Figure 20 Timing Diagram LED Dimming and Start up behavior example (V_{VIN} stable in the functional range and not during startup)

7.2 Electrical Characteristics

Table 7 EC Digital Dimming

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI Input:							
PWMI Turn On Threshold	$V_{PWMI,ON}$	2	–	–	V	–	P_7.2.1
PWMI Turn Off Threshold	$V_{PWMI,OFF}$	–	–	0.8	V	–	P_7.2.2
PWMI High Input Current	$I_{PWMI,H}$	15	30	45	µA	V_{PWMI} = 2.0 V;	P_7.2.4
PWMI Low Input Current	$I_{PWMI,L}$	6	12	18	µA	V_{PWMI} = 0.8 V;	P_7.2.5

8 Analog Dimming

The analog dimming feature allows further control of the output current. This approach is used to:

- Reduce the default current in a narrow range to adjust to different binning classes of the used LEDs.
- Adjust the load current to enable the usage of one hardware for several LED types where different current levels are required.
- Reduce the current at high temperatures (protect LEDs from overtemperature).
- Reduce the current at low input voltages (for example, cranking-pulse breakdown of the supply or power derating).

8.1 Description

The analog dimming feature is adjusting the average load current level via the control of the feedback error Amplifier voltage ($V_{FBH-FBL}$).

The SET pin is used to adjust the mean output current/voltage. The V_{SET} range where analog dimming is enabled is from 200 mV to 1.5 V. Different application scenarios are described in **Figure 22**.

Using the SET pin to adjust the output current:

For the calculation of the output current I_{OUT} the following **Equation (8.1)** is used:

$$I_{OUT} = \frac{V_{FBH} - V_{FBL}}{R_{FB}} \quad (8.1)$$

A decrease of the average output current can be achieved by controlling the voltage at the SET pin (V_{SET}) between 0.2 V and 1.4 V. The mathematical relation is given in the **Equation (8.2)** below:

$$I_{OUT} = \frac{V_{SET} - 200\ mV}{R_{FB} \cdot 8} \quad (8.2)$$

If V_{SET} is 200 mV (typ.) the LED current is only determined by the internal offset voltages of the comparators. To assure the switching activity is stopped and $I_{OUT} = 0$, V_{SET} has to be < 100 mV, see **Figure 21**.

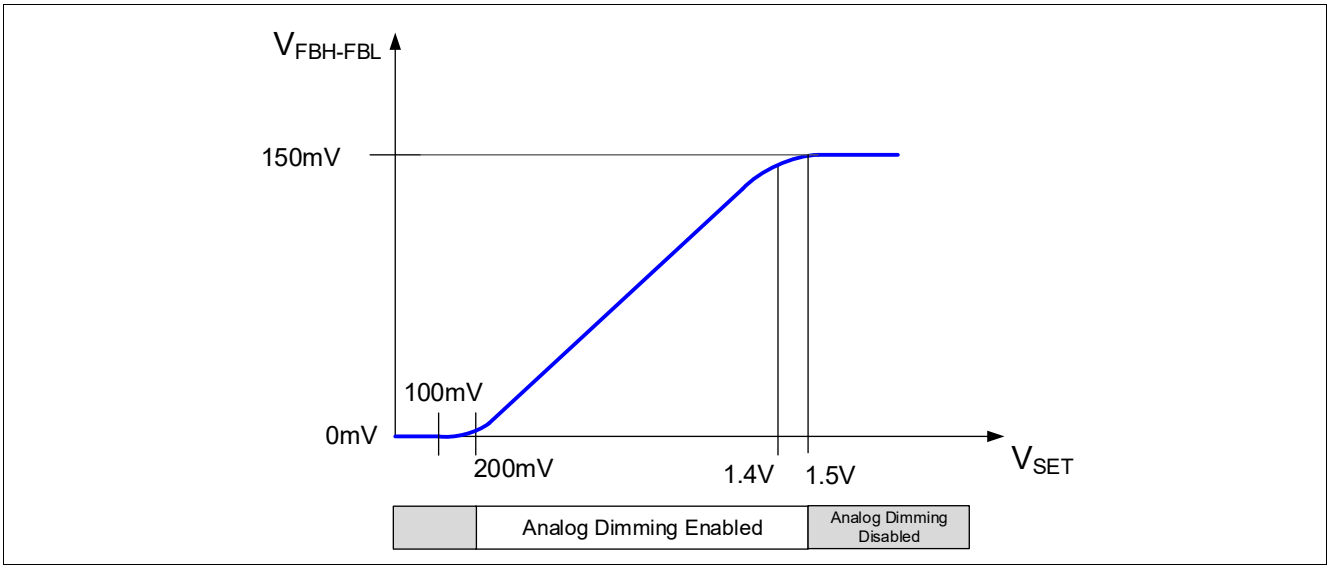


Figure 21 Analog Dimming Overview

Multi-purpose usage of the Analog dimming feature

1) A µC integrated digital analog converter (DAC) output or a stand alone DAC can be used to supply the SET pin of the TLD5190.

2) The usage of an external resistor divider connected between V_{REF} (accurate regulated supply output) SET and GND can be chosen for systems without µC on board. The concept allows control of the LED current by placing low power resistors.

3) Furthermore a temperature sensitive resistor (Thermistor) to protect the LED loads from thermal destruction can be connected.

4) If the analog dimming feature is not needed, the SET pin should be connected to the VREF pin.

5) Instead of a DAC, the µC can provide a PWM signal and an external R-C filter to produce a constant voltage for the analog dimming. The voltage level depends on the PWM frequency (f_{PWM}) and duty cycle which can be controlled by the µc software after reading the coding resistor placed on the LED module.

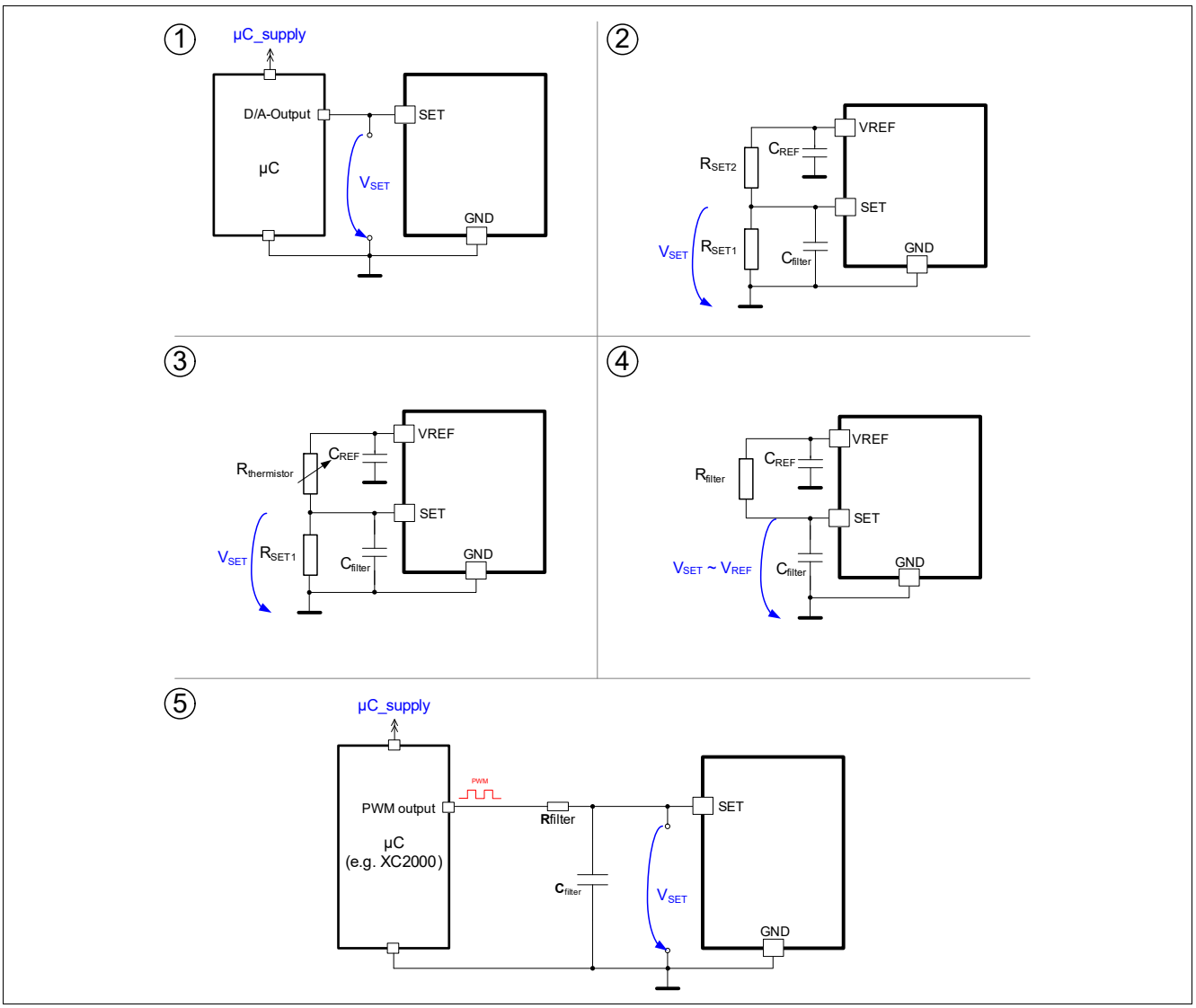


Figure 22 Different use cases for analog dimming pin SET

8.2 Electrical Characteristics

Table 8 EC Analog Dimming

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Source current on SET Pin	I_{SET_source}	–	–	1	µA	[1] V_{SET} = 0.2 V to 1.4 V;	P_8.3.4

1) Specified by design: not subject to production test.

9 Linear Regulator

The TLD5190 features an integrated voltage regulator for the supply of the internal gate driver stages. Furthermore an external voltage regulator can be connected to the IVCC_EXT pin to achieve an alternative gate driver supply if required.

9.1 IVCC Description

When the IVCC pin is connected to the IVCC_EXT pin, the internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to I_{LIM} (P_9.2.2). An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor (**Figure 23**, drawing A). Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches. A minimum capacitance value is given in parameter C_{IVCC} (P_9.2.4).

Alternative IVCC_EXT Supply Concept:

The IVCC_EXT pin can be used for an external voltage supply to alternatively supply the MOSFET Gate drivers. This concept is beneficial in the high input voltage range to avoid power losses in the IC (**Figure 23**, drawing B).

Integrated undervoltage protection for the external switching MOSFET:

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage. This undervoltage reset threshold circuit will turn OFF the gate drivers in case the IVCC or IVCC_EXT voltage falls below their undervoltage Reset switch OFF Thresholds $V_{IVCC\_RTH,d}$ (P_9.2.9) and $V_{IVCC\_EXT\_RTH,d}$ (P_9.2.5).

The Undervoltage Reset threshold for the IVCC and the IVCC_EXT pins help to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of the external logic level N-channel MOSFETs.

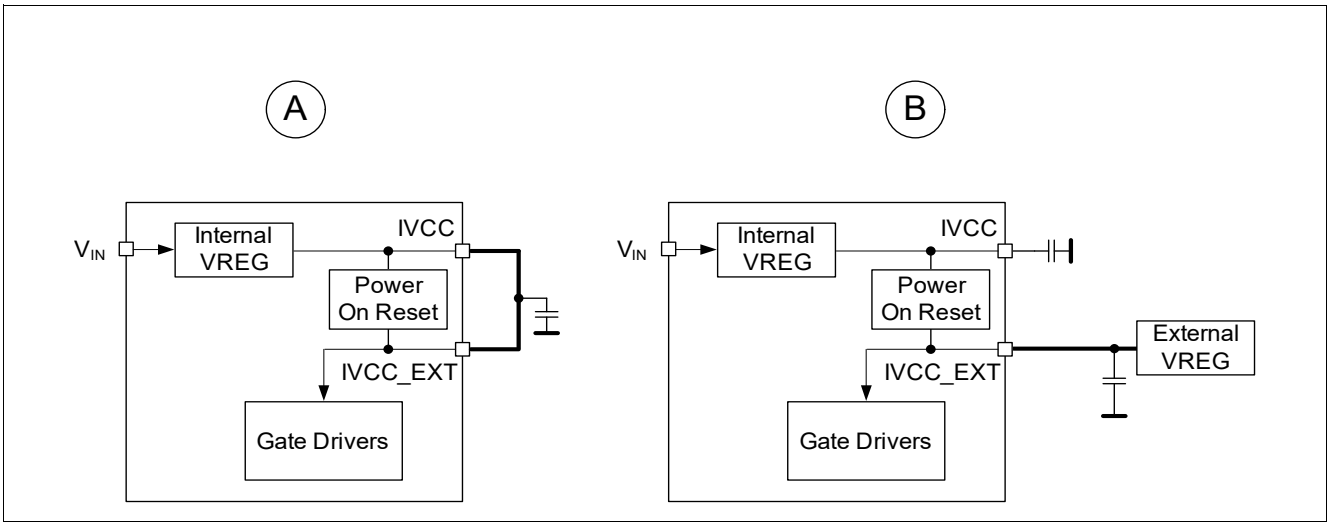


Figure 23 Voltage Regulator Configurations

9.2 Electrical Characteristics

Table 9 EC Line Regulator

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IVCC							
Output Voltage	V_{IVCC}	4.8	5	5.2	V	V_{IN}= 13.5 V; 0.1 mA ≤ I_{IVCC} ≤ 50 mA;	P_9.2.1
Output Current Limitation	I_{LIM}	70	90	110	mA	1) V_{IVCC} = 4 V;	P_9.2.2
Drop out Voltage (V_{IN} - V_{IVCC})	V_{DR}	–	200	350	mV	V_{IN} = 5 V; I_{IVCC} = 10 mA;	P_9.2.3
IVCC Buffer Capacitor	C_{IVCC}	10	–	–	µF	1) 2)	P_9.2.4
IVCC_EXT Undervoltage Reset switch OFF Threshold	$V_{IVCC\_EXT\_RTH,d}$	3.7	3.9	4.1	V	3) V_{IVCC_EXT} decreasing;	P_9.2.5
IVCC Undervoltage Reset switch OFF Threshold	$V_{IVCC\_RTH,d}$	3.7	3.9	4.1	V	3) V_{IVCC} decreasing;	P_9.2.9
IVCC and IVCC_EXT Undervoltage Hysterisis	V_{IVCCX_HYST}	0.3	0.33	0.36	V	V_{IVCC} increasing; V_{IVCC_EXT} increasing;	P_9.2.6
VREF voltage	V_{REF}	1.94	2	2.06	V	0 ≤ I_{VREF} ≤ 200 µA;	P_9.2.8

1) Not subject to production test, specified by design

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum. Use capacitors with LOW ESR.

3) Selection of external switching MOSFET is crucial. $V_{IVCC\_EXT\_RTH,d}$ and $V_{IVCC\_RTH,d}$ min. as worst case V_{GS} must be considered.

10 Protection and Diagnostic Functions

10.1 Description

The TLD5190 has integrated circuits to diagnose and protect against overvoltage, open load, short circuits of the load and overtemperature faults.

In IDLE state, only the Over temperature Shut Down, Over Temperature Warning, IVCC or IVCC_EXT Undervoltage Monitor or $V_{EN/INUVLO}$ Undervoltage Monitor are reported according to specifications.

In **Figure 24** a summary of the protection, diagnostic and monitor functions is displayed.

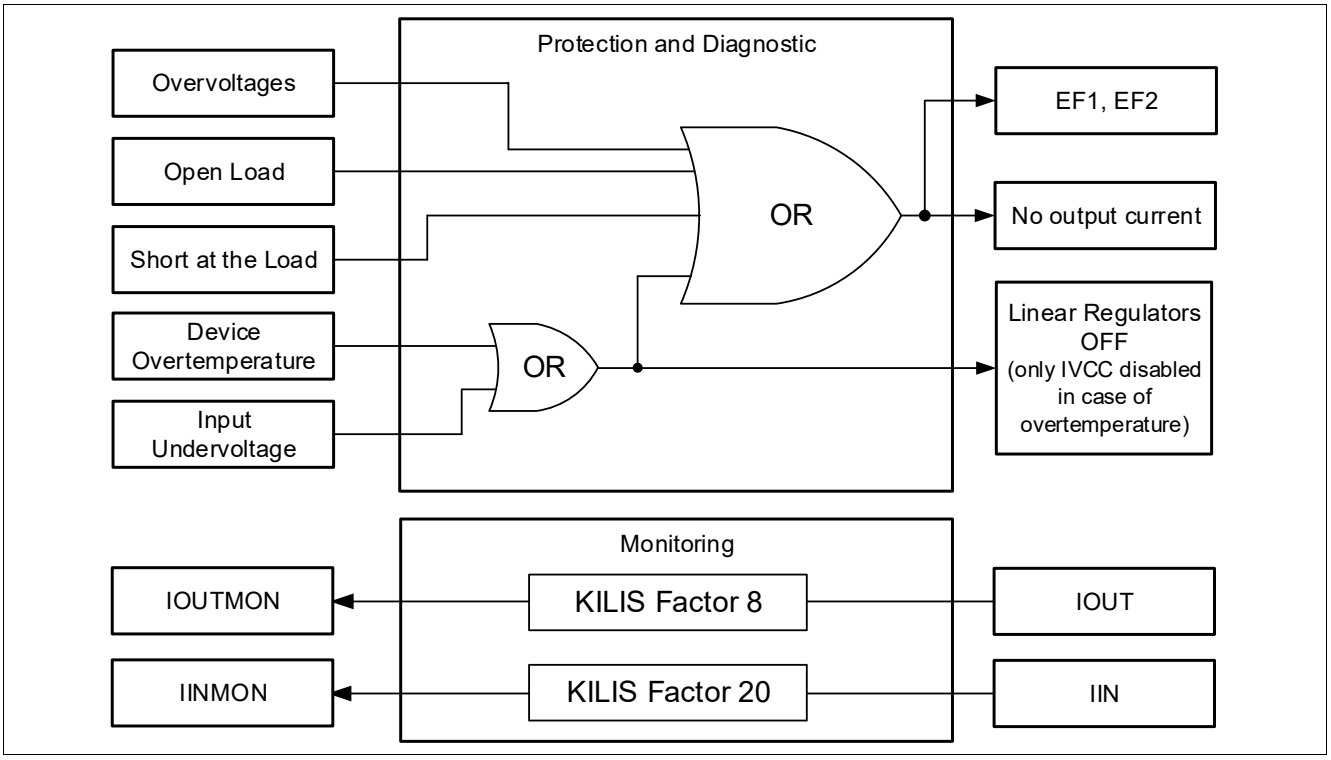


Figure 24 Protection, Diagnostic and Monitoring Overview - TLD5190

Input		Output			
Condition	Level*	EF1	EF2	Gate Drivers	IVCC
Open Load / Overvoltages	False	High	High	Sw*	Active
	True	High	Low	BL	Active
Shorted LED fault	False	High	High	Sw*	Active
	True	Low	High	BL	Active
Overtemperature	False	High	High	Sw*	Active
	True	Low	Low	AL	Shutdown

*Note:
Sw = Switching
False = Condition does not exist
True = Condition does exist
BL = Brake-Low: both LS MOSFETs ON
AL = All gate drivers outputs are low

Figure 25 Diagnostic Truth Table - TLD5190

Note: A device overtemperature event overrules all other fault events!

10.2 Output Overvoltage, Open Load, Short circuit protection

The VFB pin measures the voltage on the application output and in accordance with the populated resistor divider, short to ground, open load and output overvoltage thresholds are set. Refer to **Figure 26** for more details.

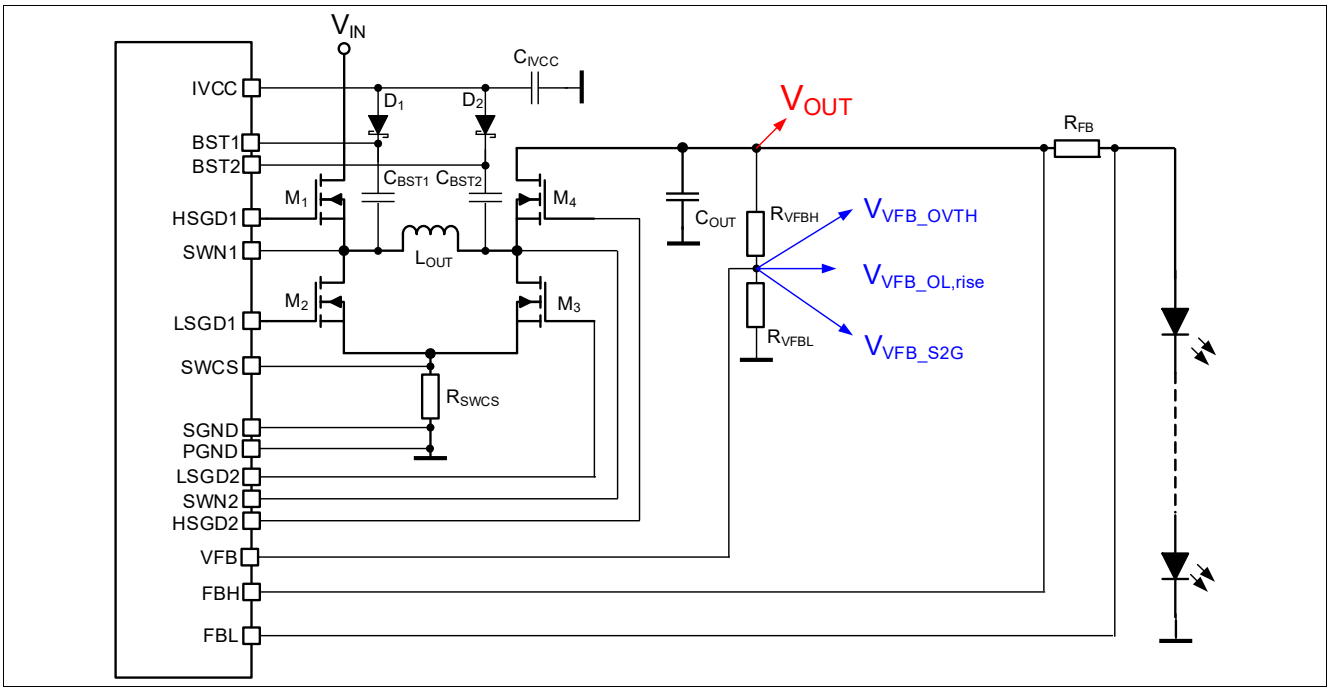


Figure 26 VFB Protection Pin - Overview

10.2.1 Short Circuit protection

The device detects a short circuit at the output if this condition is verified:

- The pin VFB falls below the threshold voltage V_{VFB_S2G} for at least 8 clock cycles

During the rising edge of the Soft Start the short circuit detection via VFB is ignored until $V_{SOFT\_START\_LOFF}$ (see **Figure 8**).

A voltage divider between V_{OUT}, VFB pin and AGND is used to adjust the application short circuit thresholds following **Equation (10.1)**.

$$V_{short\_led} = V_{VFB\_S2G} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \quad (10.1)$$

The TLD5190 provides an open-drain status pin, EF1, which pulls low when the short circuit is detected. The only time the FB pin will be below V_{VFB_S2G} is during start-up or if the LEDs are shorted. During start-up the TLD5190 ignores the detection of a short circuit or an open load until the soft-start capacitor reaches 1.75 V. To prevent false tripping after startup, a large enough soft-start capacitor must be used to allow the output to get up to approximately 50% of the final value.

*Note: If the short circuit condition disappears, the device will re-start with the soft start routine as described in **Chapter 6.2**.*

10.2.2 Output overvoltage protection

A voltage divider between V_{OUT}, VFB pin and AGND is used to adjust the overvoltage protection threshold (refer to **Figure 26**).

To fix the overvoltage protection threshold the following **Equation (10.2)** is used:

$$V_{OUT\_OV} = V_{VFB\_OVTH} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \quad (10.2)$$

In case of overvoltage event at the output, the open-drain status pin EF2 will toggle to LOW, while EF1 will stay at HIGH and the gate drivers stop switching for output regulation (Brake-Low condition both LS MOSFETs ON). After the overvoltage event disappeared the device will auto restart and the status pin EF2 will toggle to HIGH.

If the overvoltage threshold V_{OUT_OV} is set below the maximum V_{IN} application operating range, then attention needs to be paid to the overvoltage behavior.

If load current persists during overvoltage event, repetitive overvoltage triggering may occur with a high frequency. This prevents inductor current regulation and the output current may even increase. To avoid this condition, proper sizing of the external components is needed (i.e. increase the output capacitance or the overvoltage threshold in order to delay the overvoltage trigger).

10.2.3 Open Load Protection

To reliably detect an open load event, two conditions need to be observed:

1) Voltage threshold: $V_{VFB} > V_{VFB\_OL,rise}$

2) Output current information: $V_{(FBH-FBL)} < V_{FBH\_FBL\_OL}$

During the rising edge of the Soft Start the open load detection is ignored until $V_{SOFT\_START\_LOFF}$.

The TLD5190 provides an open-drain status pin, EF2, which pulls low when the VFB pin is above $V_{VFB\_OL,rise}$ threshold and the voltage across $V_{(FBH-FBL)}$ is less than $V_{FBH\_FBL\_OL}$. If the open LED clamp voltage is programmed correctly using the VFB pin, then the VFB pin should never exceed 1.28 V ($V_{VFBOL,fall}$ when the LEDs are connected.

After an Open Load error the TLD5190 is autorestarting the output control accordingly to the implemented Softstart routine. An Open Load error causes an increase of the output voltage as well. An Overvoltage condition could be reported in combination with an Open Load error (in general, multiple error detection may happen if more error detection thresholds are reached during the autorestart funcion, as possible consequence of reactive behavior at the output node during open load).

The COMP capacitor is discharged during an Open Load condition to prevent spikes if load reconnects. This measure could artificially generate Short Circuit detections after open loads events.

10.3 Input voltage monitoring, protection and power derating

Input overvoltage and undervoltage shutdown levels can both be defined through an external resistor divider, as shown in **Figure 27**.

Both INOVLO and EN/INUVLO pin voltages are internally compared to their respective thresholds by means of hysteretic comparators.

Neglecting the hysteresis, the following equations hold:

$$UV_{th} = \left(1 + \frac{R_1}{R_2 + R_3}\right) \cdot EN \ / \ INUVLO_{th} \quad (10.3)$$

$$OV_{th} = \left(1 + \frac{R_1 + R_2}{R_3}\right) \cdot INOVLO_{th} \quad (10.4)$$

$$P_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{\eta} \quad (10.5)$$

$$V_{IN\_boundary} = \frac{\left(\frac{V_{OUT} \cdot I_{OUT}}{I_{IN}}\right)}{\eta} \quad (10.6)$$

$$I_{IN} = \frac{V_{IN1-IN2}}{R_{IN}} \quad (10.7)$$

$$I_{OUT} = \frac{V_{FBH-FBL}}{R_{FB}} \quad (10.8)$$

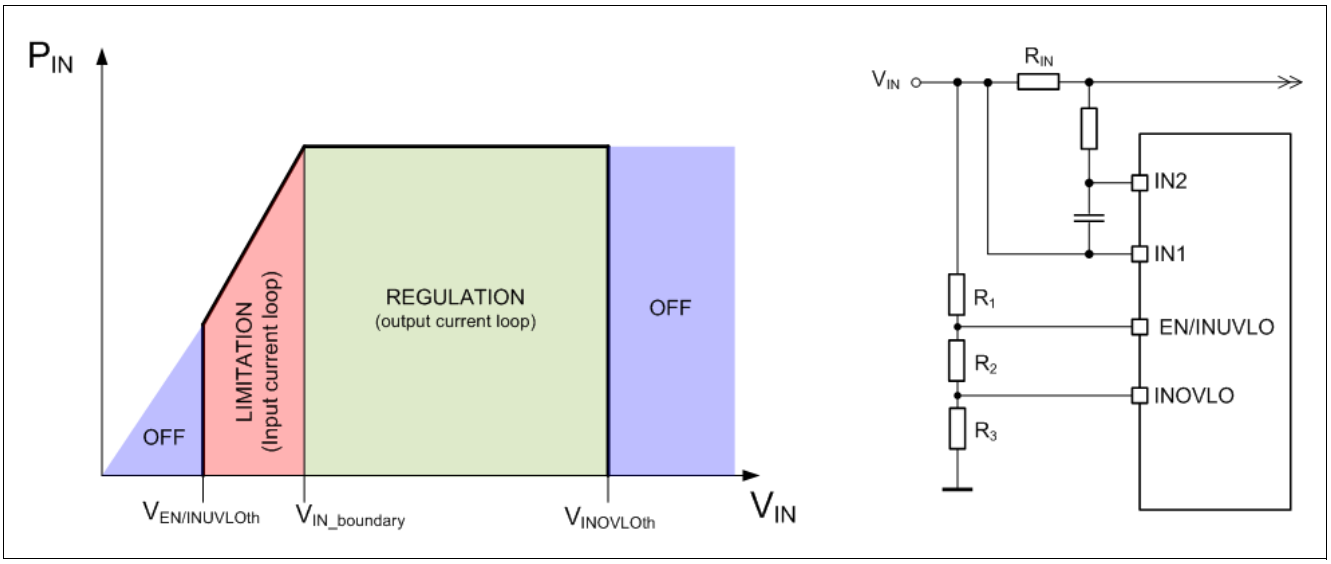


Figure 27 Input Voltage Protection

In case of overvoltage event at the input, the open-drain status pin EF2 will toggle to LOW, while EF1 will stay at HIGH. The softstart capacitor will be discharged by an internal pull down switch.

After the overvoltage event disappeared the device will auto restart with the softstart function, and the status pin EF2 will toggle to HIGH.

10.4 Input current Monitoring and Limiter

The two inputs (IIN1, IIN2) can be used to limit and monitor the Input current (Block A1 and A7 in **Figure 7**).

The control loop reduces the Comp voltage when the voltage accross the pins reaches Input Current Sense threshold $V_{IIN1-IIN2}$ to keep the input current below I_{IN}Max **Equation (10.9)**

$$I_{IN}Max = \frac{V_{IIN1-IIN2}}{R_{IIN}} \tag{10.9}$$

The IINMON pin provides a linear indication of the current flowing through the input. The following **Equation (10.10)** is applicable:

$$V_{IINMON} = I_{IN} \cdot R_{IN} \cdot 20 \tag{10.10}$$

Note: If the R_{IN} value is choosen in a way that the current limitiation is much bigger than the nominal input current during the application the current measurement becomes inaccurate. Best results for an accurate current measurement via the V_{IINMON} pin is to set the current limit only slightly above the specific application related nominal input current.

10.5 Output current Monitoring

The IOUTMON pin provides a linear indication of the current flowing through the LEDs. The following **Equation (10.11)** is applicable:

$$V_{IOUTMON} = 200\ mV + I_{OUT} \cdot R_{FB} \cdot 8 \tag{10.11}$$

10.6 Device Temperature Monitoring

A temperature sensor is integrated on the chip. The temperature monitoring circuit compares the measured temperature to the shutdown threshold.

If the internal temperature sensor reaches the shut-down temperature, the Gate Drivers plus the IVCC regulator are shut down as described in **Figure 28**.

The CLKOUT function is disabled during an overtemperature event and will autorestart when the device cooled down and IVCC is present again.

Note: The Device will start up with a soft start routine after a overtemperature condition disappear.

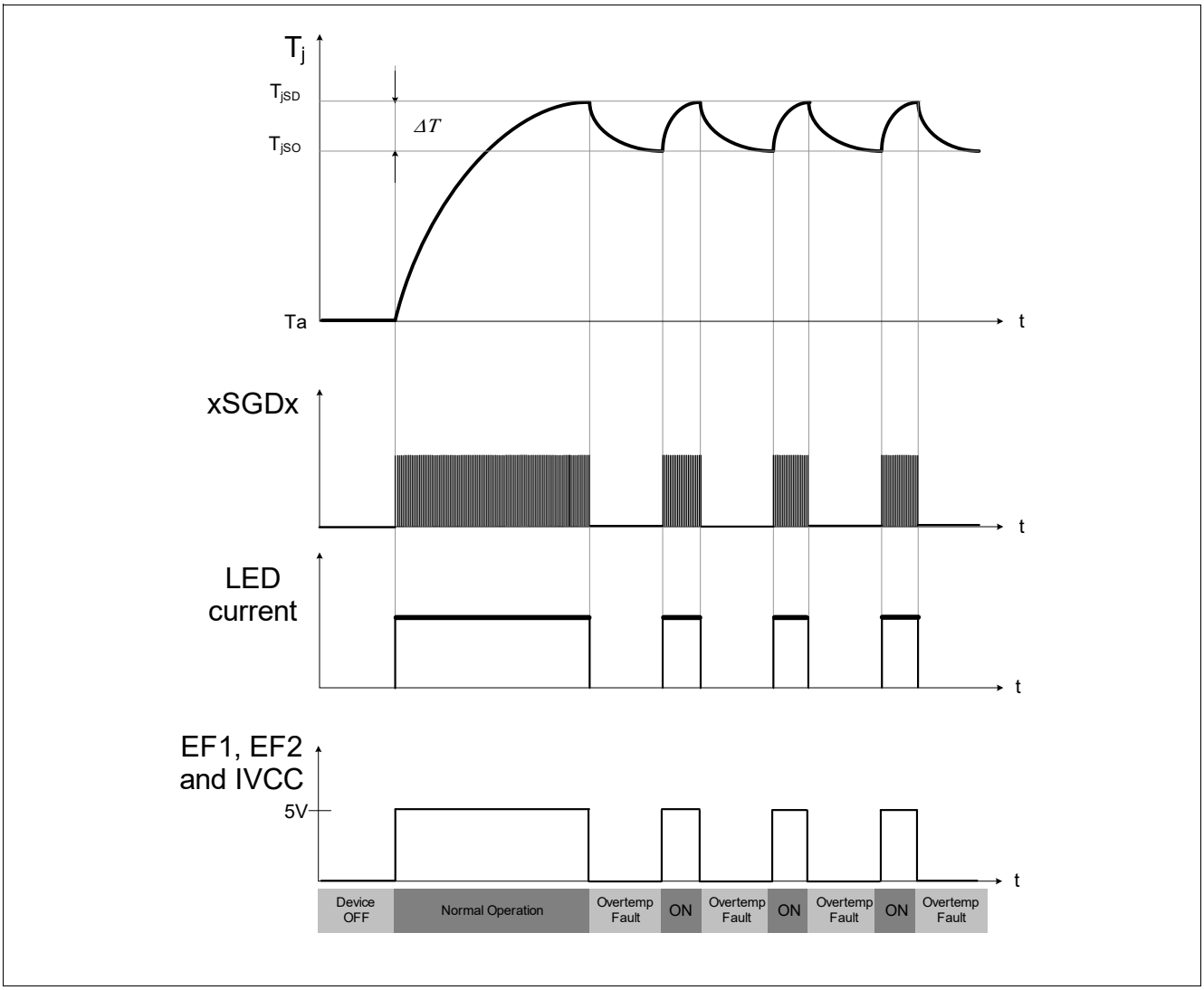


Figure 28 Device Overtemperature Protection Behavior

10.7 Electrical Characteristics

Table 10 EC Protection and Diagnosis

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Short Circuit Protection							
Short to GND threshold	V_{VFB_S2G}	0.53	0.563	0.59	V	V_{VFB} decreasing;	P_10.8.1
Temperature Protection:							
Over Temperature Shutdown	$T_{j,SD}$	160	175	190	°C	1)	P_10.8.4
Over Temperature Shutdown Hysteresis	$T_{j,SD,hyst}$	–	10	–	°C	1)	P_10.8.5
Overvoltage Protection:							
VFB Over Voltage Feedback Threshold	V_{VFB_OVTH}	1.42	1.46	1.50	V		P_10.8.6
Output Over Voltage Feedback Hysteresis	$V_{VFB\_OVTH,HYS}$	25	40	58	mV	Output Voltage decreasing;	P_10.8.7
Open Load and Open Feedback Diagnostics							
Open Load rising Threshold	$V_{VFB\_OL,rise}$	1.29	1.34	1.39	V	$V_{FBH-FBL}$ = 0 V;	P_10.8.9
Open Load reference Voltage $V_{FBH-FBL}$	$V_{FBH\_FBL\_OL}$	–	15	22.5	mV	V_{FB} = 1.4 V;	P_10.8.10
Open Load falling Threshold	$V_{VFB\_OL,fall}$	1.23	1.28	1.33	V	$V_{FBH-FBL}$ = 0 V;	P_10.8.11
Input Overvoltage protection							
Input Overvoltage rising Threshold	$V_{INOVLOth}$	1.9	2	2.1	V	–	P_10.8.12
Input Overvoltage Threshold Hysteresis	$V_{INOVLO(hyst)}$	18	40	62	mV	–	P_10.8.13
Error Flags							
EF1,2 Pin Output Impedance	R_{EF12}	–	2.1	–	kΩ	1)Fault Condition I=100uA	P_10.8.14

1) Specified by design; not subject to production test.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

11 Infineon FLAT SPECTRUM Feature set

11.1 Description

The Infineon FLAT SPECTRUM feature set has the target to minimize external additional filter circuits. The goal is to provide several beneficial concepts to provide easy adjustments for EMC improvements after the layout is already done and the HW designed.

11.2 Synchronization Function

The TLD5190 features a SYNC input pin which can be used by a µC pin to define an oscillator switching frequency. The µC is responsible to synchronize with various devices by applying appropriate SYNC signals to the dedicated DC/DC devices in the system. Refer to **Figure 29**

Note: The Synchronization function can not be used when the Spread Spectrum is active.

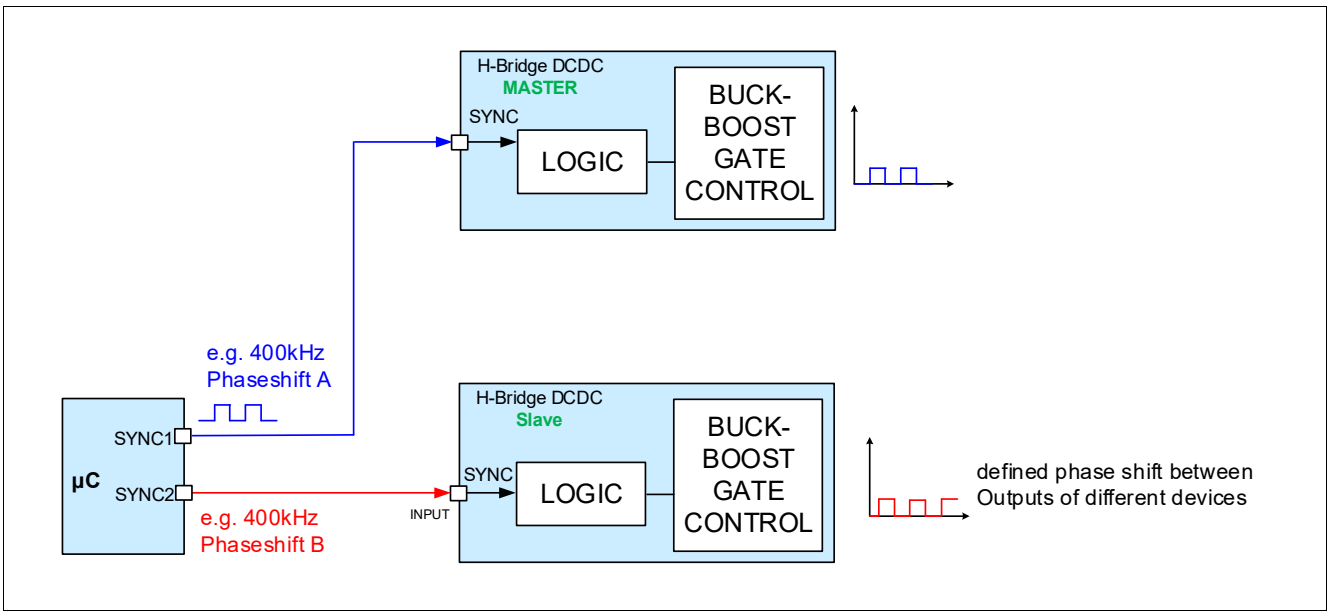


Figure 29 Synchronization Overview

11.3 CLKOUT Function

The CLKOUT pin provides an in-phase clock signal provided by the internal oscillator. This signal can be used to synchronize two devices for extending output power capability.

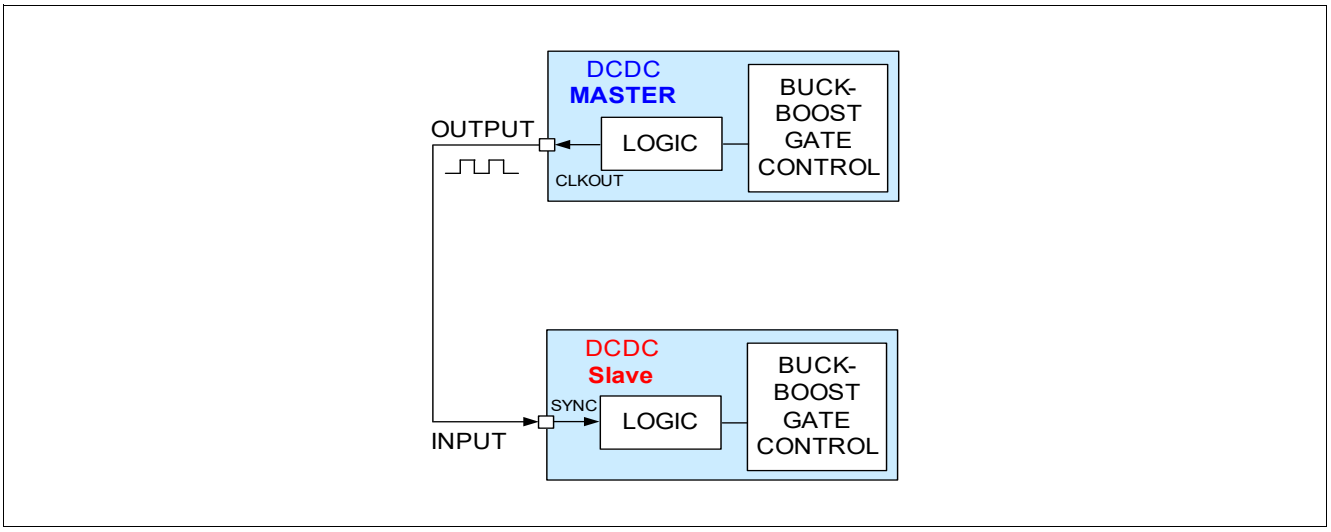


Figure 30 CLKOUT Overview

11.4 Spread Spectrum

The Spread Spectrum modulation technique significantly improves the lower frequency range of the spectrum (f < 30 MHz).

By using the spread spectrum technique, it is possible to optimize the input filter only for the peak limits, and also pass the average limits (average emission limits are -20dB lower than the peak emission limits). By using spread spectrum, the need for low ESR input capacitors is relaxed because the input capacitor series resistor is important for the low frequency filter characteristic. This can be an economic benefit if there is a strong requirement for average limits.

The TLD5190 features a built in Spread Spectrum function which can be enabled via an external Pin (SPREAD_SPECTRUM = HIGH). The modulation frequency f_{FM}, P_11.6.3 and the deviation frequency f_{dev}, P_11.6.2 are internally fixed. Refer to **Figure 31** for more details.

Note: The Spread Spectrum function can not be used when the synchronization pin is used.

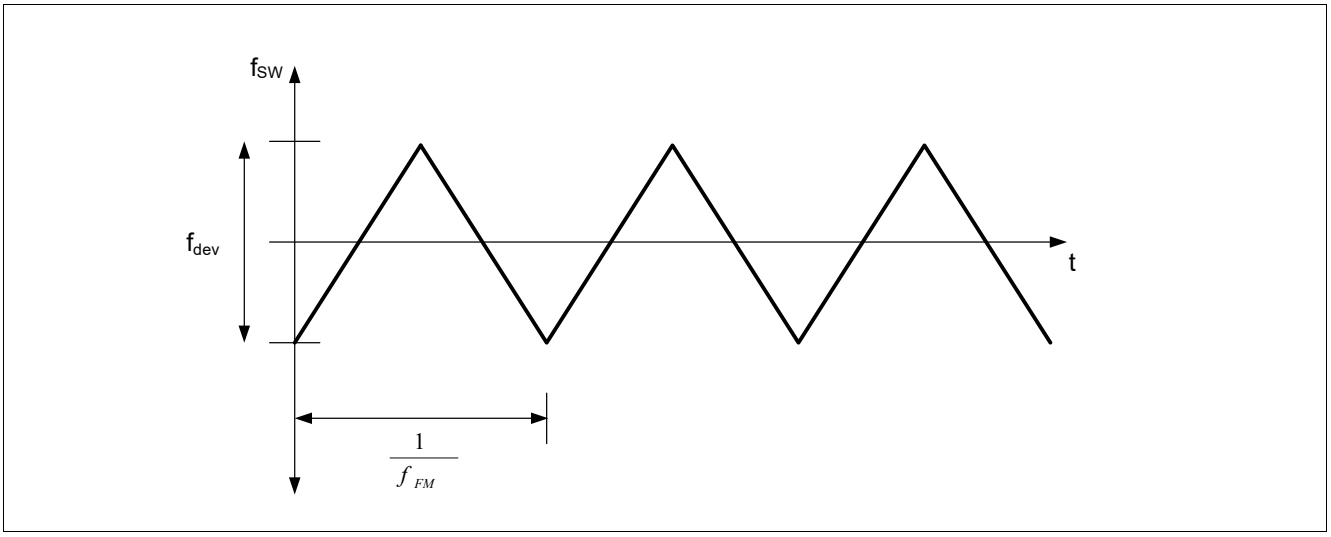


Figure 31 Spread Spectrum Overview

11.5 EMC optimized schematic

Figure 32 below displays the Application circuit with additional external components for improved EMC behavior.

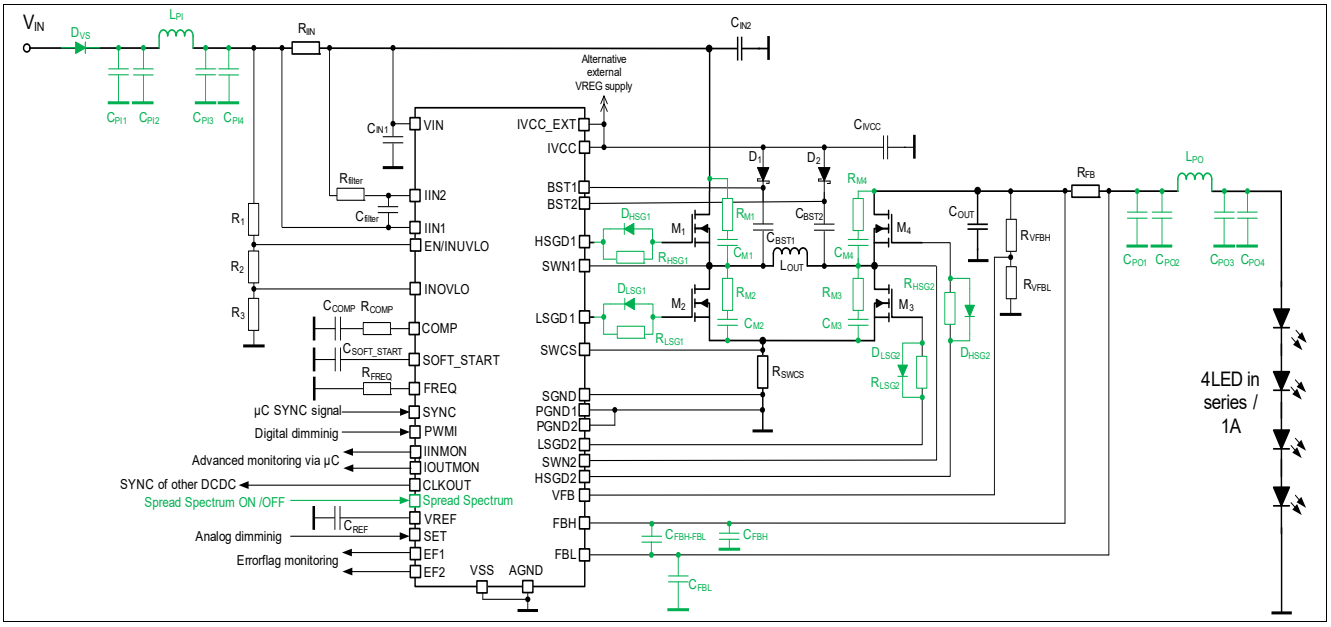


Figure 32 Application Drawing Including Additional Components for an Improved EMC Behavior

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

11.6 Electrical Characteristics

Table 11 EC Spread Spectrum

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Spread Spectrum Parameters							
Frequency Deviation	f_{dev}	–	±16	–	%	1) SPREAD_SPECTRUM = HIGH;;	P_11.6.2
Frequency Modulation	f_{FM}	–	12	–	kHz	1) SPREAD_SPECTRUM = HIGH;	P_11.6.3
Input Characteristics (SPREAD_SPECTRUM)							
SPREAD_SPECTRUM Turn On Threshold	$V_{SPREAD\_SPECTRUM,ON}$	2	–	–	V	–	P_11.6.5
SPREAD_SPECTRUM Turn Off Threshold	$V_{SPREAD\_SPECTRUM,OFF}$	–	–	0.8	V	–	P_11.6.6
SPREAD_SPECTRUM High Input Current	$I_{SPREAD\_SPECTRUM,H}$	15	30	45	µA	$V_{SPREAD\_SPECTRUM}$ = 2.0 V;	P_11.6.8
SPREAD_SPECTRUM Low Input Current	$I_{SPREAD\_SPECTRUM,L}$	6	12	18	µA	$V_{SPREAD\_SPECTRUM}$ = 0.8 V;	P_11.6.9
Output Characteristics (CLKOUT)							
L level output voltage	$V_{CLKOUT(L)}$	0	–	0.4	V	I_{CLKOUT} = -2 mA;	P_11.6.10
H level output voltage	$V_{CLKOUT(H)}$	V_{IVCC} - 0.4 V	–	V_{IVCC}	V	I_{CLKOUT} = 2 mA;	P_11.6.11

1) Specified by design; not subject to production test.

12 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

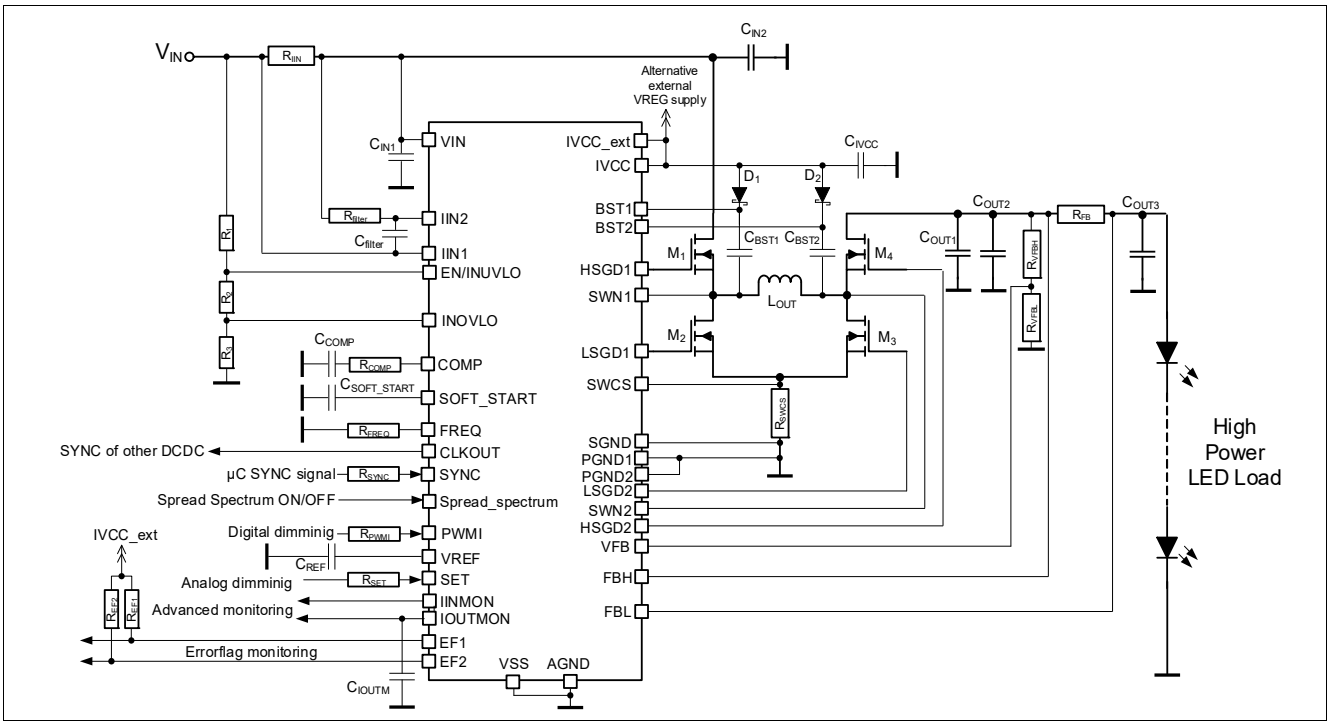


Figure 33 Application Drawing - TLD5190 as current regulator

Table 12 BOM - TLD5190 as current regulator (I_{OUT} = 1 A, f_{SW} = 300 kHz)

Reference Designator	Value	Manufacturer	Part Number	Type
D_1 , D_2	BAT46WJ	--	BAT46WJ	Diode
C_{IN1}	1 µF, 100 V	TDK	X7R	Capacitor
C_{IN2}	4.7 µF, 100 V	TDK	X7R	Capacitor
C_{filter}	470 nF, 6.3 V	TDK	X7R	Capacitor
C_{COMP}	22 nF, 16 V	TDK	X7R	Capacitor
C_{SOFT_START}	22 nF, 16 V	TDK	X7R	Capacitor
C_{OUT1}	4.7 µF, 100 V	TDK	X7R	Capacitor
C_{OUT2} , C_{OUT3} , C_{REF}	100 nF, 100 V	TDK	X7R	Capacitor
C_{IV}	10 µF , 10 V	TDK	X7R	Capacitor
$C_{IOUTMON}$	220pF , 10 V	TDK	X7R	Capacitor
C_{BST1} , C_{BST2}	100 nF, 16 V	TDK	X7R	Capacitor
IC_1	--	Infineon	TLD5190	IC
L_{OUT}	10 µH	Coilcraft	XAL1010-103MEC	Inductor
R_{filter}	50 Ω, 1%	Panasonic	--	Resistor
R_{FB}	0.150 Ω, 1%	Panasonic	--	Resistor

Table 12 BOM - TLD5190 as current regulator (I_{OUT} = 1 A, f_{SW} = 300 kHz)

Reference Designator	Value	Manufacturer	Part Number	Type
R_{IN}	0.003 Ω, 1%	Panasonic	--	Resistor
R_1 , R_2 , R_3 , R_{EN} , R_{PWMI} , R_{Sense1} , R_{Sense2} , R_{SYNC} , R_{EF1} , R_{EF2} , R_{SET}	XX kΩ, 1%	Panasonic	--	Resistor
R_{VFBL} , R_{VFBH}	1.5 kΩ, 56 kΩ, 1%	Panasonic	--	Resistor
R_{COMP}	0 Ω	Panasonic	--	Resistor
R_{FREQ}	37.4 kΩ, 1%	Panasonic	--	Resistor
R_{SWCS}	0.005 Ω, 1%	Panasonic	ERJB1CFRO5U	Resistor
M_1 , M_2 , M_3 , M_4	Dual MOSFET: 100 V / 35 mΩ, N-ch	Infineon	IPG20N10S4L-35	Transistor

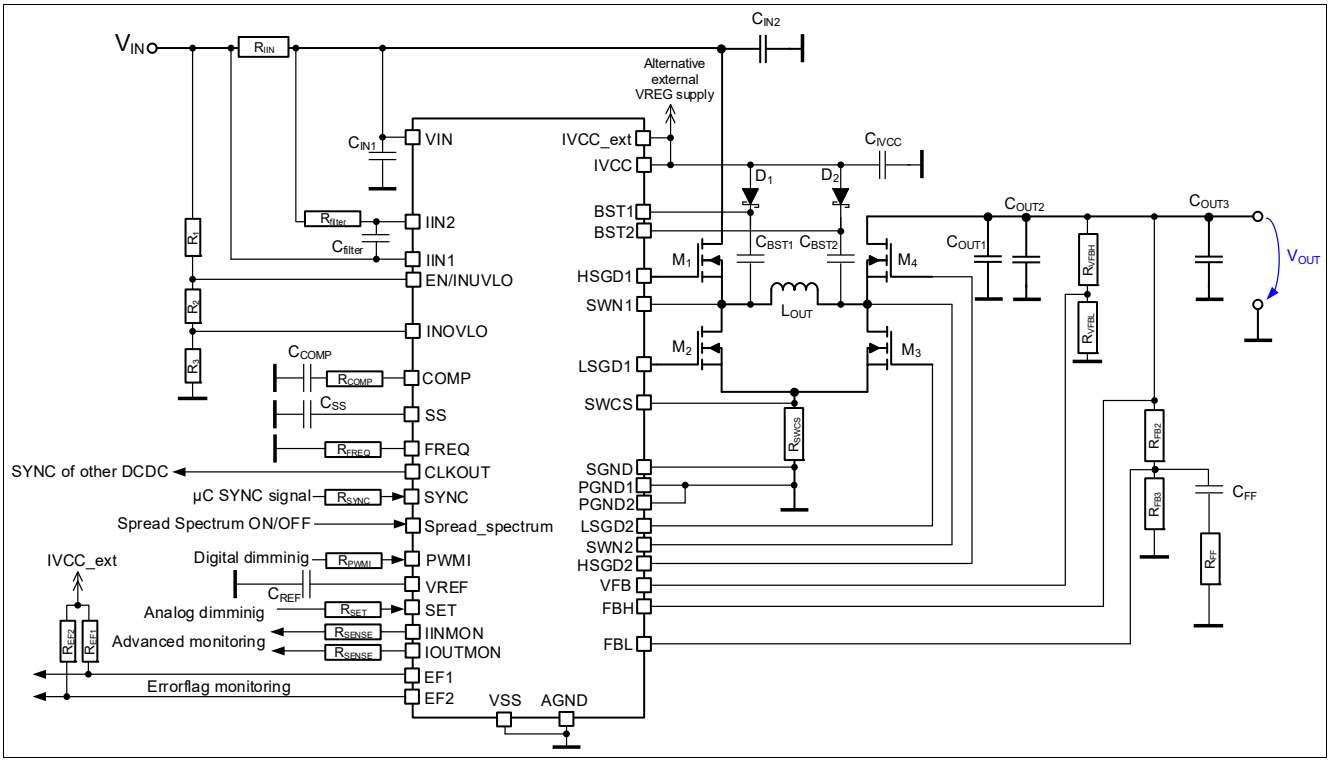


Figure 34 Application Drawing - TLD5190 as 10V voltage regulator

Table 13 BOM - TLD5190 as voltage regulator (I_{OUT} = 1 A, f_{SW} = 300 kHz)

Reference Designator	Value	Manufacturer	Part Number	Type
D_1 , D_2	BAT46WJ	--	BAT46WJ	Diode
C_{IN1}	1 µF, 100 V	TDK	X7R	Capacitor
C_{IN2}	4.7 µF, 100 V	TDK	X7R	Capacitor
C_{filter}	470 nF, 6.3 V	TDK	X7R	Capacitor
C_{COMP}	22 nF, 16 V	TDK	X7R	Capacitor
C_{FF}	10 nF, 50 V	TDK	X7R	Capacitor
C_{SOFT_START}	22 nF, 16 V	TDK	X7R	Capacitor

Table 13 BOM - TLD5190 as voltage regulator (I_{OUT} = 1 A, f_{SW} = 300 kHz)

Reference Designator	Value	Manufacturer	Part Number	Type
C_{OUT1}	4.7 µF, 100 V	TDK	X7R	Capacitor
C_{OUT2} , C_{OUT3} , C_{REF}	100 nF, 100 V	TDK	X7R	Capacitor
C_{IVCC}	10 µF , 10 V	TDK	X7R	Capacitor
C_{BST1} , C_{BST2}	100 nF, 16 V	TDK	X7R	Capacitor
IC_1	--	Infineon	TLD5190	IC
L_{OUT}	10 µH	Coilcraft	XAL1010-103MEC	Inductor
R_{filter}	50 Ω, 1%	Panasonic	--	Resistor
R_{FB2} , R_{FB3}	150Ω, 10.1kΩ, 1%	Panasonic	--	Resistor
R_{FF}	1.5 kΩ, 1%	Panasonic	--	Resistor
R_{IN}	0.003 Ω, 1%	Panasonic	--	Resistor
R_1 , R_2 , R_3 , R_{EN} , R_{PWMI} , R_{Sense1} , R_{Sense2} , R_{SYNC} , R_{EF1} , R_{EF2} , R_{SET}	XX kΩ, 1%	Panasonic	--	Resistor
R_{VFBL} , R_{VFBH}	1.5 kΩ, 56 kΩ, 1%	Panasonic	--	Resistor
R_{COMP}	0 Ω	Panasonic	--	Resistor
R_{FREQ}	37.4 kΩ, 1%	Panasonic	--	Resistor
R_{SWCS}	0.005 Ω, 1%	Panasonic	ERJB1CFRO5U	Resistor
M_1 , M_2 , M_3 , M_4	Dual MOSFET: 100 V / 35 mΩ, N-ch	Infineon	IPG20N10S4L-35	Transistor

12.1 Further Application Information

Typical Performance Characteristics of Device

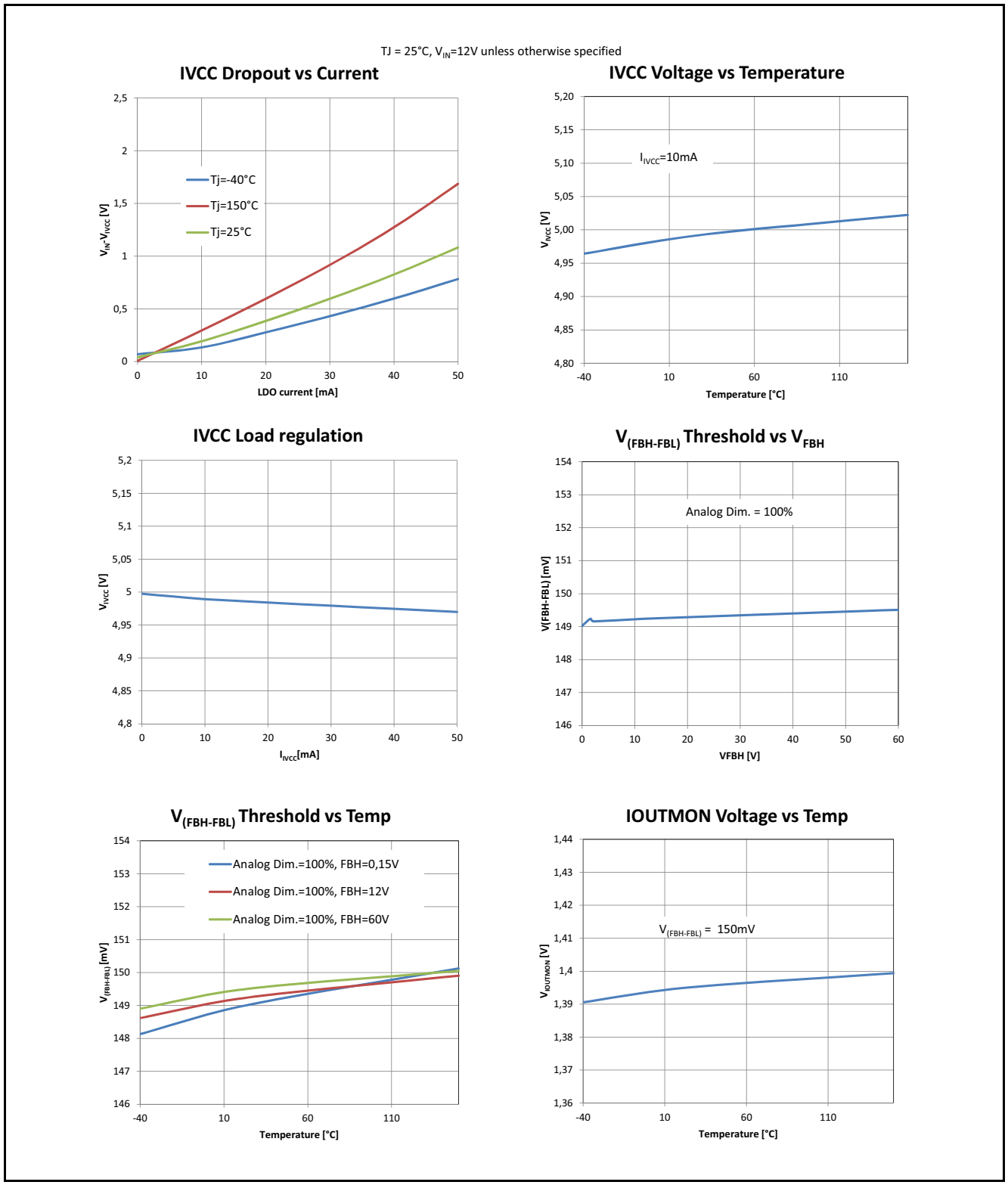


Figure 35 Characterization Diagrams 1

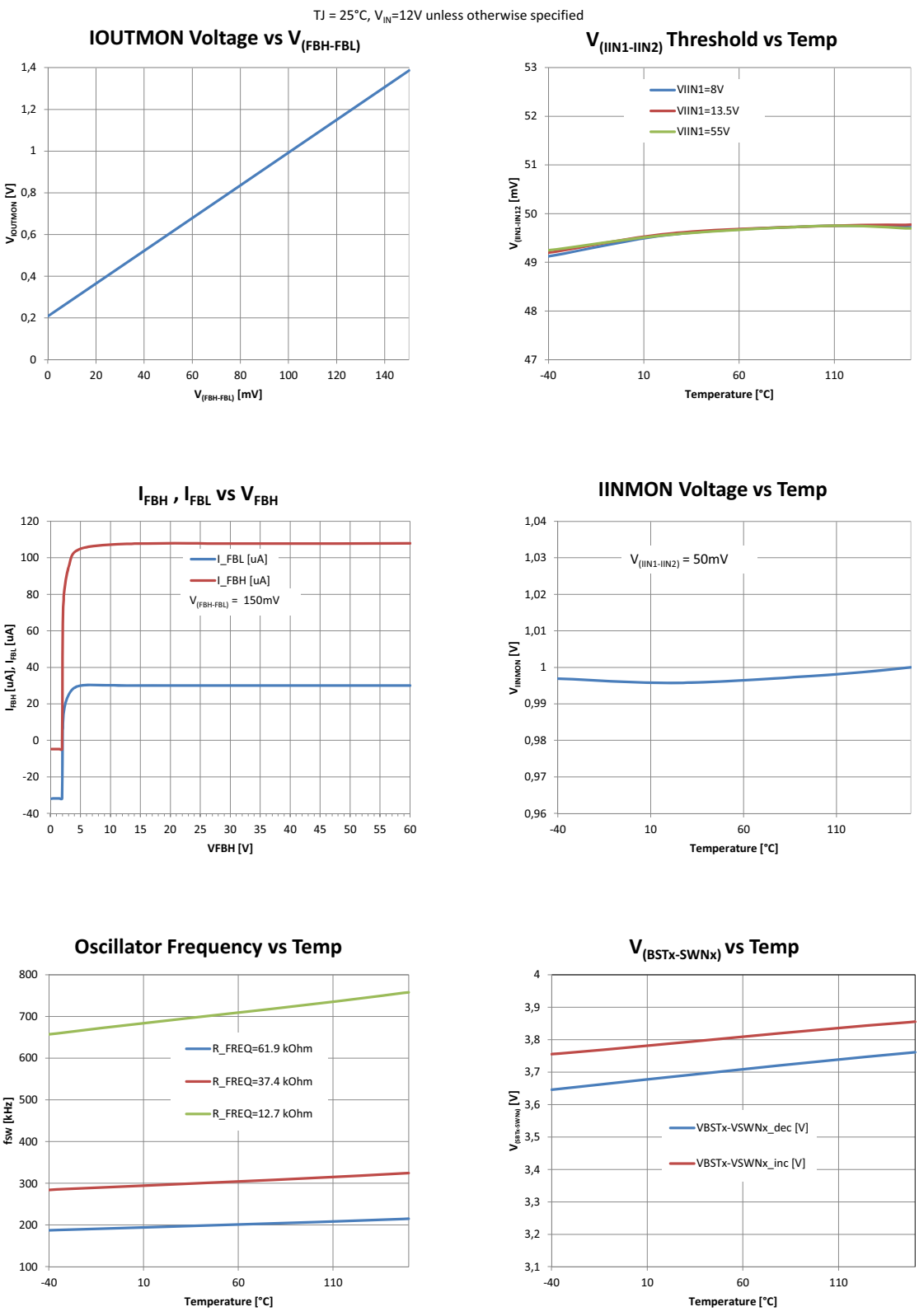


Figure 36 Characterization Diagrams 2

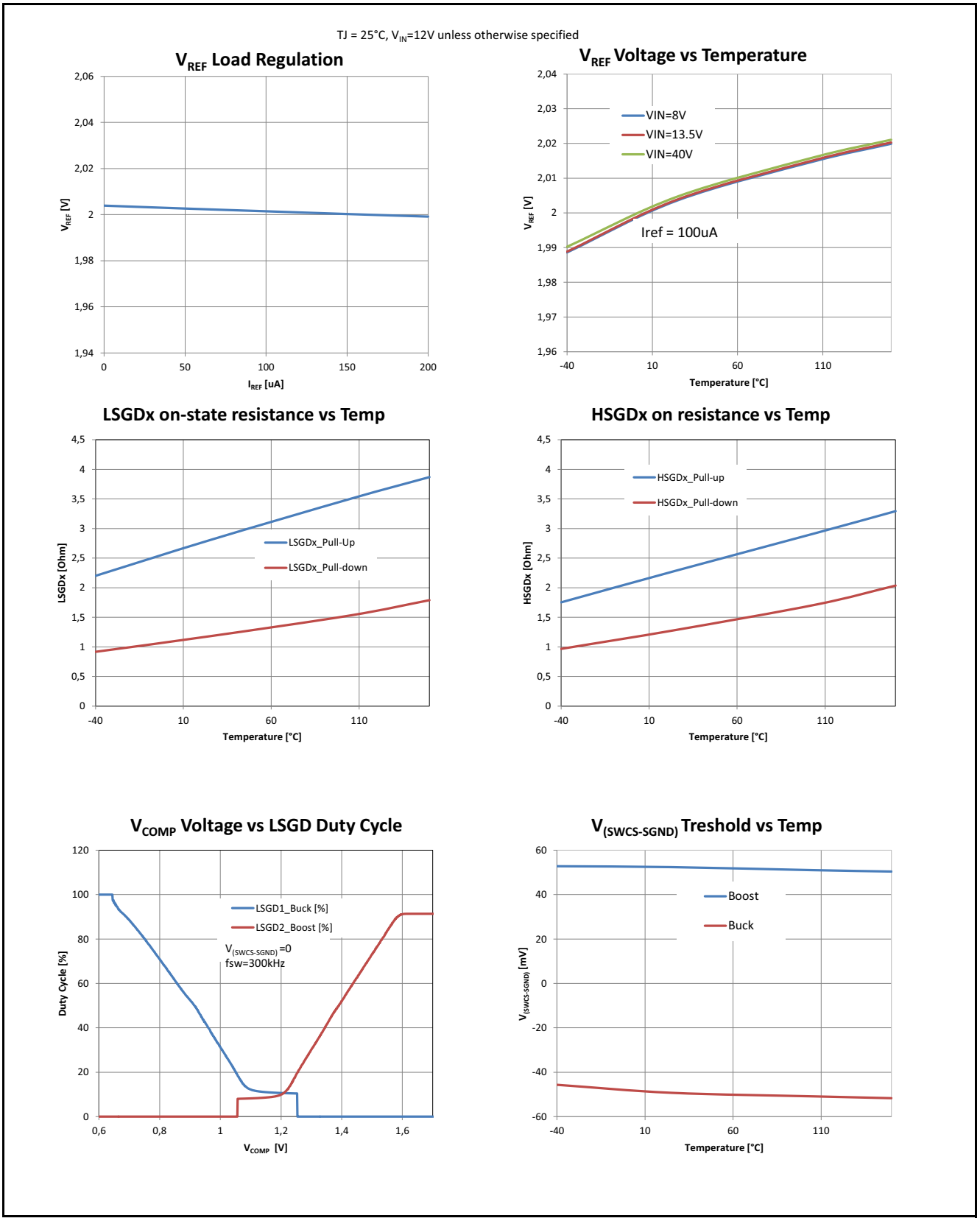


Figure 37 Characterization Diagrams 3

- For further information you may contact **http://www.infineon.com/**

13 Package Outlines

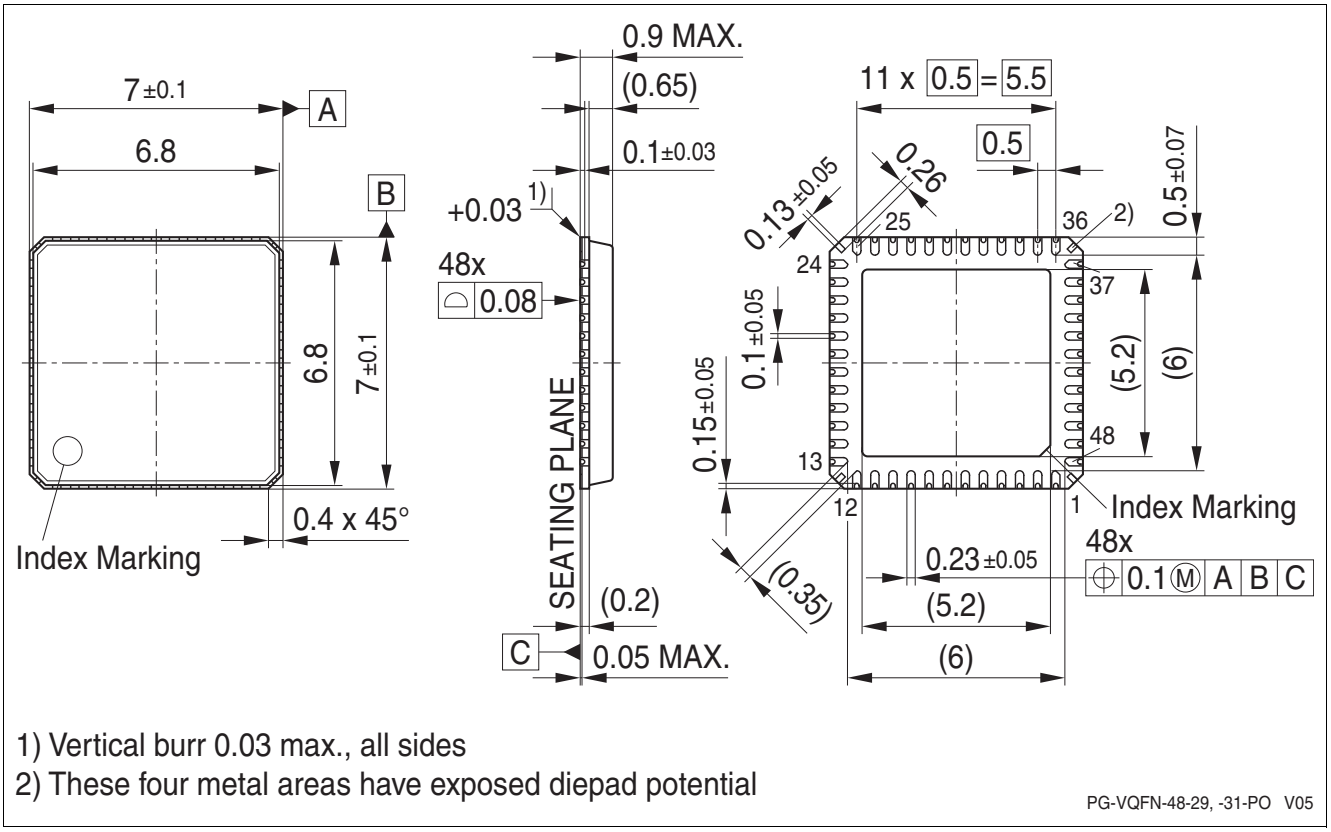


Figure 38 PG-VQFN-48-31 (with LTI)

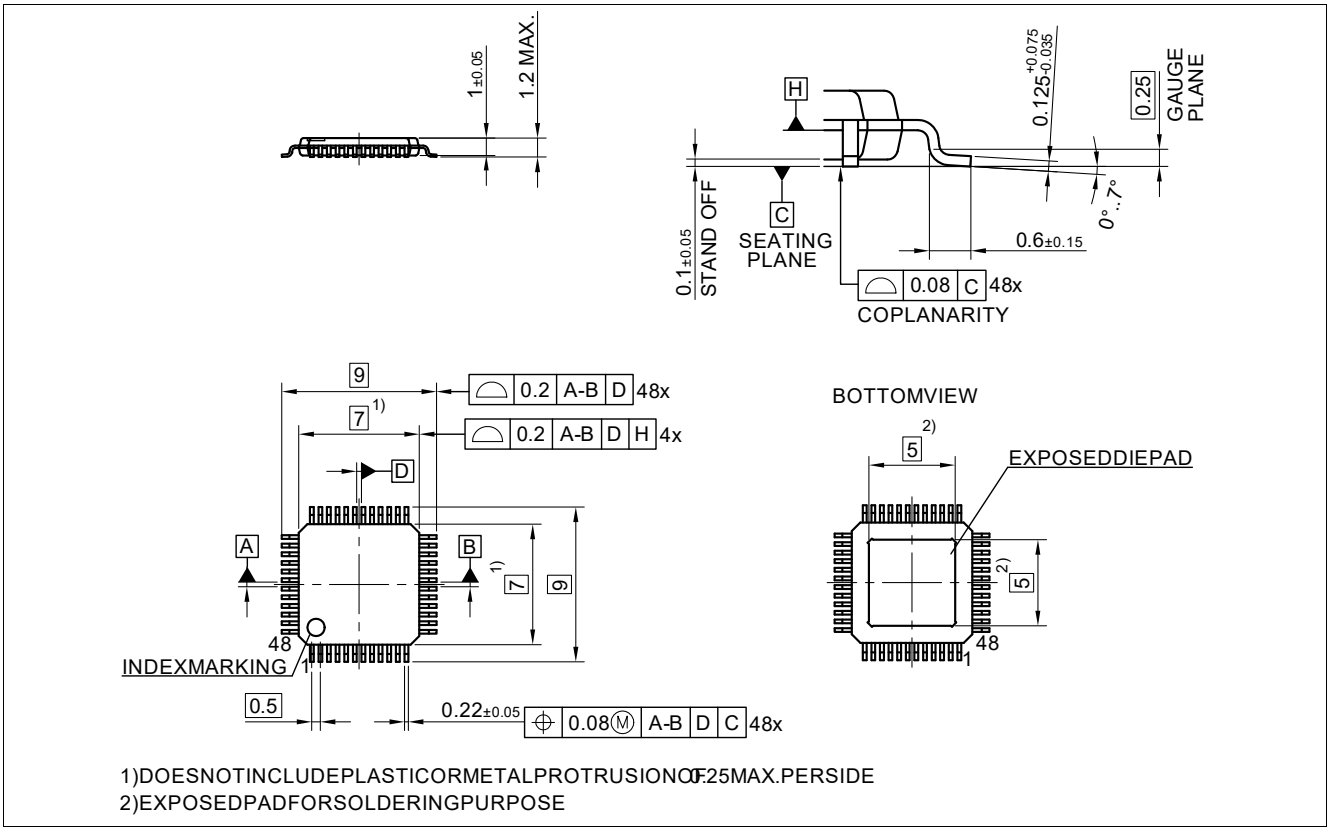


Figure 39 PG-TQFP-48-9

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

14 Revision History

Revision	Date	Changes
Rev. 1.0	2016-05-20	Released Datasheet
Rev. 1.1	2018-02-08	Added: CCM on regulator description **Chapter 6.1**
Rev. 1.1	2018-02-08	Added TQFP package
Rev. 1.1	2018-02-08	Corrected graph V_{COMP} vs DUTY
Rev. 1.1	2018-02-08	Corrected soft start behavior **Chapter 6.2** “if an open load”
Rev. 1.1	2018-02-08	Divided In and out overvoltage protection def. **Chapter 10.2 Chapter 10.3**
Rev. 1.1	2018-02-08	Removed “Flex” from Family name. **Chapter 1**
Rev. 1.1	2018-02-08	Specified Complessive gain of error amp **Chapter 6.1**
Rev. 1.1	2018-02-08	Improved description of soft start **Chapter 6.2**
Rev. 1.1	2018-02-08	Added Soft Start mask in the Short circuit description **Chapter 10.2**
Rev. 1.1	2018-02-08	Added input current limiter description **Chapter 10.4**
Rev. 1.1	2018-02-08	Removed Parameter 6.4.2 covered now by updated 6.4.1 **Chapter 6.6**
Rev. 1.2	2021-03-21	Improved regulator drawing with soft start details **Chapter 6.1**
Rev. 1.2	2021-03-21	Improved soft start description and timing diagram **Figure 8 Chapter 6.2**
Rev. 1.2	2021-03-21	Updated application drawing with IOUTMON cap **Figure 1 Figure 33**
Rev. 1.2	2021-03-21	Updated output overvoltage description/truth table **Figure 25 Chapter 10.2.2**
Rev. 1.2	2021-03-21	Updated test condition on parameter P_5.3.1

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