32-Bit

Microcontroller

TC38x

32-Bit Single-Chip Microcontroller
AD/AE-Step

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.2, 2021-03

Microcontroller

OPEN MARKET VERSION

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1 Summary of Features

The TC38x product family has the following features:

- High Performance Microcontroller with four CPU cores
- Four 32-bit super-scalar TriCore CPUs (TC1.6.2P), each having the following features:
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - up to 300 MHz operation at full temperature range
  - up to 240/96 Kbyte Data Scratch-Pad RAM (DSPR)
  - up to 64 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - up to 64 Kbyte Data RAM (DLMU)
  - 32 Kbyte Instruction Cache (ICACHE)
  - 16 Kbyte Data Cache (DCACHE)
- Lockstepped shadow cores for two TC1.6.2P
- Multiple on-chip memories
  - All embedded NVM and SRAM are ECC protected
  - up to 10 Mbyte Program Flash Memory (PFLASH)
  - up to 512 Kbyte Data Flash Memory (DFLASH 0) usable for EEPROM emulation
  - 128 Kbyte Memory (LMU)
  - BootROM (BROM)
- 128-Channel DMA Controller with safe data transfer
- Sophisticated interrupt system (ECC protected)
- High performance on-chip bus structure
  - 64-bit Cross Bar Interconnect (SRI) giving fast parallel access between bus masters, CPUs and memories
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - SRI to SPB bus bridges (SFI Bridge)
- Optional Hardware Security Module (HSM) on some variants
- Safety Management Unit (SMU) handling safety monitor alarms
- Memory Test Unit with ECC, Memory Initialization and MBIST functions (MTU)
- Hardware I/O Monitor (IOM) for checking of digital I/O
- Versatile On-chip Peripheral Units
  - 24 Asynchronous/Synchronous Serial Channels (ASCLIN) with hardware LIN support (V1.3, V2.0, V2.1 and J2602) up to 50 MBaud
  - 5 Queued SPI Interface Channels (QSPI) with master and slave capability up to 50 Mbit/s
  - 1 High Speed Serial Link (HSSL) for serial inter-processor communication up to 320 Mbit/s
  - 3 serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - 3 MCMCAN Modules with 4 CAN nodes for high efficiency data handling via FIFO buffering
  - 25 Single Edge Nibble Transmission (SENT) channels for connection to sensors
  - 2 FlexRay™ module with 2 channels (E-Ray) supporting V2.1

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  - One Generic Timer Module (GTM) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One Capture / Compare 6 module (Two kernels CCU60 and CCU61)
  - One General Purpose 12 Timer Unit (GPT120)
  - 4 channel Peripheral Sensor Interface conforming to V1.3 (PSI5)
  - 1 Peripheral Sensor Interface with Serial PHY (PSI5-S)
  - 2 Inter-Integrated Circuit Bus Interface (I2C) conforming to V2.1
  - 1 IEEE802.3 Ethernet MAC with RGMII, RMII and MII interfaces (ETH)
- Versatile Successive Approximation ADC (VADC)
  - Cluster of 16 independent ADC kernels
  - Input voltage range from 0 V to 5.5V (ADC supply)
- Delta-Sigma ADC (DSADC)
  - 10 channels
- Digital programmable I/O ports
- On-chip debug support for OCDS Level 1 (CPUs, DMA, On Chip Buses)
- multi-core debugging, real time tracing, and calibration
- four/five wire JTAG (IEEE 1149.1) or DAP (Device Access Port) interface
- Power Management System and on-chip regulators
- Clock Generation Unit with System PLL and Peripheral PLL
- Embedded Voltage Regulator
- Qualified for automotive application according to AEC-Q100 (only applicable after delivery release of the corresponding sales codes)
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL D (only applicable for sales codes listed within a released Safety Package Release Note from IFX)

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Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

Table 1-1 Platform Feature Overview

Feature		TC38x
CPUs	Type	TC1.6.2
	Cores / Checker Cores	4 / 2
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB
	DSPR	240 KB for CPU0,1 / 96 KB else
	DLMU	64 KB
SRAM global	LMU	128 KB
	DAM	64 KB
Extension Memory	TCM	- MB
	XCM	- MB
	XTM	- KB
Program Flash	Size	10 MB
	Banks	3 x 3 MB, 1 x 1 MB
Data Flash	Size (single-ended)	512 KB (DF0) + 128 KB (DF1)
DMA	Channels	128
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	8 / 64
	Secondary Groups/Channels	4 / 64
	Fast Compare Channels	4
EDSADC	Channels	10

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Table 1-1 Platform Feature Overview (cont'd)

Feature		TC38x
GTM	Clusters	9 (5 @ 200MHz, 4 @ 100MHz)
	TIM (8 ch)	7
	TOM (16 ch)	5
	ATOM (8 ch)	9
	MCS (8 ch)	7
	CMU / ICM	1 / 1
	PSM	2
	TBU channels[1)]	4 (TBU0-3)
	SPE	4
	CMP / MON	1 / 1
	BRC / DPLL	1 / 1
	CDTM modules	6
	DTM modules	20 (8 on TOM, 12 on ATOM)
Timer	GPT12	1
	CCU6	1
STM	Modules	4
FlexRay	Modules	2
	Channels	2
CAN	Modules	3
	Nodes	3 x 4
	of which support TT-CAN	1
QSPI	Modules	5
	HSCI Channels	-
ASCLIN	Modules	24
I2C	Interfaces	2
SENT	Channels	25
PSI5	Modules	4
PSI5-S	Modules	1
HSSL	Channels	1
MSC	Channels	3
SDMMC	eMMC/SD Interface	0
Ethernet (10/100Mbit/1Gbit)	Modules	1
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes
SPU	Modules	-
RIF	Modules	-
HSPDM	Modules	-

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Table 1-1 Platform Feature Overview (cont'd)

Feature		TC38x
Security	HSM+	1
Debug	OCDS	yes
	MCDS	no
	miniMCDS	yes
	miniMCDS TRAM	8 KB
	AGBT	No
Low Power Features	Standby RAM	2
	SCR	yes
Packages	Type	FBGA-516 / LFBGA-292
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
$T_{ambient}$	Range	−40 … +150°C

1) TBU3 has special purpose as angle clock.

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2 Pin Definition and Functions

The following figures are showing the Logic Symbols for the package variants:

- BGA516 (**Figure 2-1**)
- BGA292 (**Figure 2-2**)

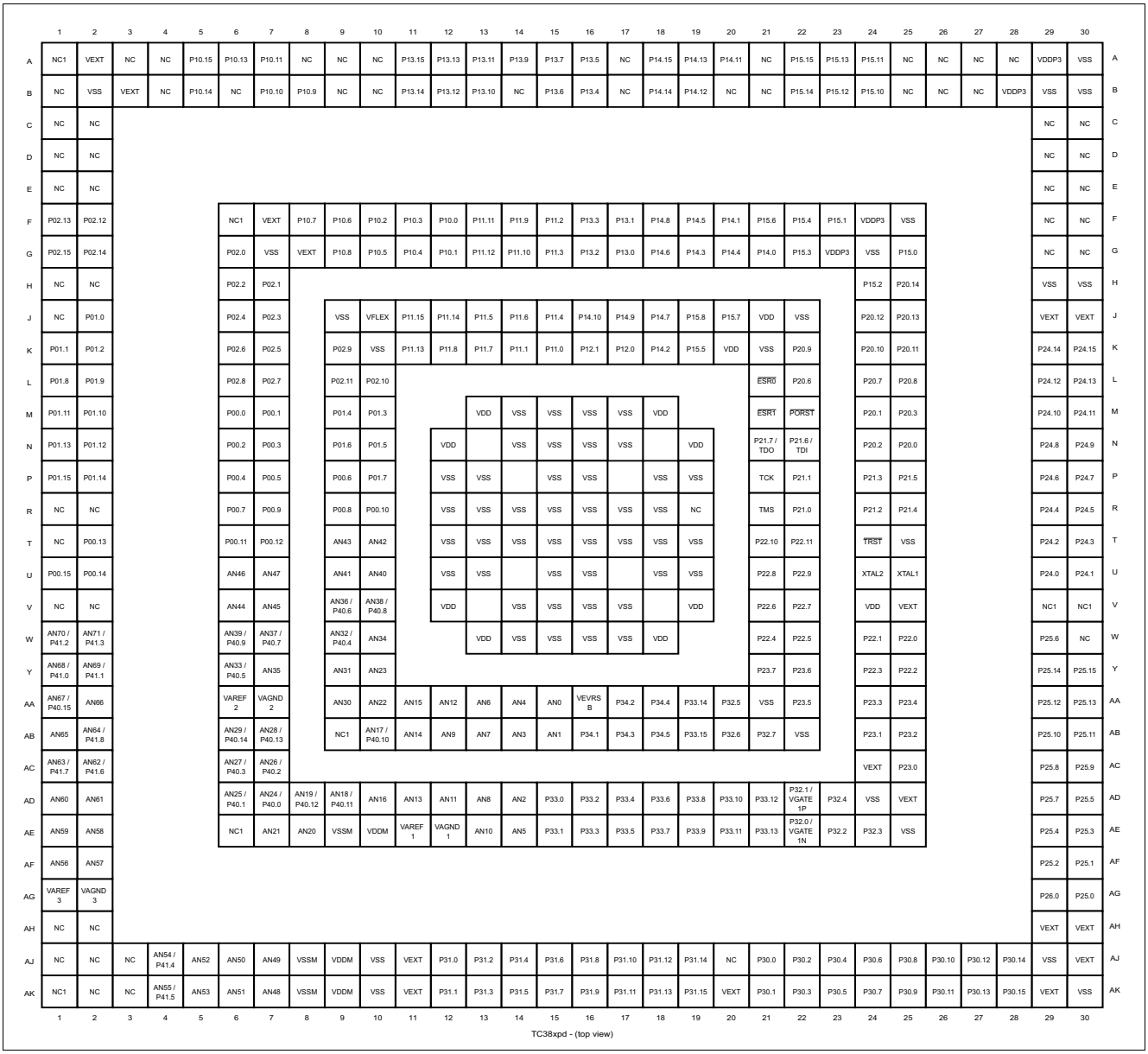

Figure 2-1 Logic Symbol for the package variant BGA516

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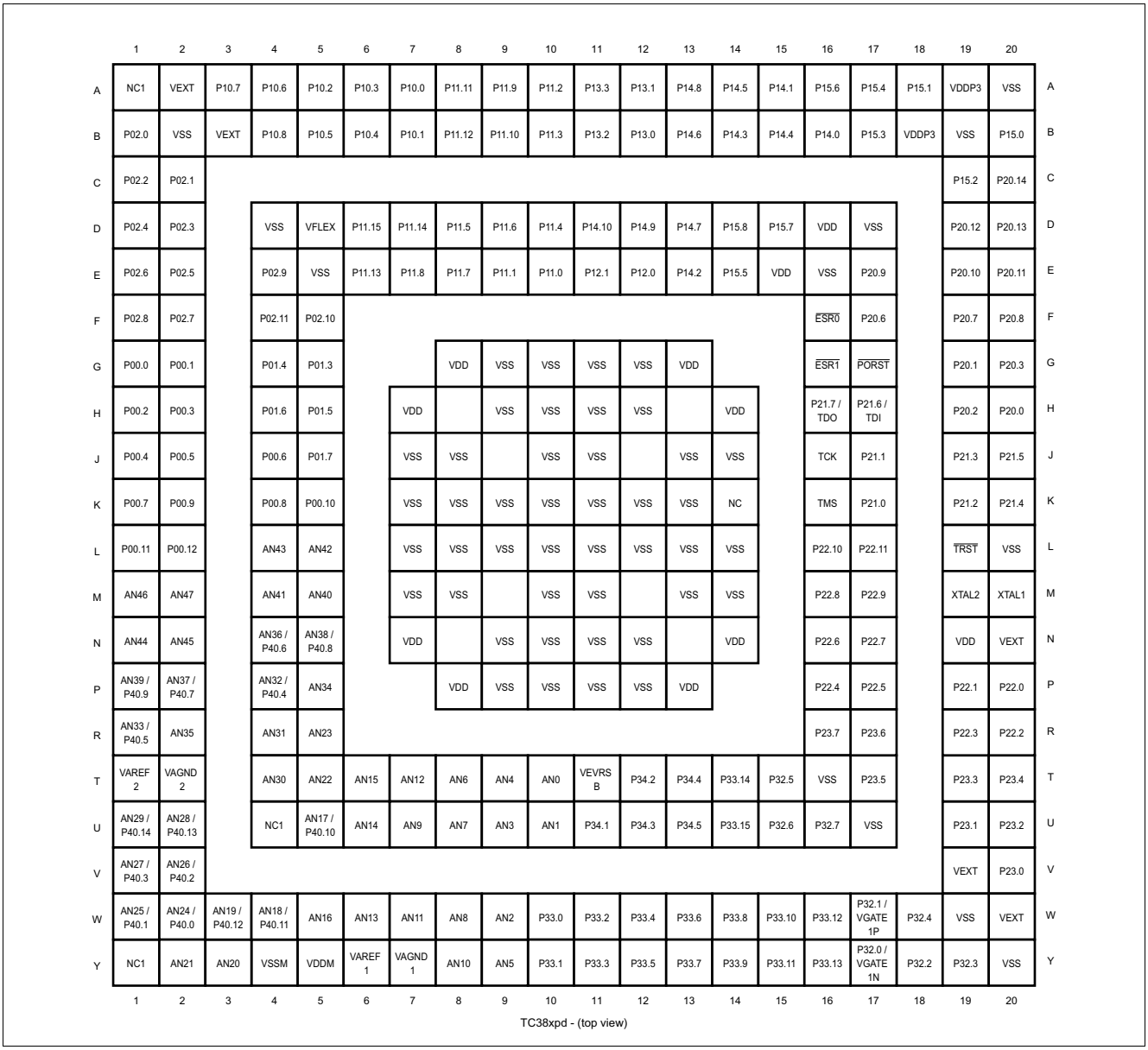

Figure 2-2 Logic Symbol for the package variant BGA292

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2.1 BGA516 Package Variant Pin Configuration

Table 2-1 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
M6	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_10			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN0_1			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M7	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_11			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN1_1			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	EDSADC_DSCIN5A			**Modulator clock input, channel 5**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EDSADC_DSCIN7B			**Modulator clock input, channel 7**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	EDSADC_EDS5NA			**Negative analog input channel 5, pin A**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	EDSADC_DSCOUT7	O5		**Modulator clock output**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N6	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN6_11			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN1_2			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	EDSADC_DSDIN7B			**Digital datastream input, channel 7**
	EDSADC_DSDIN5A			**Digital datastream input, channel 5**
	SENT_SENT1B			**Receive input channel 1**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	EDSADC_EDS5PA			**Positive analog input channel 5, pin A**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	CAN21_TXD	O3		**CAN transmit output node 1**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N7	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN7_10			**Mux input channel 7 of TIM module 5**
	GTM_TIM3_IN2_1			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	EDSADC_ITR5F			**Trigger/Gate input, channel 5**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	CAN21_RXDA			**CAN receive input node 1**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CCU61_CC61INA			**T12 capture input 61**
	ASCLIN12_ARXA			**Receive input**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	EDSADC_EDS5NB			**Negative analog input channel 5, pin B**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	ASCLIN12_ATX	O3		**Transmit output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P6	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM6_IN4_1			**Mux input channel 4 of TIM module 6**
	GTM_TIM3_IN3_1			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	GTM_DTMA5_0			**CDTM5_DTM4**
	GTM_DTMT3_0			**CDTM3_DTM0**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	EDSADC_EDS5PB			**Positive analog input channel 5, pin B**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P7	P00.5	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN4_1			**Mux input channel 4 of TIM module 3**
	GTM_TIM3_IN0_11			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN4_1			**Mux input channel 4 of TIM module 2**
	CCU60_CC62INB			**T12 capture input 62**
	EDSADC_DSCIN2A			**Modulator clock input, channel 2**
	PSI5_RX2A			**RXD inputs (receive data) channel 2**
	CCU61_CC62INA			**T12 capture input 62**
	SENT_SENT4B			**Receive input channel 4**
	CAN11_RXDB			**CAN receive input node 1**
	ASCLIN12_ARXB			**Receive input**
	GTM_DTMT1_1			**CDTM1_DTM0**
	EVADC_G9CH7	AI		**Analog input channel 7, group 9**
	P00.5	O0		**General-purpose output**
	GTM_TOUT14	O1		**GTM muxed output**
	IOM_REF0_14			**Reference input 0**
	EDSADC_CGPWMN	O2		**Negative carrier generator output**
	QSPI3_SLSO3	O3		**Master slave select output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_FC0BFLOUT	O5		**Boundary flag output, FC channel 0**
	SENT_SPC4	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P9	P00.6	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN5_1			**Mux input channel 5 of TIM module 3**
	GTM_TIM3_IN1_14			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN5_1			**Mux input channel 5 of TIM module 2**
	EDSADC_ITR4F			**Trigger/Gate input, channel 4**
	EDSADC_DSDIN2A			**Digital datastream input, channel 2**
	SENT_SENT5B			**Receive input channel 5**
	ASCLIN5_ARXA			**Receive input**
	GTM_DTMT3_1			**CDTM3_DTM0**
	EVADC_G9CH6	AI		**Analog input channel 6, group 9**
	P00.6	O0		**General-purpose output**
	GTM_TOUT15	O1		**GTM muxed output**
	IOM_REF0_15			**Reference input 0**
	EDSADC_CGPWMP	O2		**Positive carrier generator output**
	—	O3		**Reserved**
	PSI5_TX2	O4		**TXD outputs (send data)**
	IOM_REF1_15			**Reference input 1**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC5	O6		**Transmit output**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R6	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN6_1			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN2_11			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	EDSADC_DSCIN4A			**Modulator clock input, channel 4**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	EDSADC_EDS4NA			**Negative analog input channel 4, pin A**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	EVADC_FC2BFLOUT	O3		**Boundary flag output, FC channel 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R9	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN7_1			**Mux input channel 7 of TIM module 3**
	GTM_TIM3_IN3_11			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	EDSADC_DSDIN4A			**Digital datastream input, channel 4**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	EDSADC_EDS4PA			**Positive analog input channel 4, pin A**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R7	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN0_7			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN0_1			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_1			**Mux input channel 0 of TIM module 0**
	CCU61_CC62INC			**T12 capture input 62**
	SENT_SENT8B			**Receive input channel 8**
	CCU61_CCPOS2A			**Hall capture input 2**
	EDSADC_DSCIN1A			**Modulator clock input, channel 1**
	EDSADC_ITR3F			**Trigger/Gate input, channel 3**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CCU60_T12HRC			**External timer start 12**
	ASCLIN13_ARXA			**Receive input**
	EVADC_G9CH3	AI		**Analog input channel 3, group 9**
	EDSADC_EDS4NB			**Negative analog input channel 4, pin B**
	P00.9	O0		**General-purpose output**
	GTM_TOUT18	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	ASCLIN4_ATX	O5		**Transmit output**
	SENT_SPC8	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R10	P00.10	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN1_11			**Mux input channel 1 of TIM module 4**
	GTM_TIM1_IN1_1			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_1			**Mux input channel 1 of TIM module 0**
	SENT_SENT9B			**Receive input channel 9**
	EDSADC_DSDIN1A			**Digital datastream input, channel 1**
	EVADC_G9CH2	AI		**Analog input channel 2, group 9**
	EDSADC_EDS4PB			**Positive analog input channel 4, pin B**
	P00.10	O0		**General-purpose output**
	GTM_TOUT19	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	ASCLIN13_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC9	O6		**Transmit output**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
T6	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN2_11			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_1			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_1			**Mux input channel 2 of TIM module 0**
	CCU60_CTRAPA			**Trap input capture**
	EDSADC_DSCIN0A			**Modulator clock input, channel 0**
	CCU61_T12HRE			**External timer start 12**
	SENT_SENT10B			**Receive input channel 10**
	ASCLIN13_ARXB			**Receive input**
	EVADC_G9CH1	AI		**Analog input channel 1, group 9**
	EVADC_FC3CH0			**Analog input FC channel 3**
	P00.11	O0		**General-purpose output**
	GTM_TOUT20	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	ASCLIN13_ATX	O3		**Transmit output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T7	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN3_11			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	SENT_SENT11B			**Receive input channel 11**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	EVADC_FC2CH0			**Analog input FC channel 2**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
T2	P00.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_2			**Mux input channel 5 of TIM module 6**
	GTM_TIM5_IN0_1			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN0_1			**Mux input channel 0 of TIM module 4**
	EDSADC_DSDIN6A			**Digital datastream input, channel 6**
	P00.13	O0		**General-purpose output**
	GTM_TOUT167	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CCU_EXTCLK1	O4		**External Clock 1**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	P00.14	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_2			**Mux input channel 6 of TIM module 6**
	GTM_TIM5_IN7_1			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN7_1			**Mux input channel 7 of TIM module 4**
	EDSADC_DSCIN6A			**Modulator clock input, channel 6**
	P00.14	O0		**General-purpose output**
	GTM_TOUT166	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	EDSADC_DSCOUT6	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
U1	P00.15	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_2			**Mux input channel 7 of TIM module 6**
	GTM_TIM5_IN1_1			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN1_1			**Mux input channel 1 of TIM module 4**
	EDSADC_ITR6F			**Trigger/Gate input, channel 6**
	P00.15	O0		**General-purpose output**
	GTM_TOUT168	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CCU_EXTCLK0	O4		**External Clock 0**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P01.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_1			**Mux input channel 4 of TIM module 5**
	GTM_TIM4_IN4_1			**Mux input channel 4 of TIM module 4**
	GTM_TIM2_IN6_13			**Mux input channel 6 of TIM module 2**
	CAN21_RXDE			**CAN receive input node 1**
	EDSADC_ITR6E			**Trigger/Gate input, channel 6**
	CAN03_RXDF			**CAN receive input node 3**
	ASCLIN6_ARXB			**Receive input**
	P01.0	O0		**General-purpose output**
	GTM_TOUT155	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
K1	P01.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN1_2			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN1_2			**Mux input channel 1 of TIM module 4**
	EDSADC_ITR8E			**Trigger/Gate input, channel 8**
	ERAY1_RXDA1			**Receive Channel A1**
	SENT_SENT15B			**Receive input channel 15**
	P01.1	O0		**General-purpose output**
	GTM_TOUT159	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	ASCLIN6_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P01.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_1			**Mux input channel 5 of TIM module 5**
	GTM_TIM4_IN5_1			**Mux input channel 5 of TIM module 4**
	EDSADC_DSCIN7A			**Modulator clock input, channel 7**
	P01.2	O0		**General-purpose output**
	GTM_TOUT156	O1		**GTM muxed output**
	—	O2		**Reserved**
	CAN03_TXD	O3		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O4		**Reserved**
	CAN21_TXD	O5		**CAN transmit output node 1**
	EDSADC_DSCOUT7	O6		**Modulator clock output**
	—	O7		**Reserved**
M10	P01.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_2			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_14			**Mux input channel 0 of TIM module 2**
	GTM_TIM0_IN5_8			**Mux input channel 5 of TIM module 0**
	QSPI3_SLSIB			**Slave select input**
	EDSADC_ITR7F			**Trigger/Gate input, channel 7**
	EVADC_G9CH14	AI		**Analog input channel 14, group 9**
	P01.3	O0		**General-purpose output**
	GTM_TOUT111	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_SLSO9	O4		**Master slave select output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M9	P01.4	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_2			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_14			**Mux input channel 1 of TIM module 2**
	GTM_TIM0_IN6_8			**Mux input channel 6 of TIM module 0**
	CAN01_RXDC			**CAN receive input node 1**
	EDSADC_ITR7E			**Trigger/Gate input, channel 7**
	EVADC_G9CH13	AI		**Analog input channel 13, group 9**
	P01.4	O0		**General-purpose output**
	GTM_TOUT112	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ASLSO	O3		**Slave select signal output**
	QSPI3_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
N10	P01.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_2			**Mux input channel 3 of TIM module 5**
	GTM_TIM2_IN3_7			**Mux input channel 3 of TIM module 2**
	GTM_TIM2_IN2_7			**Mux input channel 2 of TIM module 2**
	QSPI3_MRSTC			**Master SPI data input**
	EDSADC_DSCIN8A			**Modulator clock input, channel 8**
	ASCLIN9_ARXA			**Receive input**
	EVADC_G9CH12	AI		**Analog input channel 12, group 9**
	P01.5	O0		**General-purpose output**
	GTM_TOUT113	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_MRST	O4		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O5		**Reserved**
	EDSADC_DSCOUT8	O6		**Modulator clock output**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N9	P01.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_2			**Mux input channel 6 of TIM module 5**
	GTM_TIM5_IN5_3			**Mux input channel 5 of TIM module 5**
	GTM_TIM2_IN5_7			**Mux input channel 5 of TIM module 2**
	QSPI3_MTSRC			**Slave SPI data input**
	EDSADC_DSDIN8A			**Digital datastream input, channel 8**
	P01.6	O0		**General-purpose output**
	GTM_TOUT114	O1		**GTM muxed output**
	ASCLIN12_ATX	O2		**Transmit output**
	ASCLIN9_ASCLK	O3		**Shift clock output**
	QSPI3_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
P10	P01.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_2			**Mux input channel 7 of TIM module 5**
	GTM_TIM2_IN7_7			**Mux input channel 7 of TIM module 2**
	QSPI3_SCLKC			**Slave SPI clock inputs**
	EDSADC_ITR8F			**Trigger/Gate input, channel 8**
	ASCLIN9_ARXB			**Receive input**
	P01.7	O0		**General-purpose output**
	GTM_TOUT115	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ATX	O3		**Transmit output**
	QSPI3_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L1	P01.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_2			**Mux input channel 4 of TIM module 5**
	GTM_TIM5_IN0_10			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN4_2			**Mux input channel 4 of TIM module 4**
	CAN00_RXDF			**CAN receive input node 0**
	ERAY1_RXDB1			**Receive Channel B1**
	EDSADC_DSDIN9A			**Digital datastream input, channel 9**
	SENT_SENT17B			**Receive input channel 17**
	ASCLIN0_ARXC			**Receive input**
	CAN20_RXDE			**CAN receive input node 0**
	ASCLIN7_ARXB			**Receive input**
	P01.8	O0		**General-purpose output**
	GTM_TOUT162	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
L2	P01.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN2_1			**Mux input channel 2 of TIM module 5**
	GTM_TIM5_IN1_11			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN2_1			**Mux input channel 2 of TIM module 4**
	EDSADC_DSCIN9A			**Modulator clock input, channel 9**
	SENT_SENT16B			**Receive input channel 16**
	P01.9	O0		**General-purpose output**
	GTM_TOUT160	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EDSADC_DSCOUT9	O6		**Modulator clock output**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M2	P01.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_2			**Mux input channel 5 of TIM module 5**
	GTM_TIM5_IN2_9			**Mux input channel 2 of TIM module 5**
	GTM_TIM4_IN5_3			**Mux input channel 5 of TIM module 4**
	EDSADC_ITR9F			**Trigger/Gate input, channel 9**
	SENT_SENT18B			**Receive input channel 18**
	GTM_DTMT3_2			**CDTM3_DTM0**
	P01.10	O0		**General-purpose output**
	GTM_TOUT163	O1		**GTM muxed output**
	ASCLIN7_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
M1	P01.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_3			**Mux input channel 7 of TIM module 5**
	GTM_TIM5_IN3_11			**Mux input channel 3 of TIM module 5**
	GTM_TIM4_IN7_2			**Mux input channel 7 of TIM module 4**
	EDSADC_ITR9E			**Trigger/Gate input, channel 9**
	SENT_SENT19B			**Receive input channel 19**
	GTM_DTMA5_1			**CDTM5_DTM4**
	P01.11	O0		**General-purpose output**
	GTM_TOUT165	O1		**GTM muxed output**
	ASCLIN7_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N2	P01.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_3			**Mux input channel 0 of TIM module 6**
	GTM_TIM5_IN0_2			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN0_2			**Mux input channel 0 of TIM module 4**
	P01.12	O0		**General-purpose output**
	GTM_TOUT158	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY1_TXDA	O6		**Transmit Channel A**
	—	O7		**Reserved**
N1	P01.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_3			**Mux input channel 1 of TIM module 6**
	GTM_TIM5_IN3_1			**Mux input channel 3 of TIM module 5**
	GTM_TIM4_IN3_1			**Mux input channel 3 of TIM module 4**
	P01.13	O0		**General-purpose output**
	GTM_TOUT161	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	CAN00_TXD	O4		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	CAN20_TXD	O5		**CAN transmit output node 0**
	ERAY1_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P2	P01.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_3			**Mux input channel 2 of TIM module 6**
	GTM_TIM5_IN6_3			**Mux input channel 6 of TIM module 5**
	GTM_TIM4_IN6_3			**Mux input channel 6 of TIM module 4**
	P01.14	O0		**General-purpose output**
	GTM_TOUT164	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY1_TXENA	O6		**Transmit Enable Channel A**
	—	O7		**Reserved**
P1	P01.15	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_3			**Mux input channel 3 of TIM module 6**
	GTM_TIM5_IN6_1			**Mux input channel 6 of TIM module 5**
	GTM_TIM4_IN6_1			**Mux input channel 6 of TIM module 4**
	EDSADC_DSDIN7A			**Digital datastream input, channel 7**
	P01.15	O0		**General-purpose output**
	GTM_TOUT157	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-3 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G6	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H7	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	QSPI4_SLSO7	O2		**Master slave select output**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H6	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	SENT_SENT14B			**Receive input channel 14**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J7	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	EDSADC_DSCIN5B			**Modulator clock input, channel 5**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	MSC1_SDI1			**Upstream assynchronous input signal**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	SENT_SENT13B			**Receive input channel 13**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J6	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	EDSADC_DSDIN5B			**Digital datastream input, channel 5**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	SENT_SENT12B			**Receive input channel 12**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K7	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	EDSADC_DSCIN4B			**Modulator clock input, channel 4**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K6	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_10			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	EDSADC_DSDIN4B			**Digital datastream input, channel 4**
	EDSADC_ITR5E			**Trigger/Gate input, channel 5**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_10			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	EDSADC_ITR4E			**Trigger/Gate input, channel 4**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	PSI5_RX2B			**RXD inputs (receive data) channel 2**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L6	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_10			**Mux input channel 2 of TIM module 3**
	GTM_TIM3_IN0_2			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	PSI5_TX2	O4		**TXD outputs (send data)**
	IOM_REF1_15			**Reference input 1**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K9	P02.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_2			**Mux input channel 2 of TIM module 4**
	GTM_TIM3_IN3_10			**Mux input channel 3 of TIM module 3**
	GTM_TIM0_IN2_10			**Mux input channel 2 of TIM module 0**
	SENT_SENT20B			**Receive input channel 20**
	ASCLIN8_ARXA			**Receive input**
	P02.9	O0		**General-purpose output**
	GTM_TOUT116	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	ASCLIN8_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
L10	P02.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_2			**Mux input channel 3 of TIM module 4**
	GTM_TIM3_IN4_11			**Mux input channel 4 of TIM module 3**
	GTM_TIM0_IN3_10			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXC			**Receive input**
	CAN01_RXDE			**CAN receive input node 1**
	SENT_SENT21B			**Receive input channel 21**
	ASCLIN8_ARXB			**Receive input**
	P02.10	O0		**General-purpose output**
	GTM_TOUT117	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L9	P02.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_3			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN5_12			**Mux input channel 5 of TIM module 3**
	GTM_TIM0_IN7_7			**Mux input channel 7 of TIM module 0**
	SENT_SENT22B			**Receive input channel 22**
	EVADC_G9CH15	AI		**Analog input channel 15, group 9**
	P02.11	O0		**General-purpose output**
	GTM_TOUT118	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN8_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
F2	P02.12	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN0_3			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN0_3			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN6_12			**Mux input channel 6 of TIM module 3**
	SENT_SENT23B			**Receive input channel 23**
	P02.12	O0		**General-purpose output**
	GTM_TOUT151	O1		**GTM muxed output**
	QSPI3_SLSO5	O2		**Master slave select output**
	QSPI4_SLSO4	O3		**Master slave select output**
	ASCLIN6_ASLSO	O4		**Slave select signal output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.13	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN2_2			**Mux input channel 2 of TIM module 5**
	GTM_TIM4_IN2_3			**Mux input channel 2 of TIM module 4**
	GTM_TIM3_IN7_11			**Mux input channel 7 of TIM module 3**
	SENT_SENT24B			**Receive input channel 24**
	P02.13	O0		**General-purpose output**
	GTM_TOUT153	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	QSPI4_SLSO6	O3		**Master slave select output**
	CAN00_TXD	O4		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
G2	P02.14	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_3			**Mux input channel 3 of TIM module 5**
	GTM_TIM4_IN3_3			**Mux input channel 3 of TIM module 4**
	GTM_TIM2_IN4_14			**Mux input channel 4 of TIM module 2**
	CAN20_RXDD			**CAN receive input node 0**
	CAN00_RXDH			**CAN receive input node 0**
	P02.14	O0		**General-purpose output**
	GTM_TOUT154	O1		**GTM muxed output**
	ASCLIN6_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P02.15	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN1_3			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN1_3			**Mux input channel 1 of TIM module 4**
	GTM_TIM2_IN5_14			**Mux input channel 5 of TIM module 2**
	P02.15	O0		**General-purpose output**
	GTM_TOUT152	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	QSPI4_SLSO5	O3		**Master slave select output**
	ASCLIN6_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	ERAY1_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

Table 2-4 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
F12	P10.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_12			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN4_2			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_2			**Mux input channel 4 of TIM module 0**
	GPT120_T6EUDB			**Count direction control input of core timer T6**
	ASCLIN11_ARXA			**Receive input**
	GETH_RXERC			**Receive Error MII**
	GTM_DTMA5_2			**CDTM5_DTM4**
	P10.0	O0		**General-purpose output**
	GTM_TOUT102	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	QSPI1_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN22_ATX	O6		**Transmit output**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G12	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_12			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN1_3			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_3			**Mux input channel 1 of TIM module 0**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	GTM_DTMT0_1			**CDTM0_DTM0**
	P10.1	O0		**General-purpose output**
	GTM_TOUT103	O1		**GTM muxed output**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	MSC0_EN1	O4		**Chip Select**
	EVADC_FC1BFLOUT	O5		**Boundary flag output, FC channel 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
F10	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_12			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN2_3			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_3			**Mux input channel 2 of TIM module 0**
	CAN02_RXDE			**CAN receive input node 2**
	MSC0_SDI1			**Upstream assynchronous input signal**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMT2_2			**CDTM2_DTM0**
	P10.2	O0		**General-purpose output**
	GTM_TOUT104	O1		**GTM muxed output**
	IOM_MON2_9			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	MSC0_EN0	O4		**Chip Select**
	EVADC_FC3BFLOUT	O5		**Boundary flag output, FC channel 3**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F11	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_10			**Mux input channel 6 of TIM module 4**
	GTM_TIM1_IN3_3			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_3			**Mux input channel 3 of TIM module 0**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	GTM_TOUT105	O1		**GTM muxed output**
	IOM_MON2_10			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	MSC0_EN0	O4		**Chip Select**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
G11	P10.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_3			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN6_2			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_2			**Mux input channel 6 of TIM module 0**
	QSPI1_MTSRC			**Slave SPI data input**
	CCU60_CCPOS0C			**Hall capture input 0**
	GPT120_T3INB			**Trigger/gate input of core timer T3**
	ASCLIN11_ARXB			**Receive input**
	ASCLIN22_ARXA			**Receive input**
	P10.4	O0		**General-purpose output**
	GTM_TOUT106	O1		**GTM muxed output**
	IOM_MON2_11			**Monitor input 2**
	ASCLIN22_ATX	O2		**Transmit output**
	QSPI1_SLSO8	O3		**Master slave select output**
	QSPI1_MTSR	O4		**Master SPI data output**
	MSC0_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G10	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_13			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	CAN20_RXDA			**CAN receive input node 0**
	MSC0_INJ1			**Injection signal from port**
	ASCLIN22_ARXB			**Receive input**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	PSI5_TX3	O7		**TXD outputs (send data)**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F9	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_13			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	PSI5_RX3C			**RXD inputs (receive data) channel 3**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	ASCLIN23_ARXA			**Receive input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	CAN20_TXD	O5		**CAN transmit output node 0**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F8	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_3			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_3			**Mux input channel 0 of TIM module 0**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	ASCLIN23_ARXB			**Receive input**
	P10.7	O0		**General-purpose output**
	GTM_TOUT109	O1		**GTM muxed output**
	IOM_REF2_11			**Reference input 2**
	ASCLIN23_ATX	O2		**Transmit output**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G9	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_13			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN5_2			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_2			**Mux input channel 5 of TIM module 0**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	CAN20_RXDB			**CAN receive input node 0**
	P10.8	O0		**General-purpose output**
	GTM_TOUT110	O1		**GTM muxed output**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	ASCLIN23_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B8	P10.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_5			**Mux input channel 0 of TIM module 6**
	GTM_TIM4_IN1_4			**Mux input channel 1 of TIM module 4**
	GTM_TIM0_IN1_10			**Mux input channel 1 of TIM module 0**
	SENT_SENT15C			**Receive input channel 15**
	ASCLIN6_ARXD			**Receive input**
	P10.9	O0		**General-purpose output**
	GTM_TOUT265	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P10.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_5			**Mux input channel 1 of TIM module 6**
	GTM_TIM4_IN2_4			**Mux input channel 2 of TIM module 4**
	GTM_TIM0_IN2_11			**Mux input channel 2 of TIM module 0**
	SENT_SENT16C			**Receive input channel 16**
	P10.10	O0		**General-purpose output**
	GTM_TOUT266	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A7	P10.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_5			**Mux input channel 2 of TIM module 6**
	GTM_TIM4_IN5_4			**Mux input channel 5 of TIM module 4**
	GTM_TIM0_IN5_9			**Mux input channel 5 of TIM module 0**
	SENT_SENT19C			**Receive input channel 19**
	P10.11	O0		**General-purpose output**
	GTM_TOUT269	O1		**GTM muxed output**
	ASCLIN6_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P10.13	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_5			**Mux input channel 3 of TIM module 6**
	GTM_TIM4_IN4_4			**Mux input channel 4 of TIM module 4**
	GTM_TIM0_IN4_9			**Mux input channel 4 of TIM module 0**
	SENT_SENT18C			**Receive input channel 18**
	P10.13	O0		**General-purpose output**
	GTM_TOUT268	O1		**GTM muxed output**
	ASCLIN6_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B5	P10.14	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_4			**Mux input channel 3 of TIM module 4**
	GTM_TIM0_IN3_11			**Mux input channel 3 of TIM module 0**
	SENT_SENT17C			**Receive input channel 17**
	P10.14	O0		**General-purpose output**
	GTM_TOUT267	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A5	P10.15	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_4			**Mux input channel 6 of TIM module 4**
	GTM_TIM0_IN6_9			**Mux input channel 6 of TIM module 0**
	P10.15	O0		**General-purpose output**
	GTM_TOUT270	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K15	P11.0	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_4			**Mux input channel 0 of TIM module 4**
	GTM_TIM2_IN0_7			**Mux input channel 0 of TIM module 2**
	ASCLIN3_ARXB			**Receive input**
	GTM_DTMA2_1			**CDTM2_DTM4**
	P11.0	O0		**General-purpose output**
	GTM_TOUT119	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN11_TXD	O5		**CAN transmit output node 1**
	GETH_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**
K14	P11.1	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_5			**Mux input channel 1 of TIM module 4**
	GTM_TIM2_IN1_6			**Mux input channel 1 of TIM module 2**
	P11.1	O0		**General-purpose output**
	GTM_TOUT120	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F15	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN1_3			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
G15	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN2_2			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J15	P11.4	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN2_5			**Mux input channel 2 of TIM module 4**
	GTM_TIM2_IN2_6			**Mux input channel 2 of TIM module 2**
	GETH_RXCLKB			**Receive Clock MII**
	P11.4	O0		**General-purpose output**
	GTM_TOUT121	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN13_TXD	O5		**CAN transmit output node 3**
	GETH_TXER	O6		**Transmit Error MII**
	GETH_TXCLK	O7		**Transmit Clock Output for RGMII**
J13	P11.5	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN3_5			**Mux input channel 3 of TIM module 4**
	GTM_TIM2_IN3_8			**Mux input channel 3 of TIM module 2**
	GETH_TXCLKA			**Transmit Clock Input for MII**
	GETH_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P11.5	O0		**General-purpose output**
	GTM_TOUT122	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J14	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN3_2			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**
K13	P11.7	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN4_5			**Mux input channel 4 of TIM module 4**
	GTM_TIM2_IN4_7			**Mux input channel 4 of TIM module 2**
	GETH_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	CAN11_RXDD			**CAN receive input node 1**
	P11.7	O0		**General-purpose output**
	GTM_TOUT123	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K12	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN5_5			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN5_8			**Mux input channel 5 of TIM module 2**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	GTM_TOUT124	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
F14	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN4_2			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G14	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN5_2			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_2			**Mux input channel 5 of TIM module 2**
	GTM_TIM2_IN0_9			**Mux input channel 0 of TIM module 2**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	MSC0_SDI0			**Upstream assynchronous input signal**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	GTM_TOUT99	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F13	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN6_2			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN0_14			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN6_2			**Mux input channel 6 of TIM module 2**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	GTM_TOUT100	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	MSC0_EN0	O5		**Chip Select**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
G13	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN7_2			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_2			**Mux input channel 7 of TIM module 2**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	GTM_TOUT101	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	GTM_CLK2	O3		**CGM generated clock**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K11	P11.13	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN6_5			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN6_7			**Mux input channel 6 of TIM module 2**
	GETH_RXERA			**Receive Error MII**
	I2C1_SDAA			**Serial Data Input 0**
	CAN13_RXDD			**CAN receive input node 3**
	P11.13	O0		**General-purpose output**
	GTM_TOUT125	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C1_SDA	O6		**Serial Data Output**
	—	O7		**Reserved**
J12	P11.14	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_4			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_8			**Mux input channel 7 of TIM module 2**
	GETH_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVB			**Receive Data Valid MII**
	GETH_CRSA			**Carrier Sense MII**
	I2C1_SCLA			**Serial Clock Input 0**
	CAN20_RXDF			**CAN receive input node 0**
	P11.14	O0		**General-purpose output**
	GTM_TOUT126	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C1_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J11	P11.15	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_5			**Mux input channel 7 of TIM module 4**
	GTM_TIM0_IN7_8			**Mux input channel 7 of TIM module 0**
	GETH_COLA			**Collision MII**
	P11.15	O0		**General-purpose output**
	GTM_TOUT127	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-6 Port 12 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P12.0	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_5			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN0_7			**Mux input channel 0 of TIM module 3**
	CAN00_RXDC			**CAN receive input node 0**
	GETH_RXCLKC			**Receive Clock MII**
	GTM_DTMA4_0			**CDTM4_DTM4**
	P12.0	O0		**General-purpose output**
	GTM_TOUT128	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_MDC	O6		**MDIO clock**
	—	O7		**Reserved**

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Table 2-6 Port 12 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K16	P12.1	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_6			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN1_6			**Mux input channel 1 of TIM module 3**
	GETH_MDIOC			**MDIO Input**
	P12.1	O0		**General-purpose output**
	GTM_TOUT129	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

Table 2-7 Port 13 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G17	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN5_3			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_3			**Mux input channel 5 of TIM module 2**
	ASCLIN10_ARXC			**Receive input**
	ASCLIN21_ARXA			**Receive input**
	P13.0	O0		**General-purpose output**
	GTM_TOUT91	O1		**GTM muxed output**
	ASCLIN10_ATX	O2		**Transmit output**
	QSPI2_SCLKN	O3		**Master SPI clock output (LVDS N line)**
	MSC0_EN1	O4		**Chip Select**
	MSC0_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	CAN10_TXD	O7		**CAN transmit output node 0**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F17	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN6_3			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_3			**Mux input channel 6 of TIM module 2**
	I2C0_SCLB			**Serial Clock Input 1**
	CAN10_RXDD			**CAN receive input node 0**
	ASCLIN10_ARXD			**Receive input**
	P13.1	O0		**General-purpose output**
	GTM_TOUT92	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLKP	O3		**Master SPI clock output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	I2C0_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**
G16	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN7_3			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_3			**Mux input channel 7 of TIM module 2**
	GPT120_CAPINA			**Trigger input to capture value of timer T5 into CAPREL register**
	I2C0_SDAB			**Serial Data Input 1**
	P13.2	O0		**General-purpose output**
	GTM_TOUT93	O1		**GTM muxed output**
	ASCLIN10_ASCLK	O2		**Shift clock output**
	QSPI2_MTSRN	O3		**Master SPI data output (LVDS N line)**
	MSC0_FCLP	O4		**Shift-clock direct part of the differential signal**
	MSC0_SON	O5		**Data output - inverted part of the differential signal**
	I2C0_SDA	O6		**Serial Data Output**
	ASCLIN21_ATX	O7		**Transmit output**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F16	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN0_3			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_3			**Mux input channel 0 of TIM module 2**
	ASCLIN21_ARXB			**Receive input**
	P13.3	O0		**General-purpose output**
	GTM_TOUT94	O1		**GTM muxed output**
	ASCLIN10_ASLSO	O2		**Slave select signal output**
	QSPI2_MTSRP	O3		**Master SPI data output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	ASCLIN21_ATX	O6		**Transmit output**
	—	O7		**Reserved**
B16	P13.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM6_IN0_4			**Mux input channel 0 of TIM module 6**
	GTM_TIM5_IN3_4			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN3_8			**Mux input channel 3 of TIM module 3**
	P13.4	O0		**General-purpose output**
	GTM_TOUT253	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	MSC2_EN0	O4		**Chip Select**
	MSC2_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	CAN23_TXD	O7		**CAN transmit output node 3**
A16	P13.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM6_IN1_4			**Mux input channel 1 of TIM module 6**
	GTM_TIM5_IN4_4			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN4_9			**Mux input channel 4 of TIM module 3**
	CAN23_RXDD			**CAN receive input node 3**
	P13.5	O0		**General-purpose output**
	GTM_TOUT254	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	MSC2_FCLP	O5		**Shift-clock direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B15	P13.6	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM6_IN2_4			**Mux input channel 2 of TIM module 6**
	GTM_TIM5_IN5_4			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN5_10			**Mux input channel 5 of TIM module 3**
	P13.6	O0		**General-purpose output**
	GTM_TOUT255	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	MSC2_SON	O5		**Data output - inverted part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
A15	P13.7	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM6_IN3_4			**Mux input channel 3 of TIM module 6**
	GTM_TIM5_IN6_4			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN6_10			**Mux input channel 6 of TIM module 3**
	P13.7	O0		**General-purpose output**
	GTM_TOUT256	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	MSC2_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P13.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_4			**Mux input channel 4 of TIM module 6**
	GTM_TIM4_IN7_6			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_12			**Mux input channel 7 of TIM module 2**
	I2C1_SCLB			**Serial Clock Input 1**
	P13.9	O0		**General-purpose output**
	GTM_TOUT248	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN21_TXD	O5		**CAN transmit output node 1**
	I2C1_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**
B13	P13.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_4			**Mux input channel 5 of TIM module 6**
	GTM_TIM5_IN1_5			**Mux input channel 1 of TIM module 5**
	GTM_TIM3_IN1_8			**Mux input channel 1 of TIM module 3**
	PSI5_RX3A			**RXD inputs (receive data) channel 3**
	P13.10	O0		**General-purpose output**
	GTM_TOUT251	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A13	P13.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_4			**Mux input channel 6 of TIM module 6**
	GTM_TIM5_IN0_9			**Mux input channel 0 of TIM module 5**
	GTM_TIM3_IN0_9			**Mux input channel 0 of TIM module 3**
	ASCLIN0_ARXE			**Receive input**
	ASCLIN7_ARXD			**Receive input**
	P13.11	O0		**General-purpose output**
	GTM_TOUT250	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	PSI5_TX3	O4		**TXD outputs (send data)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B12	P13.12	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_4			**Mux input channel 7 of TIM module 6**
	GTM_TIM4_IN0_6			**Mux input channel 0 of TIM module 4**
	GTM_TIM0_IN0_11			**Mux input channel 0 of TIM module 0**
	ASCLIN3_ARXH			**Receive input**
	I2C1_SDAB			**Serial Data Input 1**
	CAN21_RXDB			**CAN receive input node 1**
	P13.12	O0		**General-purpose output**
	GTM_TOUT249	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C1_SDA	O6		**Serial Data Output**
	—	O7		**Reserved**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P13.13	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_5			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN5_9			**Mux input channel 5 of TIM module 3**
	MSC2_INJ0			**Injection signal from port**
	PSI5_RX3B			**RXD inputs (receive data) channel 3**
	P13.13	O0		**General-purpose output**
	GTM_TOUT262	O1		**GTM muxed output**
	ASCLIN7_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B11	P13.14	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN2_4			**Mux input channel 2 of TIM module 5**
	GTM_TIM3_IN2_7			**Mux input channel 2 of TIM module 3**
	P13.14	O0		**General-purpose output**
	GTM_TOUT252	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A11	P13.15	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_4			**Mux input channel 7 of TIM module 5**
	GTM_TIM3_IN7_9			**Mux input channel 7 of TIM module 3**
	P13.15	O0		**General-purpose output**
	GTM_TOUT264	O1		**GTM muxed output**
	ASCLIN7_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	PSI5_TX3	O4		**TXD outputs (send data)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G21	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	SENT_SENT17D			**Receive input channel 17**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F20	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN4_3			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_3			**Mux input channel 4 of TIM module 0**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	SENT_SENT18D			**Receive input channel 18**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	GTM_TOUT81	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
K18	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_3			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_3			**Mux input channel 5 of TIM module 0**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	GTM_TOUT82	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G19	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
G20	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	ERAY1_TXDB	O7		**Transmit Channel B**
G18	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	ERAY1_TXENB	O7		**Transmit Enable Channel B**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J18	P14.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_10			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN0_5			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_5			**Mux input channel 0 of TIM module 0**
	ERAY0_RXDB0			**Receive Channel B0**
	ERAY1_RXDB0			**Receive Channel B0**
	CAN10_RXDB			**CAN receive input node 0**
	CAN13_RXDA			**CAN receive input node 3**
	ASCLIN9_ARXC			**Receive input**
	ASCLIN20_ARXA			**Receive input**
	P14.7	O0		**General-purpose output**
	GTM_TOUT87	O1		**GTM muxed output**
	ASCLIN0_ARTS	O2		**Ready to send output**
	QSPI2_SLSO4	O3		**Master slave select output**
	ASCLIN9_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	ASCLIN20_ATX	O7		**Transmit output**
F18	P14.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_3			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_3			**Mux input channel 2 of TIM module 2**
	ERAY0_RXDA0			**Receive Channel A0**
	CAN02_RXDD			**CAN receive input node 2**
	ASCLIN1_ARXD			**Receive input**
	ERAY1_RXDA0			**Receive Channel A0**
	P14.8	O0		**General-purpose output**
	GTM_TOUT88	O1		**GTM muxed output**
	ASCLIN5_ASLSO	O2		**Slave select signal output**
	ASCLIN7_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	ASCLIN20_ATX	O7		**Transmit output**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J17	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_3			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_3			**Mux input channel 3 of TIM module 2**
	ASCLIN0_ACTSA			**Clear to send input**
	QSPI2_MRSTFN			**Master SPI data input (LVDS N line)**
	ASCLIN9_ARXD			**Receive input**
	ASCLIN20_ARXB			**Receive input**
	P14.9	O0		**General-purpose output**
	GTM_TOUT89	O1		**GTM muxed output**
	CAN23_TXD	O2		**CAN transmit output node 3**
	MSC0_EN1	O3		**Chip Select**
	CAN10_TXD	O4		**CAN transmit output node 0**
	ERAY0_TXENB	O5		**Transmit Enable Channel B**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	ERAY1_TXENA	O7		**Transmit Enable Channel A**
J16	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_3			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_3			**Mux input channel 4 of TIM module 2**
	CAN23_RXDA			**CAN receive input node 3**
	QSPI2_MRSTFP			**Master SPI data input (LVDS P line)**
	P14.10	O0		**General-purpose output**
	GTM_TOUT90	O1		**GTM muxed output**
	—	O2		**Reserved**
	MSC0_EN0	O3		**Chip Select**
	ASCLIN1_ATX	O4		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	ERAY1_TXDA	O7		**Transmit Channel A**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A20	P14.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN1_4			**Mux input channel 1 of TIM module 5**
	GTM_TIM3_IN1_9			**Mux input channel 1 of TIM module 3**
	MSC2_SDI1			**Upstream assynchronous input signal**
	P14.11	O0		**General-purpose output**
	GTM_TOUT258	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	MSC2_EN2	O4		**Chip Select**
	MSC2_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
B19	P14.12	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_3			**Mux input channel 4 of TIM module 6**
	GTM_TIM5_IN4_5			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN4_8			**Mux input channel 4 of TIM module 3**
	MSC2_SDI0			**Upstream assynchronous input signal**
	P14.12	O0		**General-purpose output**
	GTM_TOUT261	O1		**GTM muxed output**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	ASCLIN7_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A19	P14.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_3			**Mux input channel 5 of TIM module 6**
	GTM_TIM5_IN3_5			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN3_6			**Mux input channel 3 of TIM module 3**
	P14.13	O0		**General-purpose output**
	GTM_TOUT260	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	MSC2_EN1	O4		**Chip Select**
	CAN22_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B18	P14.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_3			**Mux input channel 6 of TIM module 6**
	GTM_TIM5_IN2_3			**Mux input channel 2 of TIM module 5**
	GTM_TIM3_IN2_8			**Mux input channel 2 of TIM module 3**
	CAN22_RXDD			**CAN receive input node 2**
	P14.14	O0		**General-purpose output**
	GTM_TOUT259	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	ASCLIN7_ATX	O3		**Transmit output**
	MSC2_EN0	O4		**Chip Select**
	CAN23_TXD	O5		**CAN transmit output node 3**
	—	O6		**Reserved**
	—	O7		**Reserved**
A18	P14.15	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_3			**Mux input channel 7 of TIM module 6**
	GTM_TIM5_IN6_5			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN6_9			**Mux input channel 6 of TIM module 3**
	MSC2_INJ1			**Injection signal from port**
	ASCLIN5_ARXD			**Receive input**
	ASCLIN7_ARXA			**Receive input**
	CAN23_RXDC			**CAN receive input node 3**
	P14.15	O0		**General-purpose output**
	GTM_TOUT263	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-9 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G25	P15.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_4			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_4			**Mux input channel 3 of TIM module 2**
	P15.0	O0		**General-purpose output**
	GTM_TOUT71	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO13	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
F23	P15.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_4			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_4			**Mux input channel 4 of TIM module 2**
	CAN02_RXDA			**CAN receive input node 2**
	ASCLIN1_ARXA			**Receive input**
	QSPI2_SLSIB			**Slave select input**
	SCU_E_REQ7_2			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.1	O0		**General-purpose output**
	GTM_TOUT72	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H24	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_4			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_4			**Mux input channel 5 of TIM module 2**
	QSPI2_SLSIA			**Slave select input**
	SENT_SENT10D			**Receive input channel 10**
	QSPI2_MRSTE			**Master SPI data input**
	P15.2	O0		**General-purpose output**
	GTM_TOUT73	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
G22	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_4			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_4			**Mux input channel 6 of TIM module 2**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	P15.3	O0		**General-purpose output**
	GTM_TOUT74	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	MSC0_EN1	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F22	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_4			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT11D			**Receive input channel 11**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	ASCLIN19_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_4			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
F21	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	ASCLIN19_ARXA			**Receive input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J20	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	ASCLIN19_ARXB			**Receive input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	ASCLIN19_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
J19	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B24	P15.10	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM4_IN1_7			**Mux input channel 1 of TIM module 4**
	GTM_TIM2_IN1_8			**Mux input channel 1 of TIM module 2**
	P15.10	O0		**General-purpose output**
	GTM_TOUT242	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A24	P15.11	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM4_IN2_6			**Mux input channel 2 of TIM module 4**
	GTM_TIM2_IN2_8			**Mux input channel 2 of TIM module 2**
	P15.11	O0		**General-purpose output**
	GTM_TOUT243	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B23	P15.12	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM4_IN3_6			**Mux input channel 3 of TIM module 4**
	GTM_TIM2_IN3_6			**Mux input channel 3 of TIM module 2**
	P15.12	O0		**General-purpose output**
	GTM_TOUT244	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A23	P15.13	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM4_IN4_6			**Mux input channel 4 of TIM module 4**
	GTM_TIM2_IN4_9			**Mux input channel 4 of TIM module 2**
	P15.13	O0		**General-purpose output**
	GTM_TOUT245	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B22	P15.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_6			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN5_12			**Mux input channel 5 of TIM module 2**
	P15.14	O0		**General-purpose output**
	GTM_TOUT246	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A22	P15.15	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_6			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN6_9			**Mux input channel 6 of TIM module 2**
	P15.15	O0		**General-purpose output**
	GTM_TOUT247	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-10 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
N25	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CAN21_RXDC			**CAN receive input node 1**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
M24	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_11			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN3_5			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_5			**Mux input channel 3 of TIM module 2**
	CBS_TGI1			**Trigger input**
	GTM_DTMA1_1			**CDTM1_DTM4**
	P20.1	O0		**General-purpose output**
	GTM_TOUT60	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N24	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**
M25	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_11			**Mux input channel 5 of TIM module 4**
	GTM_TIM3_IN4_5			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
L22	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_1			**Mux input channel 0 of TIM module 6**
	GTM_TIM3_IN6_5			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L24	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_5			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	GTM_TIM6_IN1_1			**Mux input channel 1 of TIM module 6**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
L25	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_1			**Mux input channel 2 of TIM module 6**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K22	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_1			**Mux input channel 3 of TIM module 6**
	GTM_TIM3_IN5_5			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
K24	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_6			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K25	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_6			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
J24	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_5			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J25	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_4			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
H25	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_4			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	IOM_PIN_15			**GPIO pad input to FPC**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-11 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
R22	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_11			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN4_6			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_6			**Mux input channel 4 of TIM module 2**
	QSPI4_MRSTDN			**Master SPI data input (LVDS N line)**
	DMU_FDEST			**Enter destructive debug mode**
	ASCLIN11_ARXC			**Receive input**
	ASCLIN17_ARXB			**Receive input**
	P21.0	O0		**General-purpose output**
	GTM_TOUT51	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
P22	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN1_13			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_6			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_6			**Mux input channel 5 of TIM module 2**
	QSPI4_MRSTDP			**Master SPI data input (LVDS P line)**
	ASCLIN11_ARXD			**Receive input**
	ASCLIN18_ARXA			**Receive input**
	GTM_DTMA4_1			**CDTM4_DTM4**
	P21.1	O0		**General-purpose output**
	GTM_TOUT52	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R24	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_11			**Mux input channel 4 of TIM module 5**
	GTM_TIM1_IN0_7			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_7			**Mux input channel 0 of TIM module 0**
	QSPI2_MRSTCN			**Master SPI data input (LVDS N line)**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	ASCLIN3_ARXGN			**Differential Receive input (low active)**
	HSCT0_RXDN			**Rx data**
	QSPI4_MRSTCN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXE			**Receive input**
	GTM_DTMA1_0			**CDTM1_DTM4**
	P21.2	O0		**General-purpose output**
	GTM_TOUT53	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**
P24	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_12			**Mux input channel 5 of TIM module 5**
	GTM_TIM1_IN1_6			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_6			**Mux input channel 1 of TIM module 0**
	QSPI2_MRSTCP			**Master SPI data input (LVDS P line)**
	ASCLIN3_ARXGP			**Differential Receive input (high active)**
	GETH_MDIOD			**MDIO Input**
	HSCT0_RXDP			**Rx data**
	QSPI4_MRSTCP			**Master SPI data input (LVDS P line)**
	P21.3	O0		**General-purpose output**
	GTM_TOUT54	O1		**GTM muxed output**
	ASCLIN11_ASCLK	O2		**Shift clock output**
	ASCLIN18_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R25	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN6_12			**Mux input channel 6 of TIM module 5**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	ASCLIN18_ARXB			**Receive input**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	ASCLIN18_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
P25	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN7_11			**Mux input channel 7 of TIM module 5**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N22	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM4_IN2_12			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N21	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM4_IN3_12			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	GETH_RXERB			Receive Error MII
	P21.7	O0		General-purpose output
	GTM_TOUT58	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	CBS_TGO3	O		Trigger output
	DAP2	I/O		DAP: DAP2 Data I/O
	TDO	O		JTAG Module Data Output

Table 2-12 Port 22 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
W25	P22.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR	O3		Master SPI data output
	QSPI4_SCLKN	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W24	P22.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN0_8			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_8			**Mux input channel 0 of TIM module 0**
	QSPI4_MRSTB			**Master SPI data input**
	ASCLIN7_ARXE			**Receive input**
	P22.1	O0		**General-purpose output**
	GTM_TOUT48	O1		**GTM muxed output**
	ASCLIN3_ATXP	O2		**Differential Transmit output (high active)**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI4_SCLKP	O4		**Master SPI clock output (LVDS P line)**
	MSC1_FCLP	O5		**Shift-clock direct part of the differential signal**
	—	O6		**Reserved**
	ASCLIN7_ATX	O7		**Transmit output**
Y25	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	QSPI4_SLSIB			**Slave select input**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI4_SLSO3	O3		**Master slave select output**
	QSPI4_MTSRN	O4		**Master SPI data output (LVDS N line)**
	MSC1_SON	O5		**Data output - inverted part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y24	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	QSPI4_SCLKB			**Slave SPI clock inputs**
	ASCLIN5_ARXC			**Receive input**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI4_SCLK	O3		**Master SPI clock output**
	QSPI4_MTSRP	O4		**Master SPI data output (LVDS P line)**
	MSC1_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
W21	P22.4	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_8			**Mux input channel 0 of TIM module 3**
	ASCLIN7_ARXF			**Receive input**
	GTM_DTMA3_0			**CDTM3_DTM4**
	P22.4	O0		**General-purpose output**
	GTM_TOUT130	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI0_SLSO12	O4		**Master slave select output**
	—	O5		**Reserved**
	CAN13_TXD	O6		**CAN transmit output node 3**
	—	O7		**Reserved**
W22	P22.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_7			**Mux input channel 1 of TIM module 3**
	QSPI0_MTSRC			**Slave SPI data input**
	CAN13_RXDC			**CAN receive input node 3**
	P22.5	O0		**General-purpose output**
	GTM_TOUT131	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
V21	P22.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_6			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_14			**Mux input channel 6 of TIM module 2**
	QSPI0_MRSTC			**Master SPI data input**
	ASCLIN4_ARXC			**Receive input**
	P22.6	O0		**General-purpose output**
	GTM_TOUT132	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	CAN21_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
V22	P22.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_7			**Mux input channel 3 of TIM module 3**
	QSPI0_SCLKC			**Slave SPI clock inputs**
	CAN21_RXDF			**CAN receive input node 1**
	P22.7	O0		**General-purpose output**
	GTM_TOUT133	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	ASCLIN17_ATX	O3		**Transmit output**
	QSPI0_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U21	P22.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN0_4			**Mux input channel 0 of TIM module 5**
	GTM_TIM3_IN4_7			**Mux input channel 4 of TIM module 3**
	QSPI0_SCLKB			**Slave SPI clock inputs**
	P22.8	O0		**General-purpose output**
	GTM_TOUT134	O1		**GTM muxed output**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI0_SCLK	O4		**Master SPI clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
U22	P22.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN1_10			**Mux input channel 1 of TIM module 5**
	GTM_TIM3_IN5_7			**Mux input channel 5 of TIM module 3**
	QSPI0_MRSTB			**Master SPI data input**
	ASCLIN4_ARXD			**Receive input**
	CAN22_RXDE			**CAN receive input node 2**
	GTM_DTMA3_1			**CDTM3_DTM4**
	P22.9	O0		**General-purpose output**
	GTM_TOUT135	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T21	P22.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN2_8			**Mux input channel 2 of TIM module 5**
	GTM_TIM3_IN6_7			**Mux input channel 6 of TIM module 3**
	QSPI0_MTSRB			**Slave SPI data input**
	P22.10	O0		**General-purpose output**
	GTM_TOUT136	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	CAN23_TXD	O5		**CAN transmit output node 3**
	—	O6		**Reserved**
	—	O7		**Reserved**
T22	P22.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_10			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN7_7			**Mux input channel 7 of TIM module 3**
	CAN23_RXDE			**CAN receive input node 3**
	ASCLIN17_ARXA			**Receive input**
	P22.11	O0		**General-purpose output**
	GTM_TOUT137	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	ASCLIN17_ATX	O3		**Transmit output**
	QSPI0_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-13 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AC25	P23.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_1			**Mux input channel 7 of TIM module 6**
	GTM_TIM1_IN5_4			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_4			**Mux input channel 5 of TIM module 0**
	CAN10_RXDC			**CAN receive input node 0**
	P23.0	O0		**General-purpose output**
	GTM_TOUT41	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AB24	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_1			**Mux input channel 6 of TIM module 6**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	MSC1_SDI0			**Upstream assynchronous input signal**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI4_SLSO6	O3		**Master slave select output**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**

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Table 2-13 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB25	P23.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_1			**Mux input channel 5 of TIM module 6**
	GTM_TIM1_IN6_5			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_5			**Mux input channel 6 of TIM module 0**
	ASCLIN7_ARXC			**Receive input**
	P23.2	O0		**General-purpose output**
	GTM_TOUT43	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CAN23_TXD	O4		**CAN transmit output node 3**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
AA24	P23.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_2			**Mux input channel 4 of TIM module 6**
	GTM_TIM1_IN7_4			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_4			**Mux input channel 7 of TIM module 0**
	MSC1_INJ0			**Injection signal from port**
	ASCLIN6_ARXA			**Receive input**
	CAN12_RXDC			**CAN receive input node 2**
	CAN23_RXDB			**CAN receive input node 3**
	P23.3	O0		**General-purpose output**
	GTM_TOUT44	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-13 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AA25	P23.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_2			**Mux input channel 3 of TIM module 6**
	GTM_TIM1_IN7_5			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_5			**Mux input channel 7 of TIM module 0**
	P23.4	O0		**General-purpose output**
	GTM_TOUT45	O1		**GTM muxed output**
	ASCLIN6_ASLSO	O2		**Slave select signal output**
	QSPI4_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**
AA22	P23.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_2			**Mux input channel 2 of TIM module 6**
	GTM_TIM1_IN2_7			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_7			**Mux input channel 2 of TIM module 0**
	ASCLIN16_ARXA			**Receive input**
	P23.5	O0		**General-purpose output**
	GTM_TOUT46	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	QSPI4_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN1	O5		**Chip Select**
	CAN22_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**
Y22	P23.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_2			**Mux input channel 1 of TIM module 6**
	GTM_TIM4_IN2_7			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_10			**Mux input channel 2 of TIM module 1**
	CAN22_RXDC			**CAN receive input node 2**
	P23.6	O0		**General-purpose output**
	GTM_TOUT138	O1		**GTM muxed output**
	ASCLIN16_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_SLSO11	O4		**Master slave select output**
	CAN11_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-13 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y21	P23.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_2			**Mux input channel 0 of TIM module 6**
	GTM_TIM4_IN3_7			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_10			**Mux input channel 3 of TIM module 1**
	CAN11_RXDC			**CAN receive input node 1**
	ASCLIN16_ARXB			**Receive input**
	P23.7	O0		**General-purpose output**
	GTM_TOUT139	O1		**GTM muxed output**
	ASCLIN16_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-14 Port 24 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U29	P24.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_6			**Mux input channel 0 of TIM module 6**
	GTM_TIM4_IN0_8			**Mux input channel 0 of TIM module 4**
	P24.0	O0		**General-purpose output**
	GTM_TOUT222	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-14 Port 24 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U30	P24.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_6			**Mux input channel 1 of TIM module 6**
	GTM_TIM4_IN1_8			**Mux input channel 1 of TIM module 4**
	P24.1	O0		**General-purpose output**
	GTM_TOUT223	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
T29	P24.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_6			**Mux input channel 2 of TIM module 6**
	GTM_TIM4_IN2_8			**Mux input channel 2 of TIM module 4**
	P24.2	O0		**General-purpose output**
	GTM_TOUT224	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
T30	P24.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_6			**Mux input channel 3 of TIM module 6**
	GTM_TIM4_IN3_8			**Mux input channel 3 of TIM module 4**
	P24.3	O0		**General-purpose output**
	GTM_TOUT225	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-14 Port 24 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R29	P24.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_5			**Mux input channel 4 of TIM module 6**
	GTM_TIM4_IN4_7			**Mux input channel 4 of TIM module 4**
	P24.4	O0		**General-purpose output**
	GTM_TOUT226	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
R30	P24.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_5			**Mux input channel 5 of TIM module 6**
	GTM_TIM4_IN5_7			**Mux input channel 5 of TIM module 4**
	P24.5	O0		**General-purpose output**
	GTM_TOUT227	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
P29	P24.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_5			**Mux input channel 6 of TIM module 6**
	GTM_TIM4_IN6_7			**Mux input channel 6 of TIM module 4**
	P24.6	O0		**General-purpose output**
	GTM_TOUT228	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-14 Port 24 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P30	P24.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_5			**Mux input channel 7 of TIM module 6**
	GTM_TIM4_IN7_7			**Mux input channel 7 of TIM module 4**
	P24.7	O0		**General-purpose output**
	GTM_TOUT229	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
N29	P24.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN0_5			**Mux input channel 0 of TIM module 5**
	P24.8	O0		**General-purpose output**
	GTM_TOUT230	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
N30	P24.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN1_6			**Mux input channel 1 of TIM module 5**
	P24.9	O0		**General-purpose output**
	GTM_TOUT231	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-14 Port 24 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M29	P24.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN2_5			**Mux input channel 2 of TIM module 5**
	P24.10	O0		**General-purpose output**
	GTM_TOUT232	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
M30	P24.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_6			**Mux input channel 3 of TIM module 5**
	P24.11	O0		**General-purpose output**
	GTM_TOUT233	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
L29	P24.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_6			**Mux input channel 4 of TIM module 5**
	P24.12	O0		**General-purpose output**
	GTM_TOUT234	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-14 Port 24 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L30	P24.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_6			**Mux input channel 5 of TIM module 5**
	P24.13	O0		**General-purpose output**
	GTM_TOUT235	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
K29	P24.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_6			**Mux input channel 6 of TIM module 5**
	P24.14	O0		**General-purpose output**
	GTM_TOUT236	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
K30	P24.15	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_5			**Mux input channel 7 of TIM module 5**
	P24.15	O0		**General-purpose output**
	GTM_TOUT237	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 25 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AG30	P25.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_7			**Mux input channel 0 of TIM module 6**
	GTM_TIM3_IN0_12			**Mux input channel 0 of TIM module 3**
	P25.0	O0		**General-purpose output**
	GTM_TOUT206	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AF30	P25.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_7			**Mux input channel 1 of TIM module 6**
	GTM_TIM3_IN1_11			**Mux input channel 1 of TIM module 3**
	P25.1	O0		**General-purpose output**
	GTM_TOUT207	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AF29	P25.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_7			**Mux input channel 2 of TIM module 6**
	GTM_TIM3_IN2_9			**Mux input channel 2 of TIM module 3**
	P25.2	O0		**General-purpose output**
	GTM_TOUT208	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 25 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE30	P25.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_7			**Mux input channel 3 of TIM module 6**
	GTM_TIM3_IN3_9			**Mux input channel 3 of TIM module 3**
	P25.3	O0		**General-purpose output**
	GTM_TOUT209	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AE29	P25.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_6			**Mux input channel 4 of TIM module 6**
	GTM_TIM3_IN4_10			**Mux input channel 4 of TIM module 3**
	P25.4	O0		**General-purpose output**
	GTM_TOUT210	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AD30	P25.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_6			**Mux input channel 5 of TIM module 6**
	GTM_TIM3_IN5_11			**Mux input channel 5 of TIM module 3**
	P25.5	O0		**General-purpose output**
	GTM_TOUT211	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 25 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W29	P25.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_6			**Mux input channel 6 of TIM module 6**
	GTM_TIM3_IN6_14			**Mux input channel 6 of TIM module 3**
	P25.6	O0		**General-purpose output**
	GTM_TOUT212	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AD29	P25.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_6			**Mux input channel 7 of TIM module 6**
	GTM_TIM3_IN7_10			**Mux input channel 7 of TIM module 3**
	P25.7	O0		**General-purpose output**
	GTM_TOUT213	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AC29	P25.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_9			**Mux input channel 0 of TIM module 4**
	P25.8	O0		**General-purpose output**
	GTM_TOUT214	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 25 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AC30	P25.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN1_9			**Mux input channel 1 of TIM module 4**
	P25.9	O0		**General-purpose output**
	GTM_TOUT215	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AB29	P25.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_9			**Mux input channel 2 of TIM module 4**
	P25.10	O0		**General-purpose output**
	GTM_TOUT216	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AB30	P25.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_9			**Mux input channel 3 of TIM module 4**
	P25.11	O0		**General-purpose output**
	GTM_TOUT217	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 25 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AA29	P25.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_8			**Mux input channel 4 of TIM module 4**
	P25.12	O0		**General-purpose output**
	GTM_TOUT218	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AA30	P25.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_8			**Mux input channel 5 of TIM module 4**
	P25.13	O0		**General-purpose output**
	GTM_TOUT219	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
Y29	P25.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_8			**Mux input channel 6 of TIM module 4**
	P25.14	O0		**General-purpose output**
	GTM_TOUT220	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 25 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y30	P25.15	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_8			**Mux input channel 7 of TIM module 4**
	P25.15	O0		**General-purpose output**
	GTM_TOUT221	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-16 Port 26 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AG29	P26.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_9			**Mux input channel 6 of TIM module 6**
	GTM_TIM3_IN6_11			**Mux input channel 6 of TIM module 3**
	P26.0	O0		**General-purpose output**
	GTM_TOUT212	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-17 Port 30 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ21	P30.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_10			**Mux input channel 0 of TIM module 4**
	P30.0	O0		**General-purpose output**
	GTM_TOUT190	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK21	P30.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN1_10			**Mux input channel 1 of TIM module 4**
	P30.1	O0		**General-purpose output**
	GTM_TOUT191	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ22	P30.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_10			**Mux input channel 2 of TIM module 4**
	P30.2	O0		**General-purpose output**
	GTM_TOUT192	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-17 Port 30 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK22	P30.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_10			**Mux input channel 3 of TIM module 4**
	P30.3	O0		**General-purpose output**
	GTM_TOUT193	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ23	P30.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_9			**Mux input channel 4 of TIM module 4**
	P30.4	O0		**General-purpose output**
	GTM_TOUT194	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK23	P30.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_9			**Mux input channel 5 of TIM module 4**
	P30.5	O0		**General-purpose output**
	GTM_TOUT195	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-17 Port 30 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ24	P30.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_9			**Mux input channel 6 of TIM module 4**
	P30.6	O0		**General-purpose output**
	GTM_TOUT196	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK24	P30.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_9			**Mux input channel 7 of TIM module 4**
	P30.7	O0		**General-purpose output**
	GTM_TOUT197	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ25	P30.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_8			**Mux input channel 0 of TIM module 6**
	GTM_TIM5_IN0_6			**Mux input channel 0 of TIM module 5**
	P30.8	O0		**General-purpose output**
	GTM_TOUT198	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-17 Port 30 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK25	P30.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_8			**Mux input channel 1 of TIM module 6**
	GTM_TIM5_IN1_7			**Mux input channel 1 of TIM module 5**
	P30.9	O0		**General-purpose output**
	GTM_TOUT199	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ26	P30.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_8			**Mux input channel 2 of TIM module 6**
	GTM_TIM5_IN2_6			**Mux input channel 2 of TIM module 5**
	P30.10	O0		**General-purpose output**
	GTM_TOUT200	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK26	P30.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_8			**Mux input channel 3 of TIM module 6**
	GTM_TIM5_IN3_7			**Mux input channel 3 of TIM module 5**
	P30.11	O0		**General-purpose output**
	GTM_TOUT201	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-17 Port 30 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ27	P30.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_7			**Mux input channel 4 of TIM module 6**
	GTM_TIM5_IN4_7			**Mux input channel 4 of TIM module 5**
	P30.12	O0		**General-purpose output**
	GTM_TOUT202	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK27	P30.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_7			**Mux input channel 5 of TIM module 6**
	GTM_TIM5_IN5_7			**Mux input channel 5 of TIM module 5**
	P30.13	O0		**General-purpose output**
	GTM_TOUT203	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ28	P30.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_7			**Mux input channel 6 of TIM module 6**
	GTM_TIM5_IN6_7			**Mux input channel 6 of TIM module 5**
	P30.14	O0		**General-purpose output**
	GTM_TOUT204	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-17 Port 30 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK28	P30.15	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_7			**Mux input channel 7 of TIM module 6**
	GTM_TIM5_IN7_6			**Mux input channel 7 of TIM module 5**
	P30.15	O0		**General-purpose output**
	GTM_TOUT205	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-18 Port 31 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ12	P31.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_13			**Mux input channel 0 of TIM module 2**
	P31.0	O0		**General-purpose output**
	GTM_TOUT174	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK12	P31.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_9			**Mux input channel 1 of TIM module 2**
	P31.1	O0		**General-purpose output**
	GTM_TOUT175	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-18 Port 31 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ13	P31.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_9			**Mux input channel 2 of TIM module 2**
	P31.2	O0		**General-purpose output**
	GTM_TOUT176	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK13	P31.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN3_14			**Mux input channel 3 of TIM module 2**
	P31.3	O0		**General-purpose output**
	GTM_TOUT177	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ14	P31.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN4_12			**Mux input channel 4 of TIM module 2**
	P31.4	O0		**General-purpose output**
	GTM_TOUT178	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-18 Port 31 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK14	P31.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN5_13			**Mux input channel 5 of TIM module 2**
	P31.5	O0		**General-purpose output**
	GTM_TOUT179	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ15	P31.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_12			**Mux input channel 6 of TIM module 2**
	P31.6	O0		**General-purpose output**
	GTM_TOUT180	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK15	P31.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_14			**Mux input channel 7 of TIM module 2**
	P31.7	O0		**General-purpose output**
	GTM_TOUT181	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-18 Port 31 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ16	P31.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_9			**Mux input channel 0 of TIM module 6**
	GTM_TIM5_IN0_7			**Mux input channel 0 of TIM module 5**
	SENT_SENT20C			**Receive input channel 20**
	P31.8	O0		**General-purpose output**
	GTM_TOUT182	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK16	P31.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_9			**Mux input channel 1 of TIM module 6**
	GTM_TIM5_IN1_8			**Mux input channel 1 of TIM module 5**
	SENT_SENT21C			**Receive input channel 21**
	P31.9	O0		**General-purpose output**
	GTM_TOUT183	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ17	P31.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_9			**Mux input channel 2 of TIM module 6**
	GTM_TIM5_IN2_7			**Mux input channel 2 of TIM module 5**
	SENT_SENT22C			**Receive input channel 22**
	P31.10	O0		**General-purpose output**
	GTM_TOUT184	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-18 Port 31 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK17	P31.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_9			**Mux input channel 3 of TIM module 6**
	GTM_TIM5_IN3_8			**Mux input channel 3 of TIM module 5**
	SENT_SENT23C			**Receive input channel 23**
	P31.11	O0		**General-purpose output**
	GTM_TOUT185	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AJ18	P31.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_8			**Mux input channel 4 of TIM module 6**
	GTM_TIM5_IN4_8			**Mux input channel 4 of TIM module 5**
	SENT_SENT24C			**Receive input channel 24**
	P31.12	O0		**General-purpose output**
	GTM_TOUT186	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK18	P31.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_8			**Mux input channel 5 of TIM module 6**
	GTM_TIM5_IN5_8			**Mux input channel 5 of TIM module 5**
	P31.13	O0		**General-purpose output**
	GTM_TOUT187	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-18 Port 31 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ19	P31.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_8			**Mux input channel 6 of TIM module 6**
	GTM_TIM5_IN6_8			**Mux input channel 6 of TIM module 5**
	P31.14	O0		**General-purpose output**
	GTM_TOUT188	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AK19	P31.15	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_8			**Mux input channel 7 of TIM module 6**
	GTM_TIM5_IN7_7			**Mux input channel 7 of TIM module 5**
	P31.15	O0		**General-purpose output**
	GTM_TOUT189	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-19 Port 32 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AE22	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
AD22	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			**Mux input channel 3 of TIM module 3**
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-19 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE23	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_8			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_8			**Mux input channel 3 of TIM module 0**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	CAN21_RXDD			**CAN receive input node 1**
	P32.2	O0		**General-purpose output**
	GTM_TOUT38	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**
AE24	P32.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_5			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_5			**Mux input channel 4 of TIM module 0**
	P32.3	O0		**General-purpose output**
	GTM_TOUT39	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN3_ASCLK	O4		**Shift clock output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**

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Table 2-19 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD23	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	MSC1_SDI2			**Upstream assynchronous input signal**
	ASCLIN15_ARXA			**Receive input**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	PMS_DCDCSYNCO	O2		**DC-DC synchronization output**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	MSC1_EN0	O5		**Chip Select**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
AA20	P32.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_9			**Mux input channel 5 of TIM module 5**
	GTM_TIM4_IN1_14			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_8			**Mux input channel 5 of TIM module 3**
	SENT_SENT10C			**Receive input channel 10**
	P32.5	O0		**General-purpose output**
	GTM_TOUT140	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**

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Table 2-19 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB20	P32.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_9			**Mux input channel 6 of TIM module 5**
	GTM_TIM4_IN4_15			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN6_8			**Mux input channel 6 of TIM module 3**
	CAN02_RXDC			**CAN receive input node 2**
	CBS_TGI4			**Trigger input**
	ASCLIN2_ARXF			**Receive input**
	ASCLIN6_ARXC			**Receive input**
	SENT_SENT11C			**Receive input channel 11**
	P32.6	O0		**General-purpose output**
	GTM_TOUT141	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI2_SLSO12	O4		**Master slave select output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO4	O		**Trigger output**
AB21	P32.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_8			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN0_15			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN7_8			**Mux input channel 7 of TIM module 3**
	CBS_TGI5			**Trigger input**
	CAN22_RXDB			**CAN receive input node 2**
	SENT_SENT12C			**Receive input channel 12**
	ASCLIN15_ARXB			**Receive input**
	P32.7	O0		**General-purpose output**
	GTM_TOUT142	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	ASCLIN15_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO5	O		**Trigger output**

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Table 2-20 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AD15	P33.0	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_13			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN4_6			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_6			**Mux input channel 4 of TIM module 0**
	EDSADC_ITR0E			**Trigger/Gate input, channel 0**
	SENT_SENT13C			**Receive input channel 13**
	IOM_PIN_0			**GPIO pad input to FPC**
	GTM_DTMT1_2			**CDTM1_DTM0**
	EVADC_G10CH7	AI		**Analog input channel 7, group 10**
	P33.0	O0		**General-purpose output**
	GTM_TOUT22	O1		**GTM muxed output**
	IOM_MON0_0			**Monitor input 0**
	IOM_GTM_0			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	ASCLIN15_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	—	O7		**Reserved**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE15	P33.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_15			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN5_6			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_6			**Mux input channel 5 of TIM module 0**
	EDSADC_ITR1E			**Trigger/Gate input, channel 1**
	PSI5_RX0C			**RXD inputs (receive data) channel 0**
	EDSADC_DSCIN2B			**Modulator clock input, channel 2**
	SENT_SENT9C			**Receive input channel 9**
	ASCLIN8_ARXC			**Receive input**
	IOM_PIN_1			**GPIO pad input to FPC**
	EVADC_G10CH6	AI		**Analog input channel 6, group 10**
	P33.1	O0		**General-purpose output**
	GTM_TOUT23	O1		**GTM muxed output**
	IOM_MON0_1			**Monitor input 0**
	IOM_GTM_1			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	QSPI2_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD16	P33.2	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN2_14			**Mux input channel 2 of TIM module 3**
	GTM_TIM1_IN6_6			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_6			**Mux input channel 6 of TIM module 0**
	EDSADC_ITR2E			**Trigger/Gate input, channel 2**
	SENT_SENT8C			**Receive input channel 8**
	EDSADC_DSDIN2B			**Digital datastream input, channel 2**
	IOM_PIN_2			**GPIO pad input to FPC**
	EVADC_G10CH5	AI		**Analog input channel 5, group 10**
	P33.2	O0		**General-purpose output**
	GTM_TOUT24	O1		**GTM muxed output**
	IOM_MON0_2			**Monitor input 0**
	IOM_GTM_2			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	QSPI2_SLSO10	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	ASCLIN14_ATX	O7		**Transmit output**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE16	P33.3	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN3_12			**Mux input channel 3 of TIM module 3**
	GTM_TIM1_IN7_6			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_6			**Mux input channel 7 of TIM module 0**
	PSI5_RX1C			**RXD inputs (receive data) channel 1**
	SENT_SENT7C			**Receive input channel 7**
	EDSADC_DSCIN1B			**Modulator clock input, channel 1**
	ASCLIN14_ARXA			**Receive input**
	IOM_PIN_3			**GPIO pad input to FPC**
	EVADC_G10CH4	AI		**Analog input channel 4, group 10**
	P33.3	O0		**General-purpose output**
	GTM_TOUT25	O1		**GTM muxed output**
	IOM_MON0_3			**Monitor input 0**
	IOM_GTM_3			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO2	O3		**Master slave select output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	ASCLIN14_ATX	O7		**Transmit output**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD17	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_10			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_10			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_10			**Mux input channel 0 of TIM module 0**
	EDSADC_ITR0F			**Trigger/Gate input, channel 0**
	SENT_SENT6C			**Receive input channel 6**
	EDSADC_DSDIN1B			**Digital datastream input, channel 1**
	CCU61_CTRAPC			**Trap input capture**
	ASCLIN5_ARXB			**Receive input**
	ASCLIN14_ARXB			**Receive input**
	IOM_PIN_4			**GPIO pad input to FPC**
	GTM_DTMT2_0			**CDTM2_DTM0**
	EVADC_G10CH3	AI		**Analog input channel 3, group 10**
	P33.4	O0		**General-purpose output**
	GTM_TOUT26	O1		**GTM muxed output**
	IOM_MON0_4			**Monitor input 0**
	IOM_GTM_4			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC0BFLOUT	O6		**Boundary flag output, FC channel 0**
	CAN13_TXD	O7		**CAN transmit output node 3**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE17	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN5_10			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN1_8			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_8			**Mux input channel 1 of TIM module 0**
	EDSADC_DSCIN0B			**Modulator clock input, channel 0**
	EDSADC_ITR1F			**Trigger/Gate input, channel 1**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	PSI5S_RXC			**RX data input**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	PSI5_RX2C			**RXD inputs (receive data) channel 2**
	SENT_SENT5C			**Receive input channel 5**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	EVADC_G10CH2	AI		**Analog input channel 2, group 10**
	P33.5	O0		**General-purpose output**
	GTM_TOUT27	O1		**GTM muxed output**
	IOM_MON0_5			**Monitor input 0**
	IOM_GTM_5			**GTM-provided inputs to EXOR combiner**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	ASCLIN5_ASLSO	O7		**Slave select signal output**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD18	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_9			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_9			**Mux input channel 2 of TIM module 0**
	EDSADC_ITR2F			**Trigger/Gate input, channel 2**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	SENT_SENT4C			**Receive input channel 4**
	CCU61_CCPOS1C			**Hall capture input 1**
	EDSADC_DSDIN0B			**Digital datastream input, channel 0**
	ASCLIN8_ARXD			**Receive input**
	IOM_PIN_6			**GPIO pad input to FPC**
	GTM_DTMT2_1			**CDTM2_DTM0**
	EVADC_G10CH1	AI		**Analog input channel 1, group 10**
	P33.6	O0		**General-purpose output**
	GTM_TOUT28	O1		**GTM muxed output**
	IOM_MON0_6			**Monitor input 0**
	IOM_GTM_6			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	PSI5_TX2	O4		**TXD outputs (send data)**
	IOM_REF1_15			**Reference input 1**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC1BFLOUT	O6		**Boundary flag output, FC channel 1**
	PSI5S_TX	O7		**TX data output**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE18	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN3_9			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_9			**Mux input channel 3 of TIM module 0**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT14C			**Receive input channel 14**
	IOM_PIN_7			**GPIO pad input to FPC**
	EVADC_G10CH0	AI		**Analog input channel 0, group 10**
	P33.7	O0		**General-purpose output**
	GTM_TOUT29	O1		**GTM muxed output**
	IOM_MON0_7			**Monitor input 0**
	IOM_GTM_7			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO7	O3		**Master slave select output**
	ASCLIN8_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD19	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO2	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE19	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO1	O3		**Master slave select output**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD20	P33.10	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_14			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_9			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_9			**Mux input channel 0 of TIM module 0**
	QSPI4_SLSIA			**Slave select input**
	CAN01_RXDD			**CAN receive input node 1**
	ASCLIN0_ARXD			**Receive input**
	IOM_PIN_10			**GPIO pad input to FPC**
	P33.10	O0		**General-purpose output**
	GTM_TOUT32	O1		**GTM muxed output**
	IOM_MON0_10			**Monitor input 0**
	QSPI1_SLSO6	O2		**Master slave select output**
	QSPI4_SLSO0	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	PSI5S_CLK	O5		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SMU_FSP1	O		**FSP[1..0] Output Signals - Generated by SMU_core**
AE20	P33.11	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_8			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_8			**Mux input channel 2 of TIM module 0**
	QSPI4_SCLKA			**Slave SPI clock inputs**
	IOM_PIN_11			**GPIO pad input to FPC**
	P33.11	O0		**General-purpose output**
	GTM_TOUT33	O1		**GTM muxed output**
	IOM_MON0_11			**Monitor input 0**
	ASCLIN1_ASCLK	O2		**Shift clock output**
	QSPI4_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EDSADC_CGPWMN	O6		**Negative carrier generator output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD21	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_6			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_6			**Mux input channel 0 of TIM module 2**
	QSPI4_MTSRA			**Slave SPI data input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	GTM_TOUT34	O1		**GTM muxed output**
	IOM_MON0_12			**Monitor input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MTSR	O3		**Master SPI data output**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	EDSADC_CGPWMP	O6		**Positive carrier generator output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE21	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_5			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_5			**Mux input channel 1 of TIM module 2**
	ASCLIN1_ARXF			**Receive input**
	EDSADC_SGNB			**Carrier sign signal input**
	QSPI4_MRSTA			**Master SPI data input**
	MSC1_INJ1			**Injection signal from port**
	CAN22_RXDA			**CAN receive input node 2**
	P33.13	O0		**General-purpose output**
	GTM_TOUT35	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-20 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AA19	P33.14	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN0_8			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN5_14			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_8			**Mux input channel 0 of TIM module 2**
	QSPI2_SCLKD			**Slave SPI clock inputs**
	CBS_TGI6			**Trigger input**
	P33.14	O0		**General-purpose output**
	GTM_TOUT143	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**
	CBS_TGO6	O		**Trigger output**
AB19	P33.15	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN1_9			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN6_12			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_7			**Mux input channel 1 of TIM module 2**
	CBS_TGI7			**Trigger input**
	P33.15	O0		**General-purpose output**
	GTM_TOUT144	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
	CBS_TGO7	O		**Trigger output**

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Table 2-21 Port 34 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
AB16	P34.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN3_9			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN4_12			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN3_9			**Mux input channel 3 of TIM module 2**
	EVADC_G10CH11	AI		**Analog input channel 11, group 10**
	P34.1	O0		**General-purpose output**
	GTM_TOUT146	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	CAN00_TXD	O4		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
AA17	P34.2	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN4_9			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN5_13			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN4_8			**Mux input channel 4 of TIM module 2**
	ASCLIN4_ARXB			**Receive input**
	CAN00_RXDG			**CAN receive input node 0**
	CAN20_RXDC			**CAN receive input node 0**
	EVADC_G10CH10	AI		**Analog input channel 10, group 10**
	P34.2	O0		**General-purpose output**
	GTM_TOUT147	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-21 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB17	P34.3	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN5_10			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN6_13			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN5_9			**Mux input channel 5 of TIM module 2**
	EVADC_G10CH9	AI		**Analog input channel 9, group 10**
	P34.3	O0		**General-purpose output**
	GTM_TOUT148	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI2_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
AA18	P34.4	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN6_10			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN7_12			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN6_8			**Mux input channel 6 of TIM module 2**
	QSPI2_MRSTD			**Master SPI data input**
	EVADC_G10CH8	AI		**Analog input channel 8, group 10**
	P34.4	O0		**General-purpose output**
	GTM_TOUT149	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI2_MRST	O4		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-21 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB18	P34.5	I	FAST / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN7_9			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN7_12			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_9			**Mux input channel 7 of TIM module 2**
	QSPI2_MTSRD			**Slave SPI data input**
	ASCLIN8_ARXE			**Receive input**
	P34.5	O0		**General-purpose output**
	GTM_TOUT150	O1		**GTM muxed output**
	ASCLIN8_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI2_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

Table 2-22 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
AA15	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
AB15	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
AD14	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
AB14	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
AA14	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G11CH0			**Analog input channel 0, group 11**
	EVADC_G0CH4			**Analog input channel 4, group 0**
AE14	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G11CH1			**Analog input channel 1, group 11**
	EVADC_G0CH5			**Analog input channel 5, group 0**

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Table 2-22 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AA13	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G11CH2			**Analog input channel 2, group 11**
	EVADC_G0CH6			**Analog input channel 6, group 0**
AB13	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G11CH3			**Analog input channel 3, group 11**
	EVADC_G0CH7			**Analog input channel 7, group 0**
AD13	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G11CH4			**Analog input channel 4, group 11**
	EVADC_G1CH0			**Analog input channel 0, group 1**
AB12	AN9	I	D / HighZ / VDDM	**Analog Input 9**
	EVADC_G11CH5			**Analog input channel 5, group 11**
	EVADC_G1CH1			**Analog input channel 1, group 1**
AE13	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G11CH6			**Analog input channel 6, group 11**
	EVADC_G1CH2			**Analog input channel 2, group 1**
AD12	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G11CH7			**Analog input channel 7, group 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
AA12	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
AD11	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
AB11	AN14	I	D / HighZ / VDDM	**Analog Input 14**
	EVADC_G1CH6			**Analog input channel 6, group 1**
	EDSADC_EDS3PB			**Positive analog input channel 3, pin B**
AA11	AN15	I	D / HighZ / VDDM	**Analog Input 15**
	EVADC_G1CH7			**Analog input channel 7, group 1**
	EDSADC_EDS3NB			**Negative analog input channel 3, pin N**
AD10	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
AB10	AN17/P40.10	I	S / HighZ / VDDM	**Analog Input 17**
	SENT_SENT10A			**Receive input channel 10**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**

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Table 2-22 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD9	AN18/P40.11	I	S / HighZ / VDDM	**Analog Input 18**
	SENT_SENT11A			**Receive input channel 11**
	EVADC_G11CH8			**Analog input channel 8, group 11**
	EVADC_G2CH2			**Analog input channel 2, group 2**
AD8	AN19/P40.12	I	S / HighZ / VDDM	**Analog Input 19**
	SENT_SENT12A			**Receive input channel 12**
	EVADC_G11CH9			**Analog input channel 9, group 11**
	EVADC_G2CH3			**Analog input channel 3, group 2**
AE8	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
AE7	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
AA10	AN22	I	D / HighZ / VDDM	**Analog Input 22**
	EVADC_G2CH6			**Analog input channel 6, group 2**
Y10	AN23	I	D / HighZ / VDDM	**Analog Input 23**
	EVADC_G2CH7			**Analog input channel 7, group 2**
AD7	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
AD6	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
AC7	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**
	EVADC_G11CH10			**Analog input channel 10, group 11**
AC6	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
	EVADC_G11CH11			**Analog input channel 11, group 11**

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Table 2-22 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB7	AN28/P40.13	I	S / HighZ / VDDM	**Analog Input 28**
	SENT_SENT13A			**Receive input channel 13**
	EVADC_G3CH4			**Analog input channel 4, group 3**
	EVADC_G4CH4			**Analog input channel 4, group 4**
AB6	AN29/P40.14	I	S / HighZ / VDDM	**Analog Input 29**
	SENT_SENT14A			**Receive input channel 14**
	EVADC_G3CH5			**Analog input channel 5, group 3**
	EVADC_G4CH5			**Analog input channel 5, group 4**
AA9	AN30	I	D / HighZ / VDDM	**Analog Input 30**
	EVADC_G3CH6			**Analog input channel 6, group 3**
	EVADC_G4CH6			**Analog input channel 6, group 4**
Y9	AN31	I	D / HighZ / VDDM	**Analog Input 31**
	EVADC_G3CH7			**Analog input channel 7, group 3**
	EVADC_G4CH7			**Analog input channel 7, group 4**
W9	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
	EVADC_G11CH12			**Analog input channel 12, group 11**
Y6	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
	EVADC_G11CH13			**Analog input channel 13, group 11**
W10	AN34	I	D / HighZ / VDDM	**Analog Input 34**
	EVADC_G8CH2			**Analog input channel 2, group 8**
	EVADC_G11CH14			**Analog input channel 14, group 11**
Y7	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
	EVADC_G11CH15			**Analog input channel 15, group 11**
V9	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**

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Table 2-22 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W7	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
V10	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
W6	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
U10	AN40	I	D / HighZ / VDDM	**Analog Input 40**
	EVADC_G8CH8			**Analog input channel 8, group 8**
	EVADC_G4CH0			**Analog input channel 0, group 4**
U9	AN41	I	D / HighZ / VDDM	**Analog Input 41**
	EVADC_G8CH9			**Analog input channel 9, group 8**
	EVADC_G4CH1			**Analog input channel 1, group 4**
T10	AN42	I	D / HighZ / VDDM	**Analog Input 42**
	EVADC_G8CH10			**Analog input channel 10, group 8**
	EVADC_G4CH2			**Analog input channel 2, group 4**
T9	AN43	I	D / HighZ / VDDM	**Analog Input 43**
	EVADC_G8CH11			**Analog input channel 11, group 8**
	EVADC_G4CH3			**Analog input channel 3, group 4**
V6	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
V7	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
U6	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**

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Table 2-22 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U7	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**
AK7	AN48	I	D / HighZ / VDDM	**Analog Input 48**
	EVADC_G5CH0			**Analog input channel 0, group 5**
AJ7	AN49	I	D / HighZ / VDDM	**Analog Input 49**
	EVADC_G5CH1			**Analog input channel 1, group 5**
AJ6	AN50	I	D / HighZ / VDDM	**Analog Input 50**
	EVADC_G5CH2			**Analog input channel 2, group 5**
	EDSADC_EDS9PA			**Positive analog input channel 9, pin A**
AK6	AN51	I	D / HighZ / VDDM	**Analog Input 51**
	EVADC_G5CH3			**Analog input channel 3, group 5**
	EDSADC_EDS9NA			**Negative analog input channel 9, pin A**
AJ5	AN52	I	D / HighZ / VDDM	**Analog Input 52**
	EVADC_G5CH4			**Analog input channel 4, group 5**
	EDSADC_EDS6PA			**Positive analog input channel 6, pin A**
AK5	AN53	I	D / HighZ / VDDM	**Analog Input 53**
	EVADC_G5CH5			**Analog input channel 5, group 5**
	EDSADC_EDS6NA			**Negative analog input channel 6, pin A**
AJ4	AN54/P41.4	I	S / HighZ / VDDM	**Analog Input 54**
	SENT_SENT20A			**Receive input channel 20**
	EVADC_G5CH6			**Analog input channel 6, group 5**
	EDSADC_EDS6PB			**Positive analog input channel 6, pin B**
AK4	AN55/P41.5	I	S / HighZ / VDDM	**Analog Input 55**
	SENT_SENT21A			**Receive input channel 21**
	EVADC_G5CH7			**Analog input channel 7, group 5**
	EDSADC_EDS6NB			**Negative analog input channel 6, pin B**
AF1	AN56	I	D / HighZ / VDDM	**Analog Input 56**
	EVADC_G6CH0			**Analog input channel 0, group 6**
AF2	AN57	I	D / HighZ / VDDM	**Analog Input 57**
	EVADC_G6CH1			**Analog input channel 1, group 6**
AE2	AN58	I	D / HighZ / VDDM	**Analog Input 58**
	EVADC_G6CH2			**Analog input channel 2, group 6**
AE1	AN59	I	D / HighZ / VDDM	**Analog Input 59**
	EVADC_G6CH3			**Analog input channel 3, group 6**
AD1	AN60	I	D / HighZ / VDDM	**Analog Input 60**
	EVADC_G6CH4			**Analog input channel 4, group 6**
	EDSADC_EDS7PA			**Positive analog input channel 7, pin A**

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Table 2-22 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD2	AN61	I	D / HighZ / VDDM	**Analog Input 61**
	EVADC_G6CH5			**Analog input channel 5, group 6**
	EDSADC_EDS7NA			**Negative analog input channel 7, pin A**
AC2	AN62/P41.6	I	S / HighZ / VDDM	**Analog Input 62**
	SENT_SENT22A			**Receive input channel 22**
	EVADC_G6CH6			**Analog input channel 6, group 6**
	EDSADC_EDS7PB			**Positive analog input channel 7, pin B**
AC1	AN63/P41.7	I	S / HighZ / VDDM	**Analog Input 63**
	SENT_SENT23A			**Receive input channel 23**
	EVADC_G6CH7			**Analog input channel 7, group 6**
	EDSADC_EDS7NB			**Negative analog input channel 7, pin B**
AB2	AN64/P41.8	I	S / HighZ / VDDM	**Analog Input 64**
	SENT_SENT24A			**Receive input channel 24**
	EVADC_G7CH0			**Analog input channel 0, group 7**
AB1	AN65	I	D / HighZ / VDDM	**Analog Input 65**
	EVADC_G7CH1			**Analog input channel 1, group 7**
AA2	AN66	I	D / HighZ / VDDM	**Analog Input 66**
	EVADC_G7CH2			**Analog input channel 2, group 7**
AA1	AN67/P40.15	I	S / HighZ / VDDM	**Analog Input 67**
	SENT_SENT15A			**Receive input channel 15**
	EVADC_G7CH3			**Analog input channel 3, group 7**
Y1	AN68/P41.0	I	S / HighZ / VDDM	**Analog Input 68**
	SENT_SENT16A			**Receive input channel 16**
	EVADC_G7CH4			**Analog input channel 4, group 7**
	EDSADC_EDS8PA			**Positive analog input channel 8, pin A**
Y2	AN69/P41.1	I	S / HighZ / VDDM	**Analog Input 69**
	SENT_SENT17A			**Receive input channel 17**
	EVADC_G7CH5			**Analog input channel 5, group 7**
	EDSADC_EDS8NA			**Negative analog input channel 8, pin A**
W1	AN70/P41.2	I	S / HighZ / VDDM	**Analog Input 70**
	SENT_SENT18A			**Receive input channel 18**
	EVADC_G7CH6			**Analog input channel 6, group 7**
	EDSADC_EDS9PB			**Positive analog input channel 9, pin B**
W2	AN71/P41.3	I	S / HighZ / VDDM	**Analog Input 71**
	SENT_SENT19A			**Receive input channel 19**
	EVADC_G7CH7			**Analog input channel 7, group 7**
	EDSADC_EDS9NB			**Negative analog input channel 9, pin B**

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Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

1. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
2. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-23 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
M21	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
L21	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**
AD22	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
AE22	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
U25	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
U24	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
T24	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
P21	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**

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Table 2-23 System I/O (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R21	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**
M22	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.

Table 2-24 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
N19, V19, M18, W18, W13, V12, J21, K20, N12, M13	VDD	I	—	**Digital Core Power Supply (1.25V)**
AJ30, AH29, AD25, AC24, G8, F7, B3, A2, J29, J30, AH30, AK29, AK20, AJ11, AK11	VEXT	I	—	**External Power Supply (5V / 3.3V)**
J10	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
AE10, AJ9, AK9	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
A29, B28, F24, G23	VDDP3	I	—	**Flash Power Supply (3.3V)**
AK30, AJ29, AE25, AD24, AB22, AA21, K10, J9, G7, B2, A30, B30, B29, F25, G24, J22, K21, H30, H29, AJ10, AK10	VSS	I	—	**Digital Ground**
AE9, AJ8, AK8	VSSM	I	—	**Analog Ground for VDDM**

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Table 2-24 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P19, U19, P18, R18, T18, U18, M15, M16, M17, N17, R17, T17, V17, W17, N16, P16, R16, T16, U16, V16, N15, P15, R15, T15, U15, V15, M14, N14, R14, T14, V14, W14, P13, R13, T13, U13, P12, U12, T19, W15, W16, R12, T12	VSS	I	—	**Digital Ground**
T25	VSS	I	—	**Oscillator Ground, VSS(OSC)**
AE11	VAREF1	I	—	**Positive Analog Reference Voltage 1**
AE12	VAGND1	I	—	**Negative Analog Reference Voltage 1**
AA6	VAREF2	I	—	**Positive Analog Reference Voltage 2**
AA7	VAGND2	I	—	**Negative Analog Reference Voltage 2**

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Table 2-24 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C30, D30, E30, F30, G30, W30, C29, D29, E29, F29, G29, A28, A27, B27, A26, B26, A25, A21, AJ20, B21, B20, A17, B17, A10, B10, A9, B9, A8, A4, B4, A3, AJ3, AK3, C2, D2, E2, H2, R2, AH2, AJ2, AK2, B1, C1, D1, E1, H1, J1, R1, T1, AH1, AJ1, B6, B14, B25, V1, V2, R19	NC	I	—	**Not connected. These pins are reserved for future extensions and shall not be connected externally**
AB9, F6, AE6, A1, AK1, V30, V29	NC1	I	—	**Not connected. These pins are not connected on package level and will not be used for future extensions**
AA16	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
V24	VDD	I	—	**Digital Power Supply for Oscillator (1.25V), VDD(OSC)**
V25	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**
AG1	VAREF3	I	—	**Positive Analog Reference Voltage 3**
AG2	VAGND3	I	—	**Negative Analog Reference Voltage 3**

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2.2 BGA292 Package Variant Pin Configuration

Table 2-25 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_10			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN0_1			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_11			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN1_1			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	EDSADC_DSCIN5A			**Modulator clock input, channel 5**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EDSADC_DSCIN7B			**Modulator clock input, channel 7**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	EDSADC_EDS5NA			**Negative analog input channel 5, pin A**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	EDSADC_DSCOUT7	O5		**Modulator clock output**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H1	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN6_11			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN1_2			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	EDSADC_DSDIN7B			**Digital datastream input, channel 7**
	EDSADC_DSDIN5A			**Digital datastream input, channel 5**
	SENT_SENT1B			**Receive input channel 1**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	EDSADC_EDS5PA			**Positive analog input channel 5, pin A**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	CAN21_TXD	O3		**CAN transmit output node 1**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN7_10			**Mux input channel 7 of TIM module 5**
	GTM_TIM3_IN2_1			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	EDSADC_ITR5F			**Trigger/Gate input, channel 5**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	CAN21_RXDA			**CAN receive input node 1**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CCU61_CC61INA			**T12 capture input 61**
	ASCLIN12_ARXA			**Receive input**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	EDSADC_EDS5NB			**Negative analog input channel 5, pin B**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	ASCLIN12_ATX	O3		**Transmit output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM6_IN4_1			**Mux input channel 4 of TIM module 6**
	GTM_TIM3_IN3_1			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	GTM_DTMA5_0			**CDTM5_DTM4**
	GTM_DTMT3_0			**CDTM3_DTM0**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	EDSADC_EDS5PB			**Positive analog input channel 5, pin B**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P00.5	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN4_1			**Mux input channel 4 of TIM module 3**
	GTM_TIM3_IN0_11			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN4_1			**Mux input channel 4 of TIM module 2**
	CCU60_CC62INB			**T12 capture input 62**
	EDSADC_DSCIN2A			**Modulator clock input, channel 2**
	PSI5_RX2A			**RXD inputs (receive data) channel 2**
	CCU61_CC62INA			**T12 capture input 62**
	SENT_SENT4B			**Receive input channel 4**
	CAN11_RXDB			**CAN receive input node 1**
	ASCLIN12_ARXB			**Receive input**
	GTM_DTMT1_1			**CDTM1_DTM0**
	EVADC_G9CH7	AI		**Analog input channel 7, group 9**
	P00.5	O0		**General-purpose output**
	GTM_TOUT14	O1		**GTM muxed output**
	IOM_REF0_14			**Reference input 0**
	EDSADC_CGPWMN	O2		**Negative carrier generator output**
	QSPI3_SLSO3	O3		**Master slave select output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_FC0BFLOUT	O5		**Boundary flag output, FC channel 0**
	SENT_SPC4	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J4	P00.6	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN5_1			**Mux input channel 5 of TIM module 3**
	GTM_TIM3_IN1_14			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN5_1			**Mux input channel 5 of TIM module 2**
	EDSADC_ITR4F			**Trigger/Gate input, channel 4**
	EDSADC_DSDIN2A			**Digital datastream input, channel 2**
	SENT_SENT5B			**Receive input channel 5**
	ASCLIN5_ARXA			**Receive input**
	GTM_DTMT3_1			**CDTM3_DTM0**
	EVADC_G9CH6	AI		**Analog input channel 6, group 9**
	P00.6	O0		**General-purpose output**
	GTM_TOUT15	O1		**GTM muxed output**
	IOM_REF0_15			**Reference input 0**
	EDSADC_CGPWMP	O2		**Positive carrier generator output**
	—	O3		**Reserved**
	PSI5_TX2	O4		**TXD outputs (send data)**
	IOM_REF1_15			**Reference input 1**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC5	O6		**Transmit output**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN6_1			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN2_11			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	EDSADC_DSCIN4A			**Modulator clock input, channel 4**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	EDSADC_EDS4NA			**Negative analog input channel 4, pin A**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	EVADC_FC2BFLOUT	O3		**Boundary flag output, FC channel 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K4	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN7_1			**Mux input channel 7 of TIM module 3**
	GTM_TIM3_IN3_11			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	EDSADC_DSDIN4A			**Digital datastream input, channel 4**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	EDSADC_EDS4PA			**Positive analog input channel 4, pin A**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN0_7			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN0_1			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_1			**Mux input channel 0 of TIM module 0**
	CCU61_CC62INC			**T12 capture input 62**
	SENT_SENT8B			**Receive input channel 8**
	CCU61_CCPOS2A			**Hall capture input 2**
	EDSADC_DSCIN1A			**Modulator clock input, channel 1**
	EDSADC_ITR3F			**Trigger/Gate input, channel 3**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CCU60_T12HRC			**External timer start 12**
	ASCLIN13_ARXA			**Receive input**
	EVADC_G9CH3	AI		**Analog input channel 3, group 9**
	EDSADC_EDS4NB			**Negative analog input channel 4, pin B**
	P00.9	O0		**General-purpose output**
	GTM_TOUT18	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	ASCLIN4_ATX	O5		**Transmit output**
	SENT_SPC8	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K5	P00.10	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN1_11			**Mux input channel 1 of TIM module 4**
	GTM_TIM1_IN1_1			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_1			**Mux input channel 1 of TIM module 0**
	SENT_SENT9B			**Receive input channel 9**
	EDSADC_DSDIN1A			**Digital datastream input, channel 1**
	EVADC_G9CH2	AI		**Analog input channel 2, group 9**
	EDSADC_EDS4PB			**Positive analog input channel 4, pin B**
	P00.10	O0		**General-purpose output**
	GTM_TOUT19	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	ASCLIN13_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC9	O6		**Transmit output**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
L1	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN2_11			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_1			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_1			**Mux input channel 2 of TIM module 0**
	CCU60_CTRAPA			**Trap input capture**
	EDSADC_DSCIN0A			**Modulator clock input, channel 0**
	CCU61_T12HRE			**External timer start 12**
	SENT_SENT10B			**Receive input channel 10**
	ASCLIN13_ARXB			**Receive input**
	EVADC_G9CH1	AI		**Analog input channel 1, group 9**
	EVADC_FC3CH0			**Analog input FC channel 3**
	P00.11	O0		**General-purpose output**
	GTM_TOUT20	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	ASCLIN13_ATX	O3		**Transmit output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-25 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN3_11			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	SENT_SENT11B			**Receive input channel 11**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	EVADC_FC2CH0			**Analog input FC channel 2**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

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Table 2-26 Port 01 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G5	P01.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_2			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_14			**Mux input channel 0 of TIM module 2**
	GTM_TIM0_IN5_8			**Mux input channel 5 of TIM module 0**
	QSPI3_SLSIB			**Slave select input**
	EDSADC_ITR7F			**Trigger/Gate input, channel 7**
	EVADC_G9CH14	AI		**Analog input channel 14, group 9**
	P01.3	O0		**General-purpose output**
	GTM_TOUT111	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_SLSO9	O4		**Master slave select output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
G4	P01.4	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_2			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_14			**Mux input channel 1 of TIM module 2**
	GTM_TIM0_IN6_8			**Mux input channel 6 of TIM module 0**
	CAN01_RXDC			**CAN receive input node 1**
	EDSADC_ITR7E			**Trigger/Gate input, channel 7**
	EVADC_G9CH13	AI		**Analog input channel 13, group 9**
	P01.4	O0		**General-purpose output**
	GTM_TOUT112	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ASLSO	O3		**Slave select signal output**
	QSPI3_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-26 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H5	P01.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_2			**Mux input channel 3 of TIM module 5**
	GTM_TIM2_IN3_7			**Mux input channel 3 of TIM module 2**
	GTM_TIM2_IN2_7			**Mux input channel 2 of TIM module 2**
	QSPI3_MRSTC			**Master SPI data input**
	EDSADC_DSCIN8A			**Modulator clock input, channel 8**
	ASCLIN9_ARXA			**Receive input**
	EVADC_G9CH12	AI		**Analog input channel 12, group 9**
	P01.5	O0		**General-purpose output**
	GTM_TOUT113	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_MRST	O4		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O5		**Reserved**
	EDSADC_DSCOUT8	O6		**Modulator clock output**
	—	O7		**Reserved**
H4	P01.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_2			**Mux input channel 6 of TIM module 5**
	GTM_TIM5_IN5_3			**Mux input channel 5 of TIM module 5**
	GTM_TIM2_IN5_7			**Mux input channel 5 of TIM module 2**
	QSPI3_MTSRC			**Slave SPI data input**
	EDSADC_DSDIN8A			**Digital datastream input, channel 8**
	P01.6	O0		**General-purpose output**
	GTM_TOUT114	O1		**GTM muxed output**
	ASCLIN12_ATX	O2		**Transmit output**
	ASCLIN9_ASCLK	O3		**Shift clock output**
	QSPI3_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-26 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J5	P01.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_2			**Mux input channel 7 of TIM module 5**
	GTM_TIM2_IN7_7			**Mux input channel 7 of TIM module 2**
	QSPI3_SCLKC			**Slave SPI clock inputs**
	EDSADC_ITR8F			**Trigger/Gate input, channel 8**
	ASCLIN9_ARXB			**Receive input**
	P01.7	O0		**General-purpose output**
	GTM_TOUT115	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ATX	O3		**Transmit output**
	QSPI3_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-27 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	QSPI4_SLSO7	O2		**Master slave select output**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	SENT_SENT14B			**Receive input channel 14**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D2	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	EDSADC_DSCIN5B			**Modulator clock input, channel 5**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	MSC1_SDI1			**Upstream assynchronous input signal**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	SENT_SENT13B			**Receive input channel 13**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	EDSADC_DSDIN5B			**Digital datastream input, channel 5**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	SENT_SENT12B			**Receive input channel 12**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	EDSADC_DSCIN4B			**Modulator clock input, channel 4**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_10			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	EDSADC_DSDIN4B			**Digital datastream input, channel 4**
	EDSADC_ITR5E			**Trigger/Gate input, channel 5**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_10			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	EDSADC_ITR4E			**Trigger/Gate input, channel 4**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	PSI5_RX2B			**RXD inputs (receive data) channel 2**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_10			**Mux input channel 2 of TIM module 3**
	GTM_TIM3_IN0_2			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	PSI5_TX2	O4		**TXD outputs (send data)**
	IOM_REF1_15			**Reference input 1**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E4	P02.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_2			**Mux input channel 2 of TIM module 4**
	GTM_TIM3_IN3_10			**Mux input channel 3 of TIM module 3**
	GTM_TIM0_IN2_10			**Mux input channel 2 of TIM module 0**
	SENT_SENT20B			**Receive input channel 20**
	ASCLIN8_ARXA			**Receive input**
	P02.9	O0		**General-purpose output**
	GTM_TOUT116	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	ASCLIN8_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
F5	P02.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_2			**Mux input channel 3 of TIM module 4**
	GTM_TIM3_IN4_11			**Mux input channel 4 of TIM module 3**
	GTM_TIM0_IN3_10			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXC			**Receive input**
	CAN01_RXDE			**CAN receive input node 1**
	SENT_SENT21B			**Receive input channel 21**
	ASCLIN8_ARXB			**Receive input**
	P02.10	O0		**General-purpose output**
	GTM_TOUT117	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-27 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F4	P02.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_3			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN5_12			**Mux input channel 5 of TIM module 3**
	GTM_TIM0_IN7_7			**Mux input channel 7 of TIM module 0**
	SENT_SENT22B			**Receive input channel 22**
	EVADC_G9CH15	AI		**Analog input channel 15, group 9**
	P02.11	O0		**General-purpose output**
	GTM_TOUT118	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN8_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-28 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P10.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_12			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN4_2			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_2			**Mux input channel 4 of TIM module 0**
	GPT120_T6EUDB			**Count direction control input of core timer T6**
	ASCLIN11_ARXA			**Receive input**
	GETH_RXERC			**Receive Error MII**
	GTM_DTMA5_2			**CDTM5_DTM4**
	P10.0	O0		**General-purpose output**
	GTM_TOUT102	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	QSPI1_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN22_ATX	O6		**Transmit output**
	—	O7		**Reserved**

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Table 2-28 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_12			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN1_3			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_3			**Mux input channel 1 of TIM module 0**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	GTM_DTMT0_1			**CDTM0_DTM0**
	P10.1	O0		**General-purpose output**
	GTM_TOUT103	O1		**GTM muxed output**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	MSC0_EN1	O4		**Chip Select**
	EVADC_FC1BFLOUT	O5		**Boundary flag output, FC channel 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
A5	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_12			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN2_3			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_3			**Mux input channel 2 of TIM module 0**
	CAN02_RXDE			**CAN receive input node 2**
	MSC0_SDI1			**Upstream assynchronous input signal**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMT2_2			**CDTM2_DTM0**
	P10.2	O0		**General-purpose output**
	GTM_TOUT104	O1		**GTM muxed output**
	IOM_MON2_9			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	MSC0_EN0	O4		**Chip Select**
	EVADC_FC3BFLOUT	O5		**Boundary flag output, FC channel 3**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-28 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_10			**Mux input channel 6 of TIM module 4**
	GTM_TIM1_IN3_3			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_3			**Mux input channel 3 of TIM module 0**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	GTM_TOUT105	O1		**GTM muxed output**
	IOM_MON2_10			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	MSC0_EN0	O4		**Chip Select**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
B6	P10.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_3			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN6_2			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_2			**Mux input channel 6 of TIM module 0**
	QSPI1_MTSRC			**Slave SPI data input**
	CCU60_CCPOS0C			**Hall capture input 0**
	GPT120_T3INB			**Trigger/gate input of core timer T3**
	ASCLIN11_ARXB			**Receive input**
	ASCLIN22_ARXA			**Receive input**
	P10.4	O0		**General-purpose output**
	GTM_TOUT106	O1		**GTM muxed output**
	IOM_MON2_11			**Monitor input 2**
	ASCLIN22_ATX	O2		**Transmit output**
	QSPI1_SLSO8	O3		**Master slave select output**
	QSPI1_MTSR	O4		**Master SPI data output**
	MSC0_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-28 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B5	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_13			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	CAN20_RXDA			**CAN receive input node 0**
	MSC0_INJ1			**Injection signal from port**
	ASCLIN22_ARXB			**Receive input**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	PSI5_TX3	O7		**TXD outputs (send data)**

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Table 2-28 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A4	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_13			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	PSI5_RX3C			**RXD inputs (receive data) channel 3**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	ASCLIN23_ARXA			**Receive input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	CAN20_TXD	O5		**CAN transmit output node 0**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

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Table 2-28 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A3	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_3			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_3			**Mux input channel 0 of TIM module 0**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	ASCLIN23_ARXB			**Receive input**
	P10.7	O0		**General-purpose output**
	GTM_TOUT109	O1		**GTM muxed output**
	IOM_REF2_11			**Reference input 2**
	ASCLIN23_ATX	O2		**Transmit output**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

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Table 2-28 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B4	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_13			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN5_2			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_2			**Mux input channel 5 of TIM module 0**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	CAN20_RXDB			**CAN receive input node 0**
	P10.8	O0		**General-purpose output**
	GTM_TOUT110	O1		**GTM muxed output**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	ASCLIN23_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-29 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_4			**Mux input channel 0 of TIM module 4**
	GTM_TIM2_IN0_7			**Mux input channel 0 of TIM module 2**
	ASCLIN3_ARXB			**Receive input**
	GTM_DTMA2_1			**CDTM2_DTM4**
	P11.0	O0		**General-purpose output**
	GTM_TOUT119	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN11_TXD	O5		**CAN transmit output node 1**
	GETH_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_5			**Mux input channel 1 of TIM module 4**
	GTM_TIM2_IN1_6			**Mux input channel 1 of TIM module 2**
	P11.1	O0		**General-purpose output**
	GTM_TOUT120	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
A10	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN1_3			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B10	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN2_2			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN2_5			**Mux input channel 2 of TIM module 4**
	GTM_TIM2_IN2_6			**Mux input channel 2 of TIM module 2**
	GETH_RXCLKB			**Receive Clock MII**
	P11.4	O0		**General-purpose output**
	GTM_TOUT121	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN13_TXD	O5		**CAN transmit output node 3**
	GETH_TXER	O6		**Transmit Error MII**
	GETH_TXCLK	O7		**Transmit Clock Output for RGMII**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D8	P11.5	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN3_5			**Mux input channel 3 of TIM module 4**
	GTM_TIM2_IN3_8			**Mux input channel 3 of TIM module 2**
	GETH_TXCLKA			**Transmit Clock Input for MII**
	GETH_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P11.5	O0		**General-purpose output**
	GTM_TOUT122	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN3_2			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E8	P11.7	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN4_5			**Mux input channel 4 of TIM module 4**
	GTM_TIM2_IN4_7			**Mux input channel 4 of TIM module 2**
	GETH_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	CAN11_RXDD			**CAN receive input node 1**
	P11.7	O0		**General-purpose output**
	GTM_TOUT123	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
E7	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN5_5			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN5_8			**Mux input channel 5 of TIM module 2**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	GTM_TOUT124	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN4_2			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN5_2			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_2			**Mux input channel 5 of TIM module 2**
	GTM_TIM2_IN0_9			**Mux input channel 0 of TIM module 2**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	MSC0_SDI0			**Upstream assynchronous input signal**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	GTM_TOUT99	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN6_2			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN0_14			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN6_2			**Mux input channel 6 of TIM module 2**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	GTM_TOUT100	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	MSC0_EN0	O5		**Chip Select**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
B8	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN7_2			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_2			**Mux input channel 7 of TIM module 2**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	GTM_TOUT101	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	GTM_CLK2	O3		**CGM generated clock**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN6_5			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN6_7			**Mux input channel 6 of TIM module 2**
	GETH_RXERA			**Receive Error MII**
	I2C1_SDAA			**Serial Data Input 0**
	CAN13_RXDD			**CAN receive input node 3**
	P11.13	O0		**General-purpose output**
	GTM_TOUT125	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C1_SDA	O6		**Serial Data Output**
	—	O7		**Reserved**
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_4			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_8			**Mux input channel 7 of TIM module 2**
	GETH_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVB			**Receive Data Valid MII**
	GETH_CRSA			**Carrier Sense MII**
	I2C1_SCLA			**Serial Clock Input 0**
	CAN20_RXDF			**CAN receive input node 0**
	P11.14	O0		**General-purpose output**
	GTM_TOUT126	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C1_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**

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Table 2-29 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_5			**Mux input channel 7 of TIM module 4**
	GTM_TIM0_IN7_8			**Mux input channel 7 of TIM module 0**
	GETH_COLA			**Collision MII**
	P11.15	O0		**General-purpose output**
	GTM_TOUT127	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-30 Port 12 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_5			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN0_7			**Mux input channel 0 of TIM module 3**
	CAN00_RXDC			**CAN receive input node 0**
	GETH_RXCLKC			**Receive Clock MII**
	GTM_DTMA4_0			**CDTM4_DTM4**
	P12.0	O0		**General-purpose output**
	GTM_TOUT128	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_MDC	O6		**MDIO clock**
	—	O7		**Reserved**

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Table 2-30 Port 12 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_6			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN1_6			**Mux input channel 1 of TIM module 3**
	GETH_MDIOC			**MDIO Input**
	P12.1	O0		**General-purpose output**
	GTM_TOUT129	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

Table 2-31 Port 13 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN5_3			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_3			**Mux input channel 5 of TIM module 2**
	ASCLIN10_ARXC			**Receive input**
	ASCLIN21_ARXA			**Receive input**
	P13.0	O0		**General-purpose output**
	GTM_TOUT91	O1		**GTM muxed output**
	ASCLIN10_ATX	O2		**Transmit output**
	QSPI2_SCLKN	O3		**Master SPI clock output (LVDS N line)**
	MSC0_EN1	O4		**Chip Select**
	MSC0_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	CAN10_TXD	O7		**CAN transmit output node 0**

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Table 2-31 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN6_3			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_3			**Mux input channel 6 of TIM module 2**
	I2C0_SCLB			**Serial Clock Input 1**
	CAN10_RXDD			**CAN receive input node 0**
	ASCLIN10_ARXD			**Receive input**
	P13.1	O0		**General-purpose output**
	GTM_TOUT92	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLKP	O3		**Master SPI clock output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	I2C0_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**
B11	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN7_3			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_3			**Mux input channel 7 of TIM module 2**
	GPT120_CAPINA			**Trigger input to capture value of timer T5 into CAPREL register**
	I2C0_SDAB			**Serial Data Input 1**
	P13.2	O0		**General-purpose output**
	GTM_TOUT93	O1		**GTM muxed output**
	ASCLIN10_ASCLK	O2		**Shift clock output**
	QSPI2_MTSRN	O3		**Master SPI data output (LVDS N line)**
	MSC0_FCLP	O4		**Shift-clock direct part of the differential signal**
	MSC0_SON	O5		**Data output - inverted part of the differential signal**
	I2C0_SDA	O6		**Serial Data Output**
	ASCLIN21_ATX	O7		**Transmit output**

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Table 2-31 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN0_3			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_3			**Mux input channel 0 of TIM module 2**
	ASCLIN21_ARXB			**Receive input**
	P13.3	O0		**General-purpose output**
	GTM_TOUT94	O1		**GTM muxed output**
	ASCLIN10_ASLSO	O2		**Slave select signal output**
	QSPI2_MTSRP	O3		**Master SPI data output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	ASCLIN21_ATX	O6		**Transmit output**
	—	O7		**Reserved**

Table 2-32 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	SENT_SENT17D			**Receive input channel 17**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-32 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN4_3			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_3			**Mux input channel 4 of TIM module 0**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	SENT_SENT18D			**Receive input channel 18**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	GTM_TOUT81	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
E13	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_3			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_3			**Mux input channel 5 of TIM module 0**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	GTM_TOUT82	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

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Table 2-32 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
B15	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

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Table 2-32 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	ERAY1_TXDB	O7		**Transmit Channel B**
B13	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	ERAY1_TXENB	O7		**Transmit Enable Channel B**

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Table 2-32 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D13	P14.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_10			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN0_5			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_5			**Mux input channel 0 of TIM module 0**
	ERAY0_RXDB0			**Receive Channel B0**
	ERAY1_RXDB0			**Receive Channel B0**
	CAN10_RXDB			**CAN receive input node 0**
	CAN13_RXDA			**CAN receive input node 3**
	ASCLIN9_ARXC			**Receive input**
	ASCLIN20_ARXA			**Receive input**
	P14.7	O0		**General-purpose output**
	GTM_TOUT87	O1		**GTM muxed output**
	ASCLIN0_ARTS	O2		**Ready to send output**
	QSPI2_SLSO4	O3		**Master slave select output**
	ASCLIN9_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	ASCLIN20_ATX	O7		**Transmit output**
A13	P14.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_3			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_3			**Mux input channel 2 of TIM module 2**
	ERAY0_RXDA0			**Receive Channel A0**
	CAN02_RXDD			**CAN receive input node 2**
	ASCLIN1_ARXD			**Receive input**
	ERAY1_RXDA0			**Receive Channel A0**
	P14.8	O0		**General-purpose output**
	GTM_TOUT88	O1		**GTM muxed output**
	ASCLIN5_ASLSO	O2		**Slave select signal output**
	ASCLIN7_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	ASCLIN20_ATX	O7		**Transmit output**

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Table 2-32 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_3			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_3			**Mux input channel 3 of TIM module 2**
	ASCLIN0_ACTSA			**Clear to send input**
	QSPI2_MRSTFN			**Master SPI data input (LVDS N line)**
	ASCLIN9_ARXD			**Receive input**
	ASCLIN20_ARXB			**Receive input**
	P14.9	O0		**General-purpose output**
	GTM_TOUT89	O1		**GTM muxed output**
	CAN23_TXD	O2		**CAN transmit output node 3**
	MSC0_EN1	O3		**Chip Select**
	CAN10_TXD	O4		**CAN transmit output node 0**
	ERAY0_TXENB	O5		**Transmit Enable Channel B**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	ERAY1_TXENA	O7		**Transmit Enable Channel A**
D11	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_3			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_3			**Mux input channel 4 of TIM module 2**
	CAN23_RXDA			**CAN receive input node 3**
	QSPI2_MRSTFP			**Master SPI data input (LVDS P line)**
	P14.10	O0		**General-purpose output**
	GTM_TOUT90	O1		**GTM muxed output**
	—	O2		**Reserved**
	MSC0_EN0	O3		**Chip Select**
	ASCLIN1_ATX	O4		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	ERAY1_TXDA	O7		**Transmit Channel A**

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Table 2-33 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B20	P15.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_4			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_4			**Mux input channel 3 of TIM module 2**
	P15.0	O0		**General-purpose output**
	GTM_TOUT71	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO13	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
A18	P15.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_4			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_4			**Mux input channel 4 of TIM module 2**
	CAN02_RXDA			**CAN receive input node 2**
	ASCLIN1_ARXA			**Receive input**
	QSPI2_SLSIB			**Slave select input**
	SCU_E_REQ7_2			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.1	O0		**General-purpose output**
	GTM_TOUT72	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-33 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_4			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_4			**Mux input channel 5 of TIM module 2**
	QSPI2_SLSIA			**Slave select input**
	SENT_SENT10D			**Receive input channel 10**
	QSPI2_MRSTE			**Master SPI data input**
	P15.2	O0		**General-purpose output**
	GTM_TOUT73	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
B17	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_4			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_4			**Mux input channel 6 of TIM module 2**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	P15.3	O0		**General-purpose output**
	GTM_TOUT74	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	MSC0_EN1	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-33 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_4			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT11D			**Receive input channel 11**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	ASCLIN19_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-33 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_4			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
A16	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	ASCLIN19_ARXA			**Receive input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-33 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D15	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	ASCLIN19_ARXB			**Receive input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	ASCLIN19_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
D14	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-34 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CAN21_RXDC			**CAN receive input node 1**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
G19	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_11			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN3_5			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_5			**Mux input channel 3 of TIM module 2**
	CBS_TGI1			**Trigger input**
	GTM_DTMA1_1			**CDTM1_DTM4**
	P20.1	O0		**General-purpose output**
	GTM_TOUT60	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**

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Table 2-34 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H19	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**
G20	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_11			**Mux input channel 5 of TIM module 4**
	GTM_TIM3_IN4_5			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
F17	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_1			**Mux input channel 0 of TIM module 6**
	GTM_TIM3_IN6_5			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-34 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_5			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	GTM_TIM6_IN1_1			**Mux input channel 1 of TIM module 6**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
F20	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_1			**Mux input channel 2 of TIM module 6**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-34 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E17	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_1			**Mux input channel 3 of TIM module 6**
	GTM_TIM3_IN5_5			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
E19	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_6			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-34 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_6			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
D19	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_5			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-34 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_4			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
C20	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_4			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	IOM_PIN_15			**GPIO pad input to FPC**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-35 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_11			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN4_6			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_6			**Mux input channel 4 of TIM module 2**
	QSPI4_MRSTDN			**Master SPI data input (LVDS N line)**
	DMU_FDEST			**Enter destructive debug mode**
	ASCLIN11_ARXC			**Receive input**
	ASCLIN17_ARXB			**Receive input**
	P21.0	O0		**General-purpose output**
	GTM_TOUT51	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
J17	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN1_13			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_6			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_6			**Mux input channel 5 of TIM module 2**
	QSPI4_MRSTDP			**Master SPI data input (LVDS P line)**
	ASCLIN11_ARXD			**Receive input**
	ASCLIN18_ARXA			**Receive input**
	GTM_DTMA4_1			**CDTM4_DTM4**
	P21.1	O0		**General-purpose output**
	GTM_TOUT52	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**

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Table 2-35 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_11			**Mux input channel 4 of TIM module 5**
	GTM_TIM1_IN0_7			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_7			**Mux input channel 0 of TIM module 0**
	QSPI2_MRSTCN			**Master SPI data input (LVDS N line)**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	ASCLIN3_ARXGN			**Differential Receive input (low active)**
	HSCT0_RXDN			**Rx data**
	QSPI4_MRSTCN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXE			**Receive input**
	GTM_DTMA1_0			**CDTM1_DTM4**
	P21.2	O0		**General-purpose output**
	GTM_TOUT53	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**
J19	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_12			**Mux input channel 5 of TIM module 5**
	GTM_TIM1_IN1_6			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_6			**Mux input channel 1 of TIM module 0**
	QSPI2_MRSTCP			**Master SPI data input (LVDS P line)**
	ASCLIN3_ARXGP			**Differential Receive input (high active)**
	GETH_MDIOD			**MDIO Input**
	HSCT0_RXDP			**Rx data**
	QSPI4_MRSTCP			**Master SPI data input (LVDS P line)**
	P21.3	O0		**General-purpose output**
	GTM_TOUT54	O1		**GTM muxed output**
	ASCLIN11_ASCLK	O2		**Shift clock output**
	ASCLIN18_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

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Table 2-35 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN6_12			**Mux input channel 6 of TIM module 5**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	ASCLIN18_ARXB			**Receive input**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	ASCLIN18_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
J20	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN7_11			**Mux input channel 7 of TIM module 5**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

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Table 2-35 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM4_IN2_12			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**

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Table 2-35 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM4_IN3_12			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	GETH_RXERB			Receive Error MII
	P21.7	O0		General-purpose output
	GTM_TOUT58	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	CBS_TGO3	O		Trigger output
	DAP2	I/O		DAP: DAP2 Data I/O
	TDO	O		JTAG Module Data Output

Table 2-36 Port 22 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
P20	P22.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR	O3		Master SPI data output
	QSPI4_SCLKN	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output

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Table 2-36 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P19	P22.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN0_8			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_8			**Mux input channel 0 of TIM module 0**
	QSPI4_MRSTB			**Master SPI data input**
	ASCLIN7_ARXE			**Receive input**
	P22.1	O0		**General-purpose output**
	GTM_TOUT48	O1		**GTM muxed output**
	ASCLIN3_ATXP	O2		**Differential Transmit output (high active)**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI4_SCLKP	O4		**Master SPI clock output (LVDS P line)**
	MSC1_FCLP	O5		**Shift-clock direct part of the differential signal**
	—	O6		**Reserved**
	ASCLIN7_ATX	O7		**Transmit output**
R20	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	QSPI4_SLSIB			**Slave select input**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI4_SLSO3	O3		**Master slave select output**
	QSPI4_MTSRN	O4		**Master SPI data output (LVDS N line)**
	MSC1_SON	O5		**Data output - inverted part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-36 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R19	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	QSPI4_SCLKB			**Slave SPI clock inputs**
	ASCLIN5_ARXC			**Receive input**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI4_SCLK	O3		**Master SPI clock output**
	QSPI4_MTSRP	O4		**Master SPI data output (LVDS P line)**
	MSC1_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
P16	P22.4	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_8			**Mux input channel 0 of TIM module 3**
	ASCLIN7_ARXF			**Receive input**
	GTM_DTMA3_0			**CDTM3_DTM4**
	P22.4	O0		**General-purpose output**
	GTM_TOUT130	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI0_SLSO12	O4		**Master slave select output**
	—	O5		**Reserved**
	CAN13_TXD	O6		**CAN transmit output node 3**
	—	O7		**Reserved**
P17	P22.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_7			**Mux input channel 1 of TIM module 3**
	QSPI0_MTSRC			**Slave SPI data input**
	CAN13_RXDC			**CAN receive input node 3**
	P22.5	O0		**General-purpose output**
	GTM_TOUT131	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-36 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N16	P22.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_6			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_14			**Mux input channel 6 of TIM module 2**
	QSPI0_MRSTC			**Master SPI data input**
	ASCLIN4_ARXC			**Receive input**
	P22.6	O0		**General-purpose output**
	GTM_TOUT132	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	CAN21_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
N17	P22.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_7			**Mux input channel 3 of TIM module 3**
	QSPI0_SCLKC			**Slave SPI clock inputs**
	CAN21_RXDF			**CAN receive input node 1**
	P22.7	O0		**General-purpose output**
	GTM_TOUT133	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	ASCLIN17_ATX	O3		**Transmit output**
	QSPI0_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-36 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M16	P22.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN0_4			**Mux input channel 0 of TIM module 5**
	GTM_TIM3_IN4_7			**Mux input channel 4 of TIM module 3**
	QSPI0_SCLKB			**Slave SPI clock inputs**
	P22.8	O0		**General-purpose output**
	GTM_TOUT134	O1		**GTM muxed output**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI0_SCLK	O4		**Master SPI clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
M17	P22.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN1_10			**Mux input channel 1 of TIM module 5**
	GTM_TIM3_IN5_7			**Mux input channel 5 of TIM module 3**
	QSPI0_MRSTB			**Master SPI data input**
	ASCLIN4_ARXD			**Receive input**
	CAN22_RXDE			**CAN receive input node 2**
	GTM_DTMA3_1			**CDTM3_DTM4**
	P22.9	O0		**General-purpose output**
	GTM_TOUT135	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-36 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L16	P22.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN2_8			**Mux input channel 2 of TIM module 5**
	GTM_TIM3_IN6_7			**Mux input channel 6 of TIM module 3**
	QSPI0_MTSRB			**Slave SPI data input**
	P22.10	O0		**General-purpose output**
	GTM_TOUT136	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	CAN23_TXD	O5		**CAN transmit output node 3**
	—	O6		**Reserved**
	—	O7		**Reserved**
L17	P22.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_10			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN7_7			**Mux input channel 7 of TIM module 3**
	CAN23_RXDE			**CAN receive input node 3**
	ASCLIN17_ARXA			**Receive input**
	P22.11	O0		**General-purpose output**
	GTM_TOUT137	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	ASCLIN17_ATX	O3		**Transmit output**
	QSPI0_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-37 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
V20	P23.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN7_1			**Mux input channel 7 of TIM module 6**
	GTM_TIM1_IN5_4			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_4			**Mux input channel 5 of TIM module 0**
	CAN10_RXDC			**CAN receive input node 0**
	P23.0	O0		**General-purpose output**
	GTM_TOUT41	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
U19	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN6_1			**Mux input channel 6 of TIM module 6**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	MSC1_SDI0			**Upstream assynchronous input signal**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI4_SLSO6	O3		**Master slave select output**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**

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Table 2-37 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U20	P23.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN5_1			**Mux input channel 5 of TIM module 6**
	GTM_TIM1_IN6_5			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_5			**Mux input channel 6 of TIM module 0**
	ASCLIN7_ARXC			**Receive input**
	P23.2	O0		**General-purpose output**
	GTM_TOUT43	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CAN23_TXD	O4		**CAN transmit output node 3**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
T19	P23.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN4_2			**Mux input channel 4 of TIM module 6**
	GTM_TIM1_IN7_4			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_4			**Mux input channel 7 of TIM module 0**
	MSC1_INJ0			**Injection signal from port**
	ASCLIN6_ARXA			**Receive input**
	CAN12_RXDC			**CAN receive input node 2**
	CAN23_RXDB			**CAN receive input node 3**
	P23.3	O0		**General-purpose output**
	GTM_TOUT44	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-37 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T20	P23.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN3_2			**Mux input channel 3 of TIM module 6**
	GTM_TIM1_IN7_5			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_5			**Mux input channel 7 of TIM module 0**
	P23.4	O0		**General-purpose output**
	GTM_TOUT45	O1		**GTM muxed output**
	ASCLIN6_ASLSO	O2		**Slave select signal output**
	QSPI4_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**
T17	P23.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN2_2			**Mux input channel 2 of TIM module 6**
	GTM_TIM1_IN2_7			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_7			**Mux input channel 2 of TIM module 0**
	ASCLIN16_ARXA			**Receive input**
	P23.5	O0		**General-purpose output**
	GTM_TOUT46	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	QSPI4_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN1	O5		**Chip Select**
	CAN22_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**
R17	P23.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN1_2			**Mux input channel 1 of TIM module 6**
	GTM_TIM4_IN2_7			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_10			**Mux input channel 2 of TIM module 1**
	CAN22_RXDC			**CAN receive input node 2**
	P23.6	O0		**General-purpose output**
	GTM_TOUT138	O1		**GTM muxed output**
	ASCLIN16_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_SLSO11	O4		**Master slave select output**
	CAN11_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-37 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R16	P23.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM6_IN0_2			**Mux input channel 0 of TIM module 6**
	GTM_TIM4_IN3_7			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_10			**Mux input channel 3 of TIM module 1**
	CAN11_RXDC			**CAN receive input node 1**
	ASCLIN16_ARXB			**Receive input**
	P23.7	O0		**General-purpose output**
	GTM_TOUT139	O1		**GTM muxed output**
	ASCLIN16_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-38 Port 32 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-38 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W17	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			**Mux input channel 3 of TIM module 3**
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_8			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_8			**Mux input channel 3 of TIM module 0**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	CAN21_RXDD			**CAN receive input node 1**
	P32.2	O0		**General-purpose output**
	GTM_TOUT38	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**

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Table 2-38 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_5			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_5			**Mux input channel 4 of TIM module 0**
	P32.3	O0		**General-purpose output**
	GTM_TOUT39	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN3_ASCLK	O4		**Shift clock output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
W18	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	MSC1_SDI2			**Upstream assynchronous input signal**
	ASCLIN15_ARXA			**Receive input**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	PMS_DCDCSYNCO	O2		**DC-DC synchronization output**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	MSC1_EN0	O5		**Chip Select**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

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Table 2-38 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T15	P32.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_9			**Mux input channel 5 of TIM module 5**
	GTM_TIM4_IN1_14			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_8			**Mux input channel 5 of TIM module 3**
	SENT_SENT10C			**Receive input channel 10**
	P32.5	O0		**General-purpose output**
	GTM_TOUT140	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
U15	P32.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_9			**Mux input channel 6 of TIM module 5**
	GTM_TIM4_IN4_15			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN6_8			**Mux input channel 6 of TIM module 3**
	CAN02_RXDC			**CAN receive input node 2**
	CBS_TGI4			**Trigger input**
	ASCLIN2_ARXF			**Receive input**
	ASCLIN6_ARXC			**Receive input**
	SENT_SENT11C			**Receive input channel 11**
	P32.6	O0		**General-purpose output**
	GTM_TOUT141	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI2_SLSO12	O4		**Master slave select output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO4	O		**Trigger output**

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Table 2-38 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U16	P32.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_8			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN0_15			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN7_8			**Mux input channel 7 of TIM module 3**
	CBS_TGI5			**Trigger input**
	CAN22_RXDB			**CAN receive input node 2**
	SENT_SENT12C			**Receive input channel 12**
	ASCLIN15_ARXB			**Receive input**
	P32.7	O0		**General-purpose output**
	GTM_TOUT142	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	ASCLIN15_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO5	O		**Trigger output**

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Table 2-39 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_13			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN4_6			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_6			**Mux input channel 4 of TIM module 0**
	EDSADC_ITR0E			**Trigger/Gate input, channel 0**
	SENT_SENT13C			**Receive input channel 13**
	IOM_PIN_0			**GPIO pad input to FPC**
	GTM_DTMT1_2			**CDTM1_DTM0**
	EVADC_G10CH7	AI		**Analog input channel 7, group 10**
	P33.0	O0		**General-purpose output**
	GTM_TOUT22	O1		**GTM muxed output**
	IOM_MON0_0			**Monitor input 0**
	IOM_GTM_0			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	ASCLIN15_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	—	O7		**Reserved**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_15			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN5_6			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_6			**Mux input channel 5 of TIM module 0**
	EDSADC_ITR1E			**Trigger/Gate input, channel 1**
	PSI5_RX0C			**RXD inputs (receive data) channel 0**
	EDSADC_DSCIN2B			**Modulator clock input, channel 2**
	SENT_SENT9C			**Receive input channel 9**
	ASCLIN8_ARXC			**Receive input**
	IOM_PIN_1			**GPIO pad input to FPC**
	EVADC_G10CH6	AI		**Analog input channel 6, group 10**
	P33.1	O0		**General-purpose output**
	GTM_TOUT23	O1		**GTM muxed output**
	IOM_MON0_1			**Monitor input 0**
	IOM_GTM_1			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	QSPI2_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN2_14			**Mux input channel 2 of TIM module 3**
	GTM_TIM1_IN6_6			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_6			**Mux input channel 6 of TIM module 0**
	EDSADC_ITR2E			**Trigger/Gate input, channel 2**
	SENT_SENT8C			**Receive input channel 8**
	EDSADC_DSDIN2B			**Digital datastream input, channel 2**
	IOM_PIN_2			**GPIO pad input to FPC**
	EVADC_G10CH5	AI		**Analog input channel 5, group 10**
	P33.2	O0		**General-purpose output**
	GTM_TOUT24	O1		**GTM muxed output**
	IOM_MON0_2			**Monitor input 0**
	IOM_GTM_2			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	QSPI2_SLSO10	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	ASCLIN14_ATX	O7		**Transmit output**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN3_12			**Mux input channel 3 of TIM module 3**
	GTM_TIM1_IN7_6			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_6			**Mux input channel 7 of TIM module 0**
	PSI5_RX1C			**RXD inputs (receive data) channel 1**
	SENT_SENT7C			**Receive input channel 7**
	EDSADC_DSCIN1B			**Modulator clock input, channel 1**
	ASCLIN14_ARXA			**Receive input**
	IOM_PIN_3			**GPIO pad input to FPC**
	EVADC_G10CH4	AI		**Analog input channel 4, group 10**
	P33.3	O0		**General-purpose output**
	GTM_TOUT25	O1		**GTM muxed output**
	IOM_MON0_3			**Monitor input 0**
	IOM_GTM_3			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO2	O3		**Master slave select output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	ASCLIN14_ATX	O7		**Transmit output**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_10			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_10			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_10			**Mux input channel 0 of TIM module 0**
	EDSADC_ITR0F			**Trigger/Gate input, channel 0**
	SENT_SENT6C			**Receive input channel 6**
	EDSADC_DSDIN1B			**Digital datastream input, channel 1**
	CCU61_CTRAPC			**Trap input capture**
	ASCLIN5_ARXB			**Receive input**
	ASCLIN14_ARXB			**Receive input**
	IOM_PIN_4			**GPIO pad input to FPC**
	GTM_DTMT2_0			**CDTM2_DTM0**
	EVADC_G10CH3	AI		**Analog input channel 3, group 10**
	P33.4	O0		**General-purpose output**
	GTM_TOUT26	O1		**GTM muxed output**
	IOM_MON0_4			**Monitor input 0**
	IOM_GTM_4			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC0BFLOUT	O6		**Boundary flag output, FC channel 0**
	CAN13_TXD	O7		**CAN transmit output node 3**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN5_10			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN1_8			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_8			**Mux input channel 1 of TIM module 0**
	EDSADC_DSCIN0B			**Modulator clock input, channel 0**
	EDSADC_ITR1F			**Trigger/Gate input, channel 1**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	PSI5S_RXC			**RX data input**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	PSI5_RX2C			**RXD inputs (receive data) channel 2**
	SENT_SENT5C			**Receive input channel 5**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	EVADC_G10CH2	AI		**Analog input channel 2, group 10**
	P33.5	O0		**General-purpose output**
	GTM_TOUT27	O1		**GTM muxed output**
	IOM_MON0_5			**Monitor input 0**
	IOM_GTM_5			**GTM-provided inputs to EXOR combiner**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	ASCLIN5_ASLSO	O7		**Slave select signal output**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_9			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_9			**Mux input channel 2 of TIM module 0**
	EDSADC_ITR2F			**Trigger/Gate input, channel 2**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	SENT_SENT4C			**Receive input channel 4**
	CCU61_CCPOS1C			**Hall capture input 1**
	EDSADC_DSDIN0B			**Digital datastream input, channel 0**
	ASCLIN8_ARXD			**Receive input**
	IOM_PIN_6			**GPIO pad input to FPC**
	GTM_DTMT2_1			**CDTM2_DTM0**
	EVADC_G10CH1	AI		**Analog input channel 1, group 10**
	P33.6	O0		**General-purpose output**
	GTM_TOUT28	O1		**GTM muxed output**
	IOM_MON0_6			**Monitor input 0**
	IOM_GTM_6			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	PSI5_TX2	O4		**TXD outputs (send data)**
	IOM_REF1_15			**Reference input 1**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC1BFLOUT	O6		**Boundary flag output, FC channel 1**
	PSI5S_TX	O7		**TX data output**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN3_9			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_9			**Mux input channel 3 of TIM module 0**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT14C			**Receive input channel 14**
	IOM_PIN_7			**GPIO pad input to FPC**
	EVADC_G10CH0	AI		**Analog input channel 0, group 10**
	P33.7	O0		**General-purpose output**
	GTM_TOUT29	O1		**GTM muxed output**
	IOM_MON0_7			**Monitor input 0**
	IOM_GTM_7			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO7	O3		**Master slave select output**
	ASCLIN8_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO2	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO1	O3		**Master slave select output**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_14			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_9			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_9			**Mux input channel 0 of TIM module 0**
	QSPI4_SLSIA			**Slave select input**
	CAN01_RXDD			**CAN receive input node 1**
	ASCLIN0_ARXD			**Receive input**
	IOM_PIN_10			**GPIO pad input to FPC**
	P33.10	O0		**General-purpose output**
	GTM_TOUT32	O1		**GTM muxed output**
	IOM_MON0_10			**Monitor input 0**
	QSPI1_SLSO6	O2		**Master slave select output**
	QSPI4_SLSO0	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	PSI5S_CLK	O5		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SMU_FSP1	O		**FSP[1..0] Output Signals - Generated by SMU_core**
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_8			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_8			**Mux input channel 2 of TIM module 0**
	QSPI4_SCLKA			**Slave SPI clock inputs**
	IOM_PIN_11			**GPIO pad input to FPC**
	P33.11	O0		**General-purpose output**
	GTM_TOUT33	O1		**GTM muxed output**
	IOM_MON0_11			**Monitor input 0**
	ASCLIN1_ASCLK	O2		**Shift clock output**
	QSPI4_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EDSADC_CGPWMN	O6		**Negative carrier generator output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_6			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_6			**Mux input channel 0 of TIM module 2**
	QSPI4_MTSRA			**Slave SPI data input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	GTM_TOUT34	O1		**GTM muxed output**
	IOM_MON0_12			**Monitor input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MTSR	O3		**Master SPI data output**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	EDSADC_CGPWMP	O6		**Positive carrier generator output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_5			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_5			**Mux input channel 1 of TIM module 2**
	ASCLIN1_ARXF			**Receive input**
	EDSADC_SGNB			**Carrier sign signal input**
	QSPI4_MRSTA			**Master SPI data input**
	MSC1_INJ1			**Injection signal from port**
	CAN22_RXDA			**CAN receive input node 2**
	P33.13	O0		**General-purpose output**
	GTM_TOUT35	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-39 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T14	P33.14	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN0_8			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN5_14			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_8			**Mux input channel 0 of TIM module 2**
	QSPI2_SCLKD			**Slave SPI clock inputs**
	CBS_TGI6			**Trigger input**
	P33.14	O0		**General-purpose output**
	GTM_TOUT143	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**
	CBS_TGO6	O		**Trigger output**
U14	P33.15	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN1_9			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN6_12			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_7			**Mux input channel 1 of TIM module 2**
	CBS_TGI7			**Trigger input**
	P33.15	O0		**General-purpose output**
	GTM_TOUT144	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
	CBS_TGO7	O		**Trigger output**

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Table 2-40 Port 34 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN3_9			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN4_12			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN3_9			**Mux input channel 3 of TIM module 2**
	EVADC_G10CH11	AI		**Analog input channel 11, group 10**
	P34.1	O0		**General-purpose output**
	GTM_TOUT146	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	CAN00_TXD	O4		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN4_9			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN5_13			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN4_8			**Mux input channel 4 of TIM module 2**
	ASCLIN4_ARXB			**Receive input**
	CAN00_RXDG			**CAN receive input node 0**
	CAN20_RXDC			**CAN receive input node 0**
	EVADC_G10CH10	AI		**Analog input channel 10, group 10**
	P34.2	O0		**General-purpose output**
	GTM_TOUT147	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-40 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN5_10			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN6_13			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN5_9			**Mux input channel 5 of TIM module 2**
	EVADC_G10CH9	AI		**Analog input channel 9, group 10**
	P34.3	O0		**General-purpose output**
	GTM_TOUT148	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI2_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
T13	P34.4	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN6_10			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN7_12			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN6_8			**Mux input channel 6 of TIM module 2**
	QSPI2_MRSTD			**Master SPI data input**
	EVADC_G10CH8	AI		**Analog input channel 8, group 10**
	P34.4	O0		**General-purpose output**
	GTM_TOUT149	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI2_MRST	O4		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-40 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U13	P34.5	I	FAST / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN7_9			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN7_12			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_9			**Mux input channel 7 of TIM module 2**
	QSPI2_MTSRD			**Slave SPI data input**
	ASCLIN8_ARXE			**Receive input**
	P34.5	O0		**General-purpose output**
	GTM_TOUT150	O1		**GTM muxed output**
	ASCLIN8_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI2_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

Table 2-41 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
U10	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
W9	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
U9	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
T9	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G11CH0			**Analog input channel 0, group 11**
	EVADC_G0CH4			**Analog input channel 4, group 0**
Y9	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G11CH1			**Analog input channel 1, group 11**
	EVADC_G0CH5			**Analog input channel 5, group 0**

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Table 2-41 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T8	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G11CH2			**Analog input channel 2, group 11**
	EVADC_G0CH6			**Analog input channel 6, group 0**
U8	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G11CH3			**Analog input channel 3, group 11**
	EVADC_G0CH7			**Analog input channel 7, group 0**
W8	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G11CH4			**Analog input channel 4, group 11**
	EVADC_G1CH0			**Analog input channel 0, group 1**
U7	AN9	I	D / HighZ / VDDM	**Analog Input 9**
	EVADC_G11CH5			**Analog input channel 5, group 11**
	EVADC_G1CH1			**Analog input channel 1, group 1**
Y8	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G11CH6			**Analog input channel 6, group 11**
	EVADC_G1CH2			**Analog input channel 2, group 1**
W7	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G11CH7			**Analog input channel 7, group 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
T7	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
W6	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
U6	AN14	I	D / HighZ / VDDM	**Analog Input 14**
	EVADC_G1CH6			**Analog input channel 6, group 1**
	EDSADC_EDS3PB			**Positive analog input channel 3, pin B**
T6	AN15	I	D / HighZ / VDDM	**Analog Input 15**
	EVADC_G1CH7			**Analog input channel 7, group 1**
	EDSADC_EDS3NB			**Negative analog input channel 3, pin N**
W5	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
U5	AN17/P40.10	I	S / HighZ / VDDM	**Analog Input 17**
	SENT_SENT10A			**Receive input channel 10**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**

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Table 2-41 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W4	AN18/P40.11	I	S / HighZ / VDDM	**Analog Input 18**
	SENT_SENT11A			**Receive input channel 11**
	EVADC_G11CH8			**Analog input channel 8, group 11**
	EVADC_G2CH2			**Analog input channel 2, group 2**
W3	AN19/P40.12	I	S / HighZ / VDDM	**Analog Input 19**
	SENT_SENT12A			**Receive input channel 12**
	EVADC_G11CH9			**Analog input channel 9, group 11**
	EVADC_G2CH3			**Analog input channel 3, group 2**
Y3	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
Y2	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
T5	AN22	I	D / HighZ / VDDM	**Analog Input 22**
	EVADC_G2CH6			**Analog input channel 6, group 2**
R5	AN23	I	D / HighZ / VDDM	**Analog Input 23**
	EVADC_G2CH7			**Analog input channel 7, group 2**
W2	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
W1	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
V2	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**
	EVADC_G11CH10			**Analog input channel 10, group 11**
V1	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
	EVADC_G11CH11			**Analog input channel 11, group 11**

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Table 2-41 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	AN28/P40.13	I	S / HighZ / VDDM	**Analog Input 28**
	SENT_SENT13A			**Receive input channel 13**
	EVADC_G3CH4			**Analog input channel 4, group 3**
	EVADC_G4CH4			**Analog input channel 4, group 4**
U1	AN29/P40.14	I	S / HighZ / VDDM	**Analog Input 29**
	SENT_SENT14A			**Receive input channel 14**
	EVADC_G3CH5			**Analog input channel 5, group 3**
	EVADC_G4CH5			**Analog input channel 5, group 4**
T4	AN30	I	D / HighZ / VDDM	**Analog Input 30**
	EVADC_G3CH6			**Analog input channel 6, group 3**
	EVADC_G4CH6			**Analog input channel 6, group 4**
R4	AN31	I	D / HighZ / VDDM	**Analog Input 31**
	EVADC_G3CH7			**Analog input channel 7, group 3**
	EVADC_G4CH7			**Analog input channel 7, group 4**
P4	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
	EVADC_G11CH12			**Analog input channel 12, group 11**
R1	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
	EVADC_G11CH13			**Analog input channel 13, group 11**
P5	AN34	I	D / HighZ / VDDM	**Analog Input 34**
	EVADC_G8CH2			**Analog input channel 2, group 8**
	EVADC_G11CH14			**Analog input channel 14, group 11**
R2	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
	EVADC_G11CH15			**Analog input channel 15, group 11**
N4	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**

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Table 2-41 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P2	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
N5	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
P1	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
M5	AN40	I	D / HighZ / VDDM	**Analog Input 40**
	EVADC_G8CH8			**Analog input channel 8, group 8**
	EVADC_G4CH0			**Analog input channel 0, group 4**
M4	AN41	I	D / HighZ / VDDM	**Analog Input 41**
	EVADC_G8CH9			**Analog input channel 9, group 8**
	EVADC_G4CH1			**Analog input channel 1, group 4**
L5	AN42	I	D / HighZ / VDDM	**Analog Input 42**
	EVADC_G8CH10			**Analog input channel 10, group 8**
	EVADC_G4CH2			**Analog input channel 2, group 4**
L4	AN43	I	D / HighZ / VDDM	**Analog Input 43**
	EVADC_G8CH11			**Analog input channel 11, group 8**
	EVADC_G4CH3			**Analog input channel 3, group 4**
N1	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
N2	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
M1	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**

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Table 2-41 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M2	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

3. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
4. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-42 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
G16	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
F16	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**
W17	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
Y17	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT

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Table 2-42 System I/O (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L19	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
J16	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**
K16	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**
G17	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.

Table 2-43 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
P8, P13, N7, N14, E15, H14, D16, G13, G8, H7	VDD	I	—	**Digital Core Power Supply (1.25V)**
A2, B3, V19, W20	VEXT	I	—	**External Power Supply (5V / 3.3V)**
D5	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
Y5	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
B18, A19	VDDP3	I	—	**Flash Power Supply (3.3V)**
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS	I	—	**Digital Ground**
Y4	VSSM	I	—	**Analog Ground for VDDM**

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Table 2-43 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G10, G11, G12, L14, P10, P11, K7, L7	VSS	I	—	**Digital Ground**
L20	VSS	I	—	**Oscillator Ground, VSS(OSC)**
Y6	VAREF1	I	—	**Positive Analog Reference Voltage 1**
Y7	VAGND1	I	—	**Negative Analog Reference Voltage 1**
T1	VAREF2	I	—	**Positive Analog Reference Voltage 2**
T2	VAGND2	I	—	**Negative Analog Reference Voltage 2**
K14	NC	I	—	**Not connected. These pins are reserved for future extensions and shall not be connected externally**
A1, Y1, U4	NC1	I	—	**Not connected. These pins are not connected on package level and will not be used for future extensions**
T11	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
N19	VDD	I	—	**Digital Power Supply for Oscillator (1.25V), VDD(OSC)**
N20	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

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2.3 Sequence of Pads in Pad Frame

Table 2-44 Pad List

Number	Pad Name	Pad Type	X	Y	Comment
1	$\overline{\text{ESR1}}$	FAST / PU1 / VEXT	263799	179145	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
2	$\overline{\text{ESR0}}$	FAST / OD / VEXT	357795	179145	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
3	P20.9	FAST / PU1 / VEXT / ES	409293	348147	General-purpose I/O
4	P20.14	FAST / PU1 / VEXT / ES	456291	179145	General-purpose I/O
5	P15.0	FAST / PU1 / VEXT / ES	503289	348147	General-purpose I/O
6	P15.2	FAST / PU1 / VEXT / ES	550287	179145	General-purpose I/O
7	P15.4	FAST / PU1 / VEXT / ES	597285	348147	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
8	P15.1	FAST / PU1 / VEXT / ES	644283	179145	General-purpose I/O
9	P15.3	FAST / PU1 / VEXT / ES	691281	348147	General-purpose I/O
10	P14.0	FAST / PU1 / VEXT / ES2	738279	179145	General-purpose I/O
11	VDDP3	Vx	785277	348147	Supply Voltage
12	P15.10	FAST / PU1 / VEXT / ES6	832275	179145	General-purpose I/O
13	P15.11	FAST / PU1 / VEXT / ES6	926271	179145	General-purpose I/O
14	VDD	Vx	973269	348147	Supply Voltage
15	VSS	Vx	1048869	179145	Supply Voltage
16	P15.12	FAST / PU1 / VEXT / ES6	1124469	348147	General-purpose I/O
17	P15.6	FAST / PU1 / VEXT / ES	1171467	179145	General-purpose I/O
18	P15.13	FAST / PU1 / VEXT / ES6	1218465	348147	General-purpose I/O
19	P15.7	FAST / PU1 / VEXT / ES	1265463	179145	General-purpose I/O
20	P15.14	FAST / PU1 / VEXT / ES	1312461	348147	General-purpose I/O
21	VEXT	Vx	1359459	179145	Supply Voltage
22	P15.15	FAST / PU1 / VEXT / ES	1406457	348147	General-purpose I/O
23	VSS	Vx	1453455	179145	Supply Voltage
24	P14.4	SLOW / PU2 / VEXT / ES	1500453	348147	General-purpose I/O
25	P15.8	FAST / PU1 / VEXT / ES	1547451	179145	General-purpose I/O
26	P14.1	FAST / PU1 / VEXT / ES2	1594449	348147	General-purpose I/O
27	P14.3	SLOW / PU2 / VEXT / ES	1641447	179145	General-purpose I/O
28	P14.5	FAST / PU2 / VEXT / ES	1688445	348147	General-purpose I/O
29	P15.5	FAST / PU1 / VEXT / ES	1735443	179145	General-purpose I/O
30	P14.11	SLOW / PU1 / VEXT / ES	1782441	348147	General-purpose I/O
31	VSS	Vx	1858041	179145	Supply Voltage

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
32	P14.12	SLOW / PU1 / VEXT / ES	1933641	348147	General-purpose I/O
33	VDD	Vx	2009241	179145	Supply Voltage
34	P14.13	FAST / PU1 / VEXT / ES	2084841	348147	General-purpose I/O
35	P14.7	SLOW / PU1 / VEXT / ES	2131839	179145	General-purpose I/O
36	P14.15	SLOW / PU1 / VEXT / ES	2178837	348147	General-purpose I/O
37	P14.6	FAST / PU1 / VEXT / ES	2225835	179145	General-purpose I/O
38	VEXT	Vx	2272833	348147	Supply Voltage
39	P14.9	LVDS_RX / FAST / PU1 / VEXT / ES	2347884	179145	General-purpose I/O
40	P14.10	LVDS_RX / FAST / PU1 / VEXT / ES	2441880	179145	General-purpose I/O
41	P14.8	SLOW / PU1 / VEXT / ES	2516931	348147	General-purpose I/O
42	P14.2	SLOW / PU2 / VEXT / ES	2563929	179145	General-purpose I/O
43	P13.0	LVDS_TX / FAST / PU1 / VEXT / ES6	2675430	348147	General-purpose I/O
44	P13.1	LVDS_TX / FAST / PU1 / VEXT / ES6	2769426	348147	General-purpose I/O
45	VDD	Vx	2880927	348147	Supply Voltage
46	VSS	Vx	2936925	179145	Supply Voltage
47	P13.2	LVDS_TX / FAST / PU1 / VEXT / ES6	3048426	348147	General-purpose I/O
48	P13.3	LVDS_TX / FAST / PU1 / VEXT / ES6	3142422	348147	General-purpose I/O
49	VDD	Vx	3253923	179145	Supply Voltage
50	P13.9	FAST / PU1 / VEXT / ES	3300921	348147	General-purpose I/O
51	VSS	Vx	3347919	179145	Supply Voltage
52	P13.4	LVDS_TX / FAST / PU1 / VEXT / ES6	3459420	348147	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
53	P13.5	LVDS_TX / FAST / PU1 / VEXT / ES6	3553416	348147	General-purpose I/O
54	P13.6	LVDS_TX / FAST / PU1 / VEXT / ES6	3729420	348147	General-purpose I/O
55	P13.7	LVDS_TX / FAST / PU1 / VEXT / ES6	3823416	348147	General-purpose I/O
56	VDD	Vx	3934917	348147	Supply Voltage
57	VSS	Vx	3981915	179145	Supply Voltage
58	P13.10	SLOW / PU1 / VEXT / ES	4085973	348147	General-purpose I/O
59	VSS	Vx	4132971	179145	Supply Voltage
60	P13.12	SLOW / PU1 / VEXT / ES	4179969	348147	General-purpose I/O
61	VEXT	Vx	4226967	179145	Supply Voltage
62	VDDP3	Vx	4408965	348147	Supply Voltage
63	P13.13	SLOW / PU1 / VEXT / ES	4455963	179145	General-purpose I/O
64	VDDP3	Vx	4502961	348147	Supply Voltage
65	P13.14	SLOW / PU1 / VEXT / ES	4549959	179145	General-purpose I/O
66	VDDP3	Vx	4596957	348147	Supply Voltage
67	P13.11	SLOW / PU1 / VEXT / ES	4643955	179145	General-purpose I/O
68	P13.15	SLOW / PU1 / VEXT / ES	4690953	348147	General-purpose I/O
69	P14.14	FAST / PU1 / VEXT / ES	4737951	179145	General-purpose I/O
70	P12.0	SLOW / PU1 / VFLEX / ES	4832019	179145	General-purpose I/O
71	P12.1	SLOW / PU1 / VFLEX / ES	4879017	348147	General-purpose I/O
72	P11.0	RFAST / PU1 / VFLEX / ES	4983021	348147	General-purpose I/O
73	VFLEX	Vx	5030019	179145	Supply Voltage
74	P11.1	RFAST / PU1 / VFLEX / ES	5105223	348147	General-purpose I/O
75	VSS	Vx	5152221	179145	Supply Voltage
76	P11.2	RFAST / PU1 / VFLEX / ES	5227425	348147	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
77	VDD	Vx	5274423	179145	Supply Voltage
78	P11.4	RFAST / PU1 / VFLEX / ES	5390127	348147	General-purpose I/O
79	VSS	Vx	5477625	179145	Supply Voltage
80	P11.3	RFAST / PU1 / VFLEX / ES	5552829	348147	General-purpose I/O
81	VFLEX	Vx	5599827	179145	Supply Voltage
82	P11.6	RFAST / PU1 / VFLEX / ES	5675031	348147	General-purpose I/O
83	VSS	Vx	5722029	179145	Supply Voltage
84	P11.5	SLOW / RGMII_Input / PU1 / VFLEX / ES	5769027	348147	General-purpose I/O
85	P11.7	SLOW / RGMII_Input / PU1 / VFLEX / ES	5821407	179145	General-purpose I/O
86	P11.9	FAST / RGMII_Input / PU1 / VFLEX / ES	5872005	348147	General-purpose I/O
87	VFLEX	Vx	5922603	179145	Supply Voltage
88	P11.8	SLOW / RGMII_Input / PU1 / VFLEX / ES	5969601	348147	General-purpose I/O
89	P11.10	FAST / RGMII_Input / PU1 / VFLEX / ES	6020199	179145	General-purpose I/O
90	P11.11	FAST / RGMII_Input / PU1 / VFLEX / ES	6070797	348147	General-purpose I/O
91	VSS	Vx	6121395	179145	Supply Voltage
92	P11.12	FAST / RGMII_Input / PU1 / VFLEX / ES	6168393	348147	General-purpose I/O
93	P11.14	SLOW / PU1 / VFLEX / ES	6276357	348147	General-purpose I/O
94	P11.13	SLOW / PU1 / VFLEX / ES	6323355	179145	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
95	P11.15	SLOW / PU1 / VFLEX / ES	6370353	348147	General-purpose I/O
96	VDD	Vx	6444567	179145	Supply Voltage
97	VSS	Vx	6538563	179145	Supply Voltage
98	P10.0	SLOW / PU1 / VEXT / ES	6614163	348147	General-purpose I/O
99	VDD	Vx	6689763	179145	Supply Voltage
100	P10.3	FAST / PU1 / VEXT / ES	6765363	348147	General-purpose I/O
101	VSS	Vx	6840963	179145	Supply Voltage
102	P10.1	FAST / PU1 / VEXT / ES	6916563	348147	General-purpose I/O
103	VEXT	Vx	6972561	179145	Supply Voltage
104	P10.9	SLOW / PU1 / VEXT / ES	7089147	348147	General-purpose I/O
105	VSS	Vx	7176645	179145	Supply Voltage
106	P10.11	SLOW / PU1 / VEXT / ES	7306641	179145	General-purpose I/O
107	P10.4	FAST / PU1 / VEXT / ES	7391295	263799	General-purpose I/O
108	P10.10	SLOW / PU1 / VEXT / ES	7391295	357795	General-purpose I/O
109	P10.15	SLOW / PU1 / VEXT / ES	7222293	451791	General-purpose I/O
110	P10.13	SLOW / PU1 / VEXT / ES	7391295	545787	General-purpose I/O
111	P10.2	FAST / PU1 / VEXT / ES	7222293	639783	General-purpose I/O
112	P10.14	SLOW / PU1 / VEXT / ES	7391295	733779	General-purpose I/O
113	P10.6	SLOW / PU2 / VEXT / ES	7222293	795888	General-purpose I/O
114	P10.5	SLOW / PU2 / VEXT / ES	7391295	842886	General-purpose I/O
115	P10.8	SLOW / PU1 / VEXT / ES	7391295	936882	General-purpose I/O
116	P10.7	SLOW / PU1 / VEXT / ES	7222293	983880	General-purpose I/O
117	P02.0	FAST / PU1 / VEXT / ES	7391295	1030878	General-purpose I/O
118	P02.2	FAST / PU1 / VEXT / ES	7222293	1077876	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
119	P02.1	SLOW / PU1 / VEXT / ES	7391295	1124874	General-purpose I/O
120	P02.5	FAST / PU1 / VEXT / ES	7222293	1171872	General-purpose I/O
121	P02.3	SLOW / PU1 / VEXT / ES	7391295	1218870	General-purpose I/O
122	P02.13	SLOW / PU1 / VEXT / ES	7222293	1265868	General-purpose I/O
123	P02.11	SLOW / PU1 / VEXT / ES	7391295	1312866	General-purpose I/O
124	P02.12	SLOW / PU1 / VEXT / ES	7222293	1359864	General-purpose I/O
125	P02.4	FAST / PU1 / VEXT / ES	7391295	1406862	General-purpose I/O
126	P02.15	FAST / PU1 / VEXT / ES	7222293	1453860	General-purpose I/O
127	VDD	Vx	7391295	1529460	Supply Voltage
128	VSS	Vx	7391295	1623456	Supply Voltage
129	P02.14	SLOW / PU1 / VEXT / ES	7222293	1699056	General-purpose I/O
130	P02.6	FAST / PU1 / VEXT / ES	7391295	1746054	General-purpose I/O
131	P01.0	SLOW / PU1 / VEXT / ES	7222293	1793052	General-purpose I/O
132	P02.7	FAST / PU1 / VEXT / ES	7391295	1840050	General-purpose I/O
133	P01.1	SLOW / PU1 / VEXT / ES	7222293	1887048	General-purpose I/O
134	P02.8	SLOW / PU1 / VEXT / ES	7391295	1934046	General-purpose I/O
135	P01.2	SLOW / PU1 / VEXT / ES	7222293	1981044	General-purpose I/O
136	P02.9	SLOW / PU1 / VEXT / ES	7391295	2028042	General-purpose I/O
137	P01.8	SLOW / PU1 / VEXT / ES	7222293	2075040	General-purpose I/O
138	VEXT	Vx	7391295	2122038	Supply Voltage
139	P01.9	SLOW / PU1 / VEXT / ES	7222293	2169036	General-purpose I/O
140	VSS	Vx	7391295	2216034	Supply Voltage
141	P01.11	SLOW / PU1 / VEXT / ES	7222293	2263032	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
142	P02.10	SLOW / PU1 / VEXT / ES	7391295	2310030	General-purpose I/O
143	P01.10	SLOW / PU1 / VEXT / ES	7222293	2357028	General-purpose I/O
144	VSS	Vx	7391295	2432628	Supply Voltage
145	VDD	Vx	7391295	2526624	Supply Voltage
146	P00.0	FAST / PU1 / VEXT / ES	7391295	2620620	General-purpose I/O
147	P01.13	FAST / PU1 / VEXT / ES	7222293	2667618	General-purpose I/O
148	P01.4	SLOW / PU1 / VEXT / ES	7391295	2714616	General-purpose I/O
149	P01.12	FAST / PU1 / VEXT / ES	7222293	2761614	General-purpose I/O
150	P01.3	SLOW / PU1 / VEXT / ES	7391295	2808612	General-purpose I/O
151	P01.15	SLOW / PU1 / VEXT / ES	7222293	2855610	General-purpose I/O
152	P01.6	FAST / PU1 / VEXT / ES	7391295	2902608	General-purpose I/O
153	P01.14	FAST / PU1 / VEXT / ES	7222293	2949606	General-purpose I/O
154	P01.5	SLOW / PU1 / VEXT / ES	7391295	2996604	General-purpose I/O
155	P00.15	FAST / PU1 / VEXT / ES	7222293	3043602	General-purpose I/O
156	P01.7	FAST / PU1 / VEXT / ES	7391295	3090600	General-purpose I/O
157	P00.13	FAST / PU1 / VEXT / ES	7222293	3137598	General-purpose I/O
158	RESERVED	Vx	7391295	3184596	PBIST_OFFMust be bonded to VSS
159	RESERVED	Vx	7391295	3278592	OTPMust be bonded to VSS
160	P00.14	SLOW / PU1 / VEXT / ES	7222293	3325590	General-purpose I/O
161	VSS	Vx	7391295	3401190	Supply Voltage
162	VDD	Vx	7391295	3495186	Supply Voltage
164	P00.1	SLOW / PU1 / VEXT / ES	7222293	3572226	General-purpose I/O
165	P00.2	SLOW / PU1 / VEXT / ES1	7391295	3619224	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
166	P00.3	SLOW / PU1 / VEXT / ES1	7222293	3666222	General-purpose I/O
167	P00.4	SLOW / PU1 / VEXT / ES1	7391295	3713220	General-purpose I/O
168	P00.5	SLOW / PU1 / VEXT / ES1	7222293	3760218	General-purpose I/O
169	VSS	Vx	7391295	3807216	Supply Voltage
170	P00.6	SLOW / PU1 / VEXT / ES1	7222293	3854214	General-purpose I/O
171	VEXT	Vx	7391295	3901212	Supply Voltage
172	P00.7	SLOW / PU1 / VEXT / ES1	7222293	3948210	General-purpose I/O
173	P00.8	SLOW / PU1 / VEXT / ES1	7391295	3995208	General-purpose I/O
174	P00.9	SLOW / PU1 / VEXT / ES1	7222293	4042206	General-purpose I/O
175	P00.10	SLOW / PU1 / VEXT / ES1	7391295	4089204	General-purpose I/O
176	P00.11	SLOW / PU1 / VEXT / ES1	7222293	4136202	General-purpose I/O
177	P00.12	SLOW / PU1 / VEXT / ES1	7391295	4183200	General-purpose I/O
179	AN47	D / HighZ / VDDM	7222293	4257414	Analog Input 47
180	AN46	D / HighZ / VDDM	7391295	4304412	Analog Input 46
181	AN45	D / HighZ / VDDM	7222293	4351410	Analog Input 45
182	AN44	D / HighZ / VDDM	7391295	4398408	Analog Input 44
183	VDDM	Vx	7222293	4445406	Supply Voltage
184	VSSM	Vx	7391295	4492404	Supply Voltage
185	VAREF5	Vx	7222293	4539402	Supply Voltage
186	VAREF4	Vx	7391295	4586400	Supply Voltage
187	VAGND5	Vx	7222293	4633398	Supply Voltage
188	VAGND4	Vx	7391295	4680396	Supply Voltage
189	AN43	D / HighZ / VDDM	7222293	4727394	Analog Input 43
190	AN42	D / HighZ / VDDM	7391295	4774392	Analog Input 42
191	AN41	D / HighZ / VDDM	7222293	4821390	Analog Input 41

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
192	VSSM	Vx	7391295	4868388	Supply Voltage
193	VDDM	Vx	7222293	4915386	Supply Voltage
194	AN40	D / HighZ / VDDM	7391295	4962384	Analog Input 40
195	AN39/P40.9	S / HighZ / VDDM	7222293	5009382	Analog Input 39
196	VSSM	Vx	7391295	5056380	Supply Voltage
197	AN38/P40.8	S / HighZ / VDDM	7222293	5103378	Analog Input 38
198	VDDM	Vx	7391295	5150376	Supply Voltage
199	AN37/P40.7	S / HighZ / VDDM	7222293	5197374	Analog Input 37
200	AN36/P40.6	S / HighZ / VDDM	7391295	5244372	Analog Input 36
201	AN35	D / HighZ / VDDM	7222293	5291370	Analog Input 35
202	AN34	D / HighZ / VDDM	7391295	5338368	Analog Input 34
203	AN33/P40.5	S / HighZ / VDDM	7222293	5385366	Analog Input 33
204	AN32/P40.4	S / HighZ / VDDM	7391295	5432364	Analog Input 32
205	VAREF3	Vx	7222293	5479362	Supply Voltage
206	VAREF2	Vx	7391295	5526360	Supply Voltage
207	VAGND3	Vx	7222293	5573358	Supply Voltage
208	VAGND2	Vx	7391295	5620356	Supply Voltage
209	AN71/P41.3	S / HighZ / VDDM	7222293	5667354	Analog Input 71
210	AN70/P41.2	S / HighZ / VDDM	7391295	5714352	Analog Input 70
211	AN69/P41.1	S / HighZ / VDDM	7222293	5761350	Analog Input 69
212	AN68/P41.0	S / HighZ / VDDM	7391295	5808348	Analog Input 68
213	AN67/P40.15	S / HighZ / VDDM	7222293	5855346	Analog Input 67
214	AN66	D / HighZ / VDDM	7391295	5902344	Analog Input 66
215	AN65	D / HighZ / VDDM	7222293	5949342	Analog Input 65
216	AN64/P41.8	S / HighZ / VDDM	7391295	5996340	Analog Input 64

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
217	VDDM	Vx	7222293	6043338	Supply Voltage
218	VSSM	Vx	7391295	6090336	Supply Voltage
219	AN63/P41.7	S / HighZ / VDDM	7222293	6137334	Analog Input 63
220	AN62/P41.6	S / HighZ / VDDM	7391295	6184332	Analog Input 62
221	AN61	D / HighZ / VDDM	7222293	6231330	Analog Input 61
222	AN60	D / HighZ / VDDM	7391295	6278328	Analog Input 60
223	AN59	D / HighZ / VDDM	7222293	6325326	Analog Input 59
224	AN58	D / HighZ / VDDM	7391295	6372324	Analog Input 58
225	AN57	D / HighZ / VDDM	7222293	6419322	Analog Input 57
226	AN56	D / HighZ / VDDM	7391295	6466320	Analog Input 56
227	AN55/P41.5	S / HighZ / VDDM	7222293	6513318	Analog Input 55
228	AN54/P41.4	S / HighZ / VDDM	7391295	6560316	Analog Input 54
229	AN53	D / HighZ / VDDM	7222293	6607314	Analog Input 53
230	AN52	D / HighZ / VDDM	7391295	6654312	Analog Input 52
231	AN51	D / HighZ / VDDM	7222293	6701310	Analog Input 51
232	AN50	D / HighZ / VDDM	7391295	6748308	Analog Input 50
233	AN49	D / HighZ / VDDM	7222293	6795306	Analog Input 49
234	AN48	D / HighZ / VDDM	7391295	6842304	Analog Input 48
235	AN31	D / HighZ / VDDM	7391295	6936300	Analog Input 31
236	AN30	D / HighZ / VDDM	7302141	7058295	Analog Input 30
237	AN29/P40.14	S / HighZ / VDDM	7208145	7058295	Analog Input 29
238	AN28/P40.13	S / HighZ / VDDM	7161147	6889293	Analog Input 28

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
239	AN27/P40.3	S / HighZ / VDDM	7114149	7058295	Analog Input 27
240	AN26/P40.2	S / HighZ / VDDM	7067151	6889293	Analog Input 26
241	AN25/P40.1	S / HighZ / VDDM	7020153	7058295	Analog Input 25
242	AN24/P40.0	S / HighZ / VDDM	6973155	6889293	Analog Input 24
243	AN23	D / HighZ / VDDM	6926157	7058295	Analog Input 23
244	AN22	D / HighZ / VDDM	6879159	6889293	Analog Input 22
245	AN21	D / HighZ / VDDM	6832161	7058295	Analog Input 21
246	AN20	D / HighZ / VDDM	6785163	6889293	Analog Input 20
247	AN19/P40.12	S / HighZ / VDDM	6738165	7058295	Analog Input 19
248	AN18/P40.11	S / HighZ / VDDM	6691167	6889293	Analog Input 18
249	AN17/P40.10	S / HighZ / VDDM	6644169	7058295	Analog Input 17
250	AN16	D / HighZ / VDDM	6597171	6889293	Analog Input 16
251	AN15	D / HighZ / VDDM	6550173	7058295	Analog Input 15
252	VAGND1	Vx	6503175	6889293	Supply Voltage
253	VAGND0	Vx	6456177	7058295	Supply Voltage
254	VAREF1	Vx	6409179	6889293	Supply Voltage
255	VAREF0	Vx	6362181	7058295	Supply Voltage
256	AN14	D / HighZ / VDDM	6315183	6889293	Analog Input 14
257	AN13	D / HighZ / VDDM	6268185	7058295	Analog Input 13
258	VDDM	Vx	6221187	6889293	Supply Voltage
259	VSSM	Vx	6174189	7058295	Supply Voltage
260	AN12	D / HighZ / VDDM	6127191	6889293	Analog Input 12
261	VSSM	Vx	6080193	7058295	Supply Voltage
262	VDDM	Vx	6033195	6889293	Supply Voltage
263	AN11	D / HighZ / VDDM	5986197	7058295	Analog Input 11

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
264	AN10	D / HighZ / VDDM	5939199	6889293	Analog Input 10
265	AN9	D / HighZ / VDDM	5892201	7058295	Analog Input 9
266	AN8	D / HighZ / VDDM	5845203	6889293	Analog Input 8
267	AN7	D / HighZ / VDDM	5798205	7058295	Analog Input 7
268	AN6	D / HighZ / VDDM	5751207	6889293	Analog Input 6
269	AN5	D / HighZ / VDDM	5704209	7058295	Analog Input 5
270	AN4	D / HighZ / VDDM	5657211	6889293	Analog Input 4
271	AN3	D / HighZ / VDDM	5610213	7058295	Analog Input 3
272	AN2	D / HighZ / VDDM	5563215	6889293	Analog Input 2
273	AN1	D / HighZ / VDDM	5516217	7058295	Analog Input 1
274	AN0	D / HighZ / VDDM	5469219	6889293	Analog Input 0
276	VSS	Vx	5386005	7058295	Supply Voltage
277	VDD	Vx	5310405	6889293	Supply Voltage
278	VDD	Vx	5234805	7058295	Supply Voltage
279	VSS	Vx	5140809	7058295	Supply Voltage
280	VEXT	Vx	4961709	6889293	Supply Voltage
281	P32.1	SLOW / PU1 / VEXT / ES	4914711	7058295	General-purpose I/O
282	VGATE1P	Vx	4867713	6889293	DCDC P ch. MOSFET gate driver output
283	VSS	Vx	4802715	7058295	Supply Voltage
284	VGATE1N	Vx	4737717	6889293	DCDC N ch. MOSFET gate driver output
285	P32.0	SLOW / PU1 / VEXT / ES	4690719	7058295	General-purpose I/O
286	VEVRSB	Vx	4607505	6889293	Supply Voltage
287	VEVRSB	Vx	4560507	7058295	Supply Voltage
288	P33.1	SLOW / PU1 / VEVRSB / ES5	4513509	6889293	General-purpose I/O
289	VSS	Vx	4466511	7058295	Supply Voltage

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
290	VSS	—	4354515	7058295	Supply Voltage
291	VDD	—	4307517	6889293	Supply Voltage
292	P33.0	SLOW / PU1 / VEVRSB / ES5	4260519	7058295	General-purpose I/O
293	P33.3	SLOW / PU1 / VEVRSB / ES5	4213521	6889293	General-purpose I/O
294	P33.2	SLOW / PU1 / VEVRSB / ES5	4166523	7058295	General-purpose I/O
295	P33.5	SLOW / PU1 / VEVRSB / ES5	4119525	6889293	General-purpose I/O
296	VSS	Vx	4016925	7058295	Supply Voltage
297	VDD	Vx	3969927	6889293	Supply Voltage
298	P34.1	SLOW / PU1 / VEVRSB / ES5	3922929	7058295	General-purpose I/O
299	P33.4	SLOW / PU1 / VEVRSB / ES5	3875931	6889293	General-purpose I/O
300	P34.3	SLOW / PU1 / VEVRSB / ES	3828933	7058295	General-purpose I/O
301	P33.7	SLOW / PU1 / VEVRSB / ES5	3781935	6889293	General-purpose I/O
302	P34.2	SLOW / PU1 / VEVRSB / ES	3734937	7058295	General-purpose I/O
303	P33.6	SLOW / PU1 / VEVRSB / ES5	3687939	6889293	General-purpose I/O
304	P34.5	FAST / PU1 / VEVRSB / ES	3640941	7058295	General-purpose I/O
305	P33.9	SLOW / PU1 / VEVRSB / ES5	3593943	6889293	General-purpose I/O
306	VEVRSB	Vx	3546945	7058295	Supply Voltage
307	P33.8	FAST / HighZ / VEVRSB	3499947	6889293	General-purpose I/O
308	P34.4	SLOW / PU1 / VEVRSB / ES	3452949	7058295	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
309	P33.11	FAST / PU1 / VEVRSB / ES5	3405951	6889293	General-purpose I/O
310	VSS	Vx	3303153	7058295	Supply Voltage
311	VDD	Vx	3256155	6889293	Supply Voltage
312	VSS	Vx	3209157	7058295	Supply Voltage
313	P33.10	FAST / PU1 / VEVRSB / ES5	3162159	6889293	General-purpose I/O
314	P33.15	SLOW / PU1 / VEVRSB / ES5	3115161	7058295	General-purpose I/O
315	P33.13	FAST / PU1 / VEVRSB / ES5	3068163	6889293	General-purpose I/O
316	P33.14	FAST / PU1 / VEVRSB / ES5	3021165	7058295	General-purpose I/O
317	P33.12	FAST / PU1 / VEVRSB / ES5	2974167	6889293	General-purpose I/O
318	VDD	—	2890953	7058295	Supply Voltage
319	VSS	—	2796957	7058295	Supply Voltage
320	P32.2	SLOW / PU1 / VEXT / ES	2721357	6889293	General-purpose I/O
321	P32.5	SLOW / PU1 / VEXT / ES	2674359	7058295	General-purpose I/O
322	P32.4	FAST / PU1 / VEXT / ES	2627361	6889293	General-purpose I/O
323	VSS	Vx	2580363	7058295	Supply Voltage
324	VEXT	Vx	2533365	6889293	Supply Voltage
325	P32.3	SLOW / PU1 / VEXT / ES	2486367	7058295	General-purpose I/O
326	P32.7	SLOW / PU1 / VEXT / ES	2439369	6889293	General-purpose I/O
327	VSS	Vx	2363769	7058295	Supply Voltage
328	P32.6	SLOW / PU1 / VEXT / ES	2288169	6889293	General-purpose I/O
329	VDD	Vx	2212569	7058295	Supply Voltage
330	P31.1	FAST / PU1 / VEXT / ES	2136969	6889293	General-purpose I/O
331	P31.0	FAST / PU1 / VEXT / ES	2089971	7058295	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
332	P31.3	FAST / PU1 / VEXT / ES	2042973	6889293	General-purpose I/O
333	P31.2	FAST / PU1 / VEXT / ES	1995975	7058295	General-purpose I/O
334	P31.4	FAST / PU1 / VEXT / ES	1948977	6889293	General-purpose I/O
335	P31.5	FAST / PU1 / VEXT / ES	1901979	7058295	General-purpose I/O
336	P31.6	FAST / PU1 / VEXT / ES	1854981	6889293	General-purpose I/O
337	P31.7	FAST / PU1 / VEXT / ES	1807983	7058295	General-purpose I/O
338	P31.8	FAST / PU1 / VEXT / ES	1760985	6889293	General-purpose I/O
339	P31.10	FAST / PU1 / VEXT / ES	1713987	7058295	General-purpose I/O
340	P31.9	FAST / PU1 / VEXT / ES	1666989	6889293	General-purpose I/O
341	P31.12	FAST / PU1 / VEXT / ES	1619991	7058295	General-purpose I/O
342	P31.11	FAST / PU1 / VEXT / ES	1572993	6889293	General-purpose I/O
343	P31.14	FAST / PU1 / VEXT / ES	1525995	7058295	General-purpose I/O
344	P31.13	FAST / PU1 / VEXT / ES	1478997	6889293	General-purpose I/O
345	VDD	Vx	1403397	7058295	Supply Voltage
346	VSS	Vx	1309401	7058295	Supply Voltage
347	P31.15	FAST / PU1 / VEXT / ES	1233801	6889293	General-purpose I/O
348	P30.2	FAST / PU1 / VEXT / ES	1186803	7058295	General-purpose I/O
349	P30.0	FAST / PU1 / VEXT / ES	1139805	6889293	General-purpose I/O
350	VSS	Vx	1092807	7058295	Supply Voltage
351	P30.1	FAST / PU1 / VEXT / ES	1045809	6889293	General-purpose I/O
352	VEXT	Vx	998811	7058295	Supply Voltage
353	P30.3	FAST / PU1 / VEXT / ES	951813	6889293	General-purpose I/O
354	P30.5	FAST / PU1 / VEXT / ES	904815	7058295	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
355	P30.4	FAST / PU1 / VEXT / ES	857817	6889293	General-purpose I/O
356	P30.8	FAST / PU1 / VEXT / ES	810819	7058295	General-purpose I/O
357	VDD	Vx	763821	6889293	Supply Voltage
358	VSS	Vx	716823	7058295	Supply Voltage
359	VDD	Vx	614223	6889293	Supply Voltage
360	VSS	Vx	538623	7058295	Supply Voltage
361	P30.6	FAST / PU1 / VEXT / ES	463023	6889293	General-purpose I/O
362	P30.9	FAST / PU1 / VEXT / ES	357795	7058295	General-purpose I/O
363	P30.7	FAST / PU1 / VEXT / ES	263799	7058295	General-purpose I/O
369	P30.10	FAST / PU1 / VEXT / ES	179145	6973641	General-purpose I/O
370	P30.11	FAST / PU1 / VEXT / ES	179145	6879645	General-purpose I/O
371	P30.14	FAST / PU1 / VEXT / ES	348147	6828147	General-purpose I/O
372	P30.15	FAST / PU1 / VEXT / ES	179145	6781149	General-purpose I/O
373	P30.13	FAST / PU1 / VEXT / ES	348147	6734151	General-purpose I/O
374	P30.12	FAST / PU1 / VEXT / ES	179145	6687153	General-purpose I/O
375	P26.0	SLOW / PU1 / VEXT / ES	348147	6640155	General-purpose I/O
376	P25.0	FAST / PU1 / VEXT / ES	179145	6593157	General-purpose I/O
377	P23.0	SLOW / PU1 / VEXT / ES	348147	6546159	General-purpose I/O
378	P23.1	FAST / PU1 / VEXT / ES	179145	6499161	General-purpose I/O
379	P23.2	SLOW / PU1 / VEXT / ES	348147	6443163	General-purpose I/O
380	P25.2	FAST / PU1 / VEXT / ES	179145	6396165	General-purpose I/O
381	P23.3	SLOW / PU1 / VEXT / ES	348147	6349167	General-purpose I/O
382	P25.1	FAST / PU1 / VEXT / ES	179145	6302169	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
383	VEXT	Vx	348147	6255171	Supply Voltage
384	P25.4	FAST / PU1 / VEXT / ES	179145	6208173	General-purpose I/O
385	VSS	Vx	348147	6161175	Supply Voltage
386	P23.5	FAST / PU1 / VEXT / ES	179145	6114177	General-purpose I/O
387	P23.6	SLOW / PU1 / VEXT / ES	348147	6067179	General-purpose I/O
388	P23.7	SLOW / PU1 / VEXT / ES	179145	6020181	General-purpose I/O
389	P25.3	FAST / PU1 / VEXT / ES	348147	5973183	General-purpose I/O
390	P22.4	SLOW / PU1 / VEXT / ES	179145	5926185	General-purpose I/O
391	P25.7	FAST / PU1 / VEXT / ES	348147	5879187	General-purpose I/O
392	P25.5	FAST / PU1 / VEXT / ES	179145	5832189	General-purpose I/O
393	P25.8	FAST / PU1 / VEXT / ES	348147	5785191	General-purpose I/O
394	P25.9	FAST / PU1 / VEXT / ES	179145	5738193	General-purpose I/O
395	P25.10	FAST / PU1 / VEXT / ES	348147	5691195	General-purpose I/O
396	P22.5	SLOW / PU1 / VEXT / ES	179145	5644197	General-purpose I/O
397	P25.11	FAST / PU1 / VEXT / ES	348147	5588199	General-purpose I/O
398	VSS	Vx	179145	5512599	Supply Voltage
399	VDD	Vx	348147	5436999	Supply Voltage
400	P25.12	FAST / PU1 / VEXT / ES	179145	5390001	General-purpose I/O
401	P23.4	FAST / PU1 / VEXT / ES	348147	5343003	General-purpose I/O
402	P25.14	FAST / PU1 / VEXT / ES	179145	5296005	General-purpose I/O
403	P25.13	FAST / PU1 / VEXT / ES	348147	5249007	General-purpose I/O
404	P25.15	FAST / PU1 / VEXT / ES	179145	5202009	General-purpose I/O
405	P25.6	FAST / PU1 / VEXT / ES	348147	5155011	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
406	P24.1	FAST / PU1 / VEXT / ES	179145	5108013	General-purpose I/O
407	P24.0	FAST / PU1 / VEXT / ES	348147	5061015	General-purpose I/O
408	P24.3	FAST / PU1 / VEXT / ES	179145	5014017	General-purpose I/O
409	P24.2	FAST / PU1 / VEXT / ES	348147	4967019	General-purpose I/O
410	P24.5	FAST / PU1 / VEXT / ES	179145	4920021	General-purpose I/O
411	P24.4	FAST / PU1 / VEXT / ES	348147	4873023	General-purpose I/O
412	VEXT	Vx	179145	4826025	Supply Voltage
413	VSS	Vx	348147	4779027	Supply Voltage
414	P22.7	SLOW / PU1 / VEXT / ES	179145	4732029	General-purpose I/O
415	P24.9	FAST / PU1 / VEXT / ES	348147	4685031	General-purpose I/O
416	P22.6	SLOW / PU1 / VEXT / ES	179145	4638033	General-purpose I/O
417	P24.8	FAST / PU1 / VEXT / ES	348147	4591035	General-purpose I/O
418	P22.8	SLOW / PU1 / VEXT / ES	179145	4544037	General-purpose I/O
419	P22.2	LVDS_TX / FAST / PU1 / VEXT / ES6	348147	4432536	General-purpose I/O
420	P22.3	LVDS_TX / FAST / PU1 / VEXT / ES6	348147	4338540	General-purpose I/O
421	VDD	Vx	179145	4227039	Supply Voltage
422	P22.0	LVDS_TX / FAST / PU1 / VEXT / ES6	348147	4115538	General-purpose I/O
423	P22.1	LVDS_TX / FAST / PU1 / VEXT / ES6	348147	4021542	General-purpose I/O
424	VSS	Vx	179145	3910041	Supply Voltage
425	P24.6	FAST / PU1 / VEXT / ES	348147	3834441	General-purpose I/O
426	P24.7	FAST / PU1 / VEXT / ES	179145	3787443	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
427	P24.11	FAST / PU1 / VEXT / ES	348147	3740445	General-purpose I/O
428	VSS	Vx	179145	3664845	Supply Voltage
429	VDD	Vx	348147	3570849	Supply Voltage
430	P24.10	FAST / PU1 / VEXT / ES	179145	3495249	General-purpose I/O
432	VDD	Vx	348147	3406041	Supply Voltage
433	VSS	Vx	179145	3359043	Supply Voltage
434	XTAL1	XTAL / VEXT	179145	3199392	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
435	XTAL2	XTAL / VEXT	179145	3105396	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
436	VSS	—	179145	2945745	Supply Voltage
437	VEXT	Vx	348147	2898747	Supply Voltage
439	P24.13	FAST / PU1 / VEXT / ES	348147	2764233	General-purpose I/O
440	P22.11	SLOW / PU1 / VEXT / ES	179145	2717235	General-purpose I/O
441	P24.12	FAST / PU1 / VEXT / ES	348147	2670237	General-purpose I/O
442	P22.10	SLOW / PU1 / VEXT / ES	179145	2623239	General-purpose I/O
443	P24.15	FAST / PU1 / VEXT / ES	348147	2576241	General-purpose I/O
444	P22.9	SLOW / PU1 / VEXT / ES	179145	2529243	General-purpose I/O
445	P24.14	FAST / PU1 / VEXT / ES	348147	2482245	General-purpose I/O
446	$\overline{\text{TRST}}$	FAST / PU2 / VEXT	179145	2435247	JTAG Module Reset/Enable Input
447	P21.0	LVDS_RX / FAST / PU1 / VEXT / ES	348147	2360196	General-purpose I/O
448	P21.1	LVDS_RX / FAST / PU1 / VEXT / ES	348147	2266200	General-purpose I/O
449	VDD	Vx	179145	2191149	Supply Voltage

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
450	P21.2	LVDS_RX / FAST / PU1 / VEXT / ES	348147	2116098	General-purpose I/O
451	P21.3	LVDS_RX / FAST / PU1 / VEXT / ES	348147	2022102	General-purpose I/O
452	VSS	Vx	179145	1947051	Supply Voltage
453	P21.4	LVDS_TX / FAST / PU1 / VEXT / ES6	348147	1835550	General-purpose I/O
454	P21.5	LVDS_TX / FAST / PU1 / VEXT / ES6	348147	1741554	General-purpose I/O
455	VDD	Vx	348147	1630053	Supply Voltage
456	VSS	Vx	179145	1554453	Supply Voltage
457	VSS	Vx	348147	1460457	Supply Voltage
458	VEXT	Vx	179145	1413459	Supply Voltage
459	P20.0	FAST / PU1 / VEXT / ES	348147	1366461	General-purpose I/O
460	TCK	FAST / PD2 / VEXT	179145	1319463	JTAG Module Clock Input
461	P20.2	S / PU / VEXT	348147	1272465	General-purpose I/O This pin is latched at power on reset release to enter test mode.
462	TMS	FAST / PD2 / VEXT	179145	1225467	JTAG Module State Machine Control Input
463	P20.3	SLOW / PU1 / VEXT / ES	348147	1178469	General-purpose I/O
464	P21.7/TDO	FAST / PU2 / VEXT / ES4	179145	1131471	General-purpose I/O
465	P20.1	SLOW / PU1 / VEXT / ES	348147	1084473	General-purpose I/O
466	VEXT	Vx	179145	1037475	Supply Voltage
467	P20.8	FAST / PU1 / VEXT / ES	348147	990477	General-purpose I/O
468	VSS	Vx	179145	943479	Supply Voltage
469	P20.7	FAST / PU1 / VEXT / ES	348147	896481	General-purpose I/O
470	VDD	Vx	179145	820881	Supply Voltage
471	P20.11	FAST / PU1 / VEXT / ES	348147	745281	General-purpose I/O

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Table 2-44 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
472	P21.6/TDI	FAST / PD / PU2 / VEXT / ES3	179145	698283	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
473	P20.10	FAST / PU1 / VEXT / ES	348147	651285	General-purpose I/O
474	VSS	Vx	179145	575685	Supply Voltage
475	P20.13	FAST / PU1 / VEXT / ES	348147	500085	General-purpose I/O
476	$\overline{\text{PORST}}$	PORST / PD / VEXT	179145	451791	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
477	P20.12	FAST / PU1 / VEXT / ES	179145	357795	General-purpose I/O
478	P20.6	SLOW / PU1 / VEXT / ES	179145	263799	General-purpose I/O

Whenever in table of section 3 'Electrical Specification' the term 'neighbor pads' is used, the detailed definition is provided by **Figure 2-44**. This statement is also valid for next/nearest neighbor pads.

In order to find out who is affecting operation on a target pad (interfering) a number of active close-neighbor pads (ACNP) has to be defined.

Finding close-neighbor pads.

The Pad Ring has four edges: bottom, left, top, right. Each edge is limited, i.e. it has two ends.

Each pad has two direct (first) neighbors unless it is located at the end of the edge. In that case it only has one neighbor. Similarly, each pad has two indirect (second) neighbors unless it or its first neighbor is located at the end of the edge. These first and second neighbors we will collectively call Close-Neighbor pads. Therefore each pad has 2 to 4 close-neighbor pads.

Finding close-neighbors can be done with the following sequence:

1.) Choose a target pad and lookup its "X" and "Y" coordinates in table **Figure 2-44**.

2.) Find first and second neighbors by calculating "X" and "Y" distance from the selected pad. **Figure 2-44** is sorted by "Y" coordinate, which might help locate the 4 close-neighbor candidates (if the pad is near the edge, it might end up with less than 4 close-neighbors).

Defining active pads:

Pad is active if it is currently in use and if it doesn't have "Vxx" in the name.

Figuring out number of active close-neighbor pads follow next rules:

- If the first neighbor is active, then we count it and also check if second neighbor (on the same side of selected pad) is active.

- If the first neighbor is not active, then we do not check the second on the same side.

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2.4 Legend

The data in this chapter 2 match with the file TC38xpd_IO_Spirit_v1.0.0.1.21.xml.

Column “Ctrl.”:

I = Input (for GPIO port lines with IOCR bit field Selection PCx = $0XXX_B$)

O = Output (for GPIO port lines the ´O´ represents in most cases the port HWOUT function)

O0 = Output with IOCR bit field selection PCx = $1X000_B$

O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)

O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)

O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)

O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)

O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)

O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)

O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Column “Buffer Type”:

RFAST = Pad class RFAST (5V/3.3V)

FAST = Pad class FAST (5V/3.3V)

SLOW = Pad class SLOW (5V/3.3V)

LVDS_TX = Pad class LVDS Transmit

LVDS_RX = Pad class LVDS Receive

S = Pad class S (Analog Input overlayed with General Purpose Input)

D = Pad class D (Analog Input)

Porst = Porst input Pad

XTAL1 = XTAL1 input Pad

XTAL2 = XTAL2 input Pad

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)

PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1)]

PU2 = with pull-up device connected during startup and reset, HighZ in Standby mode

PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)

PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1)]

PD2 = with pull-down device connected during startup and reset, HighZ in Standby mode

OD = open drain during reset ($\overline{\text{PORST}}$ = 0)

ES = Supports Emergency Stop

ES1 = ES. ES can be overruled by VADC, control via P00_PCSR

ES2 = ES. ES can be overruled by DXCPL - DAP over CAN physical layer, No overruling for DXCM - Debug over CAN message

ES3 = ES. ES can be overruled by JTAG mode if this pin is used as TDI

ES4 = ES. ES can be overruled by JTAG or Three Pin DAP mode

1) The default state of GPIOs (Px.y) during and after PORST active is controllled via HWCFG6 (P14.4). Pls. see also chapter PMS, HWCFG[6].

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ES5 = ES. ES can be overruled by the Standby Controller - SCR - if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR

ES6 = ES. On LVDS TX pads the ES affects the pads only in CMOS mode, not in LVDS mode. Thus, only when LPCRx.TX_EN selects the CMOS Mode, the output is switched off in the ES event

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3 Electrical Specification

3.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC38x and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC38x and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must be provided by the microcontroller system in which the TC38x designed in.

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3.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the Operational Conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	150	°C	upto 65h @ T_J = 150°C
Voltage at V_{DD} power supply pins with respect to V_{SS} 1) 2)	V_{DD} SR	-	-	1.65	V	upto 2.8h
		-	-	1.45	V	upto 72h
Voltage at V_{DDP3} power supply pins with respect to V_{SS}	V_{DDP3} SR	-	-	4.43	V	
Voltage at V_{DDM}, V_{EXT}, V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}	V_{DDM} SR	-	-	6.75	V	upto 2.8h
		-	-	5.6	V	upto 72h
Voltage on all analog and class S input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Voltage on all other input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Input current on any pin during overload condition 4) 5)	I_{IN} SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition. 4)	ΣI_{IN} SR	-100	-	100	mA	

1) Valid for cumulated for up to 2.8h and pulse forms followed a power supply switch on phase, where the rise and fall times are related to the system capacities and coils.

2) Due to EVRC output voltage oscillation during switch off phase V_{DD} can drop down to -0.72V. For V_{DD} an input level down to -0.72V during switch off phase will not cause any damage or reliability problem.

3) Voltages below V_{INmin} have no Impact to the device reliability as Long as the times and currents defined in section Pin Reliability in Overload for the affected pad(s) are not violated.

4) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.

5) The specified min. and max. values represent the current limits, which have to be maintained, in case of a short circuit condition on the output of any Fast, RFast, Slow and Class S pad, not being used during operation.
This covers also output currents due to switching in operation for C_L=200pF.

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3.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- allowed time interval (defined in Note column) for overload condition is not exceeded. If no time limit is defined the allowed time includes both ‘Operation Lifetime hours’ and ‘Inactive Lifetime hours’. The number of hours in **Table 3-68** and **Table 3-69** are examples only and the applicable numbers are defined by the customer profiles accepted by Infineon.
- **Operating Conditions** are met for
  - pad supply levels
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Table 3-2 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	except LVDS pins
		-15 [1]	-	15 [1]	mA	except LVDS pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-3	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	V_{SS} - 2	-	$V_{EXT/FLEX}$ + 2	V	limited to 60h over lifetime; Valid for non LVDS and analoge pads
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	I_{OUT} CC	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong

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Table 3-2 Overload Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for digital inputs, negative	K_{OVDN} CC	-	-	$3*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor fast pads; -5mA < I_{IN} < 0mA
		-	-	$2*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads VGASTE1N and VGATE1P; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; -5mA < I_{IN} < 0mA
		-	-	0.8		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	0.5		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for digital inputs, positive	K_{OVDP} CC	-	-	$1.5*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	$5*10^{-3}$		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for analog inputs, negative [2)]	K_{OVAN} CC	-	-	$1*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-5}$		else; -5mA < I_{IN} < 0mA

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Table 3-2 Overload Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, positive [2]	K_{OVAP} CC	-	-	$2*10^{-4}$		Analoge inputs overlaid with slow pads or pull down diagnostics; 0mA < I_{IN} < 5mA
		-	-	$2*10^{-5}$		else; 0mA < I_{IN} < 5mA

1) Reduced VADC / DSADC result accuracy and / or GPIO input levels (V_{IL} and V_{IH}) can differ from specified parameters.

2) Overload coupling on analog inputs is caused by parasitic effects between pads, input multiplexers and surrounding structures. The given parameters have been verified for all permutations of channels. Also watch multiple connections of a pin to several channels.

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3.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC38x. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC38x must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise noticed in the Note / Test Condition column.

Table 3-3 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	f_{SRI} SR	-	-	300	MHz	
CPU Frequency (All CPUs)	f_{CPUx} SR	-	-	300	MHz	
PLL0 output frequency	f_{PLL0} SR	20	-	300	MHz	
SPB frequency	f_{SPB} SR	-	-	100	MHz	
FSI2 frequency	f_{FSI2} SR	-	-	300	MHz	
FSI frequency	f_{FSI} SR	20	-	100	MHz	
GTM frequency	f_{GTM} SR	-	-	200	MHz	
STM frequency	f_{STM} SR	-	-	100	MHz	
ERAY frequency	f_{ERAY} SR	-	80	-	MHz	
VADC frequency	f_{ADC} SR	-	-	160	MHz	
ASCLIN Operating Frequency	$f_{ASCLINx}$ SR	-	-	200	MHz	
CAN frequency	f_{CAN} SR	-	-	80	MHz	
I2C frequency	f_{I2C} SR	-	-	100	MHz	
Operating MSC Frequency	f_{MSC} SR	-	-	200	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} SR	20	-	320	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} SR	20	-	200	MHz	
QSPI Frequency	f_{QSPI} SR	-	-	200	MHz	
ADAS clock frequency	f_{ADAS} CC	200	-	300	MHz	
MCANH frequency	f_{MCANH} CC	-	-	100	MHz	
GETH frequency	f_{GETH} CC	100	-	150	MHz	
Ambient Temperature	T_A SR	-40	-	125	°C	valid for all SAK products
		-40	-	150	°C	valid for all SAL products with package
		-40	-	170	°C	valid for all SAL products without package

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Table 3-3 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction Temperature	T_J SR	-40	-	150	°C	valid for all SAK products
		-40	-	170	°C	valid for all SAL products
Core Supply Voltage	V_{DD} SR	1.125 [1]	1.25	1.375 [2]	V	
ADC analog supply voltage	V_{DDM} SR	2.97	5.0	5.5 [3]	V	
Digital external supply voltage for pads and EVR	V_{EXT} SR	4.5	5.0	5.5 [3]	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid.
		2.97	3.3	3.63	V	Nominal 3.3V Pad / Port Pin supply range with VDDP3 supplied externally and EVR33 inactive. 3.3V pad parameters are valid.
		3.6	-	4.5	V	Flash configured in cranking mode; Flash read operation with reduced performance. EVR33 active in low voltage mode. 3.3V pad parameters are valid.
		2.97	-	3.6	V	Incase EVR33 is active, Flash configured in sleep mode and execution switched to RAM. 3.3V pad parameters are valid.
Digital supply voltage for Flex port	V_{FLEX} SR	2.97	-	4.0	V	3.3V pad parameters are valid
		4.5	5.0	5.5 [3]	V	5V pad parameters are valid
Digital supply voltage for Flash	V_{DDP3} SR	2.97	3.3	3.63 [4]	V	
		2.6	-	3.63	V	Flash configured in cranking mode; Flash read operation with reduced performance.
Digital ground voltage	V_{SS} SR	0	-	-	V	
Analog ground voltage for V_{DDM}	V_{SSM} CC	-0.1	0	0.1	V	

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Table 3-3 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital external supply voltage for EVR and during Standby mode	V_{EVRSB} SR	2.97 5)	-	5.5	V	
Voltage to ensure defined pad states	V_{DDPPA} CC	1.3 6)	-	-	V	

1) For V_{DD} 1.08V ≤ V_{DD} < 1.125V operation is still possible but with relaxed parameters.
2) Voltage overshoot to 1.69V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
3) Voltage overshoot to 6.5V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
4) Voltage overshoot to 4.29V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
5) V_{EVRSB} supply voltage can drop down upto 2.6V during Standby mode. It is required to have a capictor of 100nF on V_{EVRSB} supply pin.
6) HWCFG[6] pin is latched and pull-up or tristate is activated at Port pins when VEXT has reached this level.

Limitation of Supply Voltage over Time

The maximum operation voltage for $V_{EXT/FLEX/DDM}$ supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-4 Example Voltage Profile

$V_{EXT/FLEX/DDM}$=	Duration [h]
5.4 V < $V_{EXT/FLEX/DDM}$ ≤ 5.5 V	≤ 5% of lifetime
5.15 V < $V_{EXT/FLEX/DDM}$ ≤ 5.4 V	≤ 15% of lifetime
4.85 V < $V_{EXT/FLEX/DDM}$ ≤ 5.15 V	≤ 60% of lifetime
4.6 V < $V_{EXT/FLEX/DDM}$ ≤ 4.85 V	≤ 15% of lifetime
4.5 V < $V_{EXT/FLEX/DDM}$ ≤ 4.6 V	≤ 5% of lifetime

The maximum operation voltage for V_{DD} supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-5 Example Voltage Profile

V_{DD}=	Duration [h]
1.325 V < V_{DD} ≤ 1.375 V	≤ 5% of lifetime
1.275 V < V_{DD} ≤ 1.325 V	≤ 15% of lifetime
1.225 V < V_{DD} ≤ 1.275 V	≤ 60% of lifetime
1.175 V < V_{DD} ≤ 1.225 V	≤ 15% of lifetime
1.125 V < V_{DD} ≤ 1.175V	≤ 5% of lifetime

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3.5 5 V / 3.3 V switchable Pads

Pad classes slow GPIO and fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degrade in TTL operation.

Table 3-6 $\overline{\text{PORST}}$ Pad

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{\text{PORST}}$ pad Output current	I_{PORST} CC	13	-	-	mA	V_{EXT} = 2.97V; V_{PORST} = 0.9V
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	
Spike filter pass-through blocked pulse duration	t_{SF2} CC	260	-	-	ns	without additional PORST Digtial Filter active (PORSTDF = 0).
Input hysteresis [1]	HYS CC	0.055 * V_{EXT}	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
Pull-down current [2]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; TTL (degraded, used for CIF)
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-450	-	450	nA	TJ≤150°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-500	-	500	nA	TJ≤150°C ;else
		-900	-	900	nA	TJ≤170°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-950	-	950	nA	TJ≤170°C ; else
Input high voltage level	V_{IH} SR	1.4	-	-	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		2.0	-	-	V	TTL; V_{EXT} = 4.5V
Input low voltage level	V_{IL} SR	-	-	0.5	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		-	-	0.8	V	TTL; V_{EXT} = 4.5V
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

2) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

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Table 3-7 Fast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time [1) 2)]	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18* C_L	2.5+0.27* C_L	5.0+0.35* C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08* C_L	0.5+0.11* C_L	1.0+0.17* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3)]	HYS CC	0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4)]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [5)]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL

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Table 3-7 Fast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \le 150°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-2500	-	2500	nA	$T_J \le 150°C$; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$) ; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \le 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \le 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \le 150°C$; else
		-2000	-	2000	nA	$T_J \le 170°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-4000	-	4000	nA	$T_J \le 170°C$; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$) ; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \le 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \le 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \le 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.

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3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-8 Fast 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18* C_L	1.5+0.28* C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08 *C_L	0.75+0.11 *C_L	2.5+0.21* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis 3)	HYS CC	0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

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Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \leq 150°C$; else
		-2000	-	2000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \leq 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \leq 170°C$; else

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Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-9 Slow 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
Rise / Fall time 1) 2)	t_{RF} CC	4+0.55*C_L	4+0.75*C_L	12+1*C_L	ns	driver = medium edge = medium ; C_L≤200pF
		1.5+0.25*C_L	2.5+0.40*C_L	7+0.55*C_L	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

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Table 3-9 Slow 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH};AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|130|	µA	V_{IL}; AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-300	-	300	nA	$T_J \le 150°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-400	-	400	nA	$T_J \le 150°C$; else
		-600	-	600	nA	$T_J \le 170°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-750	-	750	nA	$T_J \le 170°C$; else
		-18000	-	18000	nA	P32.0 and P32.1;$T_J \le 150°C$
		-38000	-	38000	nA	P32.0 and P32.1;$T_J \le 170°C$
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL

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Table 3-9 Slow 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-10 Slow 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
Rise / Fall time [1) 2)]	t_{RF} CC	2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium edge = medium ; C_L≤200pF
		2+0.30*C_L	3.5+0.50* C_L	5+0.70*C_L	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3)]	HYS CC	0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

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Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
		|11|	-	-	µA	V_{IH}; TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-300	-	300	nA	T_J ≤ 150°C; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-400	-	400	nA	T_J ≤ 150°C; else
		-600	-	600	nA	T_J ≤ 170°C; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-750	-	750	nA	T_J ≤ 170°C; else
		-18000	-	18000	nA	P32.0 and P32.1;T_J≤150°C
		-38000	-	38000	nA	P32.0 and P32.1;T_J≤170°C
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

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Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-11 RFast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18* C_L	2.5+0.27* C_L	5.0+0.35* C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08* C_L	0.5+0.11* C_L	1.0+0.17* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.5	-	0.5	ns	valid for all data rates excluding clock tolerance

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Table 3-11 RFast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3]	HYS CC	0.09 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \le 150°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-2100	-	2100	nA	$T_J \le 150°C$; else
		-3000	-	3000	nA	$T_J \le 170°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-4000	-	4000	nA	$T_J \le 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * V_{FLEX}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * V_{FLEX}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; V_{FLEX} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.

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5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-12 RFast 3.3V pad

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	8	20	30	Ohm	Driver = RGMII; $I_{OH/OL}$ = 8mA
		125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Input Duty Cycle	f_D SR	47.5	50	52.5		
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		-	-	1	ns	Driver = RGMII; from 20%V to 80%V; C_L=15pF
		2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18* C_L	1.5+0.28* C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08 *C_L	0.75+0.11 *C_L	2.5+0.21* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.4	-	0.4	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

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Table 3-12 RFast 3.3V pad (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.055 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \leq 150°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-2100	-	2100	nA	$T_J \leq 150°C$; else
		-3000	-	3000	nA	$T_J \leq 170°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-4000	-	4000	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * V_{FLEX}	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

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Table 3-12 RFast 3.3V pad (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{FLEX}	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{FLEX} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-13 Class S 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis 1)	HYS CC	0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current 2)	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current 3)	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL

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Table 3-13 Class S 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300	-	300	nA	$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600	-	600	nA	$T_J \leq 170°C$; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
3) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-14 Class S 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	

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Table 3-14 Class S 3.3V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [1]	*HYS* CC	0.055 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		0.065 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL (degraded used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [2]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}
Pull-down current [3]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300	-	300	nA	$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600	-	600	nA	$T_J \leq 170°C$; PDD option available
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

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Table 3-14 Class S 3.3V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
3) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-15 Class D

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300 [1]	-	300 [1]	nA	$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600 [2]	-	600 [2]	nA	$T_J \leq 170°C$; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) For AN11 100 nA need to be added.
2) For AN11 200 nA need to be added.

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Table 3-16 ADC Reference Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	I_{OZ2} CC	-2 [1]	-	2 [1]	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; for EVADC; valid for BGA292
		-7 [1]	-	7 [1]	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EVADC; valid for BGA292
		-4 [1]	-	4 [1]	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; for EVADC; valid for BGA292
		-14 [1]	-	14 [1]	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EVADC; valid for BGA292
		-1 [2]	-	1 [2]	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; for EVADC; valid for BGA516
		-2 [2]	-	2 [2]	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; for EVADC; valid for BGA516
		-3.5 [2]	-	3.5 [2]	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EVADC; valid for BGA516
		-7 [2]	-	7 [2]	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EVADC; valid for BGA516
		-2 [3]	-	2 [3]	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; for EDSADC
		-4 [3]	-	4 [3]	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; for EDSADC
		-6 [3]	-	6 [3]	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EDSADC
		-12 [3]	-	12 [3]	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EDSADC

1) Limit is valid for VAREF2 pin.
2) Limit is valid for VAREF2 and VAREF3 pins each.
3) Limit is valid for VAREF1 pin.

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Table 3-17 Driver Mode Selection for Slow Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium medium edge (m)

Table 3-18 Driver Mode Selection for Fast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Reserved, do not use this combination

Table 3-19 Driver Mode Selection for RFast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	RGMII function active

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3.6 High performance LVDS Pads

This LVDS pad type is used for the high speed chip to chip communication interface of the new TC38x. It compose out of a LVDS pad and a fast pad.

C_L = 2.5 pF for all LVDS parameters.

Table 3-20 LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance	R_0 CC	40	-	140	Ohm	V_{cm} = 1.0 V and 1.4 V
Rise time (20% - 80%)	t_{rise20} CC	-	-	0.75 [1]	ns	Z_L = 100 Ohm ±20% @2pF external load
Fall time (20% - 80%)	t_{fall20} CC	-	-	0.75 [2]	ns	Z_L = 100 Ohm ±20% @2pF external load
Output differential voltage [3]	V_{OD} CC	240	-	330	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=00
		280	-	370	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=01
		320	-	410	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=10
		380	-	500	mV	RT = 100 Ohm ± 1%; LPCRx.VDIFFADJ=11; Multi slave operation
Output voltage high	V_{OH} CC	-	-	1475	mV	RT = 100 Ohm +/- 1% VDIFFADJ=00 and 01
		-	-	1500	mV	RT = 100 Ohm ± 1% VDIFFADJ=10 and 11
Output voltage low	V_{OL} CC	925	-	-	mV	RT = 100 Ohm ± 1% VDIFFADJ=00 and 01
		900	-	-	mV	RT = 100 Ohm +/- 1% VDIFFADJ=10 and 11
Output offset (Common mode) voltage	V_{OS} CC	1125	-	1275	mV	RT = 100 Ohm ± 1%
Input voltage range	V_I SR	0	-	1600	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±10%
		0	-	2400	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±20%
Input differential threshold	V_{idth} SR	-100	-	100	mV	Driver ground potential difference < 900 mV; VDIFFADJ=10 and 11
		-100	-	100	mV	Driver ground potential difference < 925 mV; VDIFFADJ=00 and 01

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Table 3-20 LVDS - IEEE standard LVDS general purpose link (GPL) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receiver differential input impedance	R_{in} CC	80	-	120	Ohm	V_I ≤ 2400 mV
Output differential voltage Sleep Mode 4)	V_{ODSM} CC	-5	-	20	mV	RT = 100 Ohm ± 20%; LPCRx.VDIFFADJ=xx
Delta output impedance	$dR0$ SR	-	-	10	%	V_{cm} = 1.0 V and 1.4 V
Change in VOS between 0 and 1	$dVOS$ CC	-	-	25	mV	R_T = 100 Ohm ±1%
Change in Vod between 0 and 1	$dVod$ CC	-	-	25	mV	R_T = 100 Ohm ±1%
Pad set-up time	t_{SET_LVDS} CC	-	10	13	µs	
Duty cycle	t_{duty} CC	45	-	55	%	

1) t_{rise20} = 0.75ns + (C_L - 2)[pF]*20ps. C_L defines the external load.
2) t_{fall20} = 0.75ns + (C_L - 2)[pF]*20ps. C_L defines the external load.
3) Potential violations of the IEEE Std 1596.3 are intended for the new multislave support feature. To be compliant to IEEE Std 1596.3 LPCRx.VDIFFADJ has to be configured to 01.
4) Common Mode voltage of Tx is maintained.

Note: Driver ground potential difference is defined as driver-receiver potentital difference, that can result in a voltage shift when comparing driver output voltage level and receiver input voltage level of a transmitted signal.

*Note: R_T in table 'LVDS - IEEE standard LVDS general purpose Link (GPL)' is as termination resistor of the receiver according to figure 3-5 in IEEE Std 1596.3-1996 and is represent in **Figure 3-1** either by R_{in} or by R_T=100Ohm but not both. If R_T is mentioned in column Note / Test Condition always the internal resistor R_{in} in **Figure 3-1** is the selected one.*

default after start-up = CMOS function

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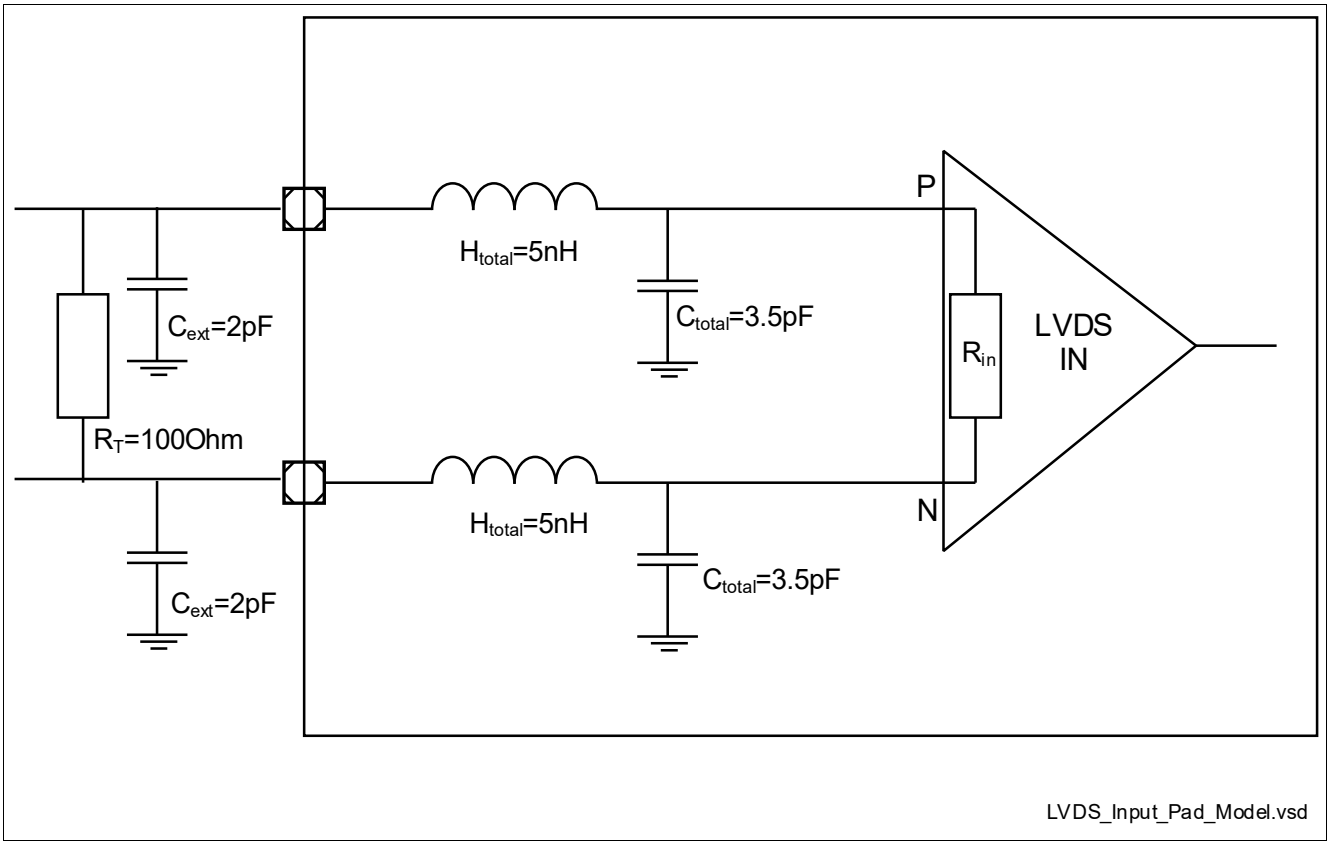

Figure 3-1 LVDS pad Input model

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3.7 VADC Parameters

The accuracy of the converter results depends on the reference voltage range. The parameters in the table below are valid for a reference voltage range of (V_{AREF} - V_{AGND}) >= 4.5 V. If the reference voltage range is below 4.5 V by a factor of k (e.g. 3.3 V), the accuracy parameters increase by a factor of 1.1/k (e.g. 1.1 × 4.5 / 3.3 = 1.5).

Noise on supply voltage V_{DDM} influences the conversion. The accuracy (error) parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).

Digital functions overlapping analog inputs influence accuracy.

The total unadjusted error (TUE) is defined without noise. The overall deviation depends on TUE and EN_{RMS} (depending on the noise distribution). Example: For a noise distribution of 4 sigma and EN_{RMS} = 1.0 the additional peak-peak noise error is ±(4 × 1.0) = 8 LSB_{12}.

Fast compare operations are executed with 10-bit values.

The noise reduction feature improves the result by adding additional conversion steps. The conversion times, therefore, increase accordingly (4 × t_{ADCI} + 3 × t_{ADC} for each of 1, 3, or 7 steps).

Table 3-21 VADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVADC IVR output voltage	V_{DDK} CC	1.15	-	1.35	V	Measured at low temperature.
Deviation of IVR output voltage V_{DDK}	dV_{DDK} CC	-2	-	2	%	Based on device-specific value
Analog reference voltage [1]	V_{AREF} SR	4.5	5.0	V_{DDM} + 0.05	V	4.5 V ≤ V_{DDM} ≤ 5.5 V
		2.97	3.3	V_{DDM} + 0.05	V	2.97 V ≤ V_{DDM} < 4.5 V
Analog reference ground	V_{AGND} SR	V_{SSM}	V_{SSM}	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Converter reference clock	f_{ADCI} SR	16	40	53.33	MHz	4.5 V ≤ V_{DDM} ≤ 5.5 V
		16	20	26.67	MHz	2.97 V ≤ V_{DDM} < 4.5 V
Total Unadjusted Error [2] [3]	TUE CC	-4	-	4	LSB	12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels
INL Error [2]	EA_{INL} CC	-3	-	3	LSB	
DNL error [2][4]	EA_{DNL} CC	-1	-	3	LSB	
Gain Error [2]	EA_{GAIN} CC	-3.5	-	3.5	LSB	
Offset Error [2][3]	EA_{OFF} CC	-4	-	4	LSB	

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Table 3-21 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMS Noise [2)5) 6)]	EN_{RMS} CC	-	0.5	0.8	LSB	Noise reduction level 3
		-	0.5	1.0	LSB	Standard conversion
Reference input charge consumption per conversion (from V_{AREF}) [7) 8) 9)]	Q_{CONV} CC	-	-	20	pC	V_{AIN} = 0 V (worst case), precharging disabled
		-	-	10	pC	V_{AIN} = 0 V (worst case), precharging enabled, V_{DDM} - 5% < V_{AREF} < V_{DDM} + 50 mV
Switched capacitance of an analog input	C_{AINS} CC	-	2.5	3.4	pF	Input buffer disabled
Analog input charge consumption [10)]	Q_{AINS} CC	-	-	3.5	pC	Primary groups and fast compare channels; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J ≤ 150°C
		-	-	3.8	pC	Primary groups and fast compare channels; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J > 150°C
		-	-	4.4	pC	Secondary groups; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J ≤ 150 °C
		-	-	4.8	pC	Secondary groups; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J > 150°C

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Table 3-21 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sampling time	t_S SR	100	-	-	ns	Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled
		300	-	-	ns	Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled
		500	-	-	ns	Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled
		700	-	-	ns	Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled
		200	-	-	ns	Primary Group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled
		400	-	-	ns	Primary group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled
		1000	-	-	ns	Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled
		1200	-	-	ns	Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled
Sampling time for calibration	t_{SCAL} SR	50	-	-	ns	4.5 V ≤ V_{DDM} ≤ 5.5 V
		100	-	-	ns	2.97 V ≤ V_{DDM} < 4.5 V
Input buffer switch-on time	t_{BUF} CC	-	0.4	1	µs	
Wakeup time	t_{WU} CC	-	0.1	0.2	µs	Fast standby mode
		-	1.6	3	µs	Slow standby mode
Broken wire detection delay against V_{AREF}	t_{BWR} CC	-	100	-	cycles	Result above 80% of full scale range, analog input buffer disabled
Broken wire detection delay against V_{AGND}	t_{BWG} CC	-	100	-	cycles	Result below 10% of full scale range, analog input buffer disabled
Converter diagnostics unit resistance [11)]	R_{CSD} CC	45	-	75	kOhm	
Converter diagnostics voltage accuracy	dV_{CSD} CC	-10	-	10	%	Percentage refers to V_{DDM}

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Table 3-21 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the multiplexer diagnostics pull-up device	R_{MDU} CC	30	-	42	kOhm	0 V ≤ V_{IN} ≤ 0.9* V_{DDM}, Automotive Levels
		56	-	78	kOhm	0 V ≤ V_{IN} ≤ 0.9* V_{DDM}, TTL Levels
Resistance of the multiplexer diagnostics pull-down device	R_{MDD} CC	43	-	58	kOhm	0.1*V_{DDM} ≤ V_{IN} ≤ V_{DDM}, Automotive level
		18	-	25	kOhm	0.1*V_{DDM} ≤ V_{IN} ≤ V_{DDM}, TTL level
Resistance of the pull-down test device	R_{PDD} CC	-	-	0.3	kOhm	Measured at pad input voltage V_{IN} = V_{DDM} / 2.

1) These limits apply to the standard reference input as well as to the alternate reference input.
2) Parameter depends on reference voltage range and supply ripple, see introduction.
Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS}.
Tests are done with postcalibration disabled, after completing the startup calibration.
3) Analog inputs mapped to pads of the type SLOW influence accuracy. The values for this parameter increase by 3 LSB_{12}.
4) Monotonic characteristic, no missing codes when calibrated.
5) Parameter EN_{RMS} refers to a 1 sigma distribution.
6) Analog inputs mapped to pads of the type SLOW the RMS noise (EN_{RMS}) can be up to 2 LSB_{12} (soft switching for DC/DC enabled).
7) For reduced reference voltages VAREF < 3.375V, the consumed charge QCONV is reduced by the factor of k2 = VAREF [V] / 3.375. For reduced reference voltages 4.5V < VAREF ≤ 3.375V, QCONV is not reduced.
8) Maximum charge increases by 15 pC when BWD (Broken Wire Detection) is active.
9) Fast compare channels only consume 1/3 of the charge for a primary/secondary group.
10) For analog inputs with overlaid digital GPIOs or with PDD function this value increases by 1 pC.
11) Use a sample time of at least 1.1 µs to enable proper settling of the test voltage.

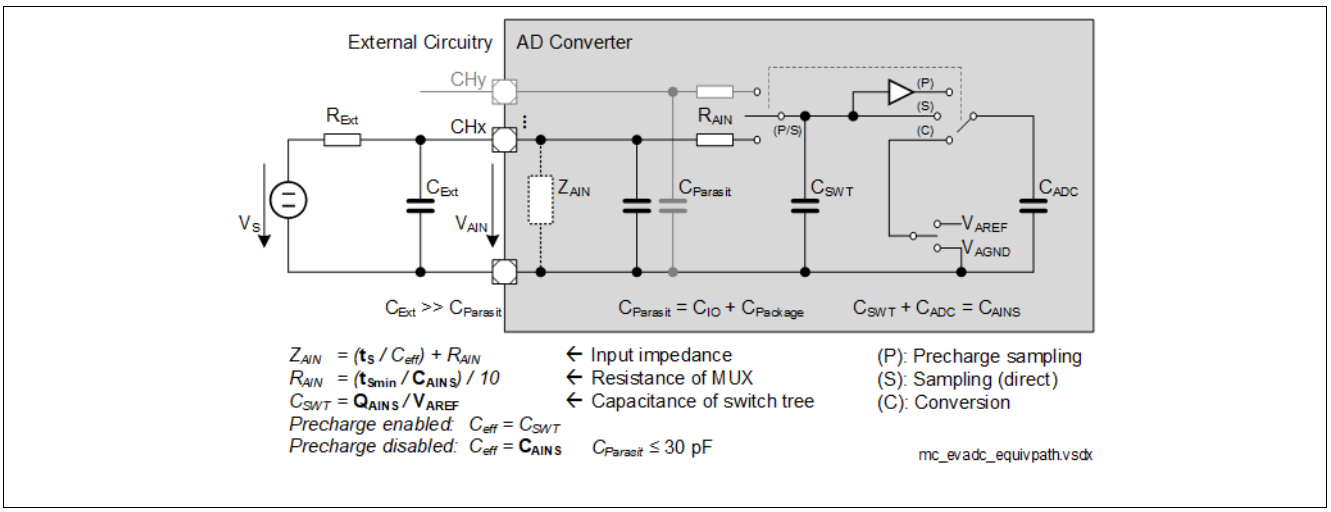

Figure 3-2 Equivalent Circuitry for Analog Inputs

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3.8 DSADC Parameters

The DSADC parameters are valid only for voltage range 4.5 V <= V_{DDM} <= 5.5 V.

These parameters describe the product properties and do not include external circuitry. The values are valid for junction temperatures T_J <= 150°C if not defined explicitly.

Calibration is specified for gain factors 1 and 2, calibrated values refer to these settings.

The signal-noise ratio (SNR) is specified for differential inputs. For single ended operation the resulting signal-noise ratio is reduced by 6 dB. For quasi-differential mode (i.e. using V_{CM}) it is reduced by 6 dB for gain = 1 and by 3 dB for gain= 2.

Table 3-22 DSADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Common mode voltage bias resistance	R_{BIAS} CC	105	130	155	kOhm	On-chip variation ≤ ±2.5%.
Positive reference voltage	V_{AREF} SR	4.5	-	V_{DDM} + 0.05	V	
Reference ground voltage	V_{AGND} SR	V_{SSM}	-	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Reference load current	I_{REF} CC	-	10	12	µA	Per modulator
		-	-	14	µA	Per modulator, T_J>150°C
Common mode voltage accuracy [1]	dV_{CM} CC	-100	-	100	mV	Deviation from selected voltage
Analog input voltage range	V_{DSIN} SR	V_{SSM}	-	2 * V_{DDM}	V	Differential;V_{DSxP} - V_{DSxN}
		V_{SSM}	-	V_{DDM}	V	Single ended
Input current [2]	I_{RMS} CC	7	10	13	µA	Exact value (±1%) available in UCB; valid for gain = 1 and f_{MOD} = 26.7 MHz
On-chip modulator clock frequency	f_{MOD} SR	16	-	40	MHz	
Gain error [3] [4]	ED_{GAIN} CC	-0.2 [5]	±0.1[5]	0.2 [5]	%	T_J≤150°C; Target, calibrated, V_{AREF} constant after calibration; f_{MOD} = 26.67 MHz
		-	±0.25	-	%	T_J>150°C; V_{AREF} constant after calibration; f_{MOD} = 26.67 MHz
		-1	-	1	%	Calibrated once; f_{MOD} = 26.67 MHz
		-2.5	-	2.5	%	Uncalibrated; f_{MOD} = 26.67 MHz

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Table 3-22 DSADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC offset error [3]	ED_{OFF} CC	-5 [5]	-	5 [5]	mV	Calibrated; f_{MOD} = 26.67 MHz
		-10	-	10	mV	Calibrated once; f_{MOD} = 26.67 MHz
		-30	-	30	mV	Uncalibrated; f_{MOD} = 26.67 MHz
Signal-Noise Ratio for differential input signals [2][6][7]	*SNR* CC	80	-	-	dB	T_J≤150°C; f_{PB} = 30 kHz; f_{MOD} = 26.67 MHz
		78	-	-	dB	T_J≤150°C; f_{PB} = 50 kHz; f_{MOD} = 26.67 MHz
		74	-	-	dB	T_J≤150°C; f_{PB} = 100 kHz; f_{MOD} = 26.67 MHz
Signal-Noise Ratio degradation	*DSNR* CC	-	-	3	dB	T_J>150°C; Resulting Signal-Noise Ratio value is SNR - DSNR
Spurious-free dynamic range [3]	*SFDR* CC	60	-	-	dB	f_{MOD} = 26.67 MHz
Output sampling rate	f_D CC	3.906	-	300	kHz	16 MHz / 4096, without integrator
Pass band	f_{PB} CC	1.302	-	100	kHz	Output data rate: f_D = f_{PB} * 3; without integrator
		1.302	-	10	kHz	Output data rate: f_D = f_{PB} * 6; without integrator
Pass band ripple	df_{PB} CC	-0.08	-	0.08	dB	FIR filters enabled
Stop band attenuation	*SBA* CC	40	-	-	dB	0.5 f_D ... 1.0 f_D
		45	-	-	dB	1.0 f_D ... 1.5 f_D
		50	-	-	dB	1.5 f_D ... 2.0 f_D
		55	-	-	dB	2.0 f_D ... 2.5 f_D
		60	-	-	dB	2.5 f_D ... OSR/2 f_D
DC compensation factor	*DCF* CC	-3	-	-	dB	10^{-5} f_D, offset compensation filter enabled (FCFGMx.OCEN = 001_B)
Modulator settling time	t_{MSET} CC	-	-	20	µs	After switching on, voltage regulator already running

1) On pins with overlaid GPIO function the max. limit increases by up to 25 mV due to leakage current for T_J > 150°C.
2) For detailed information, refer to the User Manual chapter.
3) This parameter is valid within the defined range of f_{MOD}.
4) Gain mismatch error between the different EDSADC channels is within ±0.5% if they have the same calibration strategy

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5) Recalibration needed in case of a temperature change >20ºC
6) These values are valid for an analog gain factor of 1. Subtract 3 dB for each higher gain factor.
7) For single ended input signals and gain1, the SNR is reduced by 6 dB.

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3.9 MHz Oscillator

OSC_XTAL is used as accurate and exact clock source. OSC_XTAL supports 16 MHz to 40 MHz crystals external outside of the device. Support of ceramic resonators is also provided.

Table 3-23 OSC_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-70	-	70	µA	V_{IN}>0V ; V_{IN}<V_{EXT}
Oscillator frequency	f_{OSC} SR	4	-	40	MHz	Direct Input Mode selected, if shaper is not bypassed
		16	-	40	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} CC	-	-	3 [1]	ms	20MHz ≤ f_{OSC} and 8pF load capacitance
Input voltage at XTAL1 [2]	V_{IX} SR	-0.7	-	V_{EXT} + 0.5	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	0.3*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} > 25MHz
		0.35*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} ≤ 25MHz
Internal load capacitor	C_{L0} CC	1.30	1.40	1.55	pF	enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} CC	3.05	3.35	3.70	pF	enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} CC	7.85	8.70	9.55	pF	enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} CC	12.05	13.35	14.65	pF	enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	C_{XINTS} CC	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	C_{XTAL1} CC	-	2.5	4	pF	
Duty cycle at XTAL1 [3]	DC_{X1} SR	35	-	65	%	V_{XTAL1} = 0.5*V_{PPX}
Absolute RMS jitter at XTAL1 [3]	J_{ABSX1} SR	-	-	28	ps	10 KHz to f_{OSC}/2
Slew rate at XTAL1 [3]	SR_{XTAL1} SR	0.3	-	-	V/ns	Maximum 30% difference between rising and falling slew rate

1) t_{OSCS} is defined from the moment when the Oscillator Mode is set to External Crystal Mode until the oscillations reach an amplitude at XTAL1 of 0.3 * VEXT.
This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decrease.

2) For Supply (V_{EXT} < 5.3V V_{IX}) min could be down to -0.9V. For XTAL1 an input level down to -0.9V will not cause a damage or a reliability problem operating with an external crystal.

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3) Square wave input signal for XTAL1.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

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3.10 Back-up Clock

The back-up clock provides an alternative clock source.

Table 3-24 Back-up Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock accuracy before trimming	f_{BACKUT} CC	70	100	130	MHz	V_{EXT}≥2.97V
Back-up clock accuracy after trimming [1]	f_{BACKT} CC	98	100	102	MHz	V_{EXT}≥2.97V
Standby clock	f_{SB} CC	25	70	110	kHz	V_{EXT}≥2.97V

1) A short term trimming providing the accuracy required by LIN communication is possible by periodic trimming every 2 ms for temperature and voltage drifts up to temperatures of 125 celcius

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3.11 Temperature Sensor

Table 3-25 DTS PMS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion 1)	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Calibration reference accuracy	T_{CALACC} CC	-1	-	1	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

Table 3-26 DTS Core

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion 1)	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Temperature difference between on chip temperature sensors	ΔT CC	-3	-	3	°C	
Calibration reference accuracy	T_{CALACC} CC	-2	-	2	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

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3.12 Power Supply Current

The total power supply current defined below consists of leakage and switching components.

Application relevant values are typically lower than those given in the following table and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

The real (realistic) power pattern defines the following conditions:

- T_J = 150 °C
- f_{SRI} = f_{CPUx} = 300 MHz
- f_{GTM} = 200 MHz
- f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = $f_{ASCLINx}$ = 100 MHz
- V_{DD} = 1.275 V
- $V_{DDP3/FLEX}$ = 3.366 V
- $V_{EXT\ /\ EVRSB}$ = V_{DDM} = 5.1 V
- all cores are active including two lockstep cores
- the following peripherals are inactive: HSM, HSCT, Ethernet, PSI5, I2C, FCE, and MTU

Table 3-27 Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DD} core and peripheral supply currents (incl. $I_{DDPORST}$+ ∑ I_{DDCx0}+ ∑ I_{DDCxx}+ I_{DDGTM}+I_{DDSB})	I_{DDRAIL} CC	-	-	1100	mA	max power pattern
		-	-	840	mA	real power pattern
I_{DD} core current during active power-on reset (PORST pin held low). Leakage current of core domain. [1]	$I_{DDPORST}$ CC	-	-	160	mA	V_{DD} = 1.275V; T_J=125°C
		-	-	290	mA	V_{DD} = 1.275V; T_J=150°C
		-	-	350	mA	V_{DD} = 1.275V; TJ=160°C
		-	-	380	mA	V_{DD} = 1.275V; T_J=165°C
∑ Sum of I_{DDP3} 3.3 V supply currents	$I_{DDP3RAIL}$ CC	-	-	50	mA	max power pattern incl. Flash read current and Dflash programming current.
		-	-	40 [2]	mA	real power pattern incl. Flash read current and Dflash programming current.
∑ Sum of external I_{EXT} supply currents (incl. $I_{EXTFLEX}$+I_{EVRSB}+$I_{EXTLVDS}$)	$I_{EXTRAIL}$ CC	-	-	56	mA	max power pattern
		-	-	50	mA	real power pattern

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Table 3-27 Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{EXT} and I_{FLEX} supply current	$I_{EXTFLEX}$ CC	-	-	18 [3]	mA	real power pattern with port activity absent; PORST output inactive.
I_{EVRSB} supply current [1]	I_{EVRSB} CC	-	-	8	mA	real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}$+$I_{DDMEDSADC}$)	I_{DDM} CC	-	-	48	mA	real power pattern; sum of currents of EDSADC and EVADC modules
∑ Sum of all currents (incl. $I_{EXTRAIL}$+$I_{DDMRAIL}$+$I_{DDx3RAIL}$+I_{DD})	I_{DDTOT} CC	-	-	978	mA	real power pattern; T_J=150°C
∑ Sum of all currents with DC-DC EVRC regulator active [4]	$I_{DDTOTDC3}$ CC	-	-	580	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V; T_J=150°C
∑ Sum of all currents with DC-DC EVRC regulator active [4]	$I_{DDTOTDC5}$ CC	-	-	440	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 5V; T_J=150°C
∑ Sum of all currents (SLEEP mode) [1]	I_{SLEEP} CC	-	-	27	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB}$ = 1 MHz via LPDIV divider; T_J = 25$°C$
∑ Sum of all currents (STANDBY mode) drawn at V_{EVRSB} supply pin [5]	$I_{STANDBY}$ CC	-	-	130 [6]	µA	32 kB Standby RAM block active. SCR inactive. Power to remaining domains switched off. T_J = 25$°C$; V_{EVRSB} = 5V
Maximum power dissipation [7]	PD SR	-	-	2400	mW	max power pattern
		-	-	1700	mW	real power pattern

1) Limits are defined for real power pattern (V_{DD}=1.275V). For max power pattern limit has to be multiplied by the factor 1.22.

2) Realistic Pflash read pattern with 50% Pflash bandwidth utlilization and a code mix of 50% 0s and 50% 1s. A common decoupling capacitor of atleast 100nF for (V_{DDP3}) is used. Continuous Dflash programming in burst mode with 3.3 V supply and realistic Pflash read access in parallel. Erase currents of the corresponding flash modules are less than the respective programming currents at V_{DDP3} pin. Programming and erasing flash may generate transient current spikes of up to 45 mA / 20 ns
which are handled by the decoupling and buffer capacitors. This parameter is relevant for external power supply dimensioning and not for thermal considerations.

3) The current consumption includes only minimal port activity.

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4) The total current drawn from external regulator is estimated with 72% EVRC SMPS regulator efficiency. IDDTOTDCx is calculated from IDDTOT using the scaled core current [(IDD x VDD)/(VinxEfficiency)] and constitutes all other rail currents and IDDM.
5) The same current limits apply also for the other power pattern.
6) ∑ Sum of all currents during RUN mode at VEVRSB supply pin is less than (IEVRSB + 4 mA Standby RAM current + ISCRSB if SCR active). ∑ It is recommended to have atleast 100 nF decoupling capacitor at this pin. 32kB of Standby SRAM contributes less than 10uA to ISTANDBY current.
7) The values are only valid if all supplies are applied from external and do not contain the power losses of EVR33 and EVRC.

Table 3-28 Module Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDP3} supply current for programming of a Pflash or Dflash bank [1]	$I_{DDP3PROG}$ CC	-	-	25	mA	Pflash 3.3V programming current adder when using external 3.3V supply.
		-	-	9 [2]	mA	Pflash 3.3V programming current adder when using external 5V supply.
I_{EXT} supply current added by LVDS pads in LVDS mode [1]	$I_{EXTLVDS}$ CC	-	-	9	mA	real power pattern; 6 pairs of LVDS pins active with receive function
		-	-	24	mA	real power pattern; 6 pairs of LVDS pins active with transmit function

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Table 3-28 Module Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}$+$I_{DDMEDSADC}$)	I_{DDM} CC	-	-	32	mA	real power pattern; current for EDSADC modules only and EVADC modules are inactive; 8 EDSADC channels active continuously.
		-	-	45 [3]	mA	max power pattern; current for EDSADC modules only and EVADC modules are inactive; all EDSADC channels active continuously.
		-	-	16	mA	real power pattern; current for EVADC modules only and EDSADC modules are inactive; 12 EVADC modules active.
		-	-	20 [4]	mA	max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.
I_{DDP3} supply current for erasing of a Pflash or Dflash bank	$I_{DDP3ERASE}$ CC	-	-	25	mA	Pflash 3.3V erasing current adder when using external 3.3V supply.
SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin	I_{SCRSB} CC	-	-	7 [5]	mA	SCR power pattern incl. PMS current consumption with fback clock active; f_{SYS_SCR} = 20MHz; T_J=150°C
		-	0.150	-	mA	SCR power pattern incl. PMS current consumption with fback inactive; fSYS_SCR = 70kHz; T_J=25°C
SCR 8-bit Standby Controller CPU in IDLE mode [6]	$I_{SCRIDLE}$ CC	-	-	3.5	mA	real power pattern. CPU set into idle mode.

1) The same current limits apply also for the other power pattern.
2) During Pflash programming at 5V, additional 3 mA is drawn at VEXT supply rail.
3) A single DS channel instance consumes 4 mA.

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4) A single VADC unit consumes 1.3 mA.
5) If SCR ADCOMP is activated, an additional 0.6 mA adder is to be considered.
6) Limits are defined for real power pattern (V_{DD}=1.275V). For max power pattern limit has to be multiplied by the factor 1.22.

Table 3-29 Module Core Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current of CPUx main core with CPUx lockstep core inactive	I_{DDCx0} CC	-	-	70	mA	max power pattern; IPC=1.2
		-	-	45	mA	real power pattern; IPC=0.6
I_{DD} core current of CPUx main core with CPUx lockstep core active	I_{DDCxx} CC	-	-	I_{DDCx0} + 50	mA	max power pattern; IPC=1.2
		-	-	I_{DDCx0} + 40	mA	real power pattern; IPC=0.6
I_{DD} core current added by GTM	I_{DDGTM} CC	-	-	125	mA	max power pattern
		-	-	100	mA	real power pattern; TIMx, TOMx, ATOMx , MCSx active. 3 clusters at 200 MHz.
		-	-	50	mA	TIMx, TOMx active at 100MHz. ATOMx , MCSx, DPLL inactive. 2 clusters at 100 MHz.
I_{DD} core current added by HSM	I_{DDHSM} CC	-	-	20 [1]	mA	max power pattern; HSM running at 100MHz.
I_{DD} core dynamic current added by LBIST	$I_{DDLBIST}$ CC	-	-	80 [2]	mA	LBIST Configuration A; 1.2V ≤ V_{DD}
I_{DD} core dynamic current added by MBIST	$I_{DDMBIST}$ CC	-	-	200	mA	fMBIST = 300MHz; tMBIST < 6ms. MTU Ganging procedure for SRAM test and initialization; VDD = 1.375V.

1) The current consumption includes basic HSM activity incl. AES module.
2) LBIST is executed either during start-up phase or can be triggered by application software. Secondary voltage monitors are inactive during the LBIST execution time (t_{LBIST}).
During the start-up phase externally supplied V_{DD} voltage has to be equal or greater than 1.2V (V_{DD} nominal - 4%) for static accuracy.
If V_{DD} is supplied internally by EVRC, EVRC takes care not to violate the V_{DD} 1.2V static under voltage limit.

3.12.1 Calculating the 1.25 V Current Consumption

The current consumption of the 1.25 V rail is composed of two parts:

- Static current consumption
- Dynamic current consumption

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The static current consumption is related to the device temperature T_J and the dynamic current consumption depends on the configured clocking frequencies and the software application executed. These two parts need to be added in order to get the rail current consumption.

(3.1)

$$I_0 = 4,7777\left[\frac{mA}{C}\right] \times e^{0,02273 \times T_J[C]}$$

(3.2)

$$I_0 = 11,3778\left[\frac{mA}{C}\right] \times e^{0,02114 \times T_J[C]}$$

Equation (3.1) defines the typical static current consumption and **Equation (3.2)** defines the maximum static current consumption. Both functions are valid for V_{DD} = 1.275 V.

3.13 Power Supply Infrastructure and Supply Start-up

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3.13.1 Supply Ramp-up and Ramp-down Behavior

Start-up slew rates for supply rails shall comply to SR (see **Table 3-33** Supply Ramp).

3.13.1.1 Single Supply mode (a)

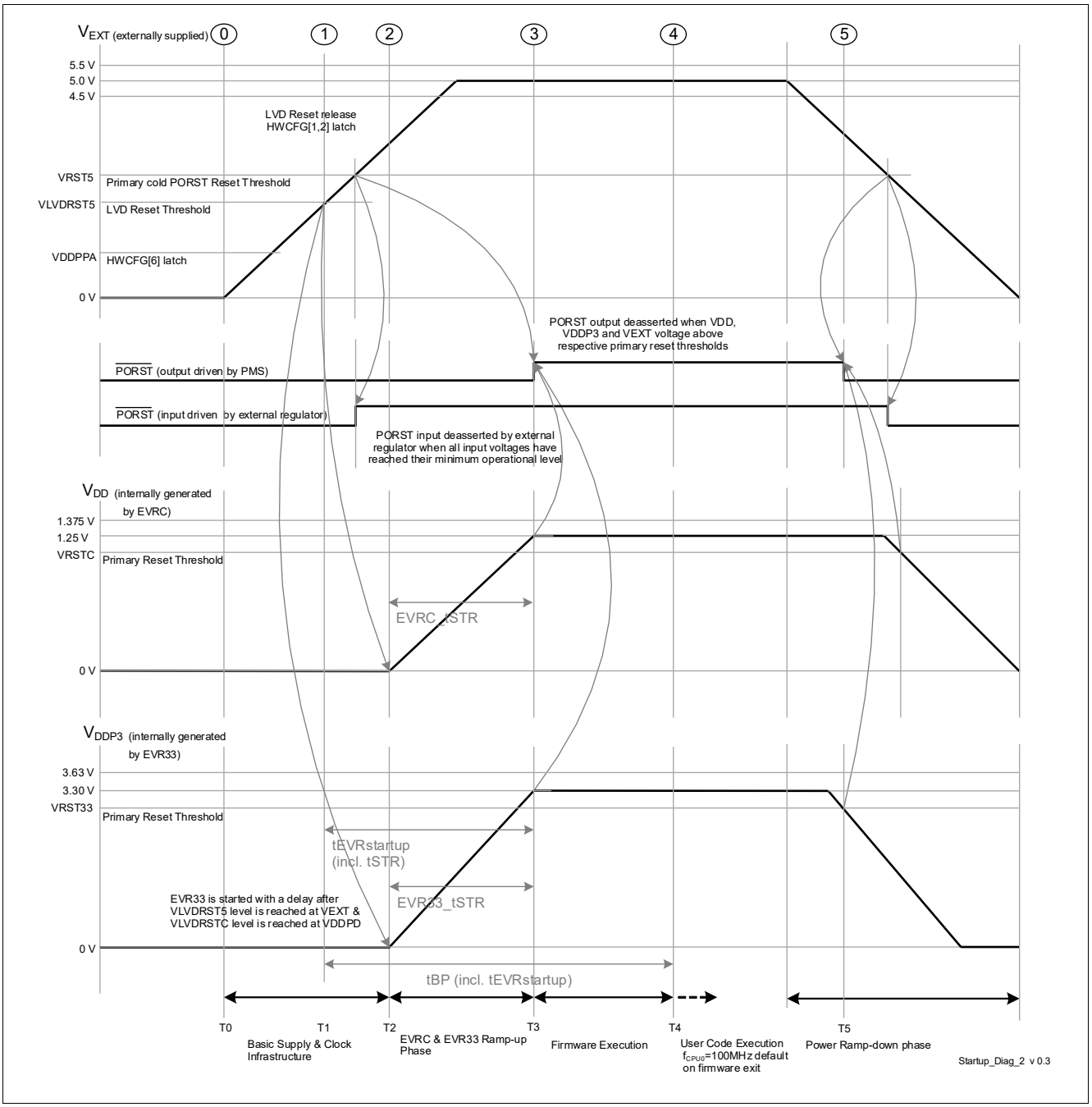

Figure 3-3 Single Supply mode (a) - VEXT (5 V) single supply

VEXT = 5 V single supply mode. VDD and VDDP3 are generated internally by the EVRC and EVR33 internal regulators.

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- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited during the basic infrastructure and EVRx regulator start-up phase (T0 up to T2) to a maximum of 100 mA with 100 us settling time. Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.
- Furthermore it is also ensured that the current drawn from the regulator (dIDD/dt) is limited during the Firmware start-up phase (T3 up to T4) to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-3** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVRC and EVR33 regulators are initiated. PORST (input) does not have any affect on EVR33 or EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR (datasheet parameter) time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC and EVR33 regulators have ramped up.
    PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup (datasheet parameter).
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.13.1.2 Single Supply mode (e)

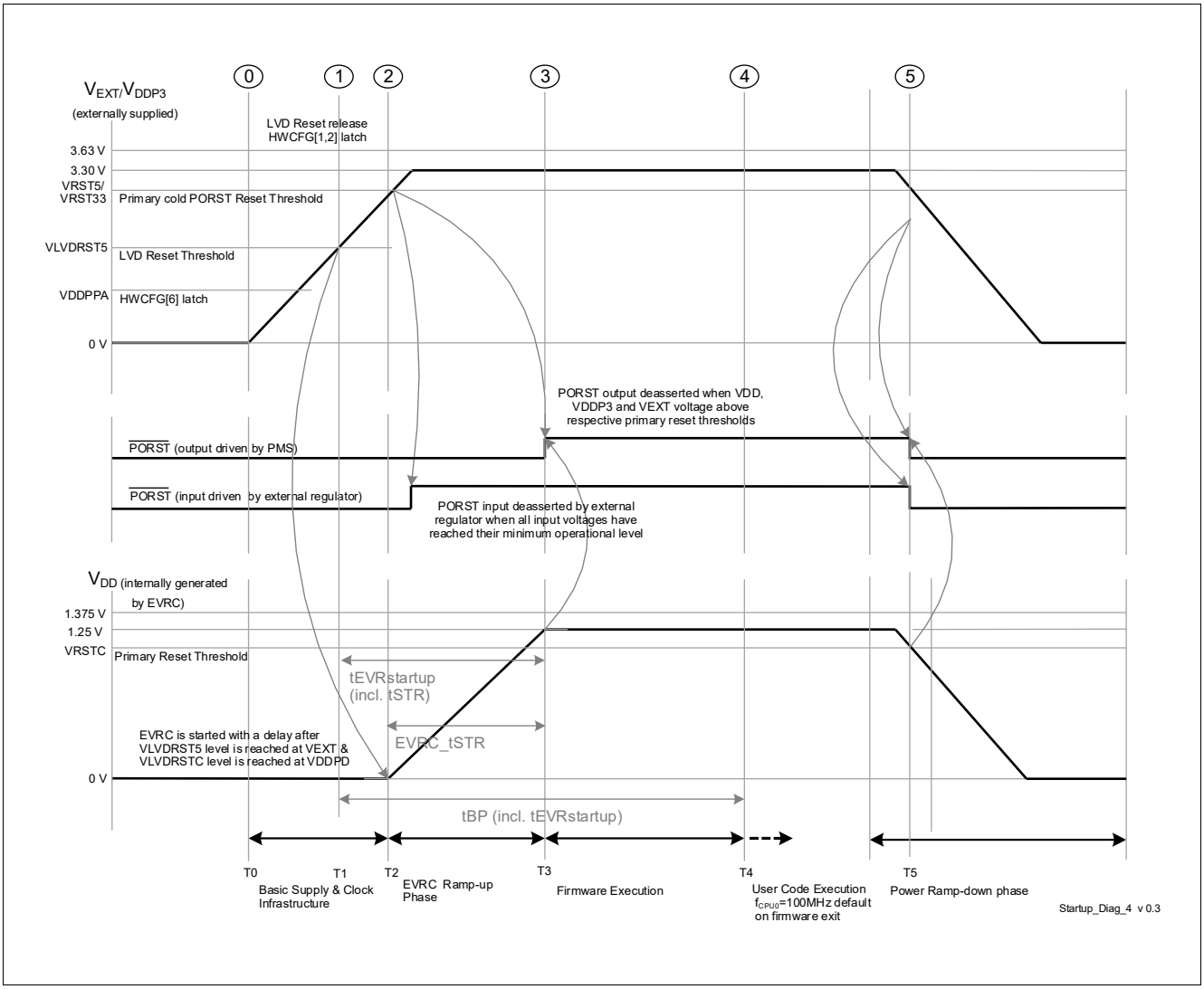

Figure 3-4 Single Supply mode (e) - (VEXT & VDDP3) 3.3 V single supply

VEXT = VDDP3 = 3.3 V single supply mode. VDD is generated internally by the EVRC regulator.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time. Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the

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basic supply and clock infrastructure is available. During reset release at T3, the load jump of upto 150 mA (dIDD) is expected.

- The power sequence as shown in **Figure 3-4** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVRC regulator is initiated. PORST (input) does not have any affect on EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR (datasheet parameter) time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC regulator has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup (datasheet parameter).
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.13.1.3 External Supply mode (d)

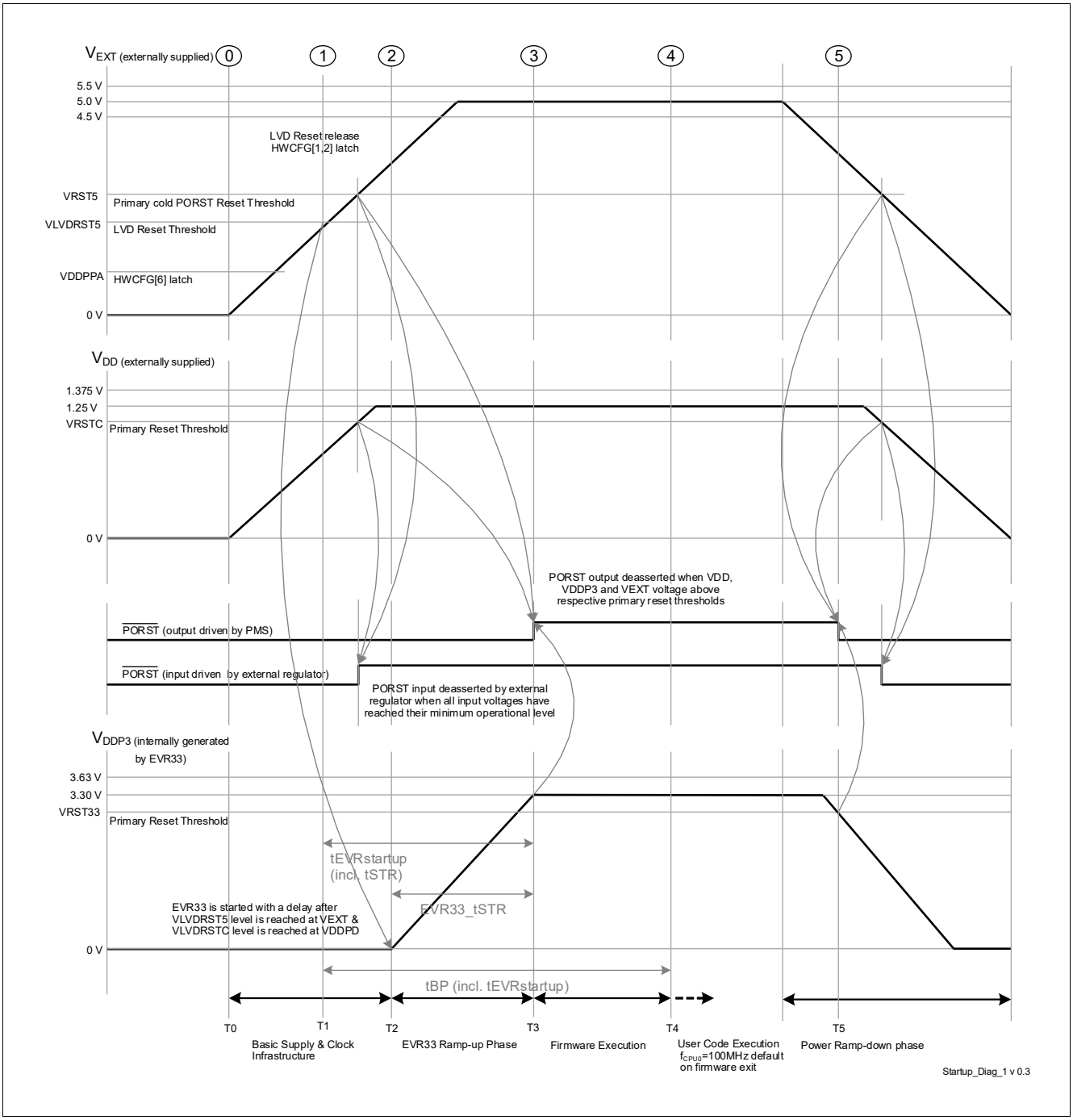

Figure 3-5 External Supply mode (d) - VEXT and VDD externally supplied

VEXT = 5 V and VDD supplies are externally supplied. 3.3V is generated internally by the EVR33 regulator.

- External supplies VEXT and VDD may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, VEXT ramps up before VDD rail. If VDD voltage

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rail is ramped up before VEXT; VDD supply overshoots during start-up shall be limited within the operational voltage range.

- The rate at which current is drawn from the external regulator (dIEXT /dt or dIDD /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of upto 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-5** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVR33 regulator is initiated. PORST (input) does not have any affect on EVR33 output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR (datasheet parameter) time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVR33 regulators has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup (datasheet parameter).
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.13.1.4 External Supply mode (h)

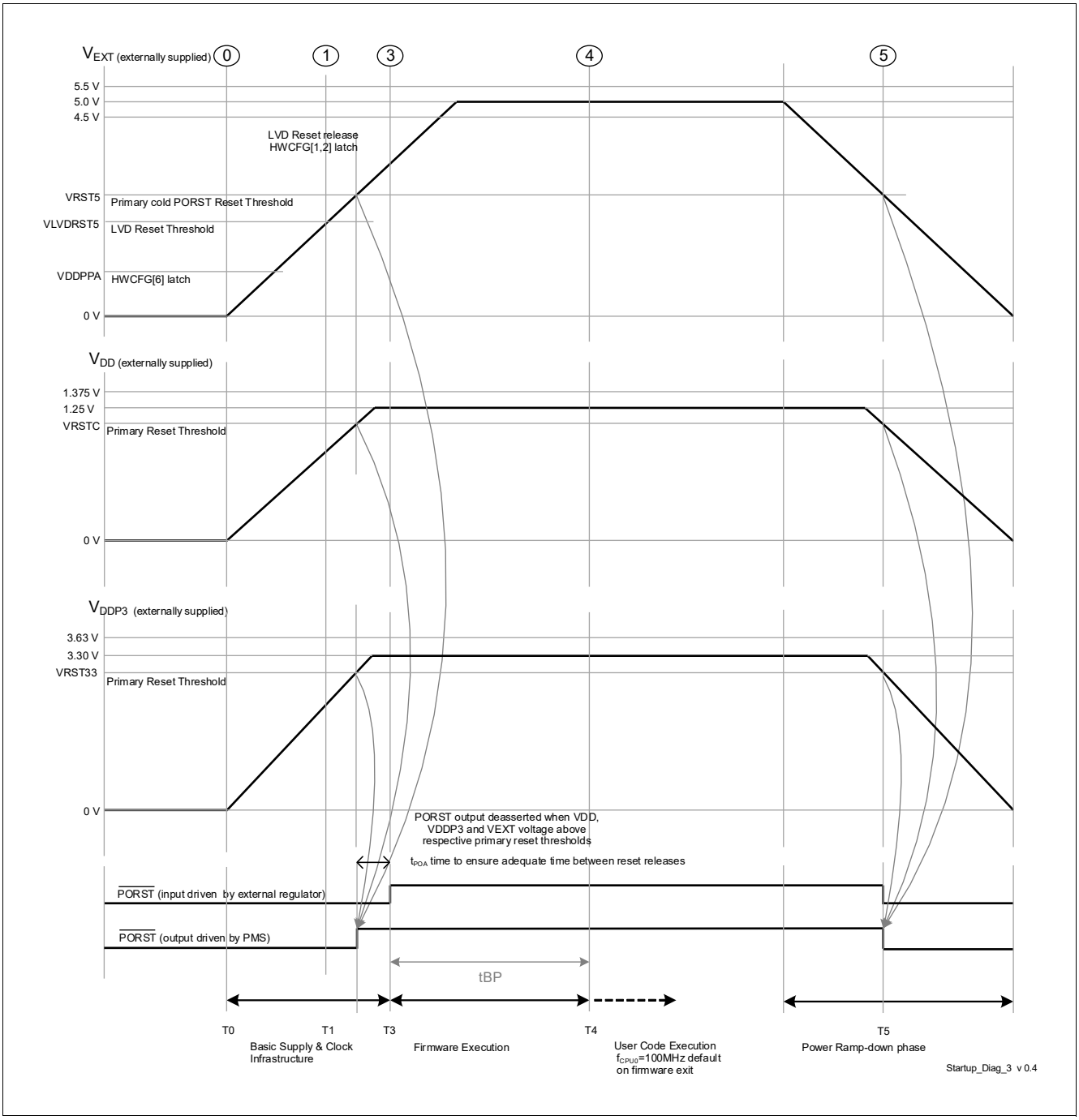

Figure 3-6 External Supply mode (h) - VEXT, VDDP3 & VDD externally supplied

All supplies, namely VEXT, VDDP3 & VDD are externally supplied.

- External supplies VEXT, VDDP3 & VDD may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, VEXT ramps up before VDDP3 and VDD rails. If smaller voltage rails are ramped up before VEXT; VDD and VDDP3 supply overshoots during start-up shall be limited within the operational voltage ranges of the respective rails.

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- The rate at which current is drawn from the external regulator (dIEXT /dt, dIDD /dt or dIDDP3 /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of upto 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-6** is enumerated below
  - T1 up to T3 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated.
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.14 Reset Timing

Table 3-30 Reset

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time	t_B CC	-	-	400	µs	operating with max. frequencies, with valid BMI header
System Reset Boot Time	t_{BS} CC	-	-	1.1	ms	RAM initialization and HSM boot time are not included, with valid BMI header
Cold Power on Reset Boot Time [1]	t_{BP} CC	-	-	3.1	ms	$dVEXT/dT$=1V/ms. $VEXT$>$VLVDRST5$. Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.
		-	-	1.6	ms	Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary monitors	t_{EVRPOR} CC	10 [2]	-	-	µs	
PMS Infrastructure, EVRC and EVR33 overall start-up time till cold PORST reset release	$t_{EVRstartup}$ CC	-	-	1	ms	dV/dT=1V/ms. EVRC and EVR33 active
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POA} SR	1 [3]	-	-	ms	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF}$ CC	600	-	1200	ns	
Warm Reset Sequencing Delay	$t_{WARMRSTSEQ}$ CC	-	-	180	µs	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} CC	16 / f_{SPB}	-	-	ns	

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Table 3-30 Reset (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	-	-	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	8000/f_{BACKT}	-	18000/f_{BACKT}	s	
Ports inactive after PORST reset active	t_{PIP} CC	-	-	150	ns	
Hold time from PORST rising edge	t_{POH} SR	150	-	-	ns	
Setup time to PORST rising edge	t_{POS} SR	0	-	-	ns	
Warm PORST reset boot time	t_{BWP} CC	-	-	1.3	ms	without RAM initalization
LBIST execution time extending the boot time	t_{LBIST} CC	-	-	6	ms	LBIST Configuration A; 1.2V ≤ V_{DD}
SCR reset boot time	t_{SCR} CC	-	-	5	µs	User Mode 0
		-	-	16	µs	User Mode 1
		-	13.3	-	µs	WDT double bit ECC, soft reset
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ CC	-	-	250	µs	external supplies are V_{EVRSB}, V_{EXT}, V_{FLEX}, V_{DDM}, V_{DDP3} and V_{DD}

1) RAM initialization add 500µs in addition.
2) Cold PORST reset is driven by uC and maintained in an extended voltage range between VDDPPA limit and absolute maximum rating VEXT/VEVRSB voltage limits.
3) The reset release on supply ramp-up or supply restoration is delayed by a voltage hysteresis of 1.5% (default value) above the undervoltage reset limit implemented on VEXT, VDDP3 and VDD rails. This mechanism helps to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released.

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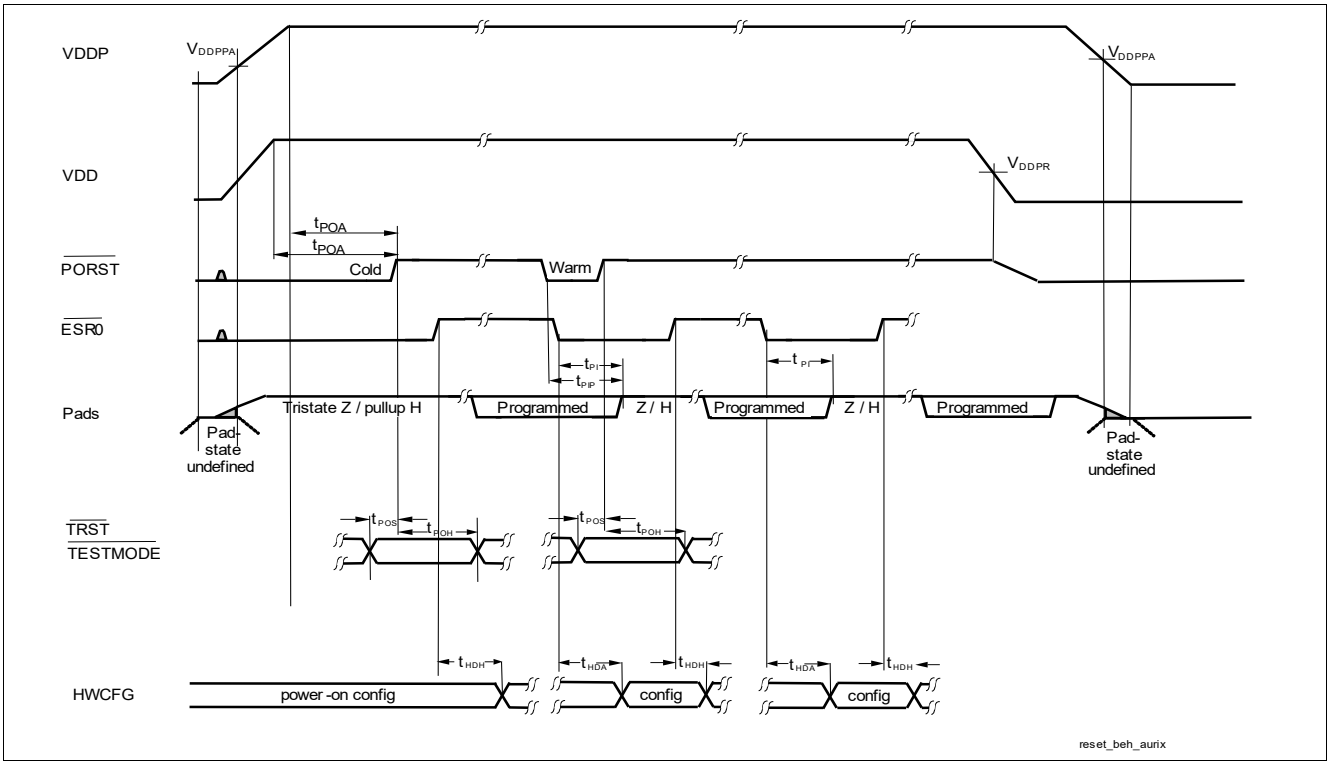

Figure 3-7 Power, Pad and Reset Timing

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3.15 PMS

Table 3-31 EVR33 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	V_{IN} SR	3.60 [1]	-	5.50	V	Normal RUN mode
		2.97 [2]	-	5.50	V	Low voltage cranking mode
Output voltage operational range including load/line regulation and aging [3]	V_{OUT} CC	2.97	3.3	3.63	V	Normal RUN mode
		2.60	3.3	3.63	V	Low voltage cranking mode; I_{DDP3}=50mA
Output V_{DDx3} static voltage accuracy after trimming and aging without dynamic load/line regulation.	V_{OUTT} CC	3.225	3.3	3.375	V	Normal RUN mode
		2.78	3.3	3.375	V	Low voltage cranking mode; I_{DDP3}=50mA
Output buffer capacitance on V_{OUT}	C_{OUT} SR	1.45	2.2	3	µF	
Output buffer capacitor ESR	C_{OUTESR} SR	-	-	100 [4]	mOhm	f > 0.5MHz; f < 10MHz
Maximum output current of the regulator	I_{MAX} CC	60 [5]	-	-	mA	Normal RUN mode
Startup time	t_{STR} CC	-	500	1000	µs	Normal RUN mode
External V_{IN} supply ramp [6]	$dVin/dt$ SR	-	1	-	V/ms	
Ripple on Output Voltage	ΔV_{OUTTC} CC	-	-	33	mV	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{OUTTC} ≥ 10mA ; I_{OUTTC} ≤ 60mA; ΔV_{OUTTC} = (peak to peak ripple / 2)
Load step response [7]	$dVout/dIout$ CC	-165	-	-	mV	Normal RUN mode; dI=10 to 60mA; dt=20ns; $Tsettle$=20us
		-	-	165	mV	Normal RUN mode; dI=60 to 10mA; dt=20ns; $Tsettle$=20us
		-180	-	-	mV	Low voltage cranking mode; dI=10 to 50 mA; dt=20ns; $Tsettle$=20us
		-	-	180	mV	Low voltage cranking mode; dI=50 to 10mA; dt=20ns; $Tsettle$=20us

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Table 3-31 EVR33 LDO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line step response	*dVout/dVin* CC	-	-	40	mV	$dVin/dT$=1V/ms; dV= 3.6 to 5V; I_{MAX}=60mA; ΔV_{OUTTC} is included
		-40	-	-	mV	$dVin/dT$=1V/ms; dV= 5 to 3.6V; I_{MAX}=60mA; ΔV_{OUTTC} is included
		-	-	280	mV	$dVin/dT$=50V/ms; dV= 3.6 to 5V; I_{MAX}=60mA
		-165	-	-	mV	$dVin/dT$=50V/ms; dV= 5 to 3.6V; I_{MAX}=60mA

1) A maximum pass device dropout voltage of 300mV is included in the minimum input voltage to ensure optimal pass device performance during normal operation.
2) VEXT Input voltage drop up to 2.97V leading to VDDP3 output voltage drop upto 2.6V can be tolerated if Flash is switched before to low performance mode.
3) No external inductive load permissible if EVR33 is used.
4) It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm. An additional decoupling capacitor of 100nF shall be located close to the pin before Cout.
5) IMAX is limited to 40 mA incase of Low voltage mode (cranking case) with on chip pass devices. In case EVR33 is not used, Injection current into 3.3V VDDP3 supply rail with active sink on 5V VEXT rail should be limited to 500 mA if during power sequencing 3.3V is supplied before 5V by external regulator.
6) EVR is robust against residual voltage ramp-up starting between 0 - 2.97 V. A VEXT voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.
7) Settling time is defined until output voltage is within +-1% of the mean(VOUTT) of the individual device.

Table 3-32 Supply Monitors

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary Undervoltage Reset threshold for V_{DDP3} before trimming [1]	V_{RST33} CC	-	-	3.00	V	by reset release before EVR trimming on supply ramp-up
Primary undervoltage reset threshold for V_{DD} before trimming	V_{RSTC} CC	-	-	1.138	V	by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis
V_{EXT} primary undervoltage monitor accuracy after trimming [2]	$V_{EXTPRIUV}$ CC	2.86	2.92	2.97	V	V_{EXT} = Undervoltage cold PORST Primary Monitor Threshold
V_{DDP3} primary undervoltage monitor accuracy after trimming [2]	$V_{DDP3PRIUV}$ CC	2.86 [3]	2.90	2.97	V	VDDP3 = Undervoltage cold PORST Primary Monitor Threshold
V_{DD} primary undervoltage monitor accuracy after trimming [2]	$V_{DDPRIUV}$ CC	1.08 [3]	1.105	1.125	V	VDD = Undervoltage cold PORST Primary Monitor Threshold

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Table 3-32 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVR primary monitor measurement latency for a new supply value	t_{PRIUV} CC	-	-	300	ns	The supply ramp / line jump slope is limited to 50V/ms for V_{EXT}, V_{DDP3} and V_{DD} rails.
V_{EXT}, V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming [4) 5)]	V_{EXTMON} CC	3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV). EVRMONFILT.SWDFIL=1.
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV)/C9h(OV). EVRMONFILT.SWDFIL=1
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EAh(UV)/ECh(OV). EVRMONFILT.SWDFIL=1
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV)/DAh(OV). EVRMONFILT.SWDFIL=1

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Table 3-32 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP3} secondary supply monitor accuracy after trimming [5]	$V_{DDP3MON}$ CC	2.97	3.035	3.1	V	EVR33xxVAL monitoring threshold=3.035V=CBh (UV)/CCh(OV). EVRMONFILT.EVR33 FIL = 3.
		3.235	3.30	3.365	V	EVR33xxVAL monitoring threshold=3.3V=DDh(OV,UV). EVRMONFILT.EVR33 FIL = 3.
		3.5	3.565	3.63	V	EVR33xxVAL monitoring threshold=3.565V=EEh (UV)/EFh(OV). EVRMONFILT.EVR33 FIL = 3.
V_{DD} & V_{DDPD} secondary supply monitor accuracy after trimming [5]	V_{DDMON} CC	1.125	1.15	1.175	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.15V=C7h(UV)/C8h(OV). EVRMONFILT.EVRCFI L = 1.
		1.225	1.25	1.275	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.25V=D9h(OV,UV). EVRMONFILT.EVRCFI L = 1.
		1.325	1.35	1.375	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.35V=EAh(UV)/EBh(OV). EVRMONFILT.EVRCFI L = 1.
V_{EXT} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5}$ CC	2.3	-	2.72	V	Power-down
		2.4	-	2.75	V	Power-up
V_{EVRSB} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRSTSB}$ CC	2.18	-	2.47	V	Power-down
		2.21	-	2.5	V	Power-up
V_{EXT} and V_{EVRSB} PBIST primary overvoltage Monitor threshold	V_{PBIST5} CC	5.63	-	-	V	

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Table 3-32 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary undervoltage reset threshold for V_{EXT} before trimming	V_{RST5} CC	-	-	3.0	V	by last cold PORST release on supply ramp-up including voltage hysteresis.
EVR secondary monitor measurement latency for all 6 supply rails	t_{MON} CC	-	-	3.2	µs	HPOSC and SHPBG bandgap trimmed. Filter inactive.

1) The reset release on supply ramp-up is delayed by a time duration 20-40 us after reaching undervoltage reset threshold and by a voltage hysteresis of 1.5% above the undervoltage reset limit. These mechanisms serve as hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The reset limit of 2,97V at pin is for the case with 3.3V generated internally from EVR33. In case the 3.3V supply is provided externally, the bondwire drop will cause a reset at a higher voltage of 3.0V at the VDDP3 pin.
2) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. The VxxPRIUV parameters are device individually tested in production with +-1% tolerance about the VxxPRIUV limits. All voltages are measured on pins.
3) VRSTxx parameters are relevant only for the first cold PORST release. Later the reset levels are trimmed by the Firmware and reflected as VxxPRIUV parameters before device is used with full performance. The cold PORST is released with a voltage hysteresis on all the primary monitors to avoid consecutive PORST toggling behavior.
4) In case the application is using 3.3V single supply (Single Supply mode (e), i.e. VEXT and VDDP3 are shorted together), it is recommended to use secondary supply monitoring on channel VDDP3, because of the better accuracy of parameter VDDP3MON.
5) To monitor voltage level not provided in conditions the values for OV and UV thresholds can be generated by a linear interpolation or extrapolation based on the given points.

Table 3-33 Supply Ramp

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External V_{EXT} & V_{EVRSB} supply ramp-up and ramp-down slope 1) 2) 3)	*dVEXT/dt* SR	8.3E-6	1	100	V/ms	
External V_{DDP3} supply ramp-up and ramp-down slope 1)3)	*dVDDP3/dt* SR	8.3E-6	1	100	V/ms	
External V_{DD} supply ramp-up and ramp-down slope 1)3)	*dVDD/dt* SR	8.3E-6	1	100	V/ms	
External V_{DDM} supply ramp-up and ramp-down slope 1)3)	*dVDDM/dt* SR	8.3E-6	1	100	V/ms	

1) The device is robust against residual voltage ramp-up starting between 0 - 2.97 V for VEXT, VEVRSB, VDDP3 and VDDM and 0-1 V for VDD. A voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation.
2) Also valid in case EVR33 or EVRC is used. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.
3) The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

- Up to 1000000 power-cycles, matching the limits defined in the table 'Supply Ramp' are allowed for TC38x, without any restriction to reliability.

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Table 3-34 EVRC SMPS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input V_{EXT} Voltage range	V_{IN} SR	2.97	-	5.5	V	Start-up VEXT voltage > 2.6 V
SMPS regulator output voltage range including load/line regulation and aging	V_{DDDC} CC	1.125	-	1.375	V	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{DDDC} ≥ 1mA ; I_{DDDC} ≤ 1.5A ; untrimmed
SMPS regulator static voltage output accuracy after trimming without dynamic load/line regulation.	V_{DDDCT} CC	1.225	1.25	1.275	V	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{DDDC} ≥ 1mA ; I_{DDDC} ≤ 1.5A
Programmable switching frequency	f_{DCDC} SR	1.6	1.82	2.0	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation.
		-	0.8	-	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation. 0.8 MHz to be set in SW.
Startup time	t_{STRDC} CC	-	-	900	µs	SMPS Start-up Mode. It is is defined beween $V_{EXTPRIUV}$ reset threshold till PORST release, on condition that all other PORST requirements were released before. I_{START} < 700mA.
Switching frequency modulation spread	Δf_{DCSPR} CC	-	1.8%	-	MHz	
Maximum ripple at I_{MAX}	ΔV_{DDDC} CC	-	-	16	mV	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{DDDC} ≥ 300mA ; I_{DDDC} ≤ 1.5A ; ΔV_{DDDC} = (Peak to Peak ripple / 2)
No load current consumption of SMPS regulator	I_{DCNL} CC	-	15	19	mA	f_{DCDC}=1.82MHz; I_{DDDC}=I_{SLEEP}; V_{EXT} > 2.97 V; T_J=25°C
		-	5	-	mA	LPM mode; I_{DDDC}=I_{SLEEP}; V_{EXT} > 2.97 V; T_J=25°C

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Table 3-34 EVRC SMPS (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SMPS regulator load transient response	dV_{DDDCT} / dI_{OUT} CC	-50	-	87	mV	dI < -450mA ; I_{DDDC}=500-1500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=100 us
		-100	-	145	mV	dI < -700mA ; I_{DDDC}=750-1500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=100 us
		-26	-	26	mV	dI < 100mA ; I_{DDDC}=50-1500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=20us;
Maximum output current	I_{MAX} CC	100	-	-	mA	LPM mode. Typical current in LPM Mode = I_{SLEEP}
		1.5	-	-	A	limited by thermal constraints and component choice
SMPS regulator line transient response	dV_{DDDCT} / dV_{IN} CC	-75	-	75	mV	dV/dT=120V/ms; dV < 2.97 - 5.5V ; I_{DDDC}=50-1500mA;
		-12.5	-	12.5	mV	dV/dT=1V/ms; dV < 2.97 - 5.5V ; I_{DDDC}=50-1500mA;
SMPS regulator efficiency	n_{DC} CC	-	80	-	%	V_{IN}=3.3V; I_{DDDC}=1500mA; f_{DCDC}=1.82MHz
		-	75	-	%	V_{IN}=5V; I_{DDDC}=1500mA; f_{DCDC}=1.82MHz
Input Synchronisation frequency	$f_{DCDCSYNC}$ SR	1.6	1.82	2.0	MHz	

Table 3-35 EVRC SMPS External components

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor value [1]	C_{OUT} SR	20.8	32	43.2	µF	I_{DDDC}=1.5A; f_{DDDC} = 0.8MHz
		15.4	22	29.7	µF	I_{DDDC}=1.5A; f_{DDDC} = 1.82MHz

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Table 3-35 EVRC SMPS External components (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor ESR	C_{OUT_ESR} SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=10Hz
External input capacitor value [1]	C_{IN} SR	6.5	10	13.5	µF	I_{DDDC}=1.5A
External input capacitor ESR	C_{IN_ESR} SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=100Hz
External inductor value	L_{DC} SR	3.29	4.7	6.11		f_{DCDC}=0.8MHz
		2.31	3.3	4.29	µH	f_{DCDC}=1.82MHz
External inductor DCR	L_{DC_DCR} SR	-	-	0.2	Ohm	
P + N-channel MOSFET logic level	V_{LL} SR	-	-	2.5	V	
P + N-channel MOSFET drain source breakdown voltage	$\|V_{BR_DS}\|$ SR	+7	-	-	V	NMOS - V_{GS} = 0.
		-	-	-7	V	PMOS - V_{GS} = 0.
P + N-channel MOSFET drain source ON-state resistance	R_{ON} SR	-	150	-	mOhm	I_{DDDC}=1.5A; $\|V_{GS\|}$=2.5V ; T_A=25°C
P + N-channel MOSFET Gate Charge	Q_G SR	-	-	8	nC	I_{DDDC}=1.5A; NMOS- $\|V_{GS\|}$=5V; 1.5A pulsed drain current
		-8	-	-	nC	I_{DDDC}=1.5A; PMOS- $\|V_{GS\|}$=5V; 1.5A pulsed drain current
External Inductor Saturation Current Margin	ΔI_{SAT} SR	400	-	-	mA	The saturation current of the coil must be larger than I_{DDDC} + ΔI_{SAT}
P + N-channel MOSFET Gate threshold voltage	V_{GSTH} SR	-	1	-	V	NMOS
		-	-1	-	V	PMOS
N-channel MOSFET reverse diode forward voltage	V_{RDN} SR	-	0.8	-	V	

1) Capacitor min-max range represent typical +-35% tolerance including DC bias effect. The trace resistance from the capacitor to the supply or ground rail should be limited to 25 mOhm.

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3.16 System Phase Locked Loop (SYS_PLL)

Table 3-36 PLL System

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCO Input frequency range	f_{REF} CC	10	-	40	MHz	
Modulation Amplitude	MA CC	0	-	2	%	
Peak Period jitter	DP CC	-200	-	200	ps	without modulation (PLL output frequency)
Peak Accumulated Jitter	D_{PP} CC	-5	-	5	ns	without modulation
Total long term jitter	J_{TOT} CC	-	-	11.5	ns	including modulation; MA 1.25%; f_{REF} 20MHz
System frequency deviation	f_{SYSD} CC	-	-	0.01	%	with active modulation
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

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3.17 Peripheral Phase Locked Loop (PER_PLL)

Table 3-37 PLL Peripheral

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak Accumulated jitter at SYSCLK pin	D_{PP} CC	-1000	-	1000	ps	Peak only
Peak accumulated jitter	D_{PPI} CC	-700	-	700	ps	Peak only
RMS Accumulated jitter	D_{RMS} CC	-100	-	100	ps	measured over 1 µs; f_{REF} = 20 MHz and f_{DCO} = 640 MHz or f_{REF} = 25 MHz and f_{DCO} = 800 MHz
Peak Period jitter	DP CC	-200	-	200	ps	f_{DCO} = 640 MHz or f_{DCO} = 800 MHz
Absolute RMS jitter (PLL out)	J_{ABS10} CC	-125	-	125	ps	f_{REF} = 10 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS20} CC	-85	-	85	ps	f_{REF} = 20 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS25} CC	-85	-	85	ps	f_{REF} = 25 MHz; f_{DCO} = 800 MHz
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
DCO input frequency range	f_{REF} CC	10	-	40	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

OPEN MARKET VERSION

3.18 AC Specifications

All AC parameters are specified for the complete operating range defined in **Chapter 3.4** unless otherwise noted in column Note / Test Condition.

Unless otherwise noted in the figures the timings are defined with the following guidelines:

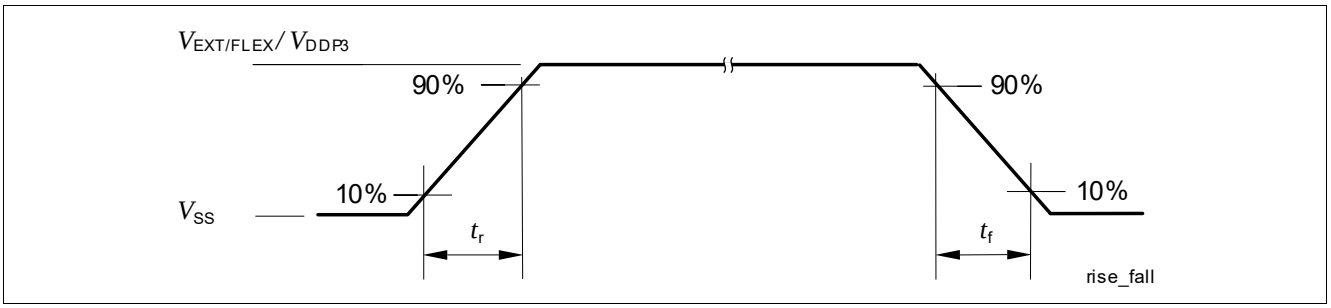

Figure 3-8 Definition of rise / fall times

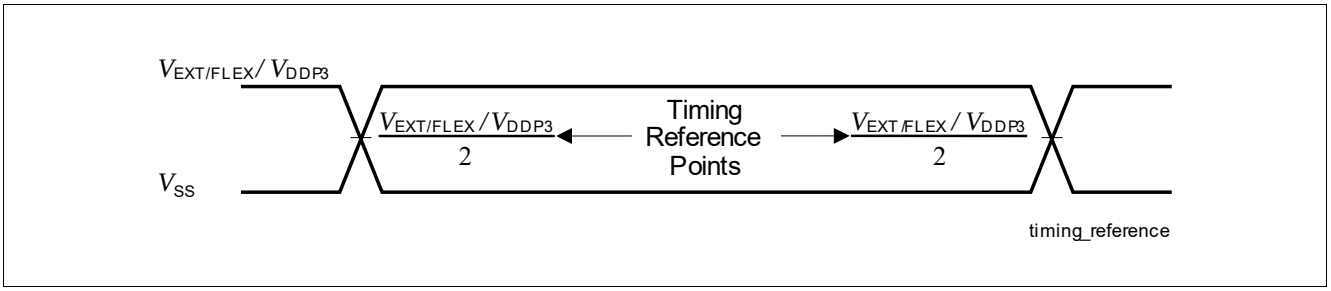

Figure 3-9 Time Reference Point Definition

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3.19 JTAG Parameters

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Table 3-38 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 CC	3.0	-	-	ns	C_L≤20pF
		-	-	25	ns	C_L≤50pF
TDO hold after TCK falling edge	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 CC	-	-	25	ns	C_L≤50pF
TDO valid output to high impedance from TCK falling edge	t_{10} CC	-	-	25	ns	C_L≤50pF

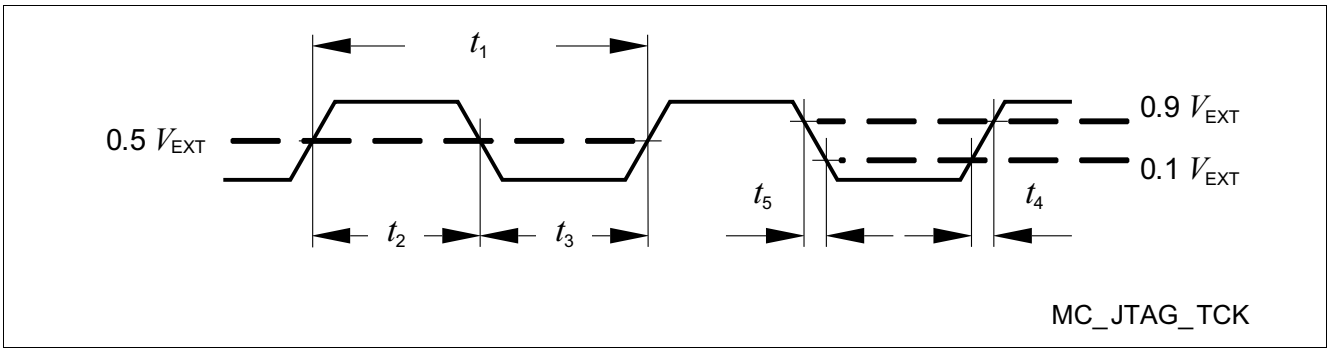

Figure 3-10 Test Clock Timing (TCK)

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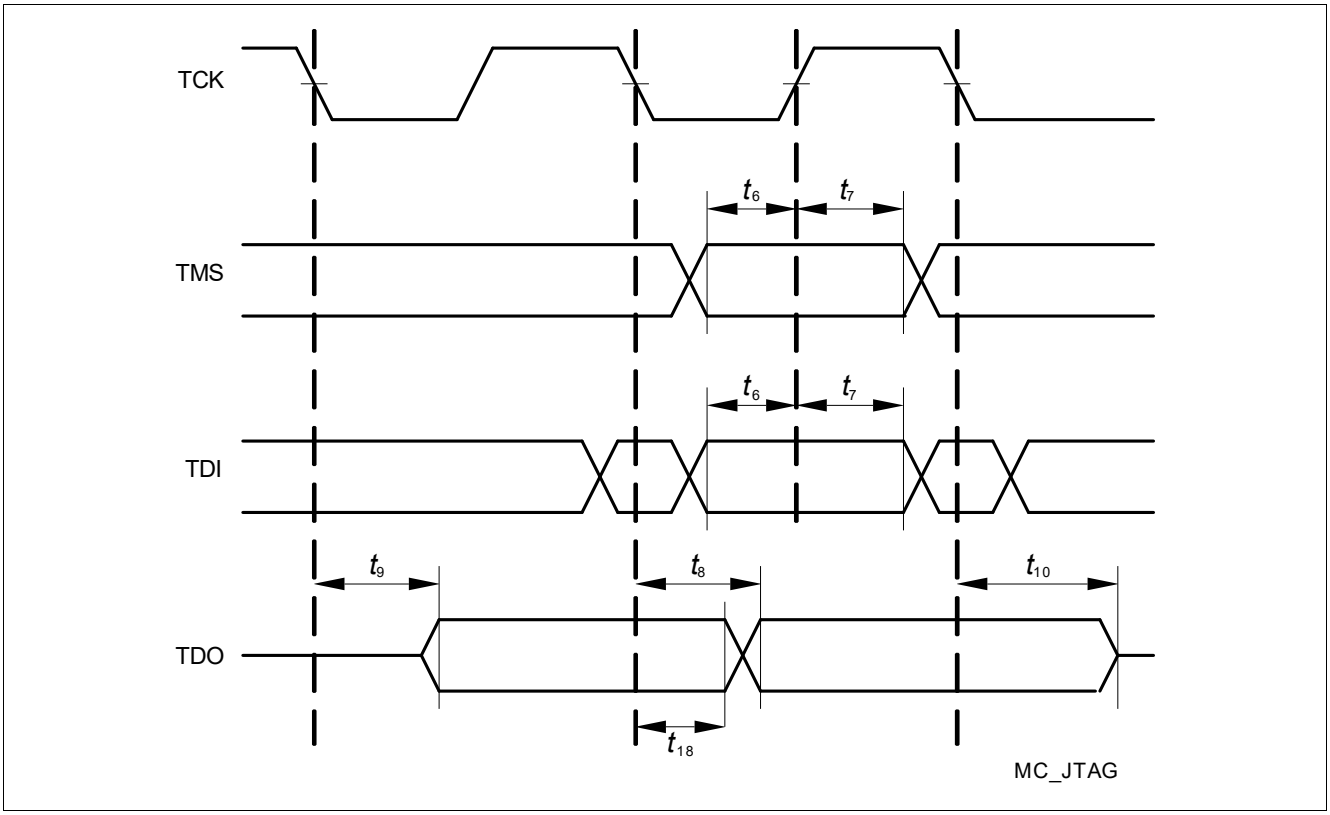

Figure 3-11 JTAG Timing

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3.20 DAP Parameters

The following parameters are applicable for communication through the DAP debug interface.

Table 3-39 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	4	-	-	ns	
		5	-	-	ns	f=40MHz
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	4	-	-	ns	C_L=20pF ; f=160MHz
		8	-	-	ns	C_L=20pF ; f=80MHz
		10	-	-	ns	C_L=50pF ; f=40MHz
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock period	t_{11} SR	6.25	-	-	ns	

Table 3-40 SCR DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	8	ns	f=20MHz
DAP0 clock fall time	t_{15} SR	-	-	8	ns	f=20MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	30	-	-	ns	C_L=20pF ; f=20MHz
DAP0 high time	t_{12} SR	15	-	-	ns	
DAP0 low time	t_{13} SR	15	-	-	ns	
DAP0 clock period	t_{11} SR	50	-	-	ns	

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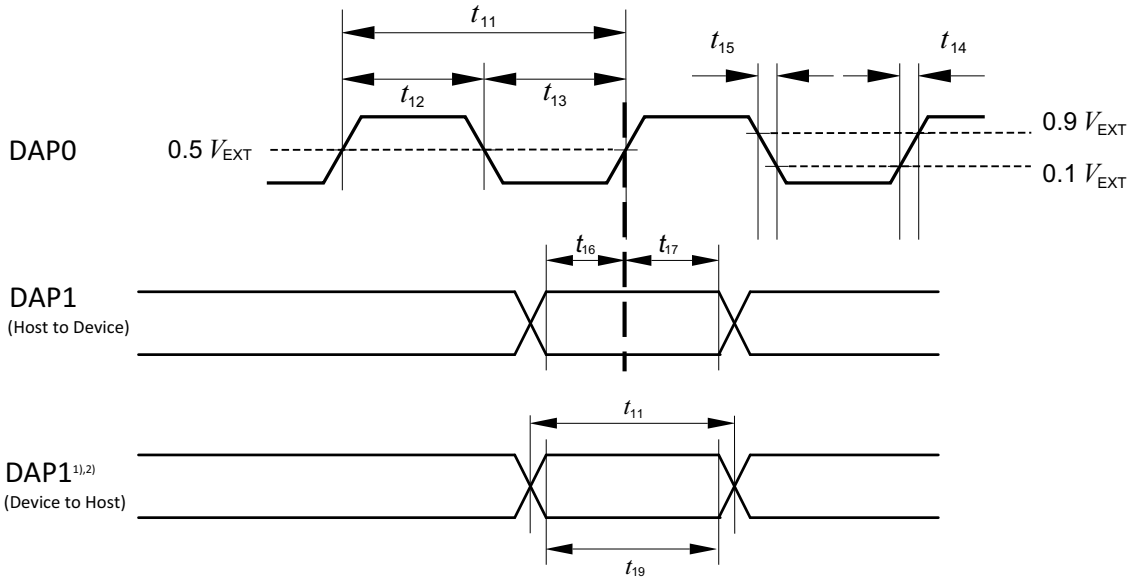

1) The DAP1 and DAP2 device to host timing is individual for both pins.
There is no guaranteed max. signal skew.

2) No explicit setup and hold times are given for DAP1 for the direction Device to Host.
Only t11 and t19 are guaranteed and the tool may set the sample point freely.

Figure 3-12 DAP Timing

Note: The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

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3.21 ASCLIN SPI Master Timing

This section defines the timings for the ASCLIN in the TC38x.

Note: Pad asymmetry is already included in the following timings.

Table 3-41 Master Mode strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	20	-	-	ns	C_L=25pF
Deviation from ideal duty cycle	t_{500} CC	-2	-	2	ns	C_L=25pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-3.5	-	3.5	ns	C_L=25pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-3	-	3.5	ns	C_L=25pF
MRST setup to ASCLKO latching edge	t_{52} SR	25	-	-	ns	C_L=25pF
MRST hold from ASCLKO latching edge	t_{53} SR	-2	-	-	ns	C_L=25pF

Table 3-42 Master Mode strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	50	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-5	-	5	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-7	-	7	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-7	-	7	ns	C_L=50pF
MRST setup to ASCLKO latching edge	t_{52} SR	35	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-5	-	-	ns	C_L=50pF

Table 3-43 Master Mode medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	160	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-10	-	10	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-20	-	20	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-20	-	20	ns	C_L=50pF

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Table 3-43 Master Mode medium (m) output pads (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to ASCLKO latching edge	t_{52} SR	80	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-15	-	-	ns	C_L=50pF

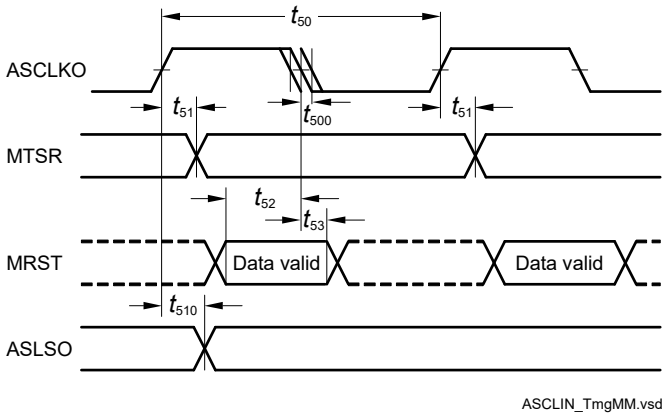

Figure 3-13 ASCLIN SPI Master Timing

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3.22 QSPI Timings, Master and Slave Mode

This section defines the timings for the QSPI in the TC38x.
It is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings:

Note: Pad asymmetry is already included in the following timings.

Table 3-44 Master Mode Timing, LVDS output pads for data and clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	20 1)	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-1 1)	-	1 1)	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-3 1)	-	4 1)	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4 1)	-	5.5 1)	ns	C_L=25pF, driver strength ss
		-10 1)	-	10 1)	ns	C_L=25pF, driver strength sm
		-30 1)	-	30 1)	ns	C_L=25pF, driver strength m
MRST setup to SCLK latching edge	t_{52} SR	18 1)	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI2 only
		19.5 1)	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI4 only
MRST hold from SCLK latching edge	t_{53} SR	-1 1)	-	-	ns	CL=25pF; valid for LVDS Input pads only

1) The load (C_L=25pF) defined in the condition list is a load definition for the single end signal SLSO and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Table 3-45 Master Mode Strong Sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-2	-	2	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-4	-	5	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4	-	5	ns	CL=25pF
MRST setup to SCLK latching edge	t_{52} SR	25 1) 2)	-	-	ns	CL=25pF
MRST hold from SCLK latching edge	t_{53} SR	-2 1)2)	-	-	ns	CL=25pF

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1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-46 Master Mode Strong Medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-5	-	5	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-7	-	7	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-7	-	7	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	35 [1) 2)]	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 [1)2)]	-	-	ns	CL=50pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-47 Master Mode Medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	160	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-10	-	10	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-20	-	20	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-20	-	20	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	80 [1) 2)]	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-15 [1)2)]	-	-	ns	CL=50pF
		-13 [1)2)]	-	-	ns	CL=50pF; SCR SSC

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-48 Slave mode timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} SR	4 x T_{MAX}	-	-	ns	
SCLK duty cycle	$t_{55/t54}$ SR	40	-	60	%	

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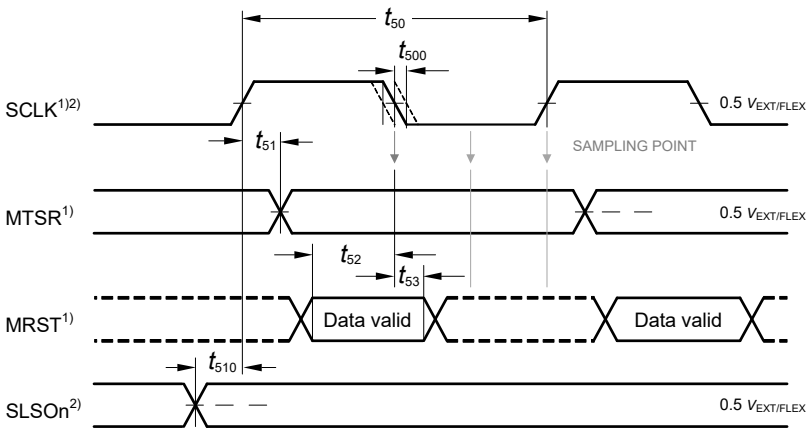
Table 3-48 Slave mode timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MTSR setup to SCLK latching edge	t_{56} SR	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MTSR hold from SCLK latching edge	t_{57} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	t_{59} SR	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	t_{60} CC	5	-	35	ns	driver = strong edge = medium ; C_L=50pF
		2	-	24	ns	driver = strong edge = sharp ; C_L=50pF
		15	-	80	ns	medium driver ; C_L=50pF
		14	-	-	ns	medium driver ; C_L=50pF; SCR SSC



1) This timing is based on the following setup: ECON.CPH = 1, ECON.CPOL = 0, ECON.B=0 (no sampling point delay).

2) t510 is the deviation from the ideal position configured with the leading delay, BACON.LPRE and BACON.LEAD > 0.

QSPI_TmgMM.vsd

Figure 3-14 Master Mode Timing

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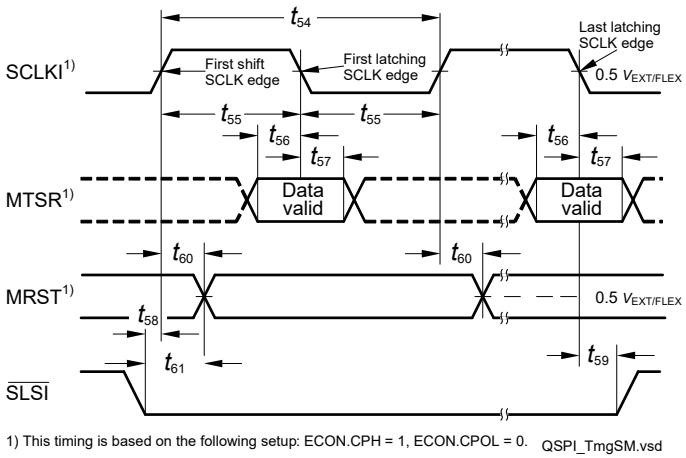

Figure 3-15 Slave Mode Timing

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3.23 MSC Timing 5 V Operation

The following section defines the timings.

Note: Pad asymmetry is already included in the following timings.

Note: Load for LVDS pads are defined as differential loads in the following timings.

Table 3-49 LVDS clock/data (LVDS pads in LVDS mode) valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A 1) 2) 3)	-	-	ns	LVDS; C_L=50pF
Deviation from ideal duty cycle	t_{400} CC	-1 3)	-	1 3)	ns	LVDS; 0 < C_L < 50pF
SOPx output delay	t_{44} CC	-3 3)	-	3 3)	ns	CL=50pF
ENx output delay	t_{45} CC	-4 3)	-	5 3)	ns	ss; C_L=50pF; ABRA block bypassed
		-4 3)	-	4 3)	ns	ss; C_L=50pF; ABRA block used
		-2 3)	-	10 3)	ns	sm; C_L=50pF
		-30 3)	-	30 3)	ns	m; C_L=50pF

1) T_A depends on the clock source selected for baud rate generation in the ABRA block of the MSC.
2) The capacitive load on the LVDS pins is differential, the capacitive load on the CMOS pins is single ended.
3) The load (C_L=50pF) defined in the condition list is a load definition for the single end signal EN and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Table 3-50 Strong sharp (ss) driver for clock/data valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-2	-	2	ns	CL=50pF
SOPx output delay	t_{44} CC	-4	-	3.5	ns	CL=50pF
ENx output delay	t_{45} CC	-4	-	3.5	ns	CL=50pF

Table 3-51 Strong medium (sm) driver for clock/data valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-5	-	5	ns	CL=50pF
SOPx output delay	t_{44} CC	-7	-	7	ns	CL=50pF
ENx output delay	t_{45} CC	-7	-	7	ns	CL=50pF

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Table 3-52 Medium (m) driver for clock/data valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-10	-	10	ns	CL=50pF
SOPx output delay	t_{44} CC	-20	-	20	ns	CL=50pF
ENx output delay	t_{45} CC	-20	-	20	ns	CL=50pF

Table 3-53 Upstream Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI bit time	t_{46} SR	8 * t_{MSC}	-	-	ns	
SDI rise time	t_{48} SR	-	-	200	ns	
SDI fall time	t_{49} SR	-	-	200	ns	

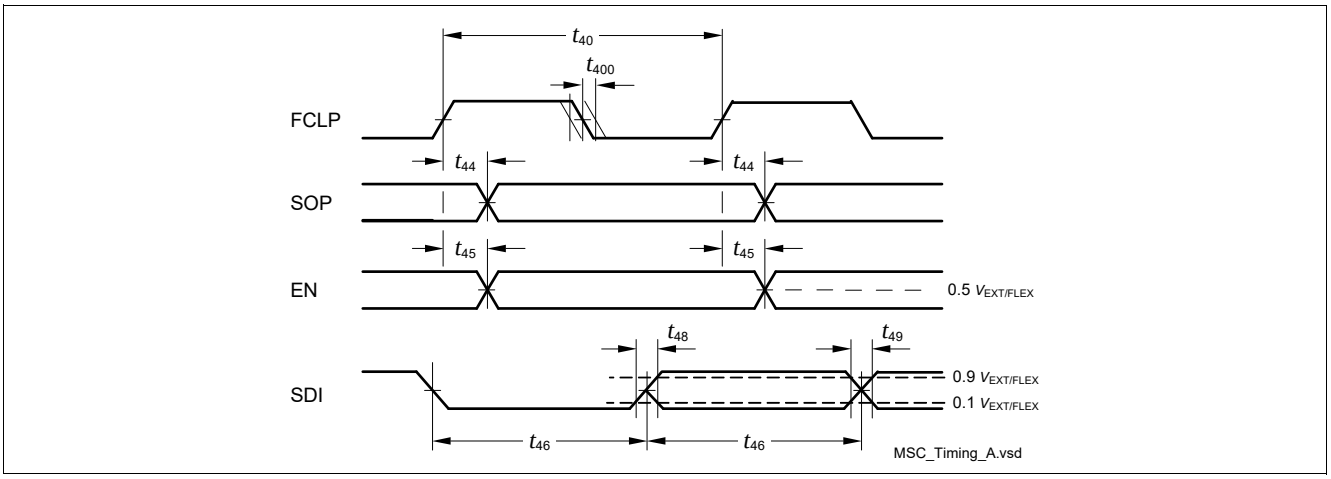

Figure 3-16 MSC Interface Timing

Note: The SOP data signal is sampled with the falling edge of FCLP in the target device.

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3.24 Ethernet Interface (ETH) Characteristics

3.24.1 ETH Measurement Reference Points

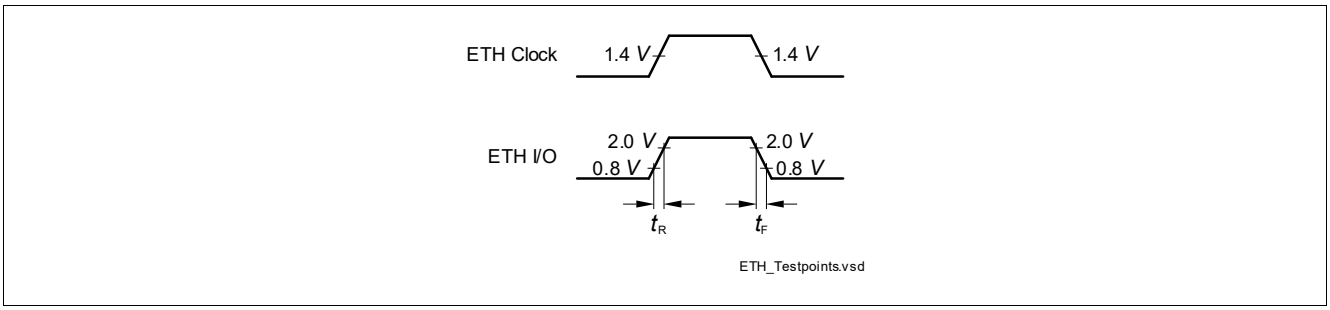

Figure 3-17 ETH Measurement Reference Points

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3.24.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 3-54 ETH Management Signal Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 CC	400	-	-	ns	CL=25pF
ETH_MDC high time	t_2 CC	160	-	-	ns	CL=25pF
ETH_MDC low time	t_3 CC	160	-	-	ns	CL=25pF
ETH_MDIO setup time (output)	t_4 CC	10	-	-	ns	CL=25pF
ETH_MDIO hold time (output)	t_5 CC	10	-	-	ns	CL=25pF
ETH_MDIO data valid (input)	t_6 SR	0	-	300	ns	CL=25pF

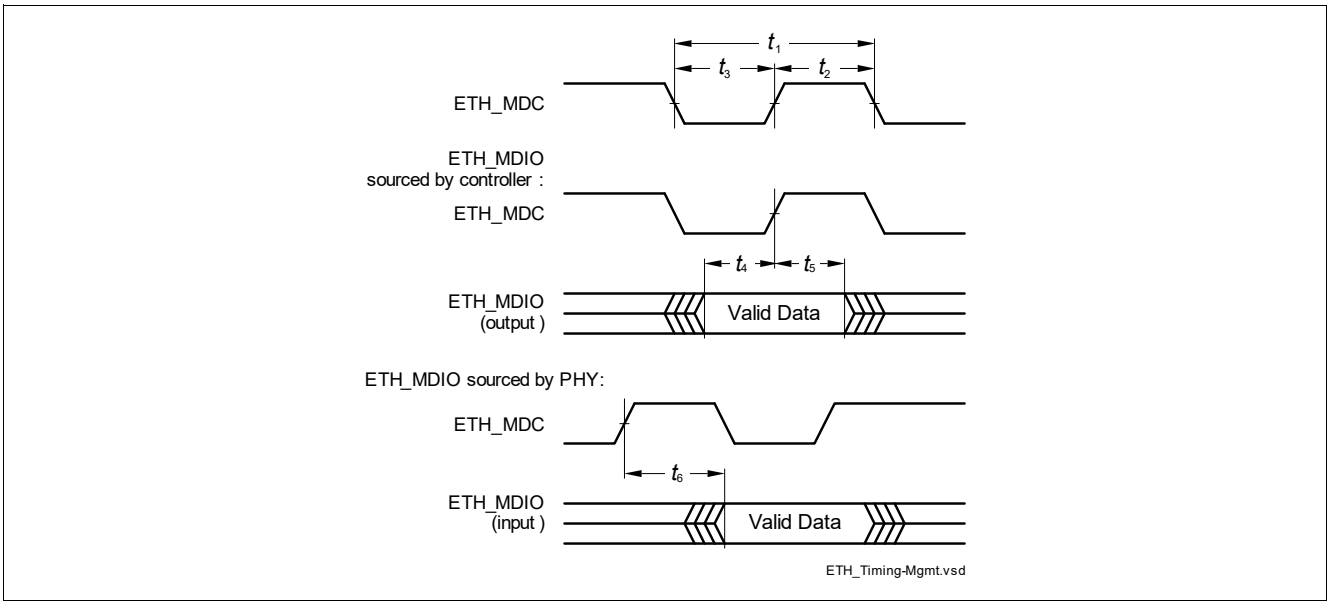

Figure 3-18 ETH Management Signal Timing

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3.24.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 3-55 ETH MII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_7 SR	-	40	-	ns	CL=25pF ; baudrate=100Mbps
		-	400	-	ns	CL=25pF ; baudrate=10Mbps
Clock high time	t_8 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Clock low time	t_9 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Input setup time	t_{10} SR	10	-	-	ns	CL=25pF
Input hold time	t_{11} SR	10	-	-	ns	CL=25pF
Output valid time	t_{12} CC	0	-	25	ns	CL=25pF

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.

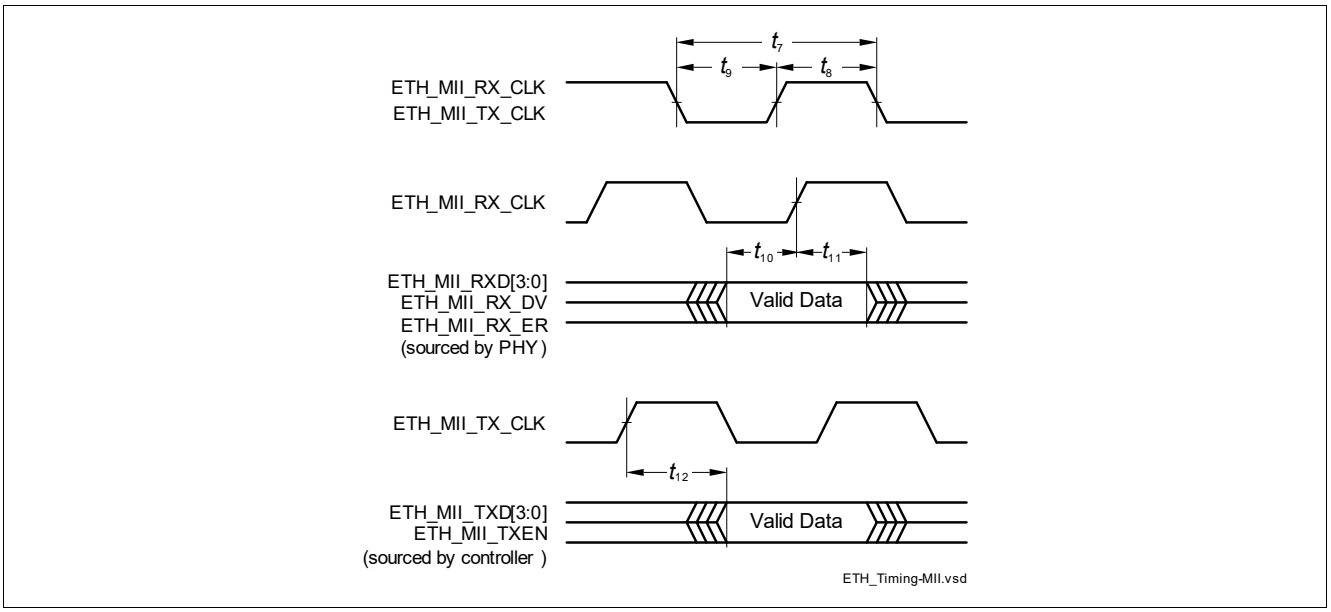

Figure 3-19 ETH MII Signal Timing

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3.24.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 3-56 ETH RMII Signal Timing Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	-	20	-	ns	50ppm ; CL=25pF
ETH_RMII_REF_CL clock high time	t_{14} SR	7 [1]	-	13 [2]	ns	CL=25pF
ETH_RMII_REF_CL clock low time	t_{15} SR	7 [1]	-	13 [2]	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time [3]	t_{16} CC	4	-	-	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time [3]	t_{17} CC	2	-	-	ns	CL=25pF

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.
3) For ETHRXD and ETHCRSDV signals this parameter is a SR.

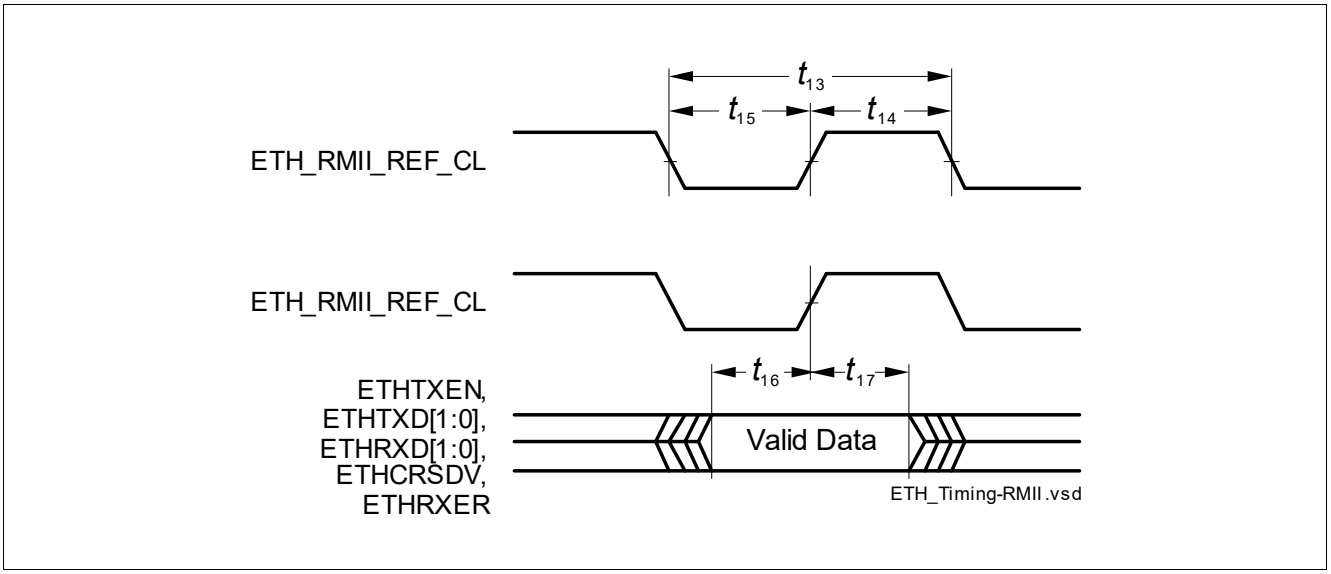

Figure 3-20 ETH RMII Signal Timing

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3.24.5 ETH RGMII Parameters

In the following, the parameters of the RGMII are described.

Table 3-57 ETH RGMII Signal Timing Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TX Clock period	t_{19} CC	36	40	44	ns	100Mbps
		360	400	440	ns	10Mbps
		7.2	8	8.8	ns	Gigabit
Data to Clock Output skew	t_{20} CC	-500	0	500	ps	
Data to Clock input skew (at receiver)	t_{21} SR	1	1.8	2.6	ns	SKEWCTL.RXCFG = 0; SKEWCTL.TXCFG = 0
Clock duty cycle	t_{duty} CC	40	50	60	%	10/100Mbps
		45	50	55	%	Gigabit
GREFCLK duty cycle	t_{duty_in} SR	45	-	55	%	
GREFCLK Input accuracy	ACC SR	-0.005	-	0.005	%	

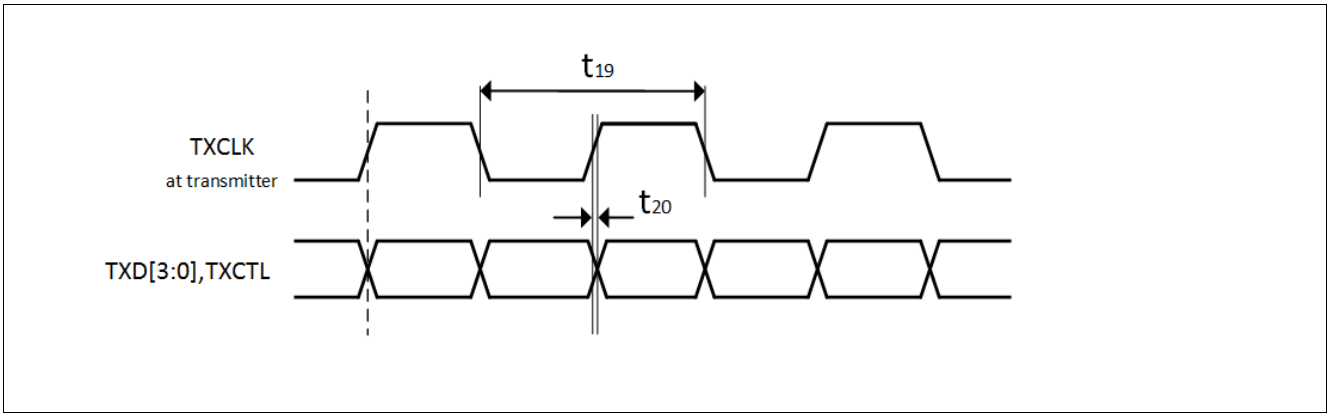

Figure 3-21 ETH RGMII TX Signal Timing (Delay on Destination (DoD))

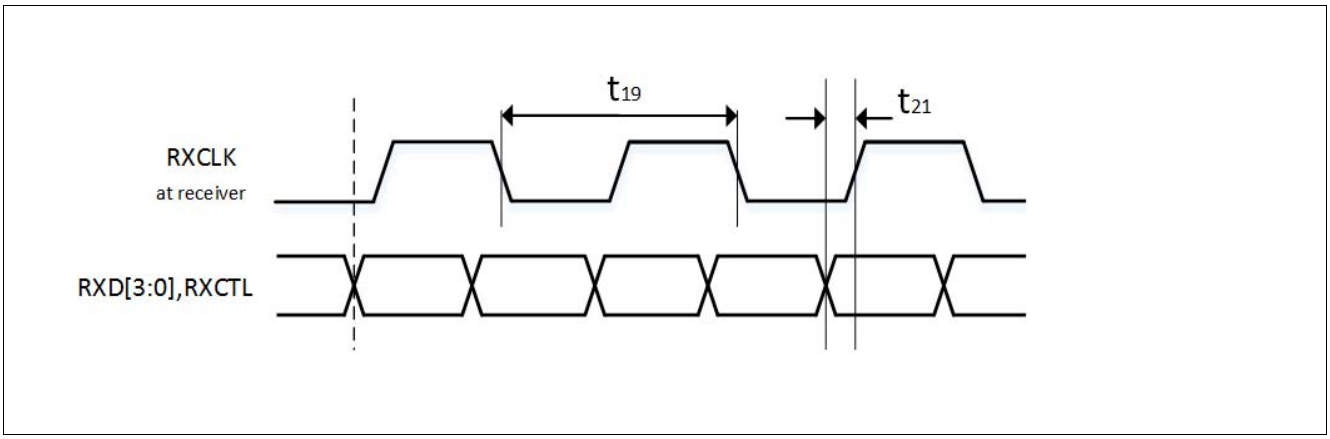

Figure 3-22 ETH RGMII RX Signal Timing (Delay on Source (DoS))

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3.25 E-Ray Parameters

The timings of this section are valid for the strong driver and sharp edge settings of the output drivers with C_L = 25 pF.

Table 3-58 Transmit Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25}$ CC	-	-	9	ns	C_L=25pF
Fall time of TxEN	$t_{dCCTxENFall25}$ CC	-	-	9	ns	C_L=25pF
Sum of rise and fall time	$t_{dCCTxRise25+dCCTxFall25}$ CC	-	-	9	ns	20% - 80% ; C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01}$ CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10}$ CC	-	-	25	ns	
Asymmetry of sending	t_{tx_asym} CC	-2.45	-	2.45	ns	C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01}$ CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10}$ CC	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	t_{txd_sum} CC	-	-	9	ns	

Table 3-59 Receive Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept25}$ SR	-30.5	-	43.0	ns	C_L=25pF
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept15}$ SR	-31.5	-	44.0	ns	C_L=15pF
Threshold for detecting logical high	$T_{uCCLogic1}$ SR	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0}$ SR	30	-	65	%	

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Table 3-59 Receive Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ CC	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ CC	-	-	10	ns	

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3.26 HSCT Parameters

Table 3-60 HSCT - Rx parasitics and loads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitance total budget	C_{total} CC	-	3.5	5	pF	Total Budget for complete receiver including silicon, package, pins and bond wire
Parasitic inductance budget	*Htotal* CC	-	5	-	nH	

Table 3-61 HSCT - Rx/Tx setup timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX o/p duty cycle	*DCrx* CC	40	-	60	%	
Disable time of the LVDS pad	$t_{LVDSDIS}$ CC	-	-	20	ns	
Enable time of the LVDS pad	t_{LVDSEN} CC	-	-	400	ns	
Wakeup time from Sleep Mode	t_{SWU} CC	-	-	250	ns	
Maximum length of a wake-up glitch that does not wake-up the receiver	t_{WUP} CC	-	-	0.2	ns	
Bias startup time	t_{bias} CC	-	5	10	µs	Bias distributor waking up from power down and provide stable Bias.
RX startup time	t_{rxi} CC	-	-	600	ns	Wake-up RX from power down.
TX startup time	t_{tx} CC	-	-	280	ns	Wake-up TX from power down.

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3.27 Inter-IC (I2C) Interface Timing

This section defines the timings for I2C in the TC38x.

All I2C timing parameter are SR for Master Mode and CC for Slave Mode.

Table 3-62 I2C Standard Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

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Table 3-62 I2C Standard Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Set-up time for (repeated) START condition	t_8	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-63 I2C Fast Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

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Table 3-63 I2C Fast Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Hold time for the (repeated) START condition	t_7	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-64 I2C High Speed Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Fall time of SCL	t_{11}	10 [1]	-	40 [1]	ns	bus line load of 100pF
Fall time of SDA	t_{12}	10 [1]	-	80 [1]	ns	bus line load of 100pF
Rise time of SCL	t_{13}	10 [1]	-	40 [1]	ns	bus line load of 100pF
Rise time of SDA	t_{14}	10 [1]	-	80 [1]	ns	bus line load of 100pF
Data hold time	t_3	0 [1]	-	70 [1]	ns	bus line load of 100pF
Data set-up time	t_4	10 [1]	-	-	ns	bus line load of 100pF
Low period of SCL clock	t_5	160 [1]	-	-	ns	bus line load of 100pF
High period of SCL clock	t_6	60 [1]	-	-	ns	bus line load of 100pF
Hold time for the (repeated) START condition	t_7	160 [1]	-	-	ns	bus line load of 100pF
Set-up time for (repeated) START condition	t_8	160 [1]	-	-	ns	bus line load of 100pF
Set-up time for STOP condition	t_9	160 [1]	-	-	ns	bus line load of 100pF

1) Values are defined for C_b = 100pF, for the Timing of C_b = 400pF see the I2C Standard.

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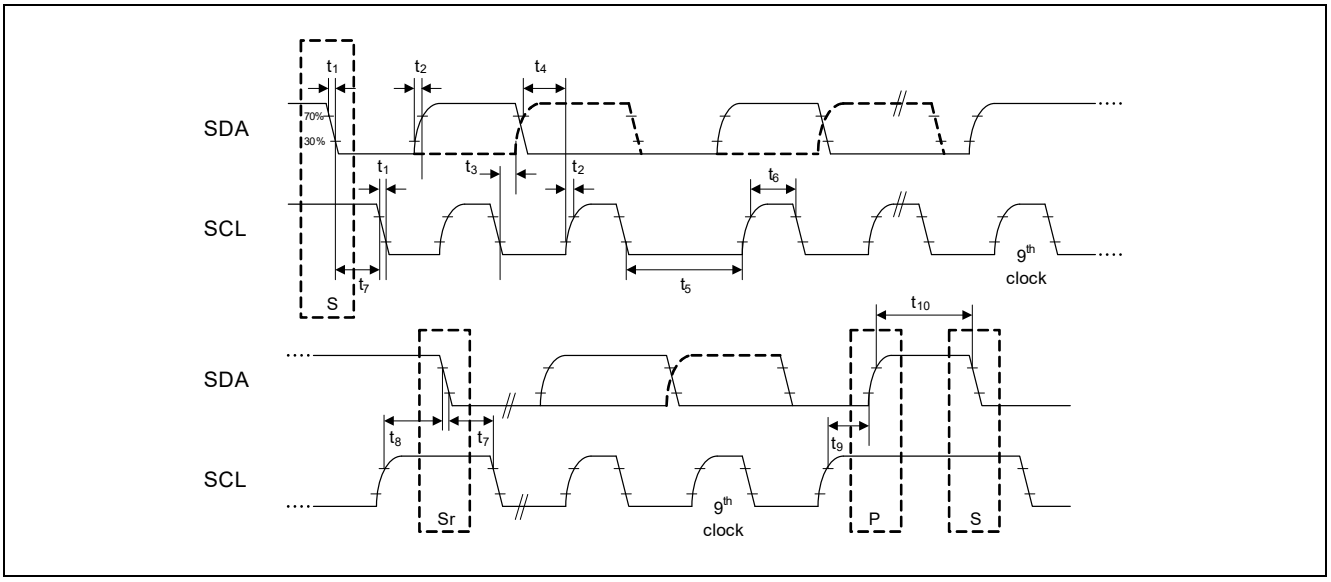

Figure 3-23 I2C Standard and Fast Mode Timing

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3.28 FSP Parameters

Table 3-65 Safety

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Skew between FSP0 and FSP1	$t_{FSPSKEW}$ CC	-8	-	9	ns	C_L=50pF, driver strength m
		-5	-	6	ns	C_L=50pF, driver strength sm
		-4	-	5	ns	C_L=50pF, driver strength ss

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3.29 Flash Target Parameters

Table 3-66 Flash

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector [1]	t_{ERP} CC	-	-	0.5	s	cycle count < 1000
Program Flash Erase Time per Multi-Sector Command [1]	t_{MERP} CC	-	-	0.5	s	For consecutive logical sectors in a physical sector with total range ≤ 512 kByte; cycle count < 1000
Program Flash program time per page in 5 V mode [1]	t_{PRP5} CC	-	-	80	µs	32 Byte
Program Flash program time per page in 3.3 V mode [1]	t_{PRP3} CC	-	-	115	µs	32 Byte
Program Flash program time per burst in 5 V mode [1]	t_{PRPB5} CC	-	-	220	µs	256 Byte
Program Flash program time per burst in 3.3 V mode [1]	t_{PRPB3} CC	-	-	530	µs	256 Byte
Program Flash program time for 1 MByte with burst programming in 3.3 V mode excluding communication [1]	t_{PRPB3_1MB} CC	-	-	2.2	s	Derived value for documentation purpose
Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication [1]	t_{PRPB5_1MB} CC	-	-	1	s	Derived value for documentation purpose
Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication [1]	t_{PRPB5_PF} CC	-	-	10	s	Derived value for documentation purpose
Write Page Once adder [1]	t_{ADD} CC	-	-	20	µs	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency [1]	t_{SPNDP} CC	-	-	120	µs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Disturb Limit (single ended sensing mode)	N_{DFD} CC	-	-	50	cycles	
Data Flash Erase Disturb Limit (complement sensing mode)	N_{DFDC} CC	-	-	500	cycles	
UCB Erase Disturb Limit	N_{UCBD} CC	-	-	500	cycles	

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Table 3-66 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page [1)2)]	t_{PRD} CC	-	-	75	µs	8 Byte
Complete Device Flash Erase Time PFlash and DFlash [1)3) 4) 5)]	t_{ER_Dev} CC	-	6.7	11.5	s	Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.
Data Flash program time per burst [1)2)]	t_{PRDB} CC	-	-	140	µs	32 Byte
Data Flash suspend to read latency [1)]	t_{SPNDD} CC	-	-	120	µs	
Wait time after margin change	$t_{FL_MarginDel}$ CC	-	-	2	µs	
Program Flash Endurance per Logical Sector	N_{E_P} CC	-	-	1000	cycles	Replace logical sector command shall be used if a sector fails during erase or program
Number of erase operations per physical sector in program flash	N_{ERP} CC	-	-	16000	cycles	
Program Flash Retention Time, Sector	t_{RET} CC	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	t_{RTU} CC	20	-	-	years	Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together
Data Flash access delay	t_{DF} CC	-	-	100	ns	see RFLASH of DMU register HF_DWAIT
Data Flash ECC Delay	t_{DFECC} CC	-	-	20	ns	see RECC of DMU register HF_DWAIT
Program Flash access delay	t_{PF} CC	-	-	30	ns	see RFLASH of DMU register HF_PWAIT
Program Flash ECC delay	t_{PFECC} CC	-	-	10	ns	see RECC and CECC of DMU register HF_PWAIT
Number of erase operations on DF0 over lifetime (complement sensing mode) [6)]	N_{ERD0C} CC	-	-	4000000	cycles	
Number of erase operations on DF0 over lifetime (single ended sensing mode) [7)]	N_{ERD0S} CC	-	-	750000	cycles	

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Table 3-66 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF1 over lifetime (complement sensing mode) [6]	N_{ERD1C} CC	-	-	2000000	cycles	
Number of erase operations on DF1 over lifetime (single ended sensing mode) [7]	N_{ERD1S} CC	-	-	500000	cycles	
Data Flash Endurance per EEPROMx sector (complement sensing mode) [8]	N_{E_EEP10C} CC	-	-	500000	cycles	Max. data retention time 10 years
DataFlash Endurance per EEPROMx sector (single ended sensing mode) [8]	N_{E_EEP10S} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Data Flash Endurance per HSMx sector (complement sensing mode) [8]	N_{E_HSMC} CC	-	-	250000	cycles	Max. data retention time 10 years
Data Flash Endurance per HSMx sector (single ended sensing mode) [8]	N_{E_HSMS} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Junction temperature limit for PFlash program/erase operations	$T_{JPFlash}$ SR	-	-	150	°C	
Data Flash Erase Time per Sector [1][3][5]	t_{ERD1} CC	-	-	0.5	s	Max. 1000 erase/program cycles
Data Flash Erase Time per Sector [1][3][5]	t_{ERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10 and NE_HSM parameters
DataFlash Adder on Erase Time per 32kByte erase size when using complement sensing mode [1]	$t_{ER_ADDC32C}$ CC	-	-	50	ms	Adder per 32 kByte on erase time; applicable only when using complement mode

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Table 3-66 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command [1)3)5)]	t_{MERD1} CC	-	-	0.5	s	Max 1000 erase/program cycles; For consecutive logical sectors ≤ 256KBytes
Data Flash Erase Time per Multi-Sector Command [1)3)5)]	t_{MERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10x and NE_HSMx Parameters; For consecutive logical sectors ≤ 256 kByte
Program Flash Access Delay at reduced VDDP3 voltage supply during cranking	$t_{PF_low_VDDP3}$ CC	-	-	60	ns	see register DMU_HF_PWAIT.CFLASH
Data Flash Erase Verify time per page (Complement Sensing) [2)]	$t_{VER_PAGE_DC}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Data Flash Erase Verify time per page (Single Ended Sensing) [1)]	$t_{VER_PAGE_DS}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page [1)]	$t_{VER_PAGE_P}$ CC	-	-	10	µs	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector (Complement Sensing) [1)]	$t_{VER_SEC_DC}$ CC	-	-	200	µs	Time per 2 KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per sector (Single Ended Sensing) [1)]	$t_{VER_SEC_DS}$ CC	-	-	360	µs	Time per 4 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector [1)]	$t_{VER_SEC_P}$ CC	-	-	360	µs	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline (Complement Sensing) [1)]	$t_{VER_WL_DC}$ CC	-	-	30	µs	
Data Flash Erase Verify time per wordline (Single Ended Sensing) [1)]	$t_{VER_WL_DS}$ CC	-	-	50	µs	
Program Flash Erase Verify time per wordline [1)]	$t_{VER_WL_P}$ CC	-	-	30	µs	

1) Only vaild for f_{FSI} = 100MHz.

2) Time is not dependent on program mode (5V or 3.3V).

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3) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
4) Using 512 kByte / 256 kByte erase commands (PFlash / DFlash).
5) If the DataFlash is operated in Complement Sensing Mode the erase time is increased by erase_size / 32kByte x tER_ADDC32C
6) Allows segmentation of addressable memory into 8 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD}.
7) Allows segmentation of addressable memory into 6 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD}.
8) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.

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3.30 Quality Declarations

Table 3-67 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	MSL CC	-	-	3		Conforming to Jedec J-STD--020C for 240C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	-	-	500 [1]	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	-	2000 [2]	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	V_{HBM1} SR	-	-	2000	V	
Operation Lifetime	t_{OP} CC	-	-	24500	hour	see below temperature profile as an example

1) Pads of the AGBT interface are limited to a maximum value of 250V.
2) Pads of the AGBT interface are limited to a maximum value of 1000V.

Example Temperature Profile

The following temperature profile is an example. Operation Lifetime plus Inactive time defines a 20 years period. Application specific temperature profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-68 Example Operation Lifetime Temperature Profile

T_J=	Duration [h]	Comment
≤ 170°C	≤ 30	
≤ 160°C	≤ 120	
≤ 150°C	≤ 220	
≤ 140°C	≤ 350	
≤ 130°C	≤ 780	
≤ 120°C	≤ 1600	
≤ 110°C	≤ 3000	
≤ 100°C	≤ 7000	
≤ 90°C	≤ 8000	
≤ 80°C	≤ 2400	
≤ 70°C	≤ 1000	
	≤ 24500	total time

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Table 3-69 Example Inactive Lifetime Temperature Profile

T_J=	Duration [h]	Comment
≤ 55°C	≤ 150700	

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3.31 Package Outline

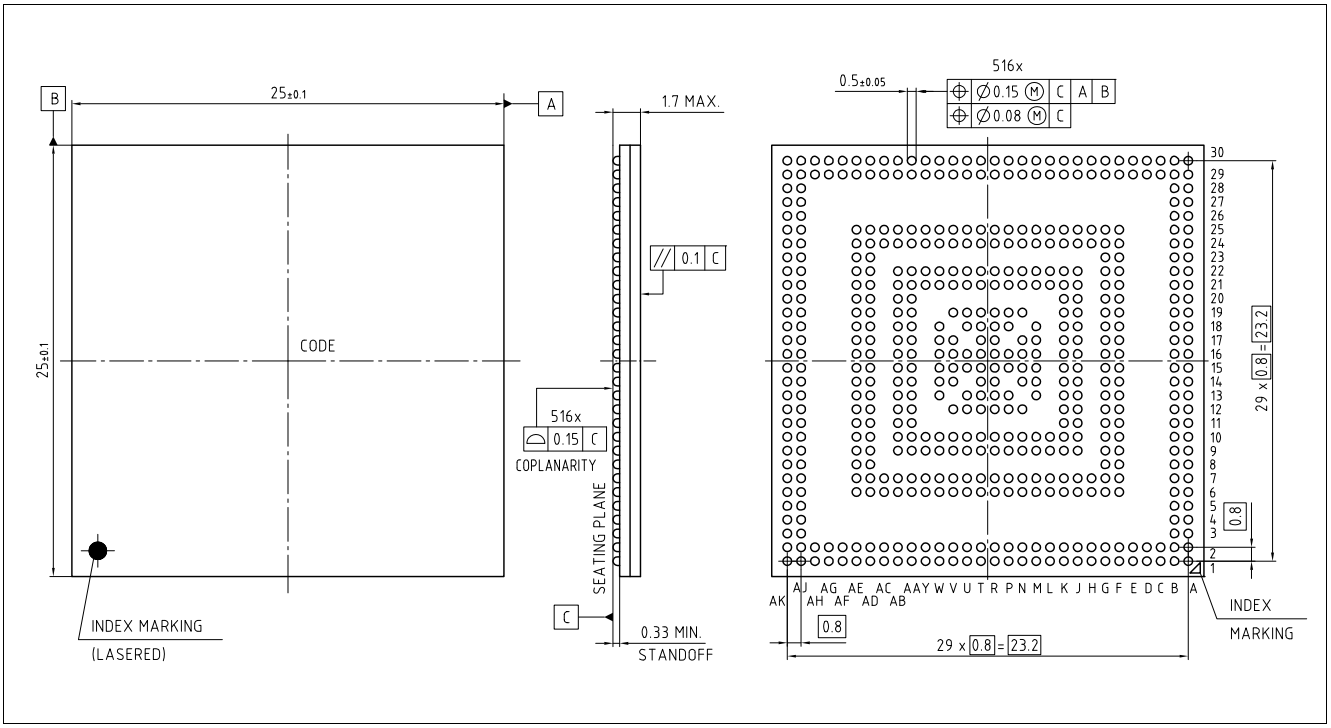

Figure 3-24 Package Outlines FBGA-516

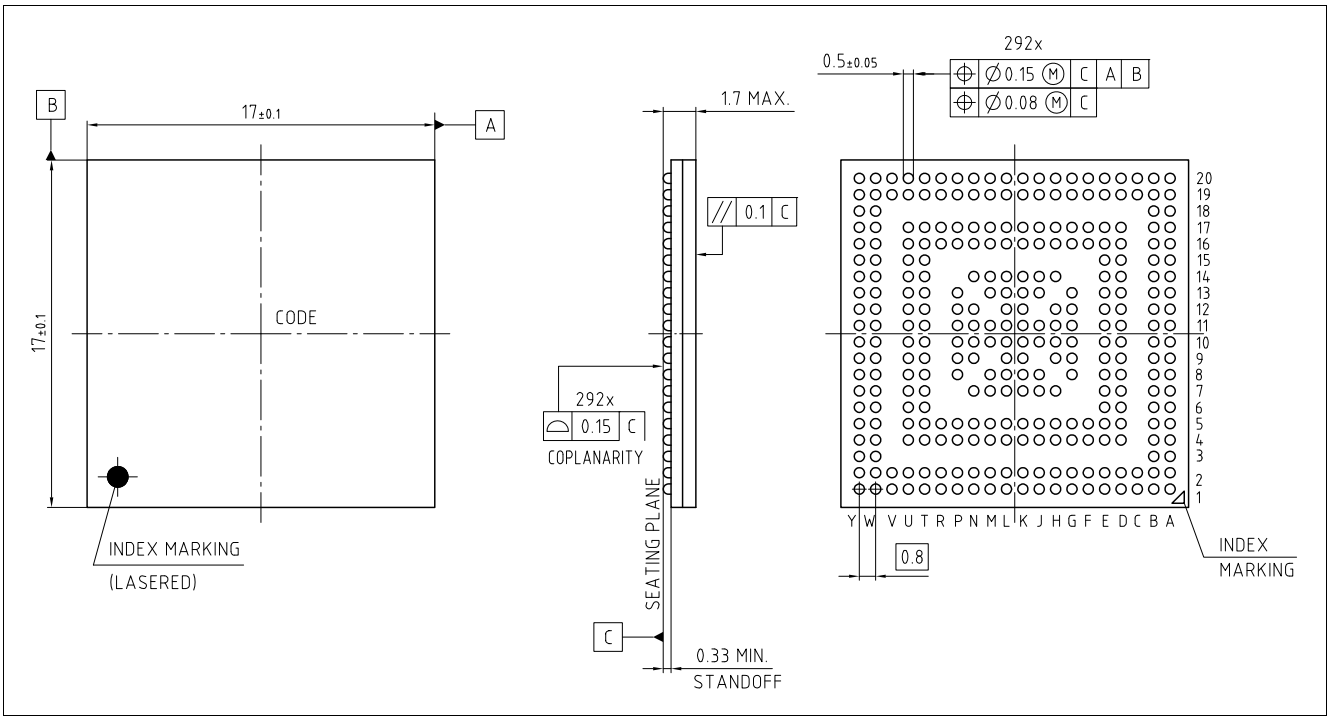

Figure 3-25 Package Outlines LFBGA-292

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

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3.31.1 Package Parameters

Table 3-70 Package Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to ambient) [1]	RTH_JA CC	-	-	14	K/W	FBGA516
		-	-	17	K/W	LFBGA292
Thermal resistance (junction to case bottom) [1]	RTH_JCB CC	-	-	3	K/W	FBGA516
		-	-	4	K/W	LFBGA292
Thermal resistance (junction to case top) [1]	RTH_JCT CC	-	-	5	K/W	FBGA516
		-	-	5	K/W	LFBGA292

1) The top and bottom thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) are to be combined with the thermal resistances between the junction and the case given above (RTH_JCT, RTH_JCB), in order to calculate the total thermal resistance between the junction and the ambient (RTH_JA). The thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) depend on the external system (PCB, case) characteristics and are under user responsibility. The junction temperature can be calculated using the following equation: TJ = TA + RTH_JA * PD, where the RTH_JA is the total thermal resistance between the junction and the ambient.
Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

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4 History

Version 0.4 is the first version of this document.

4.1 Changes from Version 0.4 to Version 0.6

- Update table Platform Feature Overview
- Changes in Pin Definition and Functions
  - Add pad type RFAST to Legend
  - Corrected ball assigmant to NC and NC1
  - P32.0 replece name from EVR13 to EVRC
  - P32.1 replece name from EVR13 to EVRC
  - Add Function description for GTM_TIM_INxx Symbols
  - Change numbering for GTM_TIM_INxx Symbols
  - Update Function description for CAN signals
  - Add missing Function description for EVADC
  - Add missing Function description for EDSADC
  - Add Function description for GTM_DTMxx Symbols
  - Update Function description for SCU_E_REQ signals
  - Change Symbol for SCU_E_REQ signals
  - Update Function description for SCU_PD_HWCFGx signals
  - remove PLL_WRAPPER_ANA_0_PAD_SYSCLK
  - Switch CBS_TGyz from inverted to non inverted
  - Add CCUEXTCLK0
  - Add EDSADC_EDS9NB to AN70
  - Add EDSADC_EDS9NB to AN71
  - Add PMS_DCDCSYNCO to P32.4
  - Add DAP3 to P21.6
  - Remove SDMMC_DS from P15.2
  - ADD TDI to P21.6
  - Add DAPE1 to P21.6
  - Add DAP2 to P21.7
  - ADD TDO to P21.7
  - Remove DAP Function description from P21.7 Input
  - Add EVADC_G5CH2 to AN50
  - Add EDSADC_EDS9PB to AN70
  - Add EDSADC_EDS9NB to AN71
- Changes in table 'Overload Parameters' of Overload
  - Change note of K_{OVDN} from "Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; -2mA < I_{IN} < 0mA" to "Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; -5mA < I_{IN} < 0mA"
  - Change max value of K_{OVDN} from '$6*10^{-4}$' to '$1*10^{-4}$'
  - Change max value of K_{OVDN} from '$1.7*10^{-3}$' to '$3*10^{-4}$'

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  - Change note of K_{OVDN} from "Overload injected on LVDS pad and affecting neighbor LVDS pads" to "Overload injected on LVDS TX pad and affecting neighbor LVDS pads"
  - Change max value of K_{OVDN} from '0.3' to '0.5'
  - Change note of K_{OVDP} from 'Overload injected on LVDS pad and affecting neighbor LVDS pads' to 'Overload injected on LVDS TX pad and affecting neighbor LVDS pads'
  - Change max value of K_{OVDP} from $5*10^{-4}$ to $5*10^{-3}$
  - Change max value of K_{OVDP} from '$1*10^{-5}$' to '$1.5*10^{-3}$'
  - Change max value of K_{OVAN} from $1*10^{-4}$ to $1*10^{-5}$
  - Change note of K_{OVAN} from 'Analog Inputs overlaid with class slow pads or pull down diagnostics; -1mA < I_{IN} < 0mA' to 'Analog Inputs overlaid with class slow pads or pull down diagnostics; -5mA < I_{IN} < 0mA'
  - Change max value of K_{OVAN} from $1*10^{-3}$ to $1*10^{-4}$
  - Change note of K_{OVAP} from '$1*10^{-5}$' to '$2*10^{-5}$'
  - Change note of K_{OVAP} from '$1*10^{-4}$' to '$2*10^{-4}$'
  - Add parameter I_{OUT}
- Operating Conditions
  - Change note of V_{DDM} from 'Lower voltage range' to ''
  - Change note of V_{EVRSB} from 'V_{EVRSB} is bonded together with V_{EXT} supply pin in smaller LQFP packages.' to ''
- Changes in table 'Fast 5V GPIO' of Standard Pads
  - Change note of HYS from '0.1 * $V_{EXT/FLEX}$ V' to '0.09 * $V_{EXT/FLEX}$ V'
  - Change note of HYS from '0.09 * $V_{EXT/FLEX}$ V' to '0.075 * $V_{EXT/FLEX}$ V'
  - Change min value of R_{DSON} from 140 Ohm to 125 Ohm
  - Change typ value of R_{DSON} from 200 Ohm to 225 Ohm
  - Change note of R_{DSON} from '260 Ohm' to '320 Ohm'
  - Change note of R_{DSON} from '35 Ohm' to '31 Ohm'
  - Change note of R_{DSON} from '50 Ohm' to '55 Ohm'
  - Change note of R_{DSON} from '65 Ohm' to '80 Ohm'
  - Change note of t_{RF} from "C_L = 25pF; driver = strong sharp edge" to "C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$"
  - Change note of t_{RF} from '2.8 ns' to '3.2 ns'
  - Change min value of t_{RF} from 0.5+0.075*C_L ns to 0.5+0.08*C_L ns
  - Change max value of t_{RF} from 0.5+0.15*C_L ns to 1.0+0.17*C_L ns
  - Change note of t_{RF} from '2.5+0.18*C_L ns' to '1.0+0.18*C_L ns'
  - Change note of t_{RF} from '2.5+0.35*C_L ns' to '5.0+0.35*C_L ns'
  - Change max value of t_{RF} from 4+0.95*C_L ns to 12+1.0*C_L ns
  - Change note of I_{OZ} from '-3900 nA' to '-5000 nA'
  - Change min value of I_{OZ} from -3600 nA to -5000 nA
  - Change min value of I_{OZ} from -6700 nA to -9000 nA
  - Change max value of I_{OZ} from 3900 nA to 5000 nA
  - Change max value of I_{OZ} from 3600 nA to 5000 nA
  - Change note of I_{OZ} from '6700 nA' to '9000 nA'
  - Change note of t_{RF} from 'C_L = 25pF; driver = strong sharp edge' to 'C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$'

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  - Change note of f_{IND} from '' to 'AL and TTL'
  - Change note of f_{OUTD} from '' to 'medium driver'
  - Change note of I_{PDL} from 'V_{IL}; AL or TTL' to 'V_{IL}; AL'
- Changes in table 'Fast 3.3V GPIO' of Standard Pads
  - Change note of *HYS* from '0.065 * $V_{EXT/FLEX}$ V' to '0.055 * $V_{EXT/FLEX}$ V'
  - Change min value of *HYS* from 0.1 * $V_{EXT/FLEX}$ V to 0.09 * $V_{EXT/FLEX}$ V
  - Change note of *HYS* from '0.07 * $V_{EXT/FLEX}$ V' to '0.055 * $V_{EXT/FLEX}$ V'
  - Change min value of R_{DSON} from 140 Ohm to 125 Ohm
  - Change note of R_{DSON} from '200 Ohm' to '225 Ohm'
  - Change note of R_{DSON} from '300 Ohm' to '320 Ohm'
  - Change note of R_{DSON} from '35 Ohm' to '31 Ohm'
  - Change typ value of R_{DSON} from 50 Ohm to 55 Ohm
  - Change max value of R_{DSON} from 77 Ohm to 80 Ohm
  - Change note of t_{RF} from "C_L = 25pF; driver = strong sharp edge" to "C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$"
  - Change note of t_{RF} from '2 ns' to '1.6 ns'
  - Change min value of t_{RF} from 4+0.57*C_L ns to 2+0.57*C_L ns
  - Change max value of t_{RF} from 0.75+0.15*C_L ns to 2.5+0.21*C_L ns
  - Change max value of t_{RF} from 1.5+0.38*C_L ns to 8+0.4*C_L ns
  - Change note of t_{RF} from '7+1.1*C_L ns' to '10+1.25*C_L ns'
  - Change min value of I_{PUH} from |19| µA to |17| µA
  - Change min value of I_{PUH} from |9| µA to |11| µA
  - Change min value of I_{PDL} from |18| µA to |15| µA
  - Change min value of I_{OZ} from -4100 nA to -5000 nA
  - Change min value of I_{OZ} from -3600 nA to -5000 nA
  - Change min value of I_{OZ} from -6700 nA to -9000 nA
  - Change max value of I_{OZ} from 4100 nA to 5000 nA
  - Change note of I_{OZ} from '3600 nA' to '5000 nA'
  - Change max value of I_{OZ} from 6700 nA to 9000 nA
  - Change note of t_{RF} from 'C_L = 25pF; driver = strong sharp edge' to 'C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$'
  - Change note of f_{OUTD} from '' to 'medium driver'
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Change min value of *HYS* from 0.1 * $V_{EXT/FLEX}$ V to 0.09 * $V_{EXT/FLEX}$ V
  - Change min value of *HYS* from 0.09 * $V_{EXT/FLEX}$ V to 0.075 * $V_{EXT/FLEX}$ V
  - Change min value of R_{DSON} from 140 Ohm to 125 Ohm
  - Change typ value of R_{DSON} from 200 Ohm to 225 Ohm
  - Change max value of R_{DSON} from 260 Ohm to 320 Ohm
  - Change note of t_{RF} from '4+0.95*C_L ns' to '12+1*C_L ns'
  - Change note of t_{RF} from '3.5+0.55*C_L ns' to '7+0.55*C_L ns'
  - Change note of I_{PUH} from 'V_{IH}; AL or TTL' to 'V_{IH}; AL or TTL; exept VGATE1P and T_J > 150°C'
  - Change note of I_{PUH} from 'V_{IL}; AL or TTL' to 'V_{IL}; AL or TTL; exept VGATE1P and T_J > 150°C'

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  - Change note of I_{PDL} from 'V_{IL}; AL or TTL' to 'V_{IL}; AL'
- Changes in table 'Slow 3.3V GPIO' of Standard Pads
  - Change min value of *HYS* from 0.1 * $V_{EXT/FLEX}$ V to 0.09 * $V_{EXT/FLEX}$ V
  - Change min value of *HYS* from 0.065 * $V_{EXT/FLEX}$ V to 0.055 * $V_{EXT/FLEX}$ V
  - Change min value of *HYS* from 0.07 * $V_{EXT/FLEX}$ V to 0.055 * $V_{EXT/FLEX}$ V
  - Change note of R_{DSON} from '140 Ohm' to '125 Ohm'
  - Change typ value of R_{DSON} from 200 Ohm to 225 Ohm
  - Change max value of R_{DSON} from 300 Ohm to 320 Ohm
  - Change note of t_{RF} from '4+0.57*C_L ns' to '2+0.57*C_L ns'
  - Change note of t_{RF} from '7+1.1*C_L ns' to '10+1.25*C_L ns'
  - Change note of I_{PUH} from 'V_{IH}; AL and TTL (degraded, used for CIF)' to 'V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P and T_J > 150°C'
  - Change min value of I_{PUH} from |19| µA to |17| µA
  - Change note of I_{PUH} from "V_{IH}; TTL" to "V_{IH}; TTL; exept VGATE1P and T_J > 150°C"
  - Change note of I_{PUH} from '|9| µA' to '|11| µA'
  - Change min value of I_{PDL} from |18| µA to |15| µA
  - Change note of I_{PUH} from 'V_{IL}; AL and TTL and TTL (degraded, used for CIF)' to 'V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P and T_J > 150°C'
  - Change note of f_{OUTD} from '' to 'medium driver'
- Changes in table '$\overline{\text{PORST}}$ Pad' of Standard Pads
  - Change note of *HYS* from 'non of the neighbor pads are used as output; TTL' to 'non of the neighbor pads are used as output;TTL (degraded, used for CIF)'
  - Change min value of *HYS* from 0.1 * $V_{EXT/FLEX}$ V to 0.055 * $V_{EXT/FLEX}$ V
  - Change note of I_{PDL} from '|18| µA' to '|15| µA'
  - Change note of *HYS* from 'two of the neighbor pads are used as output with driver=strong and edge=sharp; TTL' to 'two of the neighbor pads are used as output with driver=strong and edge=sharp; TTL (degraded, used for CIF)'
- Changes in table 'Class S 5V' of Standard Pads
  - Change min value of *HYS* from 0.1 * $V_{EXT/FLEX}$ V to 0.09 * $V_{EXT/FLEX}$ V
  - Change min value of *HYS* from 0.09 * $V_{EXT/FLEX}$ V to 0.075 * $V_{EXT/FLEX}$ V
  - Change note of I_{PDL} from 'V_{IL}; AL or TTL' to 'V_{IL}; AL'
- Changes in table 'RFast 3.3V pad' of Standard Pads
  - Change min value of *HYS* from 0.065 * $V_{EXT/FLEX}$ V to 0.055 * $V_{EXT/FLEX}$ V
  - Change min value of *HYS* from 0.1 * $V_{EXT/FLEX}$ V to 0.09 * $V_{EXT/FLEX}$ V
  - Change min value of *HYS* from 0.07 * $V_{EXT/FLEX}$ V to 0.055 * $V_{EXT/FLEX}$ V
  - Change min value of R_{DSON} from 140 Ohm to 125 Ohm
  - Change typ value of R_{DSON} from 200 Ohm to 225 Ohm
  - Change note of R_{DSON} from '300 Ohm' to '320 Ohm'
  - Change note of R_{DSON} from '35 Ohm' to '31 Ohm'
  - Change typ value of R_{DSON} from 50 Ohm to 55 Ohm
  - Change max value of R_{DSON} from 77 Ohm to 80 Ohm
  - Change note of R_{DSON} from '10 Ohm' to '8 Ohm'

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  - Change note of t_{RF} from 'C_L = 25pF; driver = strong sharp edge' to 'C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$'
  - Change min value of t_{RF} from 2 ns to 1.6 ns
  - Change min value of t_{RF} from 4+0.57*C_L ns to 2+0.57*C_L ns
  - Change note of t_{RF} from '0.75+0.15*C_L ns' to '2.5+0.21*C_L ns'
  - Change max value of t_{RF} from 1.5+0.38*C_L ns to 8+0.4*C_L ns
  - Change max value of t_{RF} from 7+1.1*C_L ns to 10+1.25*C_L ns
  - Change min value of I_{PUH} from |19| µA to |17| µA
  - Change note of I_{PUH} from '|9| µA' to '|11| µA'
  - Change min value of I_{PDL} from |18| µA to |15| µA
  - Change note of t_{RF} from 'C_L = 25pF; driver = strong sharp edge' to 'C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$'
  - Change note of f_{OUTD} from '' to 'medium driver'
- Changes in table 'RFast 5V GPIO' of Standard Pads
  - Change min value of *HYS* from 0.1 * $V_{EXT/FLEX}$ V to 0.09 * $V_{EXT/FLEX}$ V
  - Change note of *HYS* from '0.09 * $V_{EXT/FLEX}$ V' to '0.075 * $V_{EXT/FLEX}$ V'
  - Change min value of R_{DSON} from 140 Ohm to 125 Ohm
  - Change max value of R_{DSON} from 260 Ohm to 320 Ohm
  - Change typ value of R_{DSON} from 200 Ohm to 225 Ohm
  - Change note of R_{DSON} from '35 Ohm' to '31 Ohm'
  - Change max value of R_{DSON} from 65 Ohm to 80 Ohm
  - Change note of R_{DSON} from '50 Ohm' to '55 Ohm'
  - Change note of t_{RF} from '2.5+0.18*C_L ns' to '1.0+0.18*C_L ns'
  - Change note of t_{RF} from "C_L = 25pF; driver = strong sharp edge" to "C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$"
  - Change note of t_{RF} from '2.8 ns' to '3.2 ns'
  - Change min value of t_{RF} from 0.5+0.075*C_L ns to 0.5+0.08*C_L ns
  - Change note of t_{RF} from '0.5+0.15*C_L ns' to '1.0+0.17*C_L ns'
  - Change max value of t_{RF} from 4+0.95*C_L ns to 12+1.0*C_L ns
  - Change note of t_{RF} from '2.5+0.35*C_L ns' to '5.0+0.35*C_L ns'
  - Change note of t_{RF} from 'C_L = 25pF; driver = strong sharp edge' to 'C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$'
  - Change note of f_{IND} from '' to 'AL and TTL'
  - Change note of f_{OUTD} from '' to 'medium driver'
  - Change note of I_{PDL} from 'V_{IL}; AL or TTL' to 'V_{IL}; AL'
- Changes in table 'Class D' of Standard Pads
  - Update footnote of *Standard Pads* to 'For AN11 200 nA need to be added.'
  - Change note of I_{OZ} from 'T_J ≤ 150°C; PDD option available, or AltRef option available and EDSADC channel connected' to 'T_J ≤ 150°C; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected'
- Changes in table 'LVDS - IEEE standard LVDS general purpose link (GPL)' of LVDS Pads
  - Change max value of t_{rise20} from 0.5 ns to 0.75 ns
  - Change max value of t_{fall20} from 0.5 ns to 0.75 ns

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  - Change max value of V_{OD} from 450 mV to 500 mV
  - Change min value of V_{OD} from 360 mV to 380 mV
- VADC 5V
  - Change note of dV_{CSD} from '-20 %' to '-10 %'
  - Change note of dV_{CSD} from '20 %' to '10 %'
  - Change note of f_{ADCI} from 'Upper voltage range' to '4.5V ≤ V_{DDM} ≤ 5.5V'
  - Change note of t_{SCAL} from 'Upper voltage range' to '4.5V ≤ V_{DDM} ≤ 5.5V'
  - Change note of f_{ADCI} from 'Lower voltage range' to '2.97V ≤ V_{DDM} < 4.5V'
  - Change note of t_S from 'Primary group or fast compare channel, upper voltage range; input buffer disabled' to 'Primary group or fast compare channel, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer disabled'
  - Change note of t_{SCAL} from 'Lower voltage range' to '2.97V ≤ V_{DDM} < 4.5V'
  - Change note of t_S from 'Primary group or fast compare channel, upper voltage range; input buffer enabled' to 'Primary group or fast compare channel, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer enabled'
  - Change note of t_S from 'Secondary group, upper voltage range; input buffer disabled' to 'Secondary group, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer disabled'
  - Change note of t_S from 'Secondary group, upper voltage range; input buffer enabled' to 'Secondary group, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer enabled'
  - Change note of t_S from 'Primary Group or fast compare channel, lower voltage range; input buffer disabled' to 'Primary Group or fast compare channel, 2.97V ≤ V_{DDM} < 4.5V; input buffer disabled'
  - Change note of t_S from 'Primary group or fast compare channel, lower voltage range; input buffer enabled' to 'Primary group or fast compare channel, 2.97V ≤ V_{DDM} < 4.5V; input buffer enabled'
  - Change note of t_S from 'Secondary group, lower voltage range; input buffer disabled' to 'Secondary group, 2.97V ≤ V_{DDM} < 4.5V; input buffer disabled'
  - Change note of t_S from 'Secondary group, lower voltage range; input buffer enabled' to 'Secondary group, 2.97V ≤ V_{DDM} < 4.5V; input buffer enabled'
- DSADC 5V
  - Update wording in front of table DSADC 5V
  - Change note of *DCF* from '10^{-5} f_D, offset compensation filter enabled (FCFGMx.OEN = 001_B)' to '10^{-5} f_D, offset compensation filter enabled (FCFGMx.OCEN = 001_B)'
- OSC_XTAL
  - Add parameter C_{XTAL1}
  - Change typ value of C_{L1} from 2.35 pF to 3.35 pF
- Changes in table 'DTS PMS' of DTS
  - Change max value of t_M from 2.6 ms to 2.7 ms
- Add table 'DTS Core'
- Current Consumption
  - Update footnote of $C_{\text{urrent Consumption}}$ to 'A single DS channel instance consumes 4 mA.'
  - Change note of I_{DDRAIL} from '800 mA' to '840 mA'
  - Change note of I_{DDRAIL} from '920 mA' to '1100 mA'
  - Change note of I_{DDRAIL} from '960 mA' to '1100 mA'
  - Change note of I_{DDRAIL} from '1020 mA' to '1100 mA'
  - Change note of I_{DDRAIL} from '1110 mA' to '1100 mA'
  - Change note of I_{DDRAIL} from '1099 mA' to '1100 mA'

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- Changes in table 'Module Core Current Consumption' of Current Consumption
  - Change name of *Module Core Current Consumption* from Module Core Current Concumption to Module Core Current Consumption
  - Change max value of I_{DDCx0} from 40 mA to 45 mA
  - Change note of I_{DDCx0} from 'real power pattern' to 'real power pattern; IPC=0.6'
  - Change note of I_{DDCx0} from '60 mA' to '70 mA'
  - Change note of I_{DDCx0} from "max power pattern" to "max power pattern; IPC=1.2"
  - Change max value of I_{DDCxx} from I_{DDCx0} + 60 mA to I_{DDCx0} + 50 mA
  - Change note of I_{DDCxx} from 'max power pattern' to 'max power pattern; IPC=1.2'
  - Change max value of I_{DDGTM} from 60 mA to 100 mA
  - Change note of I_{DDGTM} from 'real power pattern; TIMx, TOMx, ATOMx , MCSx active. 5 clusters at 200 MHz.' to 'real power pattern; TIMx, TOMx, ATOMx , MCSx active. 3 clusters at 200 MHz.'
  - Change max value of I_{DDGTM} from 88 mA to 120 mA
  - Change note of $I_{DDMBIST}$ from '100 mA' to '200 mA'
  - Change note of I_{DDCxx} from 'real power pattern' to 'real power pattern; IPC=0.6'
  - Change max value of I_{DDGTM} from 20 mA to 50 mA
  - Change note of I_{DDGTM} from 'TIMx, TOMx active at 100MHz. ATOMx , MCSx, DPLL inactive.' to 'TIMx, TOMx active at 100MHz. ATOMx , MCSx, DPLL inactive. 2 clusters at 100 MHz.'
  - Change max value of $I_{EXTRAIL}$ from 58 mA to 50 mA
  - Change max value of $I_{EXTRAIL}$ from t.b.d mA to 56 mA
  - Change max value of $I_{EXTFLEX}$ from 30 mA to 18 mA
- Changes in table 'Module Current Consumption' of Current Consumption
  - Change max value of $I_{EXTLVDS}$ from t.b.d mA to 20 mA
  - Change note of I_{SCRSB} from '4 mA' to '6.5 mA'
  - Change note of I_{SCRSB} from "SCR 8-bit Standby Controller in STANDBY Mode drawn at V_{EVRSB} supply pin" to "SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin"
  - Change note of I_{SCRSB} from "Additional SCR 8-bit Standby Controller current in STANDBY Mode drawn at V_{EVRSB} supply pin" to "SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin"
  - Change note of I_{SCRSB} from "SCR 8-bit Standby Controller current in STANDBY Mode incl. PMS current drawn at V_{EVRSB} supply pin" to "SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin"
  - Change note of I_{SCRSB} from "SCR power pattern; f_{SYS_SCR} = 20MHz; T_J=150°C" to "SCR power pattern incl. PMS current consumption with fback clock active; f_{SYS_SCR} = 20MHz; T_J=150°C"
  - Change typ value of I_{SCRSB} from 0.025 mA to 0.190 mA
  - Change note of I_{SCRSB} from 'real power pattern; fSYS_SCR = 70kHz; T_J=25°C' to 'SCR power pattern incl. PMS current consumption with fback inactive; fSYS_SCR = 70kHz; T_J=25°C'
  - Change note of I_{SCRSB} from "SCR 8-bit Standby Controller in STANDBY Mode drawn at V_{EVRSB} supply pin" to "SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin"
  - Change note of I_{DDM} from '66 mA' to '32 mA'
  - Change note of I_{DDM} from "real power pattern ; current for EDSADC module only; 11 EDSADC channels active." to "real power pattern; current for EDSADC modules only and EVADC modules are inactive; 8 EDSADC channels active continuously."
  - Change note of I_{DDM} from '60 mA' to '45 mA'

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- Change note of I_{DDM} from "max power pattern; All EDSADC channels active 100% time." to "max power pattern; current for EDSADC modules only and EVADC modules are inactive; all EDSADC channels active continuously."
- Change note of I_{DDM} from 'real pattern;12 EVADC modules active' to 'real power pattern; current for EVADC modules only and EDSADC modules are inactive; 12 EVADC modules active.'
- Change max value of I_{DDM} from 21 mA to 20 mA
- Change note of I_{DDM} from 'max power pattern; All EVADC modules are active 100% time' to 'max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.'
- Change max value of I_{DDM} from 56 mA to 48 mA
- Change max value of I_{SLEEP} from 10 mA to 25 mA
- Change max value of I_{DDTOT} from 924 mA to 978 mA
- Change max value of *PD* from t.b.d. mW to 1700 mW
- Change max value of *PD* from t.b.d. mW to 2400 mW
- Change note of $I_{DDTOTDC5}$ from 't.b.d mA' to '440 mA'
- Change note of $I_{DDTOTDC5}$ from "real power pattern; V_{EXT} = 5V; T_J=150°C" to "real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 5V; T_J=150°C"
- Change description of $I_{DDTOTDC5}$ from '∑ Sum of all currents with DC-DC EVR13 regulator active' to '∑ Sum of all currents with DC-DC EVRC regulator active'
- Change max value of $I_{DDTOTDC3}$ from t.b.d. mA to 580 mA
- Change note of $I_{DDTOTDC3}$ from 'real power pattern; V_{EXT} = 3.3V; T_J=150°C' to 'real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V; T_J=150°C'
- Change description of $I_{DDTOTDC3}$ from '∑ Sum of all currents with DC-DC EVR13 regulator active' to '∑ Sum of all currents with DC-DC EVRC regulator active'
- Change max value of I_{EVRSB} from 4 mA to 8 mA
- Change note of $I_{DDPORST}$ from '430 mA' to '490 mA'

- Reset
  - Change min value of t_{POH} from 100 ns to 150 ns
  - Change note of t_{BP} from '*dV/dT*=1*V/ms*. including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time is not included' to '*dVEXT/dT*=1*V/ms*. *VEXT*>*VLVDRST5*. Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.'
  - Change note of t_B from 'operating with max. frequencies' to 'operating with max. frequencies, with valid BMI header'
  - Change note of t_{BS} from '' to 'RAM initialization and HSM boot time are not included, with valid BMI header'
  - Change note of t_{BP} from 'Firmware execution time; without EVR ramp-up; RAM initialization and HSM boot time is not included' to 'Firmware execution time after warm PORST without EVR ramp-up; RAM initialization and HSM boot time is not included'
  - Change type of t_{POA} from CC to SR
  - Change description of t_{POA} from 'Minimum PORST active hold time externally after power supplies are stable at operating levels' to 'Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up'
- PMS/EVR33 LDO
  - Change min value of C_{OUT} from 0.65 µF to 1.45 µF
  - Change note of C_{OUT} from '1.35 µF' to '3 µF'
  - Change note of C_{OUT} from '1 µF' to '2.2 µF'

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  - Change min value of *dVout/dIout* from -100 mV to -180 mV
  - Change max value of *dVout/dIout* from 100 mV to 180 mV
  - Change note of I_{MAX} from '100 mA' to '60 mA'
  - Change note of *dVout/dVin* from '*dVin/dT*=50*V/ms*; *dV*= 5 to 3.6*V*' to '*dVin/dT*=50*V/ms*; *dV*= 5 to 3.6*V*; I_{MAX}=60*mA*'
  - Change note of *dVout/dVin* from '*dVin/dT*=50*V/ms*; *dV*= 3.6 to 5*V*' to '*dVin/dT*=50*V/ms*; *dV*= 3.6 to 5*V*; I_{MAX}=60*mA*'
- PMS/Supply Monitors
  - Change note of $V_{LVDRST5}$ from '2.7 V' to '2.75 V'
  - Change note of $V_{LVDRST5}$ from '2.67 V' to '2.72 V'
- PMS/Supply Ramp
  - Change description of *SR_V_EXT* from 'External V_{EXT} & V_{EVRSB} supply ramp' to 'External V_{EXT} & V_{EVRSB} supply ramp-up and ramp-down slope'
  - Change description of *SR_V_DDP3* from 'External V_{DDP3} supply ramp' to 'External V_{DDP3} supply ramp-up and ramp-down slope'
  - Change description of *SR_V_DD* from 'External V_{DD} supply ramp' to 'External V_{DD} supply ramp-up and ramp-down slope'
  - Change description of *SR_V_DDM* from 'External V_{DDM} supply ramp' to 'External V_{DDM} supply ramp-up and ramp-down slope'
- Changes in table 'EVRC SMPS' of PMS/EVRC SMPS
  - Change name of *EVRC SMPS* from EVR13 SMPS to EVRC SMPS
- Changes in table 'EVRC SMPS External components' of PMS/EVRC SMPS
  - Change name of *EVRC SMPS External components* from EVR13 SMPS External components to EVRC SMPS External components
- Changes in section JTAG Parameters
  - Update figure Test Clock Timing (TCK)
- Changes in section DAP Parameters
  - Combine figures Test Clock Timing (DAP0), DAP Timing Host to Device, and DAP Timing Device to Host (DAP1 and DAP2 pins) into single figure DAP Timing
  - Add t_{14} for condition F=40MHz
  - Add t_{15} for condition F=40MHz
  - Add t_{16} for condition F=40MHz
- Changes in table 'Master Mode strong sharp (ss) output pads' of ASCLIN
  - Change min value of t_{51} from -3 ns to -3.5 ns
  - Change max value of t_{51} from 3 ns to 3.5 ns
  - Change max value of t_{510} from 3 ns to 3.5 ns
- Changes in table 'Master Mode Timing, LVDS output pads for data and clock' of QSPI
  - Change note of t_{51} from '3 ns' to '4 ns'
  - Change note of t_{52} from '17 ns' to '18 ns'
- Changes in table 'Strong sharp (ss) driver for clock/data valid for 5V' of MSC
  - Change min value of t_{45} from -3 ns to -4 ns
  - Change note of t_{44} from '-3 ns' to '-4 ns'
- Changes in table 'ETH RGMII Signal Timing Parameters valid for 3.3V' of Ethernet

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  - Add parameter t_{21}
- Changes in table 'ETH RMII Signal Timing Parameters valid for 3.3V' of Ethernet
  - Change description of t_{16} from 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; setup time' to 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time'
  - Change description of t_{17} from 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; hold time' to 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time'
- Changes in table 'HSCT - Rx/Tx setup timing' of LVDS Pads
  - Change max value of t_{tx} from 250 ns to 280 ns
- Flash
  - Change note of t_{ER_Dev} from "Derived value for documentation purpose" to "Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose."
  - Change note of t_{ER_Dev} from '17.8 s' to '11.5 s'
  - Change max value of t_{PRPB5_PF} from 16 s to 10 s
- Package Parameters
  - Update table Thermal Characteristics of the Package
  - Change package type from PG-LFBGA-516-9 to PG-LBGA-516-1
  - Change package type from PG-LFBGA-292-9 to PG-LFBGA-292-11

4.2 Changes from Version 0.6 to Version 0.7

- Changed step description from “AA” to “AB”
- Update of Data Flash to 512 KB in “Platform Feature Overview”
- Update AGBT to “no” in Platform feature overview table
- “BBB frequency” from table “Operating Conditions
- Update Ctrl. for Pin ESR0
- Update Ctrl. for Pin ESR1
- Absolute Maximum Ratings
  - Change description of V_{DDM} from 'Voltage at V_{DDM}, V_{EXT} and V_{FLEX} power supply pins with respect to V_{SS}' to 'Voltage at V_{DDM}, V_{EXT}, V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}'
- Changes in table 'Overload Parameters' of Overload
  - Change note of I_{IN} from 'except LVDS pins' to 'except LVDS pins; limited to max. Operation Livetime hours'
  - Change note of I_{INLVDS} from '' to 'limited to max. Operation Livetime hours'
  - Change note of I_{ID} from 'All power supply voltages V_{DDx} = 0' to 'All power supply voltages V_{DDx} = 0; limited to max. Inactive Livetime hours'
  - Change note of I_{OUT} from '100% duty cycle; output driver = strong' to '100% duty cycle; output driver = strong; limited to max. Operation Livetime hours'
  - Change of “Pin Reliability in Overload” praeamble
- Changes in table 'Slow 3.3V GPIO' of Standard Pads
  - Change note of V_{IL} from '0.44 * $V_{EXT/FLEX}$ V' to '0.42 * $V_{EXT/FLEX}$ V'
  - Change note of I_{PUH} from 'V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P and T_J > 150°C' to 'V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C'

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  - Change note of I_{PUH} from 'V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P and T_J > 150°C' to 'V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change note of I_{PUH} from 'V_{IH}; TTL; exept VGATE1P and T_J > 150°C' to 'V_{IH}; TTL; exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
  - Change min value of I_{OZ} from -200 nA to -300 nA
  - Change max value of I_{OZ} from 200 nA to 300 nA
  - Change min value of I_{OZ} from -250 nA to -400 nA
  - Change max value of I_{OZ} from 250 nA to 400 nA
  - Change min value of I_{OZ} from -300 nA to -600 nA
  - Change max value of I_{OZ} from 300 nA to 600 nA
  - Change min value of I_{OZ} from -500 nA to -750 nA
  - Change max value of I_{OZ} from 500 nA to 750 nA
  - Change min value of I_{OZ} from -350 nA to -300 nA
  - Change max value of I_{OZ} from 350 nA to 300 nA
  - Change min value of I_{OZ} from -550 nA to -400 nA
  - Change max value of I_{OZ} from 550 nA to 400 nA
  - Change min value of I_{OZ} from -700 nA to -600 nA
  - Change max value of I_{OZ} from 700 nA to 600 nA
  - Change min value of I_{OZ} from -1100 nA to -750 nA
  - Change max value of I_{OZ} from 1100 nA to 750 nA
  - Change max value of I_{OZ} from 11000 nA to 18000 nA
  - Change note of I_{OZ} from '-11000 nA' to '-18000 nA'
  - Change max value of I_{OZ} from 22000 nA to 38000 nA
  - Change min value of I_{OZ} from -22000 nA to -38000 nA
- Changes in table 'RFast 3.3V pad' of Standard Pads
  - Change note of V_{IL} from '0.44 * $V_{EXT/FLEX}$ V' to '0.42 * $V_{EXT/FLEX}$ V'
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'Fast 3.3V GPIO' of Standard Pads
  - Change note of V_{IL} from '0.44 * $V_{EXT/FLEX}$ V' to '0.42 * $V_{EXT/FLEX}$ V'
  - Change note of I_{OZ} from '-750 nA' to '-1100 nA'
  - Change note of I_{OZ} from '750 nA' to '1100 nA'
  - Change min value of I_{OZ} from -5000 nA to -6000 nA
  - Change note of I_{OZ} from '5000 nA' to '6000 nA'
  - Change min value of I_{OZ} from -1300 nA to -2000 nA
  - Change max value of I_{OZ} from 1300 nA to 2000 nA
  - Change min value of I_{OZ} from -2000 nA to -2500 nA
  - Change note of I_{OZ} from '2000 nA' to '2500 nA'
  - Change max value of I_{OZ} from 9000 nA to 13500 nA
  - Change min value of I_{OZ} from -9000 nA to -13500 nA

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  - Change note of I_{OZ} from '-2300 nA' to '-1100 nA'
  - Change min value of I_{OZ} from -5000 nA to -2000 nA
  - Change note of I_{OZ} from '2300 nA' to '1100 nA'
  - Change max value of I_{OZ} from 5000 nA to 2000 nA
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'Fast 5V GPIO' of Standard Pads
  - Change max value of I_{OZ} from 750 nA to 1100 nA
  - Change min value of I_{OZ} from -750 nA to -1100 nA
  - Change min value of I_{OZ} from -5000 nA to -6000 nA
  - Change max value of I_{OZ} from 5000 nA to 6000 nA
  - Change note of I_{OZ} from '-1300 nA' to '-2000 nA'
  - Change max value of I_{OZ} from 1300 nA to 2000 nA
  - Change min value of I_{OZ} from -2000 nA to -2500 nA
  - Change max value of I_{OZ} from 2000 nA to 2500 nA
  - Change note of I_{OZ} from '9000 nA' to '13500 nA'
  - Change min value of I_{OZ} from -9000 nA to -13500 nA
  - Change note of I_{OZ} from '-2300 nA' to '-1100 nA'
  - Change note of I_{OZ} from '-5000 nA' to '-2000 nA'
  - Change max value of I_{OZ} from 2300 nA to 1100 nA
  - Change max value of I_{OZ} from 5000 nA to 2000 nA
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Change note of I_{OZ} from '-250 nA' to '-400 nA'
  - Change max value of I_{OZ} from 250 nA to 400 nA
  - Change min value of I_{OZ} from -350 nA to -600 nA
  - Change max value of I_{OZ} from 350 nA to 600 nA
  - Change note of I_{OZ} from '500 nA' to '750 nA'
  - Change note of I_{OZ} from '-500 nA' to '-750 nA'
  - Change min value of I_{OZ} from -200 nA to -300 nA
  - Change max value of I_{OZ} from 200 nA to 300 nA
  - Change note of I_{PUH} from 'V_{IH}; AL or TTL; exept VGATE1P and T_J > 150°C' to 'V_{IH};AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change note of I_{PUH} from 'V_{IL}; AL or TTL; exept VGATE1P and T_J > 150°C' to 'V_{IL}; AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
  - Change min value of I_{OZ} from -350 nA to -300 nA
  - Change max value of I_{OZ} from 350 nA to 300 nA
  - Change min value of I_{OZ} from -550 nA to -400 nA
  - Change note of I_{OZ} from '550 nA' to '400 nA'
  - Change min value of I_{OZ} from -700 nA to -600 nA

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  - Change max value of I_{OZ} from 700 nA to 600 nA
  - Change min value of I_{OZ} from -1100 nA to -750 nA
  - Change max value of I_{OZ} from 1100 nA to 750 nA
  - Change max value of I_{OZ} from 11000 nA to 18000 nA
  - Change min value of I_{OZ} from -11000 nA to -18000 nA
  - Change note of I_{OZ} from '22000 nA' to '38000 nA'
  - Change min value of I_{OZ} from -22000 nA to -38000 nA
- Changes in table 'Class S 5V' of Standard Pads
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
  - Change min value of I_{OZ} from -350 nA to -300 nA
  - Change note of I_{OZ} from '350 nA' to '300 nA'
  - Change min value of I_{OZ} from -700 nA to -600 nA
  - Change max value of I_{OZ} from 700 nA to 600 nA
- Changes in table 'Class D' of Standard Pads
  - Change min value of I_{OZ} from -350 nA to -300 nA
  - Change max value of I_{OZ} from 350 nA to 300 nA
  - Change min value of I_{OZ} from -700 nA to -600 nA
  - Change max value of I_{OZ} from 700 nA to 600 nA
- Changes in table 'RFast 5V GPIO' of Standard Pads
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'LVDS - IEEE standard LVDS general purpose link (GPL)' of LVDS Pads
  - Add parameter t_{SET_LVDS}
  - Change note of R_{in} from '1600 mV < V_I ≤ 2000 mV' to 'V_I ≤ 2000 mV'
- VADC 5V
  - Add parameter *dVDDK*
  - Change note of V_{DDK} from '' to 'Measured at low temperature.'
  - Change note of t_{SCAL} from '4.5V ≤ V_{DDM} ≤ 5.5V' to '4.5 V ≤ V_{DDM} ≤ 5.5 V'
  - Change note of f_{ADCI} from '4.5V ≤ V_{DDM} ≤ 5.5V' to '4.5 V ≤ V_{DDM} ≤ 5.5 V'
  - Change note of R_{PDD} from '' to 'Measured at pad input voltage V_{IN} = V_{DDM} / 2.'
  - Change note of t_{SCAL} from '2.97V ≤ V_{DDM} < 4.5V' to '2.97 V ≤ V_{DDM} < 4.5 V'
  - Change note of t_S from 'Primary group or fast compare channel, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer disabled' to 'Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled'
  - Change note of f_{ADCI} from '2.97V ≤ V_{DDM} < 4.5V' to '2.97 V ≤ V_{DDM} < 4.5 V'
  - Change note of t_S from 'Primary group or fast compare channel, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer enabled' to 'Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled'
  - Change note of t_S from 'Secondary group, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer disabled' to 'Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled'
  - Change note of t_S from 'Secondary group, 4.5V ≤ V_{DDM} ≤ 5.5V; input buffer enabled' to 'Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled'
  - Change note of t_S from 'Primary Group or fast compare channel, 2.97V ≤ V_{DDM} < 4.5V; input buffer disabled' to 'Primary Group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled'

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  - Change note of t_S from 'Primary group or fast compare channel, 2.97V ≤ V_{DDM} < 4.5V; input buffer enabled' to 'Primary group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled'
  - Change note of t_S from 'Secondary group, 2.97V ≤ V_{DDM} < 4.5V; input buffer disabled' to 'Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled'
  - Change note of t_S from 'Secondary group, 2.97V ≤ V_{DDM} < 4.5V; input buffer enabled' to 'Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled'
  - Change of “VADC Parameters” praeamble
- DSADC 5V
  - Add parameter R_{BIAS}
  - Change type of I_{REF} from SR to CC
- Changes in table 'DTS Core' of DTS
  - Add parameter ΔT
- Current Consumption
  - Change max value of $I_{DDP3RAIL}$ from '60 mA' to '50 mA'
- Changes in table 'Module Current Consumption' of Current Consumption
  - Change max value of $I_{DDP3ERASE}$ from 20 mA to 25 mA
  - Add parameter $I_{DDP3ERASE}$
  - Change description of $I_{DDP3ERASE}$ from 'Current adder for' to 'I_{DDP3} supply current for erasing of a Pflash or Dflash bank'
  - Change typ value of I_{SCRSB} from 0.190 mA to 0.150 mA
  - Change max value of $I_{DDP3PROG}$ from '8 mA' to '9 mA'
  - Change max value of $I_{DDP3PROG}$ from '20 mA' to '25 mA'
  - Change max value of I_{SCRSB} from '6.5 mA' to '7 mA'
  - Change max value of $I_{SCRIDLE}$ from '1 mA' to '3.5 mA'
  - Change max value of $I_{DDPORST}$ from "real power pattern; T_J=125°C" to "V_{DD} = 1.275V; T_J=125°C"
  - Change max value of $I_{DDPORST}$ from '190 mA' to '185 mA'
  - Change max value of I_{SLEEP} from 25 mA to 27 mA
- Changes in table 'Module Core Current Consumption' of Current Consumption
  - Change max value of I_{DDGTM} from 120 mA to 125 mA
  - Change note of $I_{DDPORST}$ from 'real power pattern; T_J=150°C' to 'V_{DD} = 1.275V; T_J=150°C'
  - Change max value of $I_{DDPORST}$ from 340 mA to 320 mA
  - Change note of $I_{DDPORST}$ from 'real power pattern; TJ=160°C' to 'V_{DD} = 1.275V; TJ=160°C'
  - Change max value of $I_{DDPORST}$ from 450 mA to 400 mA
  - Change note of $I_{DDPORST}$ from "real power pattern; T_J=165°C" to "V_{DD} = 1.275V; T_J=165°C"
  - Change note of $I_{DDPORST}$ from '490 mA' to '430 mA'
- Reset
  - Change max value of t_{BS} from 1 ms to 1.05 ms
  - Change note of t_{BP} from 'Firmware execution time after warm PORST without EVR ramp-up; RAM initialization and HSM boot time is not included' to 'Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included'
  - Change description of t_{BP} from 'Power on Reset Boot Time' to 'Cold Power on Reset Boot Time'
  - Change note of t_{LBIST} from 'PATTERNS=0x00040, FREQU=5, SPLITSH=4' to 'LBIST Configuration A'
  - Removed parameter t_{LBIST} with note 'PATTERNS=0x00280, FREQU=5, SPLITSH=4'

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- PMS/EVR33 LDO
  - Change note of *dVout/dVin* from "*dVin/dT*=1*V/ms*; *dV*= 3.6 to 5*V*" to "*dVin/dT*=1*V/ms*; *dV*= 3.6 to 5*V*; ΔV_{OUTTC} is included"
  - Change note of *dVout/dVin* from '20 mV' to '40 mV'
  - Change min value of *dVout/dVin* from -20 mV to -40 mV
  - Change note of *dVout/dVin* from '*dVin/dT*=1*V/ms*; *dV*= 5 to 3.6*V*' to '*dVin/dT*=1*V/ms*; *dV*= 5 to 3.6*V*; ΔV_{OUTTC} is included'
  - Add parameter *dVOUTTC*
  - Change note of t_{STR} from '' to 'Normal RUN mode'
- PMS/Supply Monitors
  - Change max value of V_{RSTC} from 1.135 V to 1.138 V
- Changes in table 'EVRC SMPS' of PMS/EVRC SMPS
  - Change max value of ΔV_{DDDC} from 12 mV to 16 mV
- PLL Peripheral
  - Add parameter *JABS25*
  - Change note of *DP* from 'f_{DCO} = 640 MHz' to 'f_{DCO} = 640 MHz or f_{DCO} = 800 MHz'
  - Change note of D_{RMS} from 'measured over 1 µs; f_{REF} = 20 MHz; f_{DCO} = 640 MHz' to 'measured over 1 µs; f_{REF} = 20 MHz and f_{DCO} = 640 MHz or f_{REF} = 25 MHz and f_{DCO} = 800 MHz'
- Flash
  - Change note of N_{E_HSMS} from 'Max. data retention time 10 years' to 'max data retention time 20y, Tj=85°C'
  - Change note of N_{E_EEP10S} from 'Max. data retention time 10 years' to 'max data retention time 20y, Tj=85°C'
  - Add parameter N_{E_EEP10S}
  - Change max value of N_{E_EEP10S} to 125000 cycles
  - Add parameter N_{E_EEP10S}
  - Change max value of N_{E_EEP10S} to 125000 cycles
  - Add parameter N_{E_EEP10S}
  - Change max value of N_{E_EEP10S} to 70000 cycles
  - Add parameter N_{E_HSMS}
  - Change max value of N_{E_HSMS} to 125000 cycles
  - Add parameter N_{E_HSMS}
  - Change max value of N_{E_HSMS} to 125000 cycles
  - Add parameter N_{E_HSMS}
  - Change max value of N_{E_HSMS} to 70000 cycles
  - Add inactive time to Table 3-75 “Example Temperature Profile”
- Package Parameters
  - Update table layout for table 3-67
  - Change max value of RTH_JA from 14,8 K/W to 17 K/W
  - Change max value of RTH_JA from 12 K/W to 14 K/W
  - Change name of R_{TH_JA} from Thermal resistance (junction to ambient) to RTH_JA
  - Change description of R_{TH_JA} from '' to 'Thermal resistance (junction to ambient)'
  - Change max value of RTH_JCT from 4.5 K/W to 3 K/W
  - Change max value of RTH_JCT from 4.7 K/W to 3 K/W

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  - Change max value of RTH_JCB from 2.8 K/W to 2 K/W
  - Change description of R_{TH_JCB} from '' to 'Thermal resistance (junction to case bottom)'
  - Change note of RTH_JCB from '3.5 K/W' to '2 K/W'

4.3 Changes from Version 0.7 to Version 0.71

- Pinning
  - Corrected descriptions of HSCT pins
  - Corrected descriptions of CCU_PAD_SYSCLK pin
- Summary of Features
  - Included RGMII in the Ethernet description
- Platform feature overview
  - Corrected number of SDMMC modules from ‘1’ to ‘0’
  - Corrected the value of MCDS from “yes” to “no”
  - Corrected number of QSPI modules from ‘6’ to ‘5’
- Corrected ‘LVDSH’ to ‘LVDS’ in Section ‘High performance LVDS Pads’
- Changes in table "Absolute Maximum Ratings"
  - Change value of Parameter "VDDM"
  - Change value of Parameter "VIN"
- Change preamble of Section "Overload"
- Changes in table "Overload Parameters" of Section "Overload"
  - Change condition of Parameter "IIN"
  - Change condition of Parameter "IINLVDS"
  - Change condition of Parameter "IOUT"
  - Change condition of Parameter "IINANA"
  - Delete Parameter "IID"
- Changes in table "PORST Pad" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VEXT”
- Changes in table "Class S" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VDDM”
- Changes in table "RFast 3.3V pad" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VFLEX”
- Changes in table "RFast 5V pad" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VFLEX”
- Changes in table "Fast 3.3V pad" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VEXT/FLEX/EVRSB”
- Changes in table "Fast 5V pad" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VEXT/FLEX/EVRSB”
- Changes in table "Slow 3.3V pad" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VEXT/FLEX/EVRSB”
- Changes in table "Slow 5V pad" of Section "Switchable Pads"
  - Change reference voltage of Parameters and values from "VEXT/FLEX" to “VEXT/FLEX/EVRSB”

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- Changes in table "VADC 5V"
  - Add footnote to Parameter "QCON"
  - Update picture ‘Equivalent Circuitry for Analog Inputs’
- Changes in table "DSADC 5V"
  - Change value of Parameter "EDGAIN"
  - Change value of Parameter "EDOFF"
  - Add footnote to Parameter "EDOFF"
  - Change value of Parameter "IREF"
  - Change value of Parameter "IRMS"
  - Add footnote to Parameter "IRMS"
  - Add footnote to Parameter "SNR"
  - Add footnote to Parameter "SFDR"
- Changes in table "Current Consumption"
  - Change Parameter description of "IDDRAIL"
  - Change condition of Parameter "ISTANDBY"
  - Change value of Parameter "ISTANDBY"
  - Change footnote of Parameter "ISTANDBY"
- Changes in table "Module Core Current Consumption" of Section "Current Consumption"
  - Change condition of Parameter "IDDLBIST"
  - Change value of Parameter "IDDLBIST"
  - Add footnote to Parameter "IDDLBIST"
  - Add footnote to Parameter “ISCRSB”
  - Change condition of Parameter "IDDMBIST"
- Added section "Calculating the 1.25V Current Consumption"
- Changes in table "Reset"
  - Change value of Parameter "tB"
  - Change value of Parameter "tBS"
  - Add footnote to Parameter "tEVRPOR"
  - Change value of Parameter "tBWP"
  - Change condition of Parameter "tLBIST"
  - Change Parameter description of "tLBIST"
- Changes in table "EVR33 LDO"
  - Change condition of Parameter "dVout/dIout"
  - Change condition of Parameter "Vout/dVin"
  - Change footnote of Parameter "IMAX"
- Changes in table "Supply Monitors"
  - Change condition of Parameter "tMON"
  - Change condition of Parameter"VDDMON"
  - Change condition of Parameter "VDDP3MON"
  - Change condition of Parameter "VEXTMON"
  - Add footnote to Parameter "VEXTMON"
  - Change condition of Parameter "VRST5"

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- Changes in table "Flash"
  - Change condition of Parameter "NE_EEP10S"
  - Remove condition of Parameter "NE_EEP10S"
  - Change condition of Parameter "NE_HSMS"
  - Remove condition of Parameter "NE_HSMS"
- Changes in table "Quality Parameters" of Section "Quality Declarations"
  - Change Parameter description of "VHBM1"
- Add Section "TC380 Carrier Tape"
- OSC_XTAL
  - Removed parameter V_{ILBX}
  - Removed parameter V_{IHBX}
- Changes in table "Back-up Clock"
  - Update footnote of Parameters “fBACKT"
- Changes in table "PLL Peripheral"
  - Add Parameters “DPP"
  - Add Parameters “DPPI"
- Changes in table "Receive Parameters" of “E-ray Parameters”
  - Update Parameters description of “tdCCRxD01"

4.4 Changes from Version 0.71 to Version 1.0

- Changes in chapter “Summary of Features”
  - Changed LMU Memory size from 128 Kbyte to 256 Kbyte
- Pinning
  - Corrected descriptions of Column “Buffer Type”: PU2
- Changes in chapter Electrical Specification
  - Corrected/ added wording in sub-chapter 3.1 “Parameter Interpretation”
  - Added naming for temperature value, table 3-66, Example Operation Lifetime Profile
  - Changed naming for sub-chapter 3.16, from Phase Locked Loop (PLL) to System Phase Locked Loop (SYS_PLL)
  - corrected temperature in “Summary of Features” section

- Changes in Absolute Maximum Table
  - Add footnote 2) to V_{DD}
- Changes in Operating Conditions Table
  - Add footnote 1) to V_{DD}
- Changes in table '$\overline{\text{PORST}}$ Pad' of Standard Pads
  - Change min value of *HYS* from 0.055 * $V_{EXT/FLEX}$ V to 0.055 * V_{EXT} V
  - Change note of I_{OZ} from 'TJ≤150°C ; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$)' to 'TJ≤150°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})'
  - Changed footnote 1) from *10% to 90%* $V_{EXT/FLEX}$ 10% to 90% pad supply voltage
  - Add footnote 2) to I_{PDL}

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  - Add parameter V_{IH} for condition TTL, V_{EXT}
  - Add parameter V_{IL} for condition TTL, V_{EXT}
- Changes in table 'Fast 5V GPIO' of Standard Pads
  - Change min value of V_{IH} from 0.7 * $V_{EXT/FLEX}$ V to 0.7 * $V_{EXT/FLEX/EVRSB}$ V
  - Change note of V_{IL} from '0.44 * $V_{EXT/FLEX}$ V' to '0.44 * $V_{EXT/FLEX/EVRSB}$ V'
  - Change note of V_{ILD} from 'max. variation of 1ms; V_{DDM} = constant; AL' to 'max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL'
  - Combined equal values of I_{OZ} in single line
  - Add footnote 4) to I_{PUH}
  - Add footnote 5) to I_{PDL}
- Changes in table 'Fast 3.3V GPIO' of Standard Pads
  - Change min value of V_{IH} from 0.7 * $V_{EXT/FLEX}$ V to 0.7 * $V_{EXT/FLEX/EVRSB}$ V
  - Change note of V_{IL} from '0.42 * $V_{EXT/FLEX}$ V' to '0.42 * $V_{EXT/FLEX/EVRSB}$ V'
  - Change note of V_{ILD} from 'max. variation of 1ms; V_{DDM} = constant; AL' to 'max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL'
  - Combined equal values of I_{OZ} in single line
  - Add footnote 4) to I_{PUH}
  - Add footnote 5) to I_{PDL}
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Change min value of V_{IH} from 0.7 * $V_{EXT/FLEX}$ V to 0.7 * $V_{EXT/FLEX/EVRSB}$ V
  - Change note of V_{IL} from '0.44 * $V_{EXT/FLEX}$ V' to '0.44 * $V_{EXT/FLEX/EVRSB}$ V'
  - Change note of V_{ILD} from 'max. variation of 1ms; V_{DDM} = constant; AL' to 'max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL'
  - Combined equal values of I_{OZ} in single line
  - Add footnote 4) to I_{PUH}
  - Add footnote 5) to I_{PDL}
- Changes in table 'Slow 3.3V GPIO' of Standard Pads
  - Change min value of V_{IH} from 0.7 * $V_{EXT/FLEX}$ V to 0.7 * $V_{EXT/FLEX/EVRSB}$ V
  - Change note of V_{IL} from '0.42 * $V_{EXT/FLEX}$ V' to '0.42 * $V_{EXT/FLEX/EVRSB}$ V'
  - Change note of V_{ILD} from 'max. variation of 1ms; V_{DDM} = constant; AL' to 'max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL'
  - Combined equal values of I_{OZ} in single line
  - Add footnote 4) to I_{PUH}
  - Add footnote 5) to I_{PDL}
- Changes in table 'RFast 5V GPIO' of Standard Pads
  - Change min value of *HYS* from 0.09 * $V_{EXT/FLEX}$ V to 0.09 * V_{FLEX} V
  - Change note of *HYS* from '0.075 * $V_{EXT/FLEX}$ V' to '0.075 * V_{FLEX} V'
  - Change min value of V_{IH} from 0.7 * $V_{EXT/FLEX}$ V to 0.7 * V_{FLEX} V
  - Change note of V_{IL} from '0.44 * $V_{EXT/FLEX}$ V' to '0.44 * V_{FLEX} V'
  - Change note of t_{RF} from 'C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$' to 'C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}'
  - Change note of I_{OZ} from '$T_J \leq 170°C$; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$)' to '$T_J \leq 170°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})'

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  - Change note of I_{OZ} from '$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$' to '$T_J \leq 150°C$; $(0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})$'
  - Change note of V_{ILD} from 'max. variation of 1ms; V_{DDM} = constant; AL' to 'max. variation of 1ms; V_{FLEX} = constant; AL'
  - Add footnote 4) to I_{PUH}
  - Add footnote 5) to I_{PDL}
- Changes in table 'RFast 3.3V pad' of Standard Pads
  - Change min value of *HYS* from 0.055 * $V_{EXT/FLEX}$ V to 0.055 * V_{FLEX} V
  - Change min value of *HYS* from 0.09 * $V_{EXT/FLEX}$ V to 0.09 * V_{FLEX} V
  - Change min value of *HYS* from 0.055 * $V_{EXT/FLEX}$ V to 0.055 * V_{FLEX} V
  - Change note of V_{IH} from '0.7 * $V_{EXT/FLEX}$ V' to '0.7 * V_{FLEX} V'
  - Change note of V_{IL} from '0.42 * $V_{EXT/FLEX}$ V' to '0.42 * V_{FLEX} V'
  - Change note of t_{RF} from 'C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX}$ to 0.8 * $V_{EXT/FLEX}$' to 'C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}'
  - Change note of I_{OZ} from '$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$' to '$T_J \leq 170°C$; $(0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})$'
  - Change note of V_{ILD} from 'max. variation of 1ms; V_{DDM} = constant; AL' to 'max. variation of 1ms; V_{FLEX} = constant; AL'
  - Add footnote 4) to I_{PUH}
  - Add footnote 5) to I_{PDL}
- Changes in table 'Class S 5V' of Standard Pads
  - Change min value of *HYS* from 0.09 * $V_{EXT/FLEX}$ V to 0.09 * V_{DDM} V
  - Change min value of *HYS* from 0.075 * $V_{EXT/FLEX}$ V to 0.075 * V_{DDM} V
  - Change min value of V_{IH} from 0.7 * $V_{EXT/FLEX}$ V to 0.7 * V_{DDM} V
  - Change note of V_{IL} from '0.44 * $V_{EXT/FLEX}$ V' to '0.44 * V_{DDM} V'
  - Add footnote 2) to I_{PUH}
  - Add footnote 3) to I_{PDL}
- Add table 'Class S 3.3V' of Standard Pads
- Changes in table 'ADC Reference Pads' of Standard Pads
  - Change note of I_{OZ2} from '$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC' to '$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EVADC; valid for BGA516 and Bare Die'
  - Change note of I_{OZ2} from '$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; used for EDSADC' to '$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; for EDSADC'
  - Change note of I_{OZ2} from '$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EDSADC' to '$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EDSADC'
  - Change value of I_{OZ2} from '$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; used for EVADC' to '$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; for EVADC; valid for BGA516 and Bare Die'
  - Change note of I_{OZ2} from '$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; used for EDSADC' to '$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; for EDSADC'
  - Change note of I_{OZ2} from '$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EDSADC' to '$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EDSADC'
  - Change note of I_{OZ2} from '$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC' to '$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EVADC; valid for BGA516 and Bare Die'

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  - Change note of I_{OZ2} from '$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; used for EVADC' to '$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; for EVADC; valid for BGA516 and Bare Die'
  - Added values for I_{OZ2}
  - Add footnote 1)
  - Add footnote 2)
  - Add footnote 3)
- LVDS - IEEE standard LVDS general purpose link (GPL)
  - Added footnote 1) for max. value t_{rise20}
  - Added footnote 2) for max. value t_{fall20}
  - Changed footnote number 1) for V_{OD} to footnote number 3)
  - Changed footnote number 2) for V_{ODSM} to footnote number 4)
  - Changed marking in figure 'LVDS Input model' from 'LVDSH IN' to 'LVDS IN'
- VADC 5V
  - Change note of V_{AREF} from '' to '4.5 V $\leq V_{DDM} \leq$ 5.5 V'
  - Change min value of V_{AREF} from V_{DDMnom} * 0.9 V to 4.5 V
  - Add min value of V_{AREF}
  - Add typ value of V_{AREF}
  - Add max value of V_{AREF}
  - Add note of V_{AREF} to '2.97 V $\leq V_{DDM} \leq$ 4.5 V'
  - Add footnote 1)
- DSADC 5V
  - Change min value of V_{AREF} from V_{DDMnom} * 0.9 V to 4.5 V
  - Add max value of I_{REF} at high temperature
- OSC_XTAL
  - Add parameter for DC_{x1}
  - Add parameter for J_{ABSX1}
  - Add parameter for SR_{XTAL1}
  - Add footnote 3)
- Back-up Clock
  - Change min value of f_{SB} from 30 kHz to 25 kHz
  - Change note of If_{BACKT} from 'A short term trimming providing the accuracy required by LIN communication is possible by periodic trimming every 2 ms for temperature and voltage drifts ' to 'A short term trimming providing the accuracy required by LIN communication is possible by periodic trimming every 2 ms for temperature and voltage drifts up to temperatures of 125 celcius'
- DTS
  - Change note of T_{NL} from ‘’ to ‘T_{CALACC} has to be added in addition’
- Power Supply Current
  - Changes in conditions from 'four lockstep cores' to 'two lockstep cores'
- Current Consumption
  - Change max value of $I_{DDPORST}$ from '185 mA' to '160 mA'
  - Change max value of $I_{DDPORST}$ from '320 mA' to '290 mA'
  - Change max value of $I_{DDPORST}$ from '400 mA' to '350 mA'

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  - Change max value of $I_{DDPORST}$ from '430 mA' to '380 mA'
  - Changed footnote 3)
- Module Current Consumption
  - Add parameter of $I_{EXTLVDS}$ for receive
- Module Core Current Consumption
  - Changed footnote 1)
- Changes in chapter “Calculating the 1.25 V Current Consumption”
  - Changes in formula (3.2)
- Changes in chapter “Supply Ramp-up and Ramp-down Behavior”
  - Changed Figure and textual description for figure “Single Supply Mode (a) - VEXT (5 V) single supply”
  - Changed Figure and textual description for figure “Single Supply Mode (e) - (VEXT & VDDP3) 3.3 V single supply”
  - Changed Figure and textual description for figure “Single Supply Mode (d) - VEXT and VDD externally supplied”
  - Changed Figure and textual description for figure “Single Supply Mode (h) - VEXT, VDDP3 and VDD externally supplied”
- Reset Timing
  - Add parameter $t_{WARMRSTSEQ}$
- PMS/Supply Monitors
  - Changed min value of V_{EXTMON} from '3.235 V to 3.2 V', and max value from '3.365 V' to '3.4 V'
  - Added footnote 5) for V_{DDMON}
- EVRC SMPS
  - Added typ. value of '0.8 MHz' and note for f_{DCDC}
  - Added values for L_{DC} for 'f_{DCDC} = 0.8 MHz'
- Add chapter FSP Parameters
- PLL System
  - Deleted values for f_{MV} for 'Modulation variation frequency'
- Table 'Master Mode Timing'
  - Added footnote 1)
- Table 'LVDS clock/data'
  - Added footnote 3)
- Flash
  - Add parameter for N_{DFDC}
  - Add parameter for N_{UCBD}
  - Add parameter $t_{VER_PAGE_DC}$
  - Change description of $t_{VER_PAGE_DC}$ from 'Data Flash Erase Verify time per page' to 'Data Flash Erase Verify time per page (Complement Sensing)'
  - Change name of $t_{VER_PAGE_DS}$ from tVER_PAGE_D to tVER_PAGE_DS
  - Change description of $t_{VER_PAGE_DS}$ from 'Data Flash Erase Verify time per page' to 'Data Flash Erase Verify time per page (Single Ended Sensing)'
  - Change note of t_{RTU} from ’Max. 100 erase/program cycles per UCB, max 400 erase/program cycles for all UCBs together’ to ‘Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together’

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- Package Parameters
  - Change max value of RTH_JCT from 3 K/W to 5 K/W for LFBGA292
  - Change max value of RTH_JCT from 3 K/W to 5 K/W for LFBGA516
- TC380 Carrier Tape
  - Added disclaimer for TC380
  - Changed X and Y values for 'TC380 Chip Dimensions'
  - Changed figure for 'Carrier Tape Dimensions'
  - Added accuracy value for 'TC380 Chip Dimensions'
- Summary of Features
  - Removed ASIL value from table 'Platform Feature Overview'

4.5 Changes from Version 1.0 to Version 1.1

- Changes in table “Platform Feature Overview” - changed package types
- Changes on title page and chapter heads – AD/AE-Step”
- Changes in table “Platform Feature Overview” – package naming spelling of LFBGA-516-1 and LFBGA-292-11
- Change in table “Platform Feature Overview” – spelling of “HSPDM”
- Chapter “Bare Die Variant Pin Configuration of TC38x” - added information concerning “neighbor pads” after table “Pad List”
- Changes in chapter “Legend”
  - Added information concerning I/O-Spirit file version
  - Changed refering IO_Spirit_file version
  - Changed explanation for PD2 = with pull-down device connected during startup and reset, HighZ in Standby mode
- Changes in table “Absolute Maximum Ratings”
  - Changed description for parameter “Absolute maximum sum”
  - Added footnote 5)
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Changed conditions of parameter I_{OZ}
  - Changed value of parameter V_{IL}
- Changes in table “Slow 3.3V GPIO” of Standard Pads
  - Changed conditions of parameter I_{OZ}
- Changes in table “RFast 3.3V pad” of Standard Pads
  - Deleted parameter for f_{IND}
- Changes in table “LVDS - IEEE standard LVDS general purpose link (GPL)” of LVDS Pads
  - Changed value of parameter V_I
  - Changed condition of parameter V_{idth}
  - Added values for parameter V_{idth}
  - Changed condition of parameter R_{in}
  - Added notes/ hints to table footnotes for “Driver ground potential difference” and for parameter “RT”
- Changes in table “VADC 5V”
  - Added condition for parameter V_{AIN}

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- Changes in table “DSADC 5V”
  - Added value for parameter I_{RMS}
  - Changed footnotes of parameter ED_{GAIN}
  - Changed footnotes of parameter ED_{OFF}
  - Added footnote 4) for parameter ED_{GAIN}
- Changes in table “OSC_XTAL”
  - Changed footnote 1) for parameter t_{OSCS}
- Changes in table “Current Consumption”
  - Deleted footnote 1) for parameter $I_{EXTFLEX}$
  - Changed value in footnote 1)
  - Changed explanation in footnote 6)
- Changes in table “Module Current Consumption”
  - Changed values of parameter $I_{EXTLVDS}$
  - Changed conditions of parameter $I_{EXTLVDS}$
  - Changed value in footnote 6)
- Changes in table “Reset”
  - Changed values of parameter t_{SCR}
- Changes in table “Supply Ramp”
  - Added note “power-cycles” to supply ramp table
- Changes in table “EVRC SMPS”
  - Changed symbol for parameter “Δf_{DCSPR}”
- Changes in table “PLL System”
  - Changed value for parameter f_{REF}
- Changes in table “ETH RGMII Parameters”
  - Added figures for ETH RGMII TX and RX signals
- Changes in table “Quality Parameters”
  - Changed value for parameter V_{HBM1}
- Changes in chapter “Package Outline” - changed package types
- Changes in sub-chapter “TC380 Carrier Tape”
  - Changed number of figure “Carrier Tape Dimensions”

4.6 Changes from Version 1.1 to Version 1.2

- Changes in chapter “Revision History”
  - Chronology completed

- Changes in chapter “Summary of Features”
  - Changed wording for “DFLASH”
  - Added description for “AEC-Q100”
  - Added description for “ISO 26262 Safety Element”
  - Added description for Data Flash in table “Platform Feature Overview”
  - Changed figure for GTM clusters in table “Platform Feature Overview”

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- Changed figures for GTM/CDTM/DTM modules in table “Platform Feature Overview”
- Changed package type in table “Platform Feature Overview”

- Changes in chapter “Pin Definition and Functions”
  - Changed EDSADC function description for Port 00 in “BGA-516 Package Variant” tables
  - Changed EDSADC function description for Port 01 in “BGA-516 Package Variant” tables
  - Changed EDSADC function description for Port 02 in “BGA-516 Package Variant” tables
  - Changed PSI5S function description for Port 02 in “BGA-516 Package Variant” tables
  - Deleted PMS parameter for Port 02 in “BGA-516 Package Variant” tables
  - Deleted SCU parameter at Port 10 in “BGA-516 Package Variant” tables
  - Added PMS parameter at Port 10 in “BGA-516 Package Variant” tables
  - Changed Buffer Type description for P11.5, P11.7, P11.8, P11.9, P11.10, P11.11, P11.12 at Port 11 in “BGA-516 Package Variant” tables
  - Changed function description for GETH at Port 11 in “BGA-516 Package Variant” tables
  - Changed function description for GTM at Port 11 in “BGA-516 Package Variant” tables
  - Deleted parameter for SCU at Port 14 in “BGA-516 Package Variant” tables
  - Added parameter for PMS at Port 14 in “BGA-516 Package Variant” tables
  - Changed function description for GTM at Port 14 in “BGA-516 Package Variant” tables
  - Changed function description for HSCT0 at Port 20 in “BGA-516 Package Variant” tables
  - Changed function description for GTM at Port 20 in “BGA-516 Package Variant” tables
  - Added function description for DMU at Port 21 in “BGA-516 Package Variant” tables
  - Changed function description for HSCT0 at Port 21 in “BGA-516 Package Variant” tables
  - Changed function description for GTM at Port 23 in “BGA-516 Package Variant” tables
  - Changed EDSADC function description for Port 33 in “BGA-516 Package Variant” tables
  - Changed function description for GTM at Port 33 in “BGA-516 Package Variant” tables
  - Changed PSI5S function description for Port 33 in “BGA-516 Package Variant” tables
  - Added notes to table “System I/O” for “BGA-516 Package Variant”
  - Changed “Ctrl.” information for balls M21, L21 in “System I/O” table for “BGA-516 Package Variant”
  - Changed function description for ball M22 in “System I/O” table for “BGA-516 Package Variant”
  - Changed “Ctrl.” information for balls M22 in “System I/O” table for “BGA-516 Package Variant”
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  - Changed function descriptions for EDSADC at Port 00 in “BGA-292 Package Variant” tables
  - Changed function descriptions for EDSADC at Port 01 in “BGA-292 Package Variant” tables
  - Changed function descriptions for EDSADC at Port 02 in “BGA-292 Package Variant” tables
  - Changed function descriptions for PSI5S at Port 02 in “BGA-292 Package Variant” tables
  - Changed GTM input channel at Port 02 in “BGA-292 Package Variant” tables
  - Deleted parameter for PMS at Port 02 in “BGA-292 Package Variant” tables
  - Deleted parameter for SCU at Port 10 in “BGA-292 Package Variant” tables
  - Added parameter for PMS at Port 10 in “BGA-292 Package Variant” tables
  - Changed Buffer Type description for P11.5, P11.7, P11.8, P11.9, P11.10, P11.11, P11.12 at Port 11 in “BGA-292 Package Variant” tables
  - Changed function description for GETH at Port 11 in “BGA-292 Package Variant” tables

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- Changed GTM input channel at Port 11 in “BGA-292 Package Variant” tables
- Deleted parameter for SCU at Port 14 in “BGA-292 Package Variant” tables
- Added parameter for PMS at Port 14 in “BGA-292 Package Variant” tables
- Changed GTM input channel at Port 14 in “BGA-292 Package Variant” tables
- Added function description for DMU at Port 21 in “BGA-292 Package Variant” tables
- Changed function description for HSCT0 at Port 21 in “BGA-292 Package Variant” tables
- Changed GTM input channel at Port 23 in “BGA-292 Package Variant” tables
- Changed function descriptions for EDSADC at Port 33 in “BGA-292 Package Variant” tables
- Changed GTM input channel at Port 33 in “BGA-292 Package Variant” tables
- Changed PSI5S function description for Port 33 in “BGA-292 Package Variant” tables
- Added notes to table “System I/O” for “BGA-292 Package Variant”
- Changed “Ctrl.” information for balls G16, F16, G17 in “System I/O” table for “BGA-292 Package Variant”
- Changed function description for ball G17 in “System I/O” table for “BGA-292 Package Variant”
-
- Changed sub-chapter title from “Bare Die Variant Pin Configuration of TC38x” to “Sequence of Pads in Pad Frame”
- Changed comments for pad name VDDP3 (62, 64) in Pad List of “Sequence of Pads in Pad Frame”
- Changed pad type for pad names P11.5, P11.7, P11.9, P11.8, P11.10, P11.11, P11.12 in Pad List of “Sequence of Pads in Pad Frame”
- Changed comments for pads 158, 159 in Pad List of “Sequence of Pads in Pad Frame”
- Changed pad names for pads 198, 217, 218, 352, 383 in Pad List of “Sequence of Pads in Pad Frame”
- Changed/ revised footnote for table Pad List of “Sequence of Pads in Pad Frame”

- Changes in chapter “Legend”
  - Changed version number of “TC38xpd_IO_Spirit” file

- Changes in chapter “Electrical Specification”
  - Typos corrected in footnotes for sub-chapter “Absolute Maximum Ratings”
  - Typo corrected for parameter I_{INSA} in table “Overload Parameters” of sub-chapter “Pin Reliability in Overload”
  - Changed values for parameter GETH frequency in table “Operating Conditions”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 3.3V pad” of sub-chapter “5V/3.3V switchable Pads”
  - Changed notes for parameter I_{OZ2} in table “ADC Reference Pads” of sub-chapter “5V/3.3V switchable Pads”
  - Typos corrected in footnote 3) for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
  - Added footnote content for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”

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- Typo corrected for parameter dV_{CSD} in table “VADC 5V” in sub-chapter “VADC Parameters”
- Changed footnote 7) of table “VADC 5V” in sub-chapter “VADC Parameters”
- Changed figure “Equivalent Circuitry for Analog Inputs” in sub-chapter “VADC Parameters”
- Changed footnotes 3) and 6) for table "VADC 5V" in sub-chapter "VADC Parameters"
- Changed value of parameter I_{RMS} in table “DSADC 5V” in sub-chapter “DSADC Parameters”
- Changed footnote 4) in sub-chapter “DSADC Parameters”
- Changed spelling in footnote 2) in sub-chapter “MHz Oscillator”
- Changed spelling in initial text for sub-chapter “Power Supply Current”
- Changed footnote 2) for table “Current Consumption” in sub-chapter “Power Supply Current”
- Added footnote 7) for table “Current Consumption” in sub-chapter “Power Supply Current”
- Typos corrected in sub-chapter “Calculating the 1.25V Current Consumption”
- Added sentence to sub-chapter “Supply Ramp-up and Ramp-down Behavior”
- Changed/added value for parameter t_{PI} in table “Reset” for sub-chapter “Reset Timing”
- Changed figure “DAP Timing” in sub-chapter “DAP Parameters”
- Changed values (from Min. to Typ.) for parameter t_7 in table “ETH MII Signal Timing Parameters” for sub-chapter “ETH MII Parameters”
- Changed symbols for parameters $t_{13,}$ $t_{14,}$ t_{15} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Changed value (from Min. to Typ.) for parameter t_{13} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Added footnote 3) for table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Changed figure title to “Package Outlines FBGA-516” in sub-chapter “Package Outline”
- Changed notes in table “Package Parameters” to “FBGA” for sub-chapter “Package Parameters”
- Deleted sub-chapter “TC380 Carrier Tape”

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