

# USB PD power adapter secondary side controller

## General description

EZ-PD™ PAG1S is an integrated secondary-side synchronous flyback controller, synchronous rectifier (SR) controller, and charging port controller. EZ-PD™ PAG1S is targeted towards power adapters, it fits well into high-efficiency AC-DC flyback designs for USB Power Delivery, Qualcomm Quick Charge, and other standard charging protocols. EZ-PD™ PAG1S also supports USB Power Delivery (USB PD) programmable power supply (PPS) mode.

## Applications

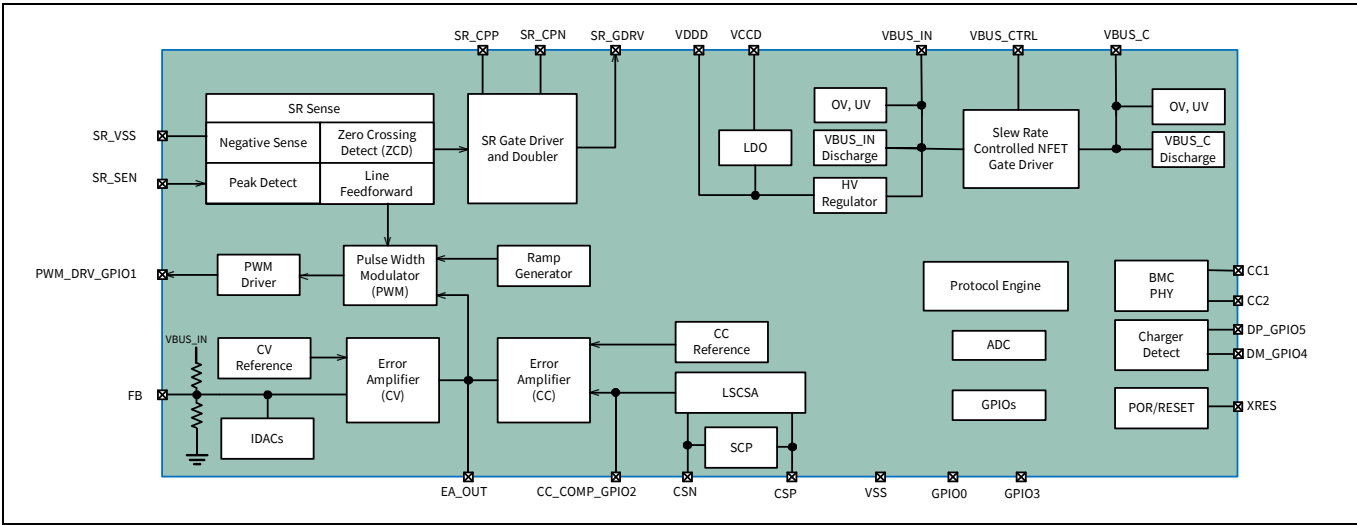
- USB PD 3.0 PPS power adapter
- Quick Charge 4.0 power adapter
- Power adapters supporting both USB PD and legacy charging

## Features

- Integrates secondary-side regulation, synchronous rectifier (SR), and charging port controller
- Optimized efficiency across line and load range, meeting CoC Tier 2 and DoE level 6 requirements
- Supports quasi-resonant (QR) or critical conduction mode (CrCM), valley switching, discontinuous conduction mode (DCM), and burst mode for light load operations
- No load power consumption of < 30 mW with EZ-PD™ PAG1P designs
- Switching frequency range of 20 kHz to 150 kHz
- Supports feed-forward line sensing for faster transient line response
- Supports constant voltage (CV) and constant current (CC) modes of operation.
- Configurable overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), short circuit protection (SCP), and over-temperature protection (OTP)
- USB PD 3.0 compliant with PPS (USB-IF certified, TID:1475)
- Supports USB PD 2.0, PD 3.0 with PPS, QC4+, QC 4.0, QC 3.0, QC 2.0, Samsung AFC, Apple charging, and BC v1.2 charging protocols
- Integrates low-side current sense amplifier (LSCSA), 2x VBUS discharge FETs, and a NFET gate driver to drive the load switch
- Protects against accidental VBUS to CC short; ESD protection on CC, VBUS, and DP/DM lines
- 24-QFN package with -40°C to +105°C extended industrial temperature range

Functional block diagram

Functional block diagram



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# 1 Pinout

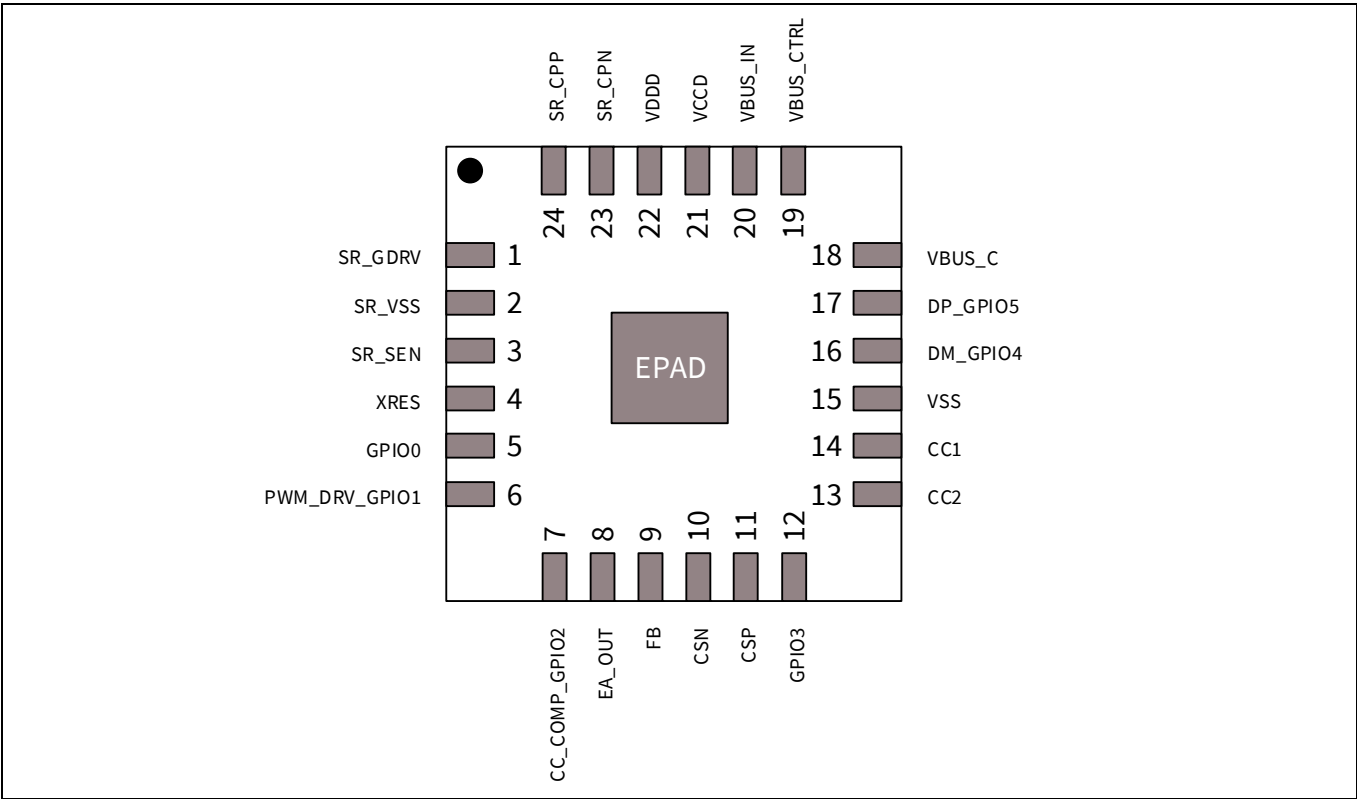


Figure 1 24-pin QFN pin map

## Pinout

**Table 1** EZ-PD™ PAG1S pin description

| Pin number | Pin name      | Description                                                    |
|------------|---------------|----------------------------------------------------------------|
| 1          | SR_GDRV       | Synchronous-rectifier NFET gate driver                         |
| 2          | SR_VSS        | Synchronous-rectifier NFET ground terminal                     |
| 3          | SR_SEN        | Synchronous-rectifier NFET drain terminal                      |
| 4          | XRES          | External reset input                                           |
| 5          | GPIO0         | GPIO P0.0                                                      |
| 6          | PWM_DRV_GPIO1 | Pulse transformer driver/GPIO P0.1                             |
| 7          | CC_COMP_GPIO2 | Pin for constant current mode compensation capacitor/GPIO P0.2 |
| 8          | EA_OUT        | Error amplifier output                                         |
| 9          | FB            | Error amplifier feedback                                       |
| 10         | CSN           | Low-side current sense amplifier negative input                |
| 11         | CSP           | Low-side current sense amplifier positive input                |
| 12         | GPIO3         | GPIO P0.3                                                      |
| 13         | CC2           | Power Delivery communication channel 2                         |
| 14         | CC1           | Power Delivery communication channel 1                         |
| 15         | VSS           | Ground                                                         |
| 16         | DM_GPIO4      | USB D-/SWD_DATA/GPIO P0.4                                      |
| 17         | DP_GPIO5      | USB D+/SWD_CLK/GPIO P0.5                                       |
| 18         | VBUS_C        | USB Type-C VBUS monitor input                                  |
| 19         | VBUS_CTRL     | Load switch NFET gate control                                  |
| 20         | VBUS_IN       | Power source input                                             |
| 21         | VCCD          | 1.8-V core voltage LDO output                                  |
| 22         | VDDD          | 3.0 V–5.5 V internal LDO Output                                |
| 23         | SR_CPN        | SR doubler capacitor negative pin                              |
| 24         | SR_CPP        | SR doubler capacitor positive pin                              |
| 25         | EPAD          | EPAD for ground                                                |

### 1.1 Pin description

SR\_GDRV, SR\_VSS, SR\_SEN, SR\_CPP, SR\_CPN. EZ-PD™ PAG1S senses the voltage across the synchronous rectifier NFET and appropriately controls the gate driver to achieve optimum efficiency. The gate driver (SR\_GDRV) can be driven to internal VDDD or twice of VDDD to achieve better RDS-On of the external NFET. The Gate Driver can be driven to twice of VDDD using an internal doubler circuit, with the doubler capacitor connected across SR\_CPP and SR\_CPN pins. The source terminal of the SR FET shall be connected to SR\_VSS pin. Based on the operating conditions, the application firmware enables or disables the doubler as needed.

EZ-PD™ PAG1S supports synchronous rectification in QR/CrCM, valley switching, and DCM. The SR sense block supports negative sense detect, ZCD (Zero Crossing Detect), peak detect and feed-forward operation. The voltage at the drain node of the external NFET is sensed using a resistive divider. The internal resistor is 2 kΩ, the external resistor needs to be chosen such that the voltage at the SR\_SEN pin does not exceed 21.5 V.

The external resistance on SR\_SEN pin depends on turns ratio of power transformer. [Table 2](#) provides the values required for various values of turns ratio.

**Table 2 External resistance on SR\_SEN vs turns ratio**

| Primary : Secondary turns ratio | Rext (Ω) |
|---------------------------------|----------|
| 4:1                             | 10K      |
| 5:1                             | 9K       |
| 6:1                             | 8K       |
| 7:1                             | 7K       |
| 8:1                             | 6K       |
| 9:1                             | 5K       |
| 10:1                            | 4K       |

The fast-negative sense comparator can detect a minimum negative voltage of 100 mV to –200 mV on SR\_SEN pin. Similarly, ZCD can detect a minimum threshold of –16 mV to 0 mV on the SR\_SEN pin. The peak detect circuit can detect the SR\_SEN pin going typically 75 mV lower than the peak. The feed-forward circuit extracts the input supply voltage from the SR\_SEN node and proportionally modifies the analog PWM ramp generator output for faster transient line response. EZ-PD™ PAG1S offers a host of configurable options: minimum on time, minimum off time, minimum operating frequency, maximum operating frequency, and SR\_SEN detect thresholds, among others. Refer [EZ-PD™ Configuration Utility](#) for more details on the configuration utility. See [Figure 2](#) and [Figure 3](#) for the waveforms representing the SR\_GDRV functionality in QR/CrCM and DCM/valley switching.

Pinout

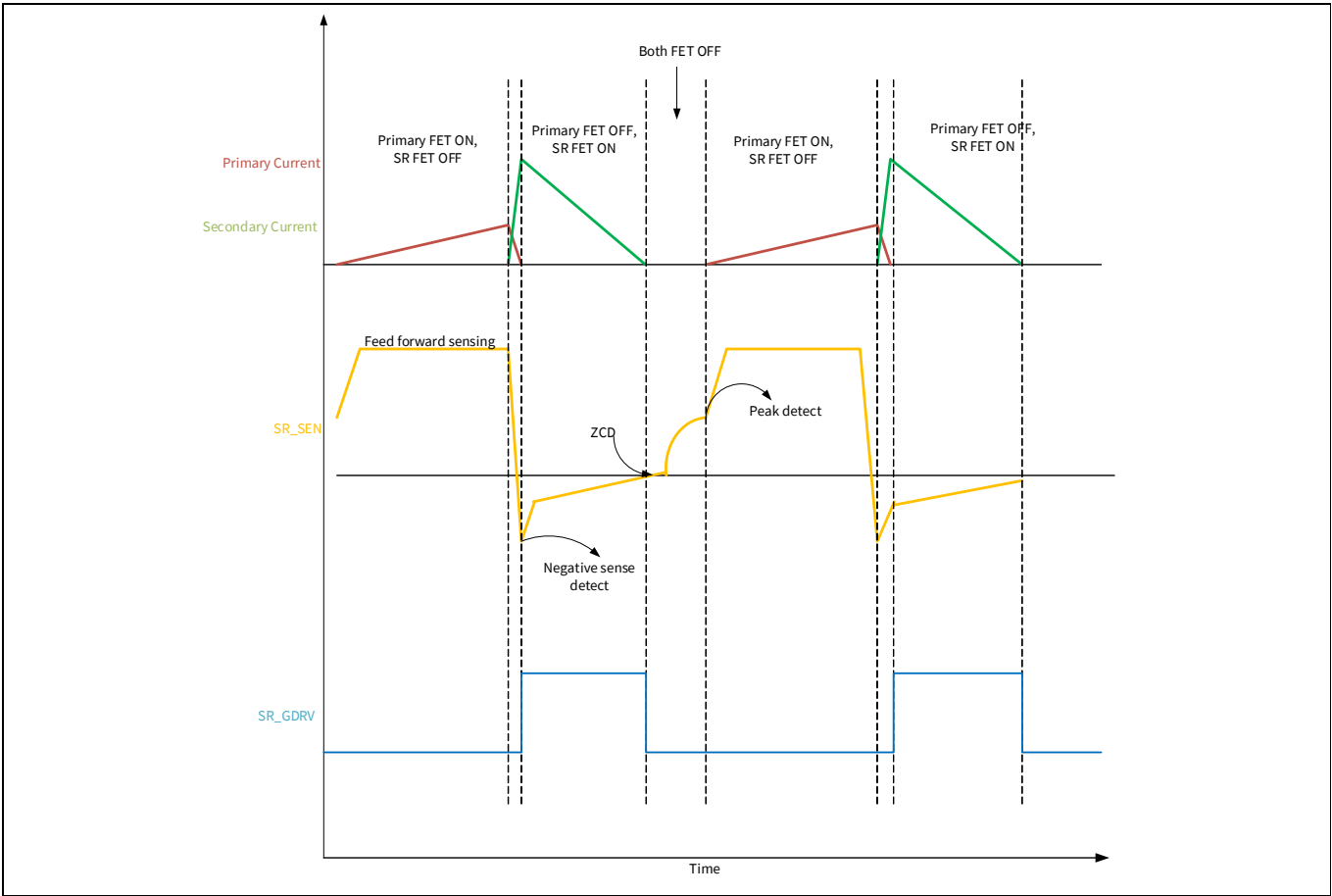
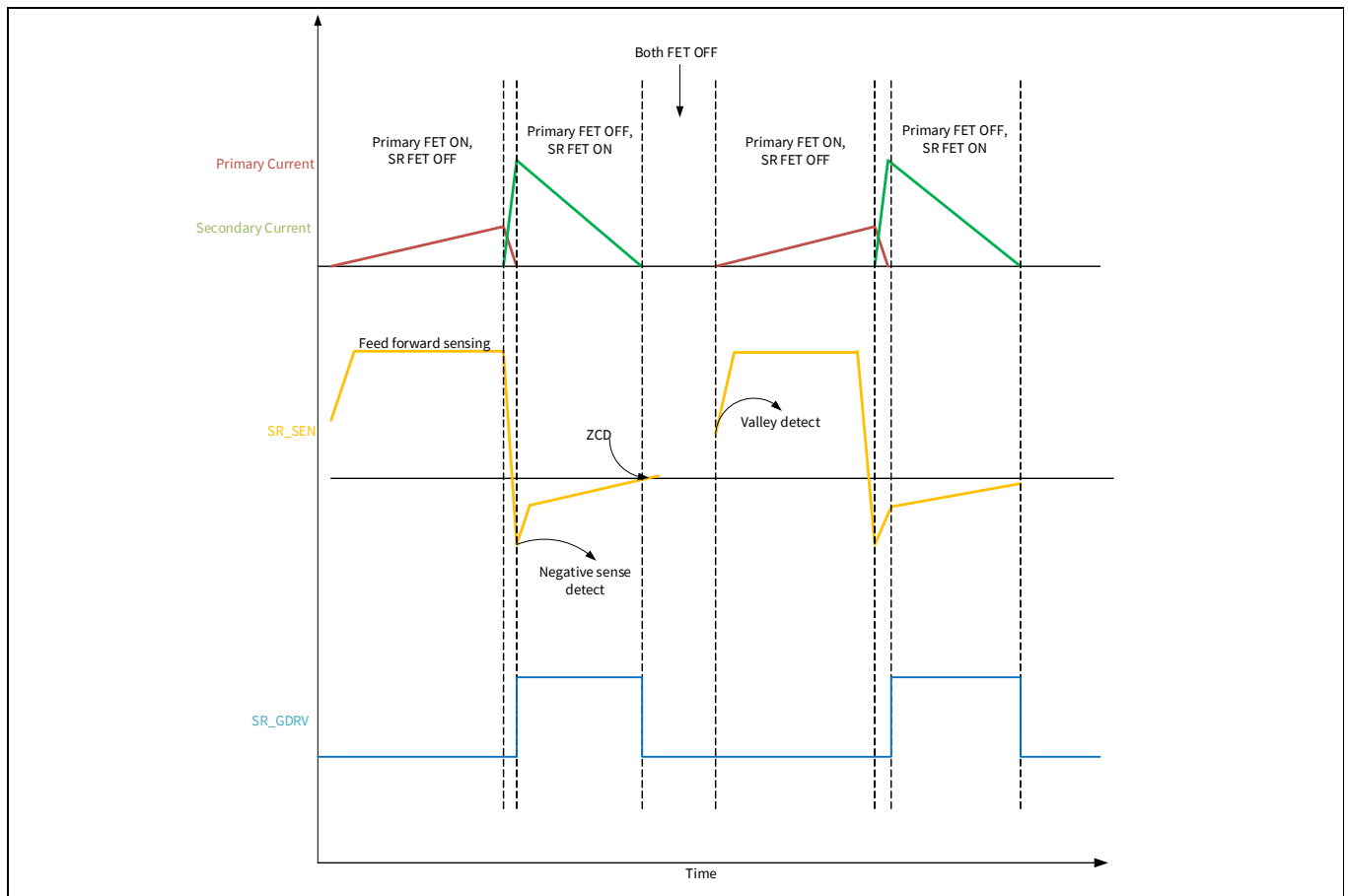


Figure 2 SR\_SEN and SR\_GDRV in QR/CrCM mode



**Figure 3** SR\_SEN and SR\_GDRV in DCM/valley switching mode

### 1.1.1 FB, EA\_OUT, CC\_COMP\_GPIO2

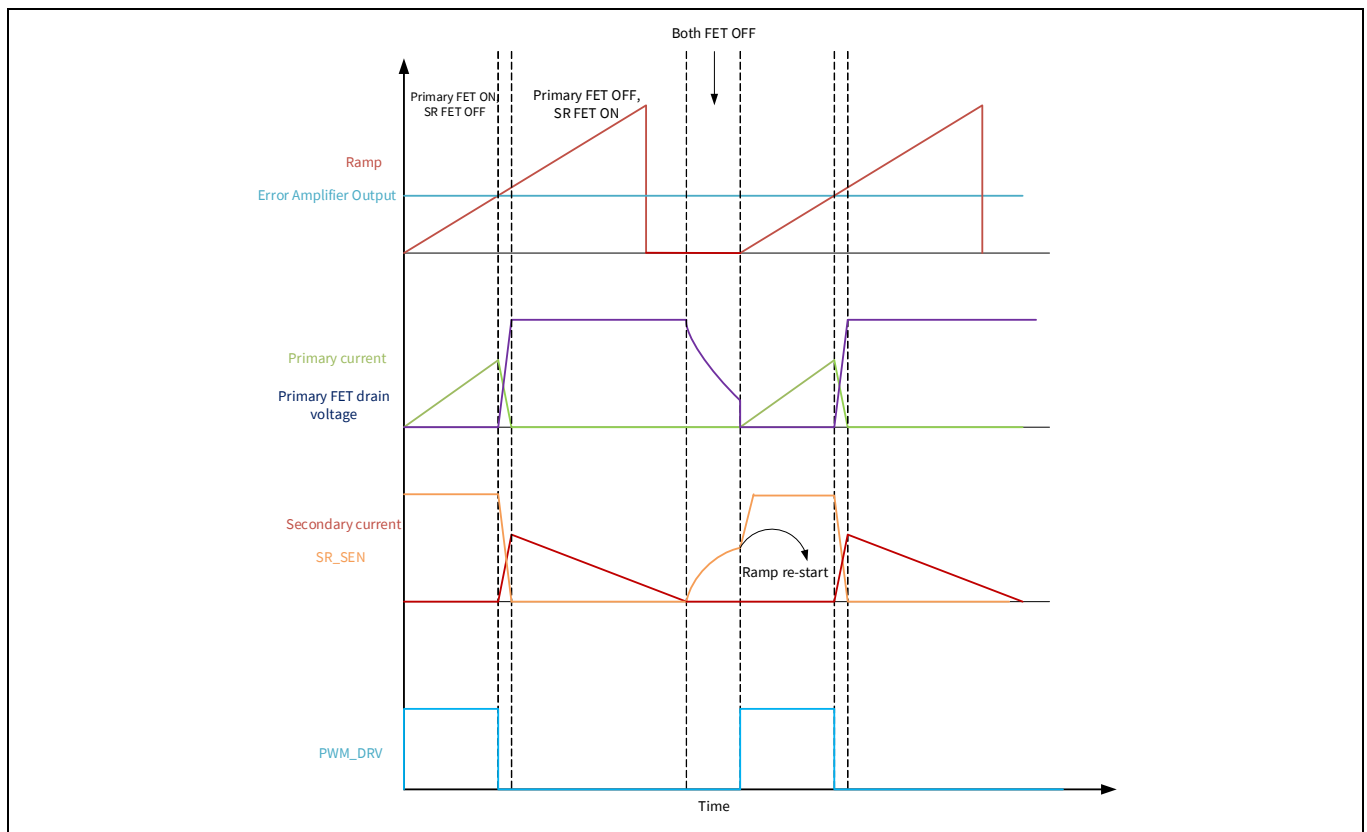
EZ-PD™ PAG1S integrates two error amplifier blocks which handles secondary output sensing and regulation for constant voltage (CV) and constant current (CC) modes. This block is responsible for both constant voltage and constant current operations. The error-amplifier output feeds in to the internal analog PWM block. The negative input of the error amplifier is the feedback (FB) pin and the positive input is internal reference of 0.744 V. The FB pin has internal resistor divider of 200 kΩ and 35 kΩ, this divider sets a default voltage of 0.744 V at FB pin when VBUS\_IN is at 5 V. Based on the desired VBUS\_C output, the voltage at the FB pin will be varied using internal current source/sink IDACs. An external compensation network is required between FB pin and EA\_OUT pin, as shown in [Figure 6](#).

Constant current operation makes use of an internal low-side current sense amplifier (LSCSA), the output of which feeds into an independent error amplifier as shown in [Figure 1](#). The reference to Constant current error-amplifier is programmable between 0.4 V to 2.1 V. Constant current mode regulation requires an external compensation network between CC\_COMP\_GPIO2 and EA\_OUT as shown in [Figure 6](#). EZ-PD™ PAG1S error amplifier can ensure constant voltage regulation from 3.3 V to 21.5 V range and constant current regulation from 1 A to 3 A as required by the USB PD PPS specification.

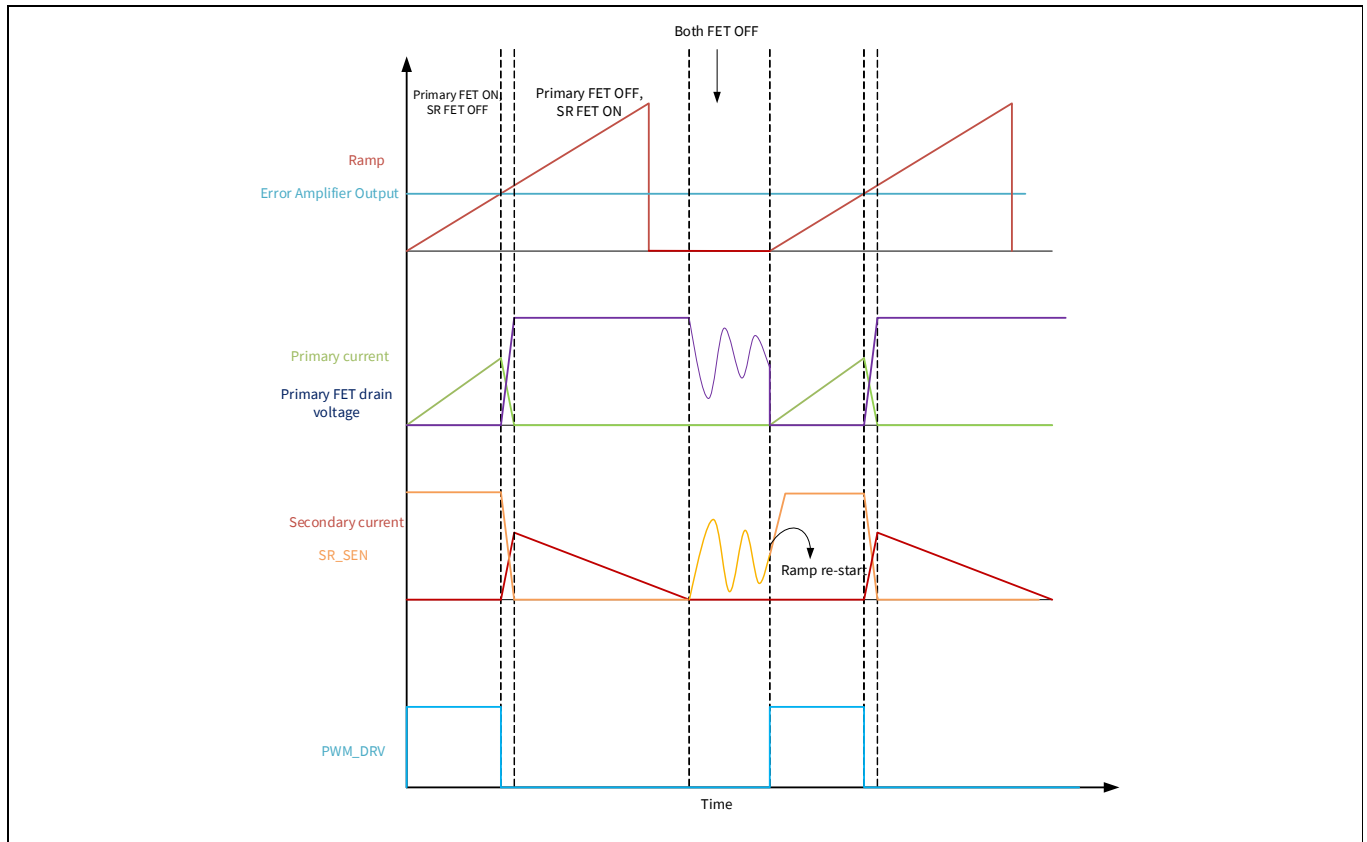
### 1.1.2 PWM\_DRV\_GPIO1

EZ-PD™ PAG1S supports an analog PWM generator, which modulates the pulse width of the primary side FET in voltage mode control. It generates a programmable ramp which is compared against the output of the error amplifier to determine the PWM pulse width. The ramp is generated by sourcing current into an internal capacitor, the source current is a programmable combination of a certain fixed current and feed forward current. The PWM signal is transferred from the secondary side to the primary side through an external pulse transformer. EZ-PD™ PAG1S also integrates a pulse transformer driver with VDDD/Ground based output. The output of the pulse transformer driver is brought out onto the PWM\_DRV\_GPIO1 pin.

See [Figure 4](#) and [Figure 5](#) for the waveforms representing PWM\_DRV functionality in QR/CrCM and DCM/valley switching.



**Figure 4** PWM\_DRV in QR/CrCM mode



**Figure 5** PWM\_DRV in DCM/valley switching mode

### 1.1.3 CC1, CC2

CC1 and CC2 are the communication channels for USB PD protocol. EZ-PD™ PAG1S integrates a USB PD transceiver consisting of a transmitter and receiver that communicate Biphase Mark Code (BMC) encoded data over the Configuration Channel (CC) channels as per the USB PD standard. All communication is half-duplex. The physical layer implements collision avoidance to minimize communication errors on the channel. This block includes all termination resistors ( $R_p$ ) and their switches as required by the USB PD specification. An external 390-pF capacitor is required on both the CC1 and CC2 pins.

### 1.1.4 DP\_GPIO4, DM\_GPIO5

The DP and DM lines are the standard USB D+ and D- lines. EZ-PD™ PAG1S integrates a charge detect block, which handles legacy charging protocols such as BC 1.2, Quick Charge, Apple charging, and Samsung AFC. This block integrates all the terminations required for these charging protocols and no external components are required. When legacy charging is not required in the system, the same DP and DM lines can be re-used as standard GPIOs.

### 1.1.5 VBUS\_IN, VDDD, VCCD

EZ-PD™ PAG1S integrates a high-voltage regulator, which is powered from the VBUS\_IN rail, the output of the regulator powers the VDDD rail. The input to the regulator can range from 3.3 V minimum to 21.5 V maximum. When the input is between 5.5 V and 21.5 V, the typical output of the regulator is 5 V. For inputs from 3.3 V to 5.5 V, the regulator output is VBUS\_IN – 300 mV.

This regulator can drive a maximum load current of 50 mA, which includes the chip current consumption. This regulator is not expected to drive any external loads or ICs. EZ-PD™ PAG1S also has an internal configurable discharge path for the VBUS\_IN rail, which is used to discharge the VBUS rail during negative voltage transitions. Through firmware settings, the internal discharge resistor can be set between 31.25  $\Omega$  to 2000  $\Omega$ .

The regulated supply VDDD, is either used to directly power some internal analog blocks or further regulated down to 1.8 V VCCD, which powers majority of the core. VDDD and VCCD is brought out on to pins to connect external capacitors for regulator stability and these are not meant to be used as power supplies.

### 1.1.6 VBUS\_C, VBUS\_CTRL

VBUS\_C is used to monitor the voltage at the Type-C connector. VBUS\_C has an internal configurable discharge path, which is used to discharge the VBUS\_C rail during negative voltage transitions. Through firmware settings, the internal discharge resistor can be set between 31.25  $\Omega$  to 2000  $\Omega$ .

The load switch is between VBUS\_IN and VBUS\_C. EZ-PD™ PAG1S integrates a NFET gate driver to control this load switch. VBUS\_CTRL is the output of this gate driver. To turn off the external NFET, the gate driver drives low. To turn on the external NFET, it drives the gate to VBUS\_IN + 8 V. In addition, there is a clamp circuit to limit the gate to VBUS\_IN + 8 V. There is an optional slow turn-on feature which is meant to avoid sudden in-rush current. For a typical gate capacitance of 3nF, a slow turn-on time of 2 ms to 10 ms is configurable using firmware.

### 1.1.7 CSP, CSN

EZ-PD™ PAG1S integrates a LSCSA to monitor the load current. CSP is the positive input pin for the LSCSA and CSN is the negative input. LSCSA offers wide gain options ranging from 5 to 150. Suggested Rsense for LSCSA is 5 m $\Omega$ . LSCSA has an active offset cancellation mechanism to improve accuracy.

### 1.1.8 GPIO0, GPIO3

EZ-PD™ PAG1S has six GPIOs, out of which two are dedicated GPIOs and the rest are multiplexed with other functionalities. These GPIOs support multiple drive modes and configurable threshold options. During power-on and reset, the I/O pins (except GPIO1) are forced to the tristate so as not to crowbar any inputs and/or cause excess turn-on current. PWM\_DRV\_GPIO1 is driven to zero at power-up to avoid spurious start of primary IC.

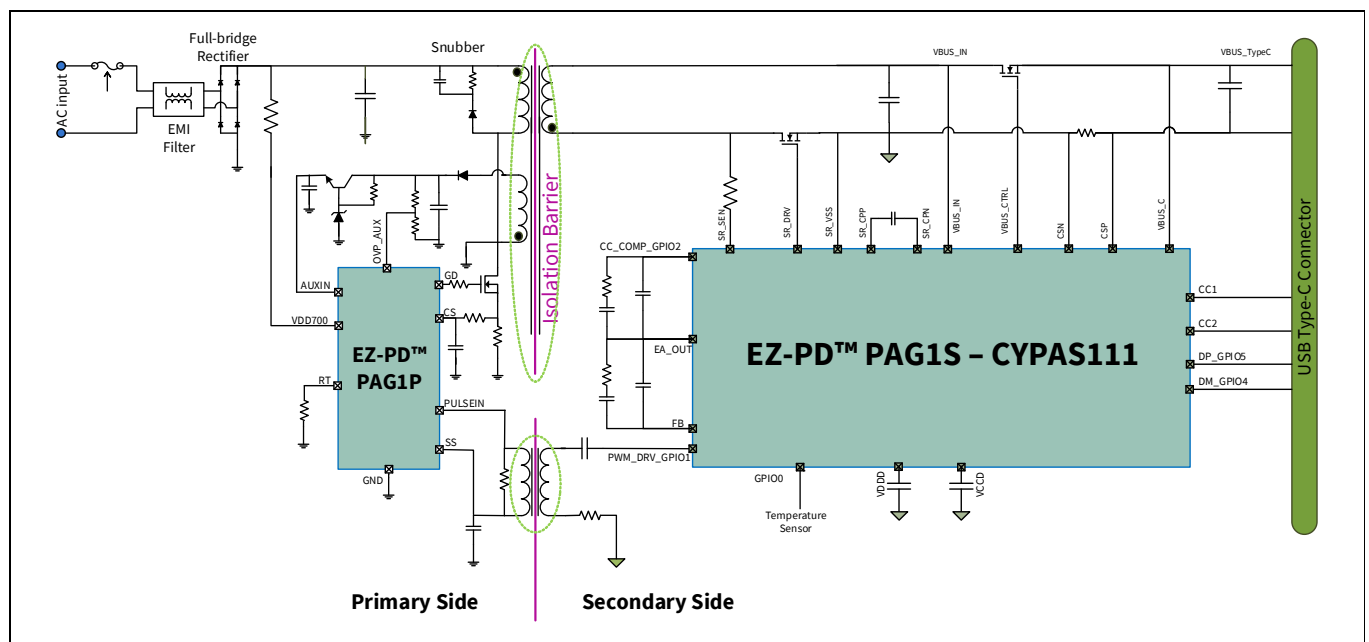
### 1.1.9 XRES

The XRES pin can be used to initiate a reset, this pin is internally pulled high and needs to be pulled low externally to trigger reset.

## 2 Application overview

## 2.1 USB Power Delivery power adapter with secondary side control

**Figure 6** shows a power adapter application diagram implementing a secondary side controlled synchronous flyback system. In this system, EZ-PD™ PAG1S modulates the pulse width of the primary MOSFET in voltage mode control. EZ-PD™ PAG1S engages the error amplifier and a programmable ramp generator to determine the pulse width of the PWM. This PWM signal is transferred from the secondary to the primary side through a pulse transformer. The primary controller can be any standard primary start-up controller and in **Figure 6**, EZ-PD™ PAG1P is used as the primary controller with EZ-PD™ PAG1S. In this topology, EZ-PD™ PAG1S integrates three key features: secondary side control, synchronous rectification, and charging port controller.



**Figure 6** Power adapter with secondary side control application diagram

### 3 Functional description

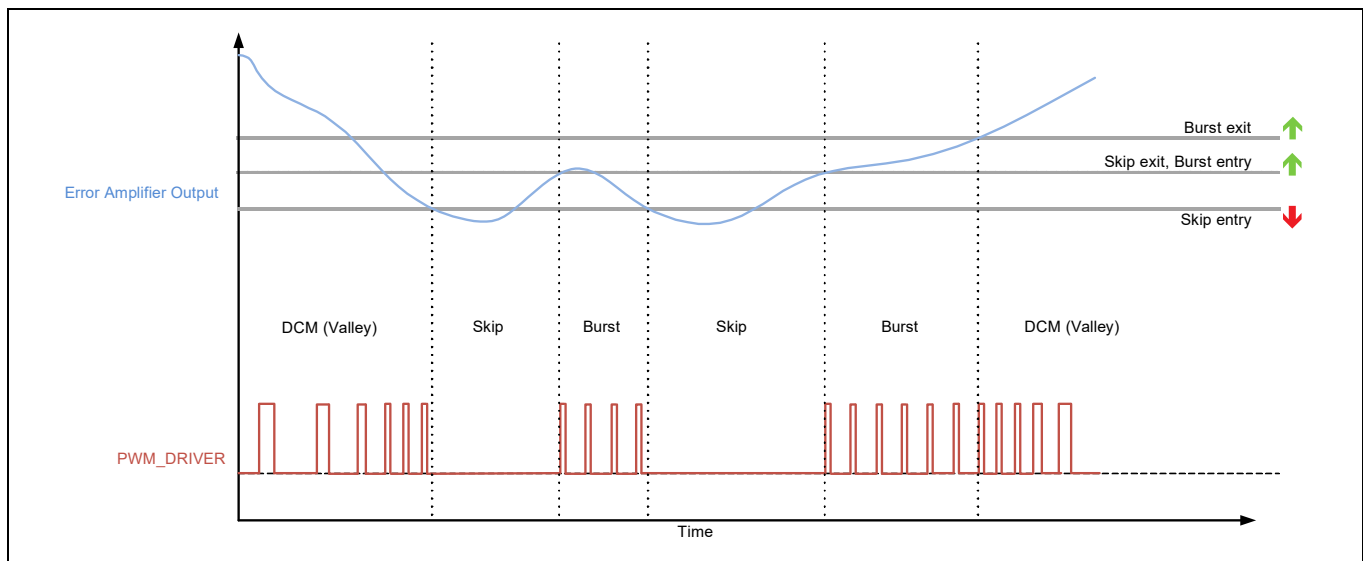
#### 3.1 Start-up behavior

On power-up, the primary side start-up controller shall start controlling the primary switch using its soft start mechanism and provide sufficient current to charge the secondary side output capacitor and the startup current required for EZ-PD™ PAG1S. The secondary output voltage is the input power supply source of EZ-PD™ PAG1S. Once VBUS\_IN voltage exceeds 3.3 V, EZ-PD™ PAG1S firmware will boot up and take control of the primary switch. EZ-PD™ PAG1S firmware boot up time is in the order of a few milliseconds.

Once the boot-up is complete, the firmware configures the error-amplifier to achieve 5 V secondary output and EZ-PD™ PAG1S will generate the PWM pulses accordingly. These pulses on PWM\_DRV\_GPIO1 are coupled to the primary start-up controller through a pulse transformer. On receiving the PWM pulses, the primary side start-up controller is expected to synchronize its internal oscillator with the PWM pulses and switch from start-up mode to secondary control mode. In the secondary control mode, the primary switch will be directly controlled by the PWM pulses generated by EZ-PD™ PAG1S.

#### 3.2 Modes of operation

EZ-PD™ PAG1S supports multiple modes of operation: Quasi-Resonant (QR) or Critical Conduction Mode (CrCM), Valley Switching, Discontinuous Conduction Mode (DCM), and Burst mode for light load operations. Analog PWM smart algorithm allows the operation to automatically transition between modes based on the output power requirement. The mode of operation stays in CrCM for higher loads, moves to DCM for medium loads and switches to pulse skip or burst mode for low and ultra-low power loads (see [Figure 7](#)). There are configurable options for minimum/maximum pulse width, minimum/maximum period and pulse skip or burst levels.



**Figure 7** Error amplifier output vs modes of operation

#### 3.3 Fault protection

##### 3.3.1 VBUS UVP and OVP

VBUS undervoltage and overvoltage faults are monitored using internal VBUS\_IN/VBUS\_C resistor dividers. The fault thresholds and response times are configurable in EZ-PD™ PAG1S. Refer [EZ-PD™ Configuration Utility](#) for more details on the configuration utility.

### 3.3.2 VBUS OCP and SCP

VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers. Same as OVP and UVP, the OCP and SCP fault thresholds and response times are configurable as well. Refer [EZ-PD™ Configuration Utility](#) for more details on the configuration utility.

### 3.3.3 OTP

Overtemperature monitoring is done using an external thermistor and internal ADC. The thermistor can be connected to any free GPIO. EZ-PD™ PAG1S contains one 8-bit SAR ADC, this is available for general purpose analog to digital conversions. The reference voltage to the ADC can be chosen from two sources: VDDD or a 2 V reference generated from internal bandgap.

### 3.3.4 ESD protection

EZ-PD™ PAG1S offers ESD protection on all the pins. The ESD protection level is 2.2-kV HBM and 500-V CDM.

### 3.3.5 VBUS to CC short protection

EZ-PD™ PAG1S offers protection against accidental short from VBUS\_C pin short to CC.

## 3.4 Power modes

EZ-PD™ PAG1S supports multiple power modes - Active, Sleep, and DeepSleep. Transitions between these modes is handled by the application firmware depending on the operating conditions.

## 4 Electrical specifications

### 4.1 Absolute maximum ratings

**Table 3** Absolute maximum ratings<sup>[1]</sup>

| Parameter                 | Description                                  | Min  | Typ | Max                    | Unit | Details/conditions |
|---------------------------|----------------------------------------------|------|-----|------------------------|------|--------------------|
| V <sub>BUS_IN_MAX</sub>   | Maximum input supply voltage                 | –    | –   | 24                     | V    | –                  |
| V <sub>DDD_MAX</sub>      | Maximum supply voltage                       | –    | –   | 6                      |      | –                  |
| V <sub>SR_DRAIN_MAX</sub> | Maximum voltage on SR_SEN pin                | –    | –   | 24                     |      | –                  |
| V <sub>GPIO_ABS</sub>     | GPIO voltage                                 | –0.5 | –   | V <sub>DDD</sub> + 0.5 |      | –                  |
| V <sub>CC_PIN_ABS</sub>   | Maximum voltage on CC1, CC2 voltage          | –    | –   | 24                     |      | –                  |
| I <sub>GPIO_ABS</sub>     | Current per GPIO                             | –    | –   | 25                     | mA   | –                  |
| ESD_HBM                   | Electrostatic discharge human body model     | 2200 | –   | –                      | V    | –                  |
| ESD_CDM                   | Electrostatic discharge charged device model | 500  | –   | –                      |      | –                  |
| I <sub>LU</sub>           | Pin current for latch-up                     | –100 | –   | 100                    | mA   | –                  |

#### Note

1. Usage of the above absolute maximum conditions listed in [Table 3](#) may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

## Electrical specifications

### 4.2 Device-level specifications

**Table 4 DC specifications**

| Spec ID     | Parameter             | Description                                                            | Min                       | Typ  | Max  | Unit | Details/conditions                                                                                                                                        |
|-------------|-----------------------|------------------------------------------------------------------------|---------------------------|------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID.PWR.1   | V <sub>DDD_REG</sub>  | V <sub>DDD</sub> output for 5.5 V ≤ V <sub>BUS_IN</sub> ≤ 21.5 V       | 4.6                       | 5.0  | 5.4  | V    | I <sub>LOAD</sub> = 0–50 mA                                                                                                                               |
| SID.PWR.2   | V <sub>DDD_MIN</sub>  | V <sub>DDD</sub> output for 3.3 V ≤ V <sub>BUS_IN</sub> ≤ 5.5 V        | V <sub>BUS_IN</sub> – 0.3 | –    | –    |      |                                                                                                                                                           |
| SID.PWR.3   | V <sub>DDD_MAX</sub>  | Max supply voltage relative to V <sub>SS</sub>                         | –                         | –    | 6    |      | –40°C to +105°C T <sub>A</sub> , Absolute Maximum                                                                                                         |
| SID.PWR.4   | V <sub>BUS_IN</sub>   | Power supply input voltage                                             | 3.3                       | –    | 21.5 |      | –                                                                                                                                                         |
| SID.PWR.6   | V <sub>CCD</sub>      | Output voltage for core logic                                          | –                         | 1.8  | –    |      | –                                                                                                                                                         |
| SID.PWR.8   | C <sub>efc</sub>      | Bypass capacitor for V <sub>CCD</sub>                                  | 0.8                       | 1    | 1.2  | μF   | X5R ceramic or better                                                                                                                                     |
| SID.PWR.9   | C <sub>exc</sub>      | Decoupling capacitor for V <sub>DDD</sub>                              | 1.8                       | –    | 2.2  |      |                                                                                                                                                           |
| SID.PWR.10  | C <sub>exv</sub>      | Decoupling capacitor for V <sub>BUS_IN</sub>                           | –                         | 1    | –    |      | Decoupling capacitor required near the IC pin.                                                                                                            |
| SID.PWR.10A | C <sub>excpp</sub>    | Capacitor between SR_CPP and SR_CPN pins                               | 0.1                       | –    | –    |      | X5R ceramic or better                                                                                                                                     |
| SID.PWR.15  | I <sub>DD_A</sub>     | Active current from V <sub>BUS_IN</sub> in Type-C attached state       | –                         | 25   | –    | mA   | V <sub>BUS_IN</sub> = 5 V, T <sub>A</sub> = 25°C, CC1/CC2 in TX or RX, CPU at 24 MHz, SR/PWM at 100 kHz, EA/ADC/CSA/UVOV blocks ON.                       |
| SID.PWR.16  | I <sub>DD_S_UA</sub>  | Sleep current from V <sub>BUS_IN</sub> in Type-C attached state        | –                         | 3.5  | –    |      | V <sub>BUS_IN</sub> = 5 V, T <sub>A</sub> = 25°C, Type-C attached, CPU OFF, PWM/EA/ADC/UVOV blocks ON. CC, watchdog timer (WDT) wakeup ON. IMO at 24 MHz. |
| SID.PWR.16A | I <sub>DD_DS_UA</sub> | Deep Sleep current from V <sub>BUS_IN</sub> in Type-C unattached state | –                         | 0.75 | –    |      | V <sub>BUS_IN</sub> = 5 V, T <sub>A</sub> = 25°C, Type-C unattached, CPU OFF, UVOV block ON, WDT Wakeup ON.                                               |
| SID.PWR.17  | V <sub>SR_DRAIN</sub> | Voltage allowed on SR_SEN pin                                          | –0.7                      | –    | 21.5 | V    | –                                                                                                                                                         |

**Table 5 AC Specifications**

| Spec ID     | Parameter              | Description                | Min | Typ | Max | Unit | Details/conditions |
|-------------|------------------------|----------------------------|-----|-----|-----|------|--------------------|
| SID.PWR.14  | T <sub>sleep</sub>     | Wakeup from sleep mode     | –   | 0   | –   | μs   | –                  |
| SID.PWR.14A | T <sub>deepsleep</sub> | Wakeup from deepsleep mode | –   | 35  | –   |      |                    |

## Electrical specifications

### 4.3 Functional block specifications

**Table 6 ADC specifications**

| Spec ID           | Parameter  | Description                              | Min                 | Typ | Max                 | Unit | Details/conditions                               |
|-------------------|------------|------------------------------------------|---------------------|-----|---------------------|------|--------------------------------------------------|
| DC specifications |            |                                          |                     |     |                     |      |                                                  |
| SID.ADC.1         | Resolution | ADC resolution                           | –                   | 8   | –                   | Bits | –                                                |
| SID.ADC.2         | INL        | Integral nonlinearity                    | –2.5                | –   | 2.5                 | LSB  | Reference voltage = VREF_ADC1                    |
| SYS.ADC.3         | INL        | Integral nonlinearity                    | –1.5                | –   | 1.5                 |      | Reference voltage = VREF_ADC2                    |
| SYS.ADC.4         | DNL        | Differential nonlinearity                | –2.5                | –   | 2.5                 |      | Reference voltage = VREF_ADC1                    |
| SYS.ADC.5         | DNL        | Differential nonlinearity                | –1.5                | –   | 1.5                 |      | Reference voltage = VREF_ADC2                    |
| SYS.ADC.6         | Gain Error | Gain error                               | –1.5                | –   | 1.5                 |      | –                                                |
| SYS.ADC.7         | VREF_ADC1  | ADC reference voltage                    | V <sub>DDDmin</sub> | –   | V <sub>DDDmax</sub> | V    | Reference voltage generated from V <sub>DD</sub> |
| SYS.ADC.8         | VREF_ADC2  | ADC reference voltage                    | 1.96                | 2.0 | 2.04                |      | Reference voltage generate from bandgap          |
| AC specifications |            |                                          |                     |     |                     |      |                                                  |
| SID.ADC.9         | Slew_Max   | Rate of change of sampled voltage signal | –                   | –   | 3                   | V/ms | Guaranteed by design                             |

**Table 7 Error amplifier**

| Spec ID                  | Parameter           | Description                           | Min  | Typ | Max | Unit | Details/conditions |
|--------------------------|---------------------|---------------------------------------|------|-----|-----|------|--------------------|
| <b>DC specifications</b> |                     |                                       |      |     |     |      |                    |
| SID.DC.VR.1              | V <sub>R</sub>      | VBUS voltage regulation accuracy      | –    | ± 3 | ± 5 | %    | –                  |
| SID.DC.VR.2              | I <sub>ka_off</sub> | Off-state EA_OUT current              | –    | 2.2 | 10  | μA   | –                  |
| SID.DC.VR.4              | DNL_ndac            | Differential nonlinearity of NMOS DAC | –1   | –   | 1   | LSB  | –                  |
| SID.DC.VR.5              | INL_ndac            | Integral nonlinearity of NMOS DAC     | –1.5 | –   | 1.5 |      | –                  |
| SID.DC.VR.6              | Gain_error_ndac     | Gain error of NMOS DAC                | –8   | –   | 8   | %    | –                  |
| SID.DC.VR.7              | DNL_pdac            | Differential nonlinearity of PMOS DAC | –0.5 | –   | 0.5 | LSB  | –                  |
| SID.DC.VR.8              | INL_pdac            | Integral nonlinearity of PMOS DAC     | –1   | –   | 1   |      | –                  |
| SID.DC.VR.9              | Gain_error_pdac     | Gain error of PMOS DAC                | –8   | –   | 8   | %    | –                  |

## Electrical specifications

**Table 8 LSCSA, SCP**

| Spec ID                  | Parameter       | Description                                                              | Min | Typ | Max | Unit | Details/conditions            |
|--------------------------|-----------------|--------------------------------------------------------------------------|-----|-----|-----|------|-------------------------------|
| <b>DC specifications</b> |                 |                                                                          |     |     |     |      |                               |
| SID.LSCSA.1              | Cin_inp         | CSP input capacitance                                                    | –   | –   | 10  | pF   | –                             |
| SID.LSCSA.2              | Csa_Acc1        | CSA accuracy with<br>5 mV < Vsense < 10 mV                               | –15 | –   | 15  | %    | –                             |
| SID.LSCSA.3              | Csa_Acc2        | CSA accuracy with<br>10 mV < Vsense < 15 mV                              | –10 | –   | 10  |      | –                             |
| SID.LSCSA.4              | Csa_Acc3        | CSA accuracy with<br>15 mV < Vsense                                      | –5  | –   | 5   |      | –                             |
| SID.LSCSA.5              | SCP_6A          | Short circuit trip point with<br>threshold set to 6 A                    | 5.4 | 6   | 6.6 | A    | Rsense = 5 mΩ                 |
| SID.LSCSA.6              | SCP_10A         | Short circuit trip point with<br>threshold set to 10 A                   | 9   | 10  | 11  |      |                               |
| SID.LSCSA.8              | Av              | CSA gain values supported:<br>5, 10, 20, 35, 50, 75, 125, 150            | 5   | –   | 150 | V/V  | –                             |
| SID.VSP.1                | V_short_trigger | Short-to-VBUS system-side<br>clamping voltage on the CC pins             | 6   | 9   | 12  | V    | –                             |
| <b>AC specifications</b> |                 |                                                                          |     |     |     |      |                               |
| SID.LSCSA.AC.1           | Tocp_gate       | Delay from OCP threshold trip<br>to external NFET gate turn off          | –   | 4.0 | 20  | μs   | –                             |
| SID.LSCSA.AC.2           | Tscp_gate       | Delay from SCP threshold trip<br>to external NFET gate turn off          | –   | 3.1 | –   |      | 1 nF NFET gate<br>capacitance |
| SID.LSCSA.AC.3           | Tscp_gate_1     | Delay from SCP threshold trip<br>to external NFET power gate<br>turn off | –   | 7.5 | –   |      | 3 nF NFET gate<br>capacitance |

**Table 9 VBUS UV, OV**

| Spec ID           | Parameter | Description                                                       | Min  | Typ | Max | Unit | Details/conditions |
|-------------------|-----------|-------------------------------------------------------------------|------|-----|-----|------|--------------------|
| DC specifications |           |                                                                   |      |     |     |      |                    |
| SID.UVOV.1        | VTHOV1    | Over-Voltage threshold Accuracy, 4 V to 11 V                      | −3   | −   | 3   | %    | −                  |
| SID.UVOV.2        | VTHOV2    | Over-Voltage threshold Accuracy, 11 V to 21.5 V                   | −3.2 | −   | 3.2 |      | −                  |
| SID.UVOV.3        | VTHUV1    | Under-Voltage threshold Accuracy, 3 V to 3.3 V                    | −4   | −   | 4   |      | −                  |
| SID.UVOV.4        | VTHUV2    | Under-Voltage threshold Accuracy, 3.3 V to 4.0 V                  | −3.5 | −   | 3.5 |      | −                  |
| SID.UVOV.5        | VTHUV3    | Under-Voltage threshold Accuracy, 4.0 V to 11 V                   | −3   | −   | 3   |      | −                  |
| SID.UVOV.6        | VTHUV4    | Under-Voltage threshold Accuracy, 11 V to 21.5 V                  | −2.9 | −   | 2.9 |      | −                  |
| AC specifications |           |                                                                   |      |     |     |      |                    |
| SID.UVOV.AC.1     | Tov_gate  | Delay from OV threshold trip to external NFET Power Gate Turn off | −    | −   | 50  | μs   | −                  |

## Electrical specifications

**Table 10 PD transceiver**

| Spec ID                  | Parameter  | Description                                                       | Min  | Typ | Max | Unit | Details/conditions                 |
|--------------------------|------------|-------------------------------------------------------------------|------|-----|-----|------|------------------------------------|
| <b>DC specifications</b> |            |                                                                   |      |     |     |      |                                    |
| SID.PD.1                 | Rp_std     | Downstream facing port (DFP) CC termination for default USB power | 64   | 80  | 96  | μA   | –                                  |
| SID.PD.2                 | Rp_1.5A    | DFP CC termination for 1.5 A USB power                            | 166  | 180 | 194 |      | –                                  |
| SID.PD.3                 | Rp_3.0A    | DFP CC termination for 3.0 A USB power                            | 304  | 330 | 356 |      | –                                  |
| SID.PD.4                 | Vgndoffset | Ground offset tolerated by BMC receiver                           | –500 | –   | 500 | mV   | Relative to remote BMC transmitter |

**Table 11 VBUS discharge**

| Spec ID                  | Parameter       | Description                                         | Min   | Typ | Max  | Unit | Details/conditions             |
|--------------------------|-----------------|-----------------------------------------------------|-------|-----|------|------|--------------------------------|
| <b>DC specifications</b> |                 |                                                     |       |     |      |      |                                |
| SID.VBUS.DISC.1          | R1              | 20 V NMOS ON resistance for discharge strength = 1  | 500   | –   | 2000 | Ω    | Measured at 0.5 V              |
| SID.VBUS.DISC.2          | R2              | 20 V NMOS ON resistance for discharge strength = 2  | 250   | –   | 1000 |      |                                |
| SID.VBUS.DISC.3          | R4              | 20 V NMOS ON resistance for discharge strength = 4  | 125   | –   | 500  |      |                                |
| SID.VBUS.DISC.4          | R8              | 20 V NMOS ON resistance for discharge strength = 8  | 62.5  | –   | 250  |      |                                |
| SID.VBUS.DISC.5          | R16             | 20 V NMOS ON resistance for discharge strength = 16 | 31.25 | –   | 125  |      |                                |
| SID.VBUS.DISC.6          | Vbus_stop_error | Error percentage of final VBUS value                | –     | –   | 10   | %    | When VBUS is discharged to 5 V |

## Electrical specifications

**Table 12 VBUS NFET gate driver**

| Spec ID                  | Parameter | Description                                                                                 | Min | Typ  | Max | Unit          | Details/conditions            |
|--------------------------|-----------|---------------------------------------------------------------------------------------------|-----|------|-----|---------------|-------------------------------|
| <b>DC specifications</b> |           |                                                                                             |     |      |     |               |                               |
| SID.GD.1                 | GD_VGS    | Gate to source overdrive during NFET ON condition                                           | 4.5 | 5.75 | 10  | V             | $V_{BUS\_IN} = 21.5\text{ V}$ |
| SID.GD.2                 | GD_Rpd    | Resistance when pull-down is enabled to turn off external NFET                              | –   | 0.57 | 2   | k $\Omega$    | –                             |
| <b>AC specifications</b> |           |                                                                                             |     |      |     |               |                               |
| AC.GD.1                  | Ton       | $V_{BUS\_ctrl}$ Low to High (1 V to $V_{BUS} + 1\text{ V}$ ) with 3 nF external capacitance | 2   | 5    | 10  | ms            | $V_{BUS\_IN} = 5\text{ V}$    |
| AC.GD.2                  | Toff      | $V_{BUS\_ctrl}$ High to Low (90% to 10%) with 3 nF external capacitance                     | –   | 7    | –   | $\mu\text{s}$ | $V_{BUS\_IN} = 21.5\text{ V}$ |

**Table 13 High-voltage regulator**

| Spec ID                  | Parameter      | Description                                          | Min | Typ | Max | Unit          | Details/conditions                                            |
|--------------------------|----------------|------------------------------------------------------|-----|-----|-----|---------------|---------------------------------------------------------------|
| <b>DC specifications</b> |                |                                                      |     |     |     |               |                                                               |
| SID.VREG.1               | VOLTAGE_DETECT | VBUS_IN voltage detect threshold                     | 1.7 | 2.1 | 2.4 | V             | –                                                             |
| SID.VREG.2               | Tstart         | Total start-up time for the regulator supply outputs | –   | 50  | 200 | $\mu\text{s}$ | From VBUS reaching Voltage_detect level to 95% of final value |

## Electrical specifications

**Table 14 SR sense and driver**

| Spec ID                  | Parameter              | Description                                                                                                                                                                           | Min  | Typ | Max | Unit | Details/conditions |
|--------------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|-----|------|--------------------|
| <b>DC specifications</b> |                        |                                                                                                                                                                                       |      |     |     |      |                    |
| SR.1                     | VCPP1                  | Voltage doubler output for $3.3\text{ V} \leq \text{VBUS\_IN} \leq 5.5\text{ V}$                                                                                                      | 5    | –   | –   | V    | –                  |
| SR.2                     | VCPP2                  | Voltage doubler output for $5.5\text{ V} \leq \text{VBUS\_IN} \leq 21.5\text{ V}$                                                                                                     | 9    | –   | 11  |      | –                  |
| SR.3                     | TR_SR                  | Rise time (20% to 80%) of SR gate driver output with $\text{CL} = 6\text{ nF}$ , $\text{VBUS\_IN} = 3.3\text{ V}$ , including doubler rise time (with and without double bypass mode) | –    | –   | 150 | ns   | –                  |
| SR.4                     | TF_SR                  | Fall time (80% to 20%) of SR gate driver output with $\text{CL} = 6\text{ nF}$ , $\text{VBUS\_IN} = 3.3\text{ V}$ , including doubler rise time (with and without double bypass mode) | –    | –   | 100 |      | –                  |
| SR.5                     | I <sub>IK_SR_VSS</sub> | Input leakage current on SR_VSS                                                                                                                                                       | –1   | –   | 1   | μA   | –                  |
| SR.6                     | VTRIP_NSN_100          | Negative sense trip voltage to turn-ON secondary switch                                                                                                                               | –140 | –90 | –60 | mV   | –                  |
| SR.7                     | VTRIP_ZCD              | Negative sense trip voltage to turn-OFF secondary switch                                                                                                                              | –8   | –5  | –3  |      | –                  |
| SR.8                     | TD_ON                  | Turn on propagation delay from SR_SEN at –100 mV to SR_GDRV reaching 1 V                                                                                                              | –    | 25  | 50  | ns   | –                  |
| SR.9                     | TD_OFF                 | Turn off propagation delay from SR_SEN at –5 mV to SR_GDRV reaching 1 V                                                                                                               | –    | 100 | 200 |      | –                  |
| SR.10                    | IO_SRC_SNK             | Output peak current (Source and sink)                                                                                                                                                 | –    | 1   | –   | A    | –                  |

**Table 15 Analog PWM generator and pulse transformer driver**

| Spec ID                  | Parameter | Description                  | Min | Typ | Max | Unit | Details/conditions |
|--------------------------|-----------|------------------------------|-----|-----|-----|------|--------------------|
| <b>DC specifications</b> |           |                              |     |     |     |      |                    |
| PWM.1                    | FSW       | Switching frequency          | 20  | –   | 150 | kHz  | –                  |
| PWM.2                    | PWM_ON    | Minimum controllable ON time | 100 | –   | –   | ns   | –                  |

## Electrical specifications

### 4.4 I/O specifications

**Table 16 I/O specifications**

| Spec ID                  | Parameter       | Description                                                                     | Min                  | Typ | Max                 | Unit | Details/conditions                           |
|--------------------------|-----------------|---------------------------------------------------------------------------------|----------------------|-----|---------------------|------|----------------------------------------------|
| <b>DC specifications</b> |                 |                                                                                 |                      |     |                     |      |                                              |
| SID.GIO.1                | I <sub>LU</sub> | Latch-up current limits                                                         | -140                 | -   | 140                 | mA   | -                                            |
| SID.GIO.2                | RPU             | Pull-up resistor value                                                          | 3.5                  | 5.6 | 8.5                 | kΩ   | -                                            |
| SID.GIO.3                | RPD             | Pull-down resistor value                                                        | 3.5                  | 5.6 | 8.5                 |      | -                                            |
| SID.GIO.4                | IIL             | Input leakage current                                                           | -                    |     | 2                   | nA   | -                                            |
| SID.GIO.5                | CPIN_A          | Max pin capacitance                                                             | -                    |     | 22                  | pF   | Capacitance on DP/DM lines                   |
| SID.GIO.6                | CPIN            | Max pin capacitance                                                             | -                    | 3   | 7                   |      | Capacitance on all GPIOs, except DP/DM lines |
| SID.GIO.7                | Voh_3V          | Output voltage high level                                                       | $V_{DD} - 0.6$       | -   | -                   | V    | Ioh = -4 mA                                  |
| SID.GIO.8                | Vol_3V          | Output voltage low level                                                        | -                    | -   | 0.6                 |      | Iol = 10 mA                                  |
| SID.GIO.9                | Vih_CMOS        | Input voltage high threshold                                                    | $0.7 \times V_{DD}$  | -   | -                   |      | -                                            |
| SID.GIO.10               | Vil_CMOS        | Input voltage low threshold                                                     | -                    | -   | $0.3 \times V_{DD}$ |      | -                                            |
| SID.GIO.11               | Vih_TTL         | LVTTL input                                                                     | 2                    | -   | -                   |      | -                                            |
| SID.GIO.12               | Vil_TTL         | LVTTL input                                                                     | -                    | -   | 0.8                 |      | -                                            |
| SID.GIO.13               | Vhysttl         | Input hysteresis LVTTL                                                          | 100                  | -   | -                   | mV   | -                                            |
| SID.GIO.14               | Vhyscmos        | Input hysteresis CMOS                                                           | $0.05 \times V_{DD}$ | -   | -                   |      | -                                            |
| SID.GIO.15               | IDIODE          | Current through protection diode to $V_{DD}/V_{SS}$                             | -                    | -   | 100                 | μA   | -                                            |
| SID.GIO.16               | TriseF          | Rise time in fast strong mode                                                   | 2                    | -   | 12                  | ns   | Cload = 25 pF                                |
| SID.GIO.17               | TfallF          | Fall time in fast strong mode                                                   | 2                    | -   | 12                  |      |                                              |
| SID.GIO.18               | TriseS          | Rise time in slow strong mode                                                   | 10                   | -   | 60                  |      |                                              |
| SID.GIO.19               | TfallS          | Fall time in slow strong mode                                                   | 10                   | -   | 60                  |      |                                              |
| SID.GIO.20               | FGPIO_OUT1      | GPIO Fout;<br>$3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ;<br>Fast strong mode. | -                    | -   | 16                  | MHz  | -                                            |
| SID.GIO.21               | FGPIO_OUT2      | GPIO Fout;<br>$3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ;<br>Slow strong mode. | 7                    | -   | -                   |      |                                              |
| SID.GIO.22               | FGPIO_IN        | GPIO input operating frequency;<br>$3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$   | 16                   | -   | -                   |      |                                              |

## 4.5 System resources specifications

**Table 17 Power-on reset (POR) specifications**

| Spec ID   | Parameter | Description                                               | Min  | Typ | Max  | Unit | Details/conditions         |
|-----------|-----------|-----------------------------------------------------------|------|-----|------|------|----------------------------|
| SID.POR.1 | VRISEIPOR | Power-on-reset (POR) rising trip voltage                  | 0.8  | –   | 1.5  | V    | –                          |
| SID.POR.2 | VFALLIPOR | POR falling trip voltage                                  | 0.7  | –   | 1.4  |      | –                          |
| SID.POR.3 | VFALLPPOR | Brown-out-detect (BOD) trip voltage<br>Active/Sleep modes | 1.48 | –   | 1.62 |      | –                          |
| SID.CLK#6 | SR_POWER  | Power supply slew rate                                    | 0.40 | –   | 67   | V/ms | On power-up and power-down |

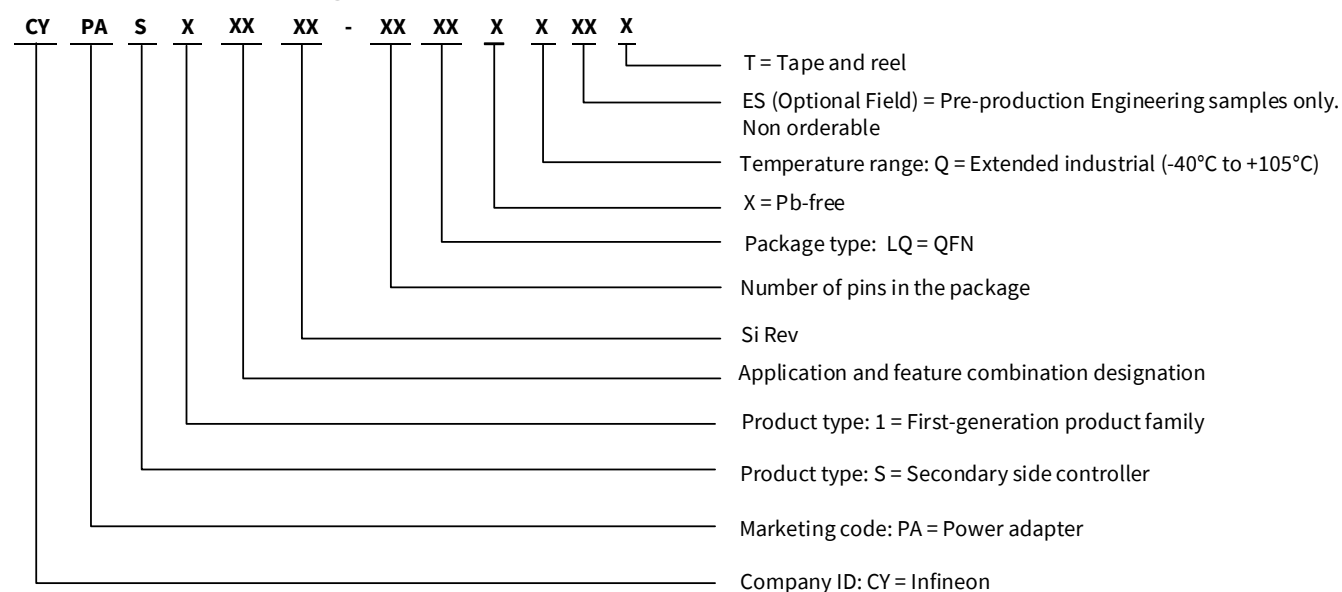
## Ordering information

## 5 Ordering information

**Table 18**      **EZ-PD™ PAG1S ordering information**

| MPN                | Application                                            | Package type | Si ID | Si Rev |
|--------------------|--------------------------------------------------------|--------------|-------|--------|
| CYPAS111A1-24LQXQ  | USB Power Delivery adapter with secondary side control | 24-pin QFN   | 2B01  | A1     |
| CYPAS111A1-24LQXQT |                                                        |              |       |        |

### 5.1 Ordering code definitions



## 6 Packaging

**Table 19** Package characteristics

| Parameter | Description                    | Conditions          | Min | Typ | Max   | Unit |
|-----------|--------------------------------|---------------------|-----|-----|-------|------|
| $T_A$     | Operating ambient temperature  | Extended industrial | -40 | 25  | 105   | °C   |
| $T_J$     | Operating junction temperature | Extended industrial | -40 | 25  | 120   |      |
| $T_{JA}$  | Package $\theta_{JA}$          | –                   | –   | –   | 19.98 | °C/W |
| $T_{JC}$  | Package $\theta_{JC}$          | –                   | –   | –   | 4.78  |      |

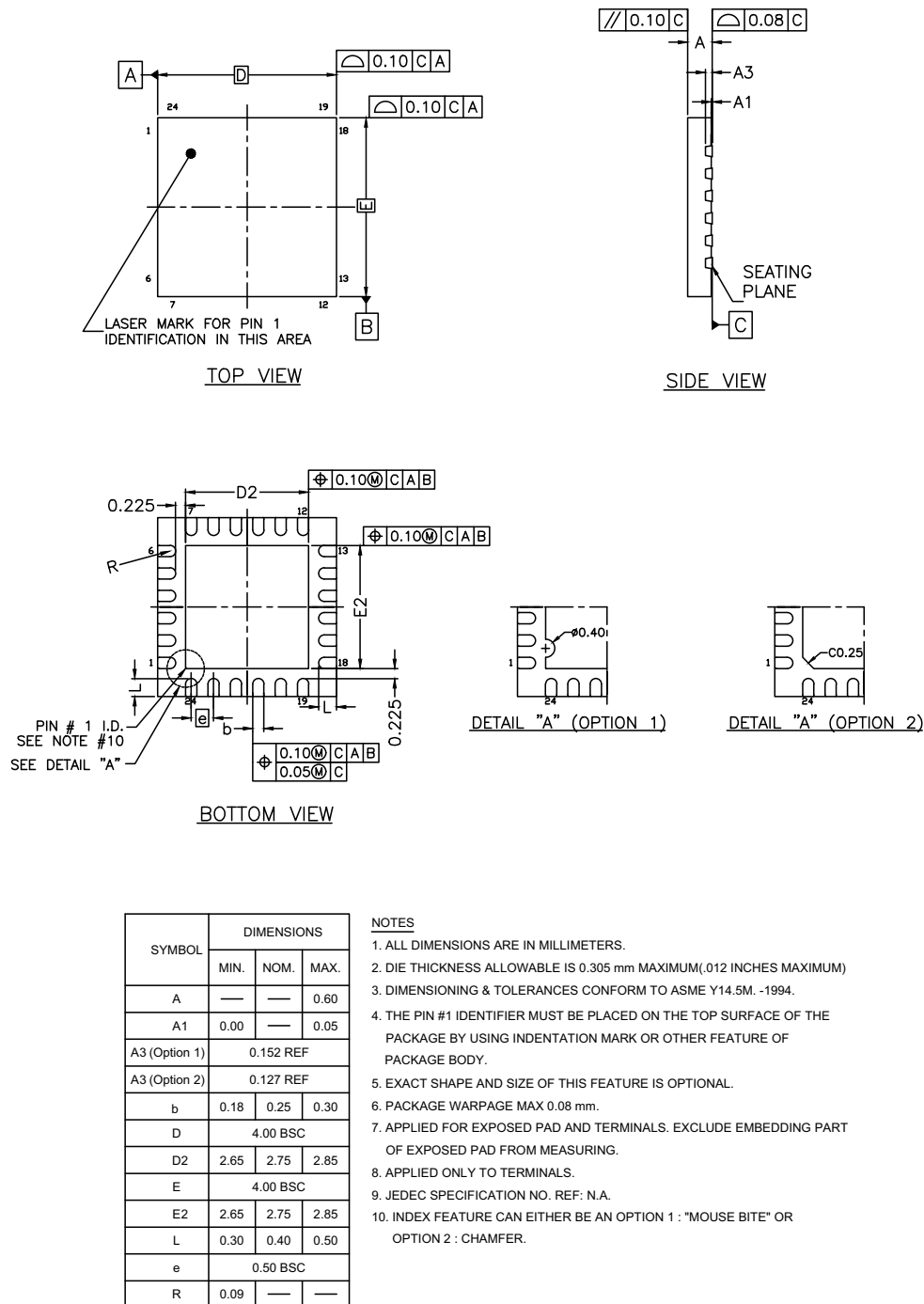
**Table 20** Solder reflow peak temperature

| Package    | Maximum peak temperature | Maximum time within 5°C of peak temperature |
|------------|--------------------------|---------------------------------------------|
| 24-pin QFN | 260°C                    | 30 seconds                                  |

**Table 21** Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

| Package    | MSL   |
|------------|-------|
| 24-pin QFN | MSL 3 |

## Packaging



002-16934 \*E

**Figure 8** 24-pin QFN ((4 x 4 x 0.6 mm), 2.75 x 2.75 mm EPAD (Sawn)) package outline, 002-16934

## 7 Acronyms

**Table 22** Acronyms used in this document

| Acronym                  | Description                                                                                                   |
|--------------------------|---------------------------------------------------------------------------------------------------------------|
| ADC                      | analog-to-digital converter                                                                                   |
| API                      | application programming interface                                                                             |
| Arm®                     | advanced RISC machine, a CPU architecture                                                                     |
| CC                       | constant current                                                                                              |
| BOD                      | Brown out Detect                                                                                              |
| BMC                      | biphase mark code                                                                                             |
| CPU                      | central processing unit                                                                                       |
| CRC                      | cyclic redundancy check, an error-checking protocol                                                           |
| CS                       | current sense                                                                                                 |
| DFP                      | downstream facing port                                                                                        |
| DIO                      | digital input/output, GPIO with only digital capabilities, no analog. See GPIO.                               |
| DRP                      | dual role port                                                                                                |
| EEPROM                   | electrically erasable programmable read-only memory                                                           |
| EMCA                     | a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports |
| EMI                      | electromagnetic interference                                                                                  |
| ESD                      | electrostatic discharge                                                                                       |
| FPB                      | flash patch and breakpoint                                                                                    |
| FS                       | full-speed                                                                                                    |
| GPIO                     | general-purpose input/output                                                                                  |
| IC                       | integrated circuit                                                                                            |
| IDE                      | integrated development environment                                                                            |
| I <sup>2</sup> C, or IIC | Inter-Integrated Circuit, a communications protocol                                                           |
| ILO                      | internal low-speed oscillator, see also IMO                                                                   |
| IMO                      | internal main oscillator, see also ILO                                                                        |
| I/O                      | input/output, see also GPIO                                                                                   |
| LSCSA                    | low side current sense amplifier                                                                              |
| LVD                      | low-voltage detect                                                                                            |
| LVTTL                    | low-voltage transistor-transistor logic                                                                       |
| MCU                      | microcontroller unit                                                                                          |
| NC                       | no connect                                                                                                    |
| NMI                      | nonmaskable interrupt                                                                                         |
| NMOS                     | N-type metal-oxide-semiconductor                                                                              |
| NVIC                     | nested vectored interrupt controller                                                                          |
| opamp                    | operational amplifier                                                                                         |
| OCP                      | overcurrent protection                                                                                        |
| OVP                      | overvoltage protection                                                                                        |

## Acronyms

**Table 22** Acronyms used in this document *(continued)*

| Acronym | Description                                                                                                  |
|---------|--------------------------------------------------------------------------------------------------------------|
| PCB     | printed circuit board                                                                                        |
| PD      | power delivery                                                                                               |
| PGA     | programmable gain amplifier                                                                                  |
| PHY     | physical layer                                                                                               |
| PMOS    | P-type metal-oxide-semiconductor                                                                             |
| POR     | power-on reset                                                                                               |
| PRES    | precise power-on reset                                                                                       |
| PSoC™   | programmable system-on-chip                                                                                  |
| PWM     | pulse-width modulator                                                                                        |
| RAM     | random-access memory                                                                                         |
| RISC    | reduced-instruction-set computing                                                                            |
| RMS     | root-mean-square                                                                                             |
| RTC     | real-time clock                                                                                              |
| RX      | receive                                                                                                      |
| SAR     | successive approximation register                                                                            |
| SCL     | I <sup>2</sup> C serial clock                                                                                |
| SDA     | I <sup>2</sup> C serial data                                                                                 |
| S/H     | sample and hold                                                                                              |
| SPI     | Serial Peripheral Interface, a communications protocol                                                       |
| SRAM    | static random access memory                                                                                  |
| SWD     | serial wire debug, a test protocol                                                                           |
| TX      | transmit                                                                                                     |
| Type-C  | a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power |
| UART    | Universal Asynchronous Transmitter Receiver, a communications protocol                                       |
| USB     | Universal Serial Bus                                                                                         |
| WDT     | watchdog timer                                                                                               |
| USBIO   | USB input/output, CCG5 pins used to connect to a USB port                                                    |
| XRES    | external reset I/O pin                                                                                       |

## 8 Document conventions

### 8.1 Units of measure

**Table 23** Units of measure

| Symbol | Unit of measure        |
|--------|------------------------|
| °C     | degrees Celsius        |
| Hz     | hertz                  |
| KB     | 1024 bytes             |
| kHz    | kilohertz              |
| kΩ     | kilo ohm               |
| Mbps   | megabits per second    |
| MHz    | megahertz              |
| MΩ     | mega-ohm               |
| Msps   | megasamples per second |
| μA     | microampere            |
| μF     | microfarad             |
| μs     | microsecond            |
| μV     | microvolt              |
| μW     | microwatt              |
| mA     | milliampere            |
| ms     | millisecond            |
| mV     | millivolt              |
| nA     | nanoampere             |
| ns     | nanosecond             |
| Ω      | ohm                    |
| pF     | picofarad              |
| ppm    | parts per million      |
| ps     | picosecond             |
| s      | second                 |
| sps    | samples per second     |
| V      | volt                   |

## Revision history

| Document version | Date of release | Description of changes                                                                                                                                                                                                                                                                                                                                                      |
|------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| *B               | 2019-08-19      | Changed document status from Preliminary to Final.                                                                                                                                                                                                                                                                                                                          |
| *C               | 2022-05-18      | Updated <b>Ordering information</b> :<br>Updated part numbers.<br>Updated <b>Packaging</b> :<br>spec 002-16934 – Changed revision from *B to *E.<br>Migrated to Infineon template.                                                                                                                                                                                          |
| *D               | 2022-06-16      | Updated <b>Electrical specifications</b> :<br>Updated <b>Device-level specifications</b> :<br>Updated <b>Table 4</b> :<br>Changed maximum value of Cexc parameter from 4.7 $\mu$ F to 2.2 $\mu$ F.<br>Updated <b>System resources specifications</b> :<br>Updated <b>Table 17</b> :<br>Added SR_POWER parameter and its corresponding details.<br>Completing Sunset Review. |

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