950 V CoolMOS™ PFD7 update from 900 V CoolMOS™ C3 for ICL5102HV LCC board

A comparison of 950 V CoolMOS™ PFD7 vs. 900 V CoolMOS™ C3

About this document

Scope and purpose

This document showcases Infineon's latest high-voltage (HV) superjunction MOSFET, the new 950 V CoolMOS™ PFD7. The electrical characteristics of the 950 V CoolMOS™ PFD7 provide all the benefits of the 950 V CoolMOS™ P7, while having a fast body diode and being available in drain-to-source resistance ($R_{DS(on)}$) as low as 60 mΩ. The fast body diode of the 950 V CoolMOS™ PFD7 enables half- and full-bridge topologies such as the LLC/LCC. This study focuses on updating the evaluation board REF-ICL5102HV-U150W, which is a power factor correction (PFC) + LCC board for lighting, from the 900 V CoolMOS™ C3 to the new 950 V CoolMOS™ PFD7. The MOSFETs to be updated are on the LCC side, so this report will focus on the performance difference of the LCC topology.

Intended audience

This document is intended for anyone who is interested in the new 950 V CoolMOS™ PFD7, especially those interested in updating their current designs from a previous-generation CoolMOS™.

Table of contents

1 Introduction

This document reports on the process and results of updating the LCC MOSFETs of the REF-ICL5102HV-U150W lighting evaluation board, from 900 V CoolMOS™ C3 to 950 V CoolMOS™ PFD7. The considerations needed before making the change, as well as the comparison in waveforms, efficiency, thermals and electromagnetic immunity (EMI) are explained.

As mentioned, this report focuses on the LCC stage of the board, due to the PFC experiencing no change. If the performance of the PFC stage is of interest, please refer to the **150 W LCC LED driver demonstration board with ICL5102HV** application note.

Please refer to the **950 V CoolMOS™ PFD7 family page** to see the full product portfolio and to the **950 V CoolMOS™ PFD7 application note** for a deeper understanding of the technology.

2 Target board description

The LCC stage of the REF-ICL5102HV-U150W board is a soft-switching half-bridge topology, where the resonant tank is comprised of one inductor and one capacitor in series, with one capacitor in parallel to the rectifier, as shown in **Figure 1**.

Table 1 Key electrical specifications of board

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
AC input voltage	$V_{in,ac}$	277	380 to 480	527	V_{RMS}	
Input frequency	f_{in}	47		63	Hz	
Inrush current	$I_{in,pk}$			35	A_{pk}	
Total harmonic distortion	THD			10%	–	50% load, 380 V_{RMS}
Efficiency	η	92%			–	50% load, 480 V_{RMS}
Rated LED voltage	V_{LED}	17		48	V DC	
Full LED current	$I_{LED,full}$	2.97		3.03	A	V_{dim} = 10 V
LCC frequency range	f_{LCC}	40		130	kHz	
Line regulation	$\Delta I_{out.line}$			±1	%	Current regulation
Load regulation	$\Delta V_{out.load}$			±1	%	I_{LED} = 1 to 100%
EMI	EN 55015					
Harmonics	EN 61000-3-2 class C					

Table 1 lists the key specifications of this demonstration board. Even if the LCC MOSFETs are being changed to the 950 V CoolMOS™ PFD7, the key electrical specifications are kept equal so that the comparison with the 900 V CoolMOS™ C3 is objective and fair.

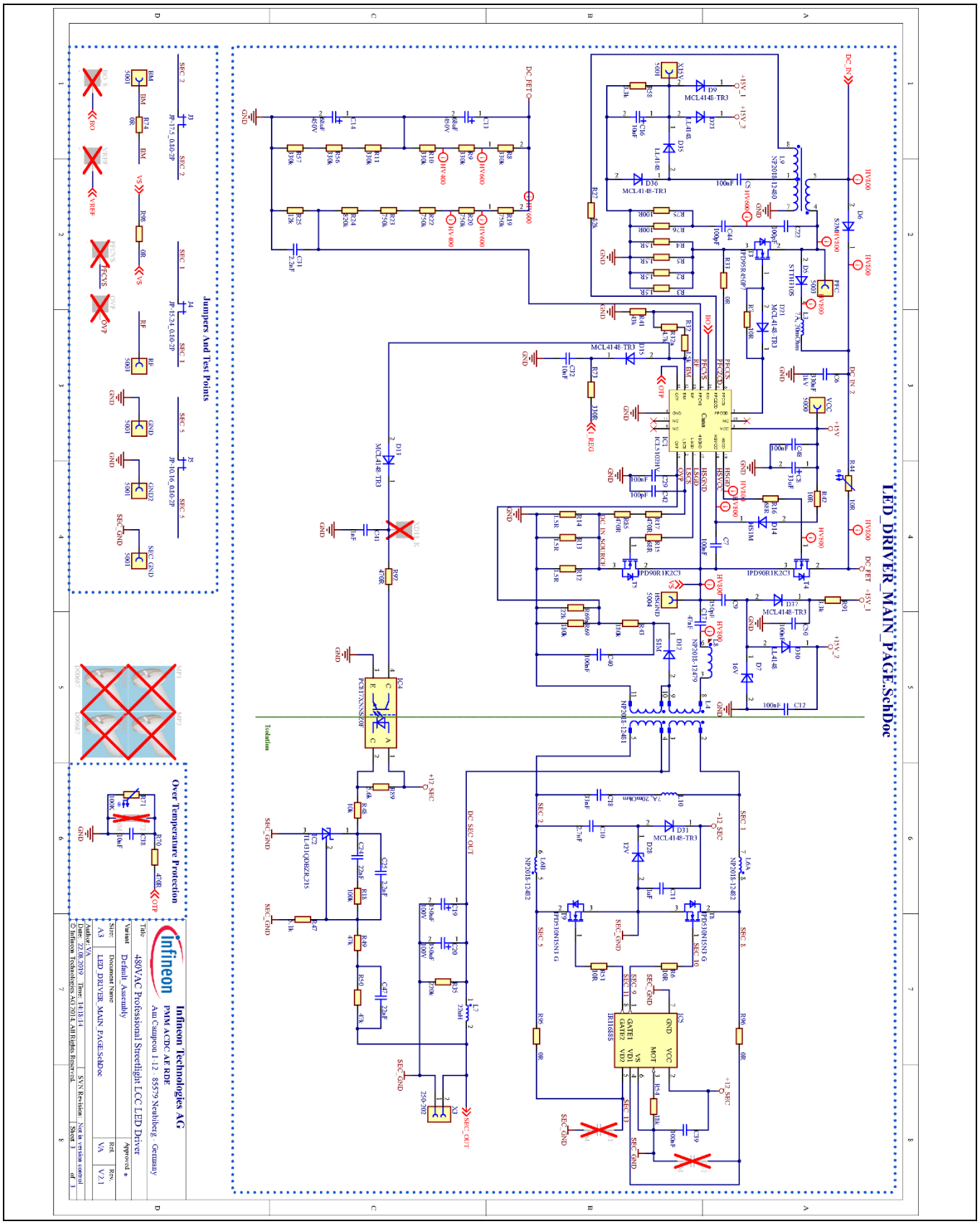

Figure 1 Board PFC and LCC stage schematic

2.1 Target MOSFET description

The MOSFET used in the original design is IPD90R1K2C3. This is a 900 V superjunction MOSFET, with an $R_{DS(on)}$ of 1200 mΩ. The chip is housed in a DPAK package. When updating the devices to 950 V CoolMOS™ PFD7, ideally an equal $R_{DS(on)}$ rated device would be chosen. However, as the current highest $R_{DS(on)}$ in the portfolio for the 950 V CoolMOS™ PFD7 family is 450 mΩ, the IPD95R450PFD7 was chosen. It is also a DPAK package, and it supports 950 V nominal blocking voltage. The robust and fast body diode of the CoolMOS™ PFD7 families enables the use of half-bridge topologies, due to their low reverse recovery charge (Q_{rr}) and therefore higher hard-commutation capability.

For further information on how to select a MOSFET for soft-switching topologies, please refer to the **Primary Side MOSFET Selection for LLC Topology** application note.

3 Considerations when updating to 950 V CoolMOS™ PFD7

Before making the change to 950 V CoolMOS™ PFD7, the differences between the MOSFET being used and the target MOSFET must be considered.

3.1 Gate driving

The main goal of this section is to derive the gate driving parameters so that the turn-on and turn-off dI/dt and dV/dt of the new design are similar to the old design, since the EMI requirements need to be met.

When updating to a newer MOSFET technology, there is usually a pitch shrink in the technology. This means that not only the static characteristics (such as $R_{DS(on)}$, $V_{(br)dss}$) change, but also the dynamic characteristics. This is mainly due to the parasitic capacitances of the MOSFET.

When coming from the older 900 V CoolMOS™ C3 technology to the 950 V CoolMOS™ PDF7, we can expect the capacitances to be smaller due to a pitch shrink of the superjunction structure. Therefore, the gate driving needs to be re-evaluated and possibly updated in order to enjoy the benefits of the new technology while maintaining the EMI performance of the previous design. Note that the C3 device is 1.2 Ω, comparatively higher than the 0.45 mΩ PFD7.

Table 2 Capacitance comparison between IPD90R1K2C3 and IPD95R450PFD7

Parameter	IPD90R1K2C3	IPD95R450PFD7	Unit	Comment on test condition
C_{iss}	710	1230	pF	V_{ds} differs, frequency differs
C_{oss}	35	17	pF	V_{ds} differs, frequency differs
$C_{o(er)}$	23	28	pF	V_{ds} differs
$C_{o(tr)}$	86	277	pF	V_{ds} differs

Table 2 gives an overview of the difference in capacitance for the two devices. However, it is difficult to make a precise comparison of the two devices due to different test conditions. The PFD7 device has somewhat larger parasitic capacitances; nevertheless, it exhibits advantages when normalized to $R_{DS(on)}$.

The typical capacitance graph found at the bottom of the datasheet gives a better picture of the capacitances.

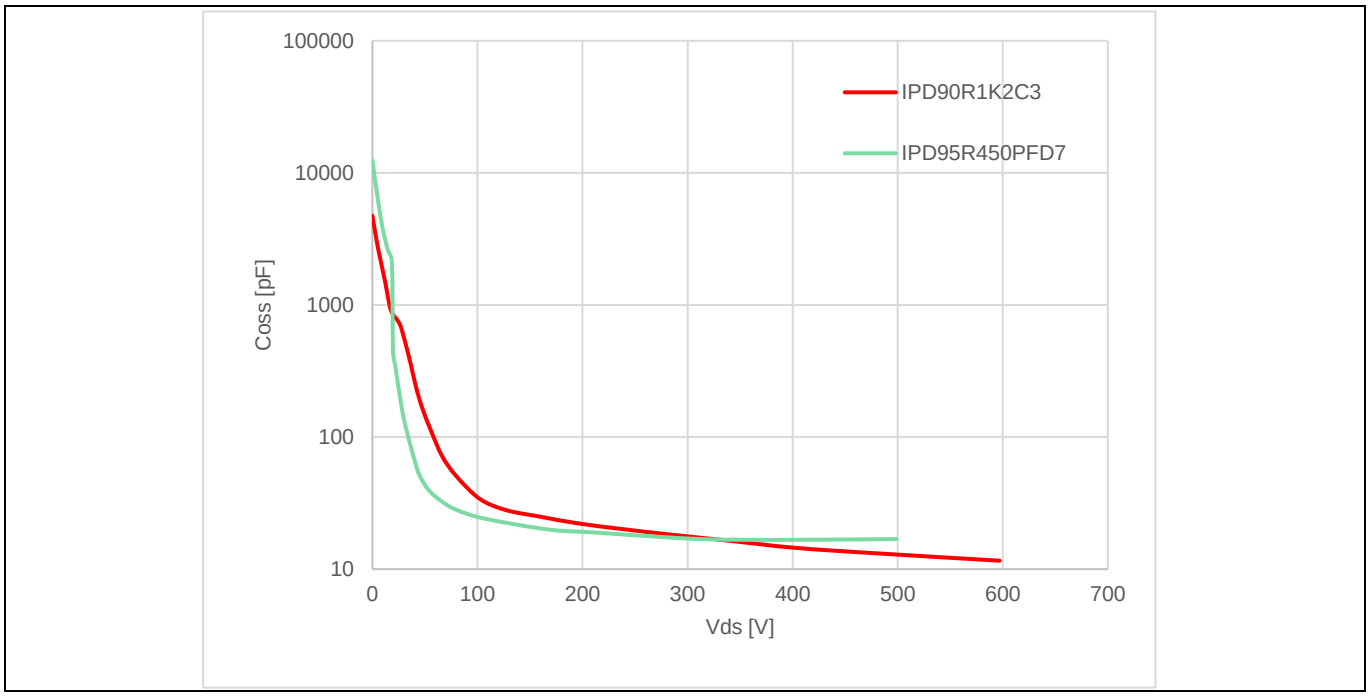

Figure 2 **C_{oss} of IPD90R1K2C3 and IPD95R450PFD7**

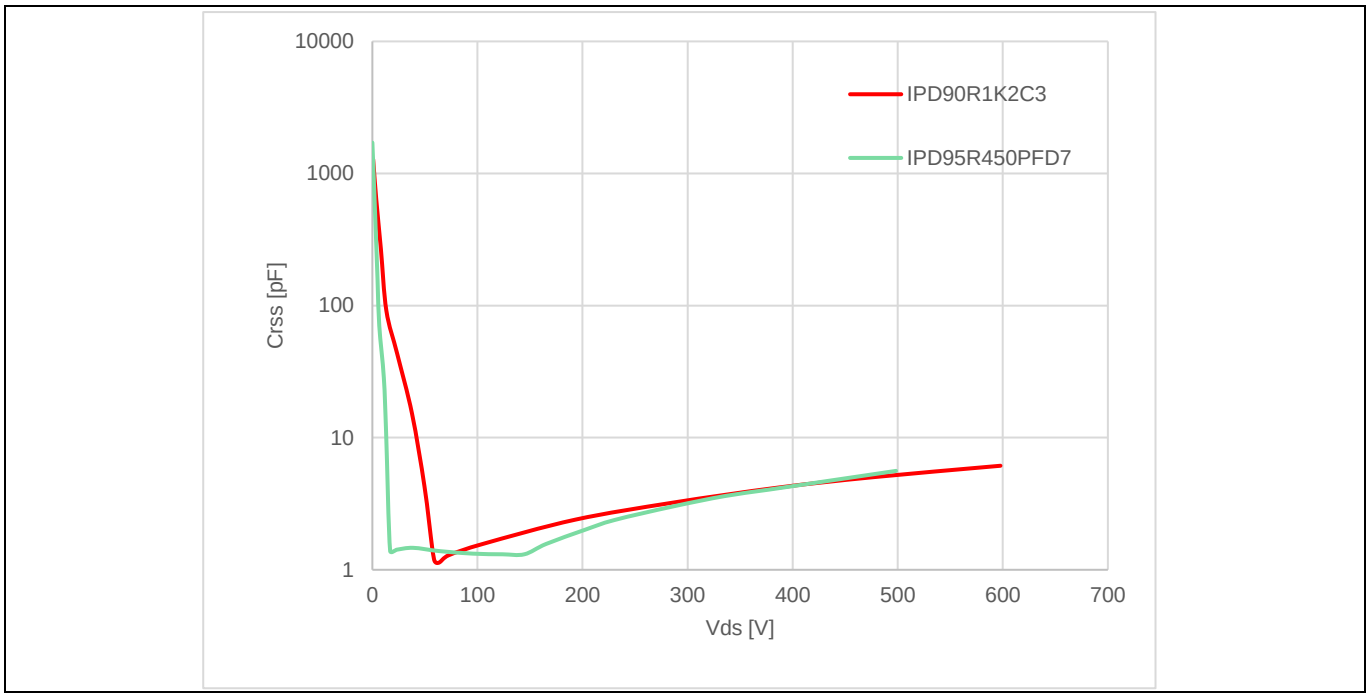

Figure 3 **C_{RSS} of IPD90R1K2C3 and IPD95R450PFD7**

For an LCC (or LLC) converter, the turn-on event does not significantly contribute to the EMI signature due to the soft-switching. The turn-off event needs to occur faster than a voltage is developed across the switch; this again avoids switching loss.

If the older 900 V CoolMOS™ C3's output capacitance (C_{oss}) was significantly higher than the 950 V CoolMOS™ PFD7, we would need to add an external drain-to-source capacitance (C_{ds}) to slow down the dV/dt of the

switching event. However, as the 900 V CoolMOS™ C3 is a high-ohmic part, the smaller relative die size compensates for the die shrink achieved in the seventh-generation CoolMOS™, resulting in very similar minimum C_{OSS} values.

Regarding the reverse capacitance (C_{RSS}), the same trend is observed. If the 900 V CoolMOS™ C3's C_{RSS} were significantly smaller than the 950 V CoolMOS™ PFD7, we would need to compensate for it by increasing the external R_g. For further information on how to update your design with the seventh-generation CoolMOS™, please refer to the **Optimizing CoolMOS™ based power supplies to meet EMI requirements** application note.

Therefore, the same R_g is used for the updated board with the PDF7, and no external C_{ds} is added.

3.2 Soft-switching

The LLC (as well as other soft-switching topologies) achieves zero voltage switching (ZVS) by discharging the output capacitance of the switch while in the off-state, so that the body diode starts conducting. It is at this point where the gate voltage is applied and the MOSFET turns on at close to 0 V.

The charge needed depends on the switch being used. The output capacitance of the switch needs to be discharged to push the voltage down to zero. If there is some charge remaining when the MOSFET is turned on, switching losses occur.

Therefore, when changing the MOSFET of a soft-switching topology, the new design must make sure that there is enough energy stored in the resonant tank to push the voltage across the MOSFET down to 0 V. Note that in a totem-pole switching node, the capacitances of both top and bottom MOSFETs are being recharged.

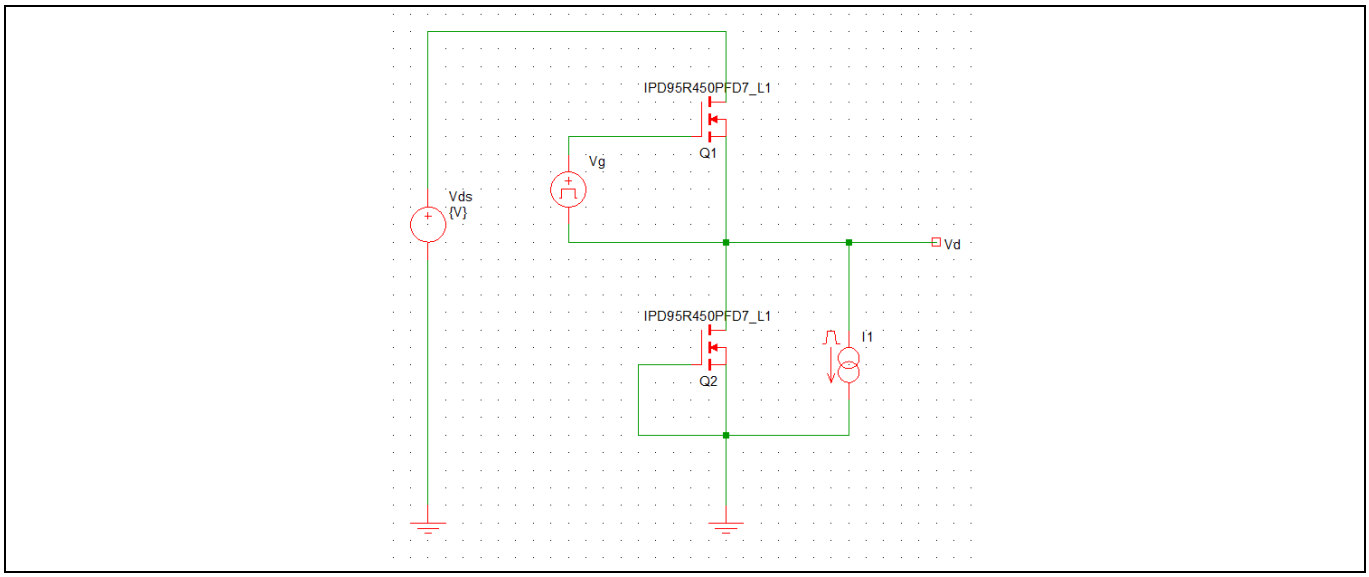

Figure 4 Q_{oss} measurement simulation schematic

For a more in-depth analysis, a SPICE simulation can be carried out. This is a double pulse test, where when the upper device turns off, the current of the current source starts charging the lower device. By integrating the current we can obtain the charge needed until the diode is forward biased.

Table 3 IPD90R1K2C3 and IPD95R450PFD7 simulated Q_{oss}

	IPD90R1K2C3	IPD95R450PFD7	Comment
Q_{oss} [nC]	53	112	From 800 V_{ds} to 0 V_{ds}

From these results, we can see that the PFD7 device stores around double the charge of the C3. This is due to the non-linearity of the output capacitance, and being a lower-ohmic part and therefore having a relatively bigger chip size.

This means that the dead time of the LCC needs to be adjusted to ensure that soft-switching is achieved. The controller in REF-ICL5102HV-U150W is an ICL5102HV, and due to its adaptive dead time, the controller automatically adjusts the required dead time by sensing the 0 V crossing of V_{ds}. The next step is to check whether the inductance of the resonant tank can provide sufficient energy within the 750 ns maximum adaptive dead time window.

For the LCC topology, the worst-case scenario of least circulating current would be at no load with the lowest V_{out}, which would require the highest frequency (135 kHz for this board). In that case, no or very little current flows through the load, which makes the circuit look like a fully reactive load from the input.

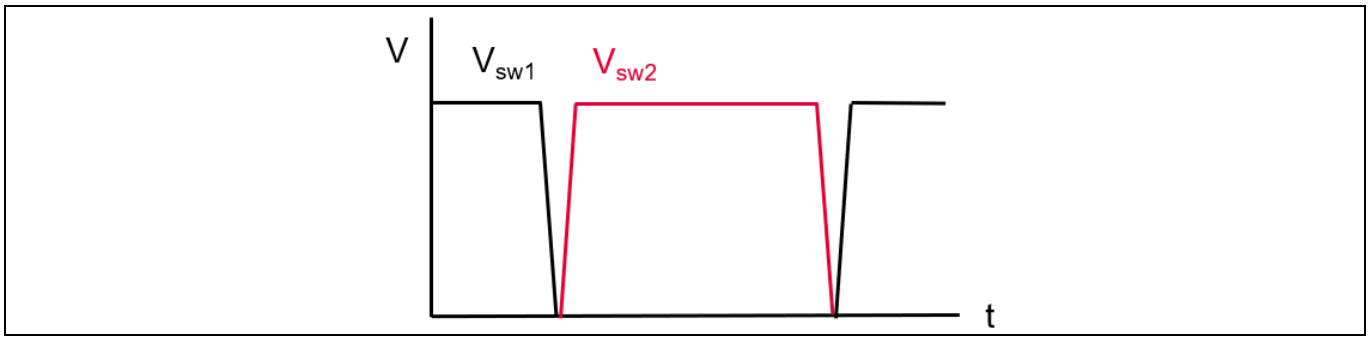

Figure 5 Simplified drain-to-source voltage waveforms in LCC

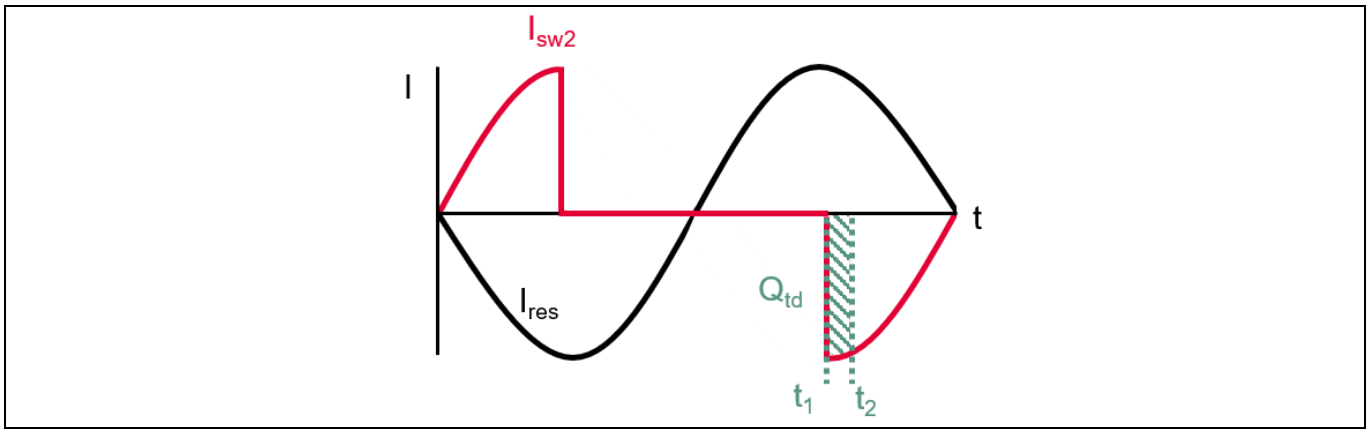

Figure 6 Simplified resonant and drain current waveforms in LCC

Figure 6 shows the timing of the dead time, where the resonant tank's charge (Q_{td}) is available. The charge (which is an integration of the current between t_1 and t_2) needs to be at least as big as the Q_{oss} of the MOSFET to be switched. In order to evaluate if the current is enough in the REF-ICL5102HV-U150W, a test was performed at the highest frequency, which is at the output voltage (V_{out}) = 17 V, output current (I_{out}) = 0 A condition.

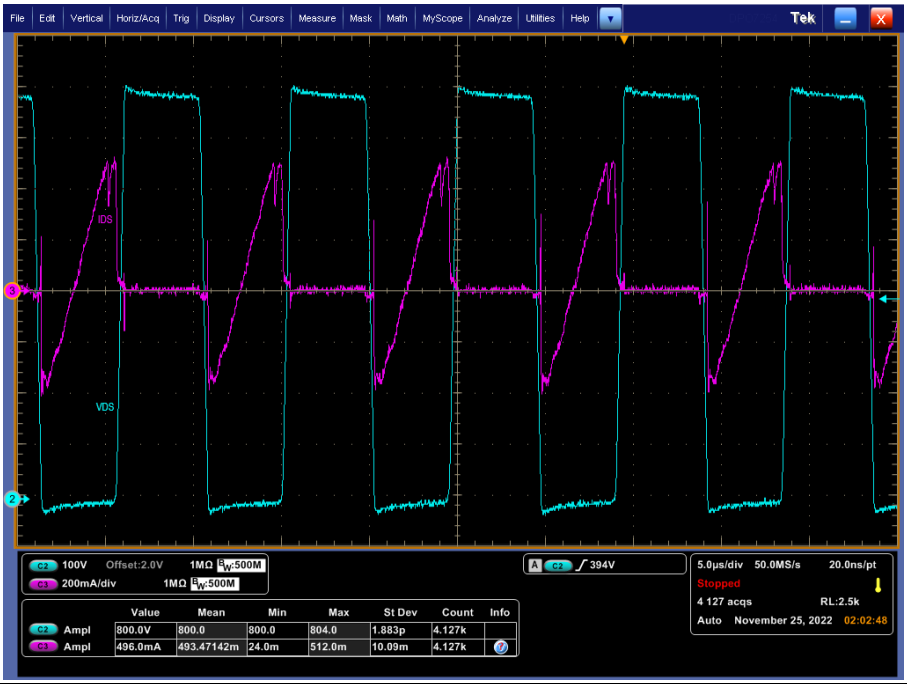

Figure 7 **V_{out} = 17 V, I_{out} = 0 A LCC drain-to-source voltage (V_{ds}) and drain current (I_d) measured on shunt**

As depicted in **Figure 6**, the available charge in the dead time period can be calculated from **Figure 7**. The peak current flowing through the lower-side MOSFET is shown to be 380 mA. The total charge available in the resonant tank within the maximum adaptive dead time of the controller can be approximated with $Q_{dt} = I_{peak} * T_{dt}$.

The resulting charge is 285 nC, which is higher than the 112 nC needed for the IPD95R450PFD7. This means that no change is needed in the design to achieve soft-switching with the new device. If the stored charge were not enough, the resonant tank components would need to be adjusted, in which case the easiest method to increase the circulating current is to increase the parallel capacitance.

4 Experimental comparison of IPD90R1K2C3 design vs. IPD95R450PFD7

In this chapter, the waveforms, efficiency, thermals and EMI performance of the two devices are shown. Both use the same design, REF-ICL5102HV-U150W, which is a PFC + LCC 150 W evaluation board. The comparison focuses only on the LCC stage, as explained in the Introduction.

4.1 LCC waveforms

The waveforms below show the drain-to-source voltage of the lower-side MOSFET and its current, measured on the shunt resistor. Both the highest and the lowest power points (10 V and 0 V dimming input, respectively) are recorded for the 48 V output voltage case as well as for the 17 V output voltage case. The input voltage to the power factor correction (PFC) stage is 300 V AC at 50 Hz. **Table 4** summarizes all the output power of the working points shown from **Figure 8** to **Figure 11**.

Table 4 Summary of waveform details for IPD90R1K2C3

	V_{out} = 48 V		V_{out} = 17 V	
	Min.	**Max.**	**Min.**	**Max.**
Power [W]	0	144	0	52
Reference figure	**Figure 8**		**Figure 9**	

Table 5 Summary of waveform details for IPD95R450PFD7

	V_{out} = 48 V		V_{out} = 17 V	
	Min.	**Max.**	**Min.**	**Max.**
Power [W]	0	144	0	52
Reference figure	**Figure 10**		**Figure 11**	

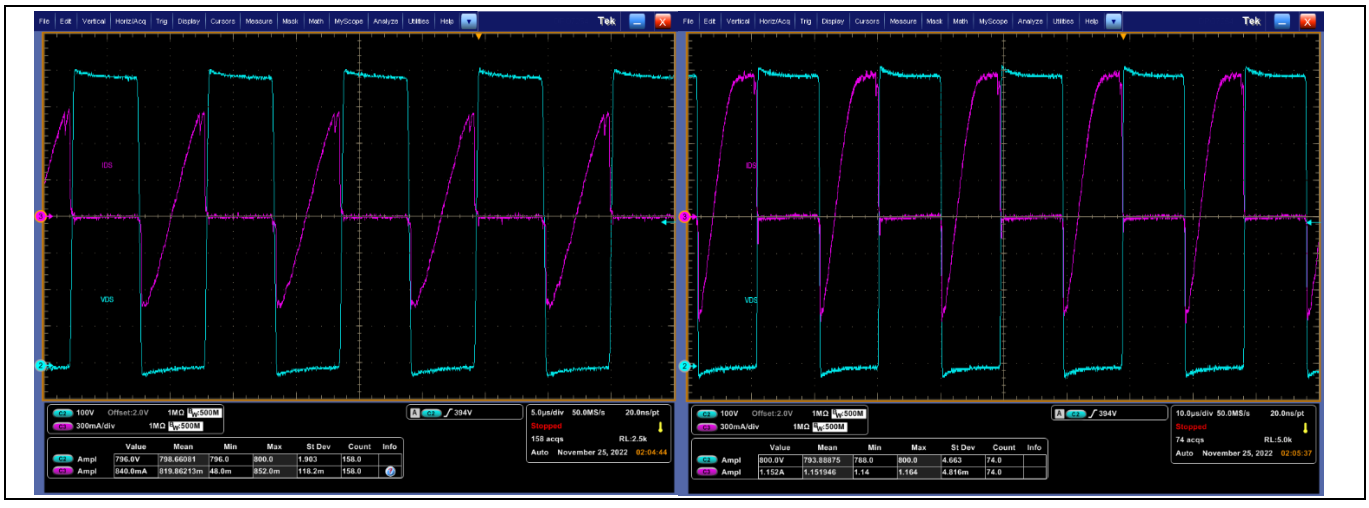

Figure 8 IPD90R1K2C3 drain-to-source voltage and drain current waveforms at V_{out} = 48 V P_{out} = 0 W on the left, P_{out} = 144 W on the right

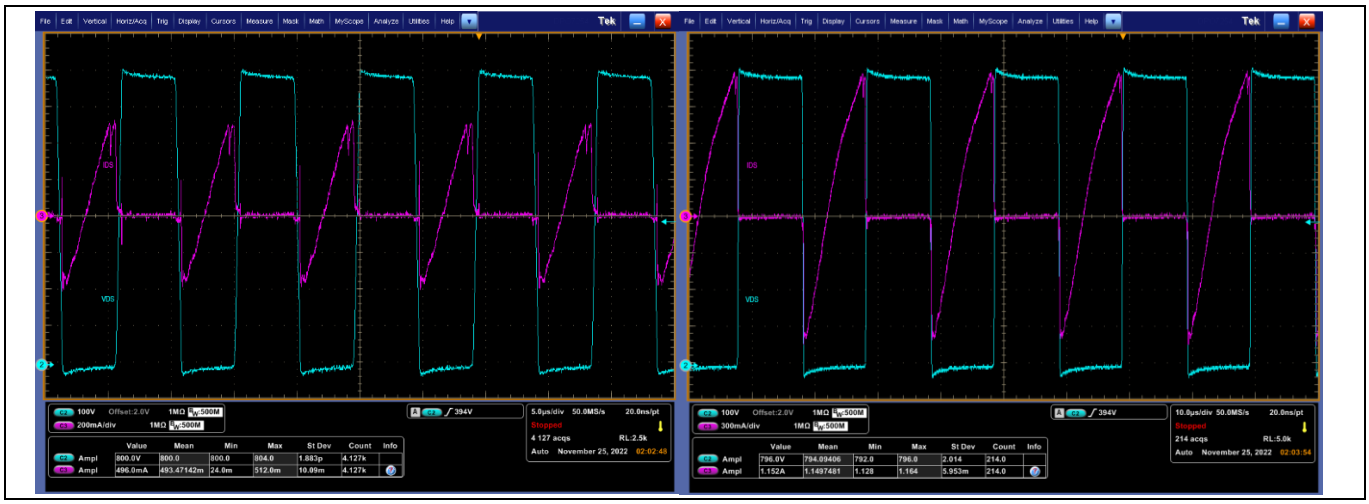

Figure 9 IPD90R1K2C3 drain-to-source voltage and drain current waveforms at V_{out} = 17 V P_{out} = 0 W on the left, P_{out} = 52 W on the right

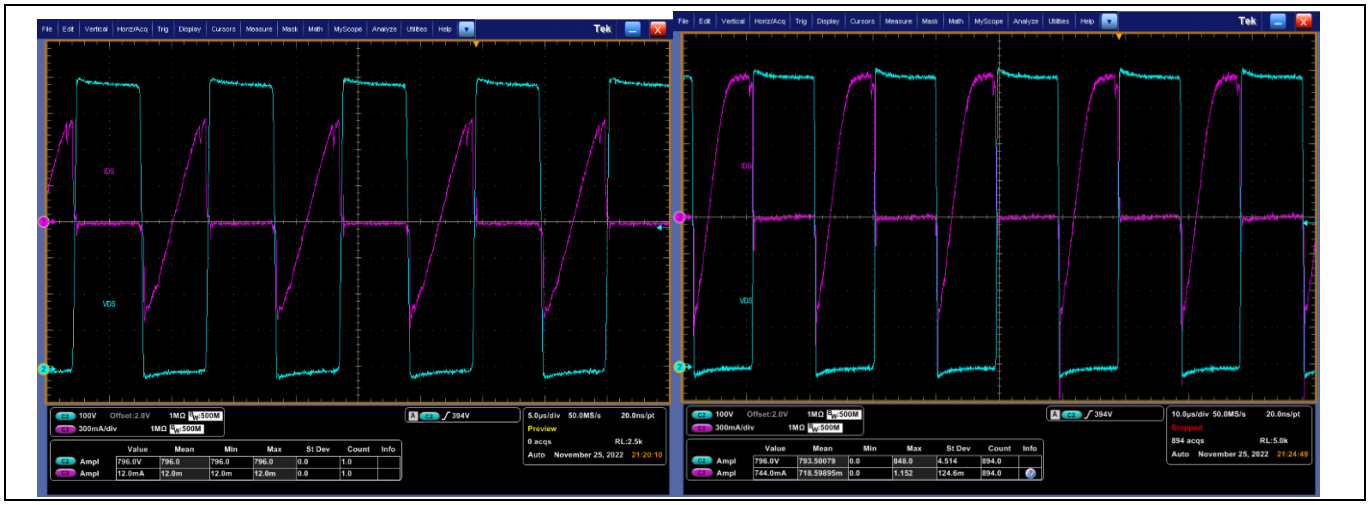

Figure 10 IPD95R450PFD7 drain-to-source voltage and drain current waveforms at V_{out} = 48 V P_{out} = 0 W on the left, P_{out} = 144 W on the right

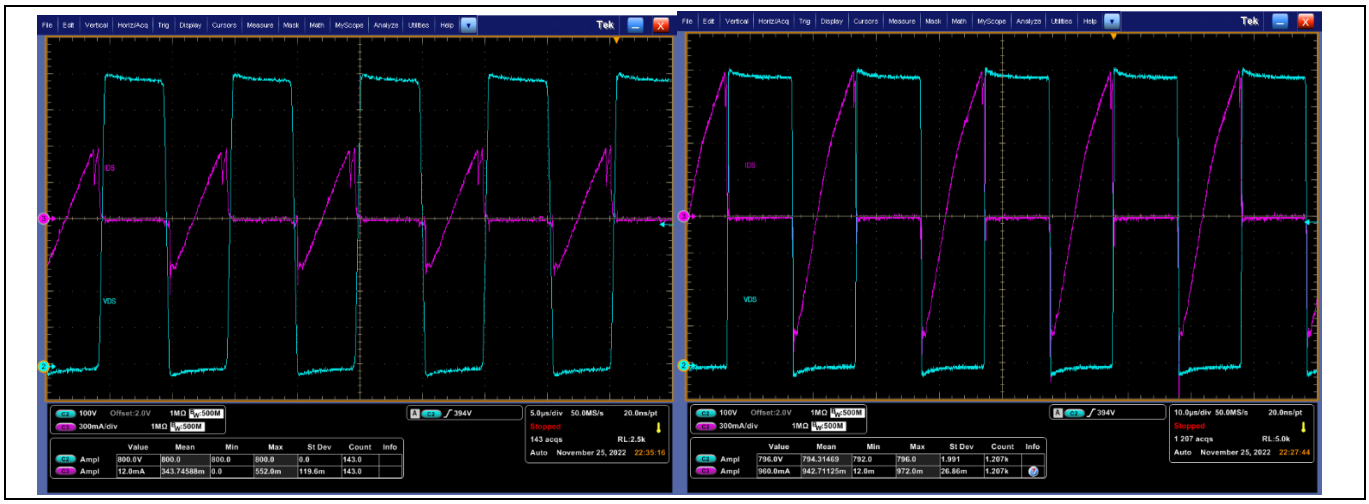

Figure 11 IPD95R450PFD7 drain-to-source voltage and drain current waveforms at V_{out} = 17 V P_{out} = 0 W on the left, P_{out} = 52W on the right

Both current and voltage waveforms match very closely. The resonant current becomes more sinusoidal the closer the converter gets to full power.

The only noteworthy point is the dip in the positive peak of the current waveform. This is caused by the turn-off of the device. The input capacitance is discharged from the nominal voltage to the threshold voltage, which causes a current to flow through the input capacitance, which is reflected in the shunt measurement. As shown in **Table 2**, the input capacitance of IPD95R1K2PFD7 is about 1.7 times bigger than that of the IPD90R1K2C3. Therefore, the current dip of the PFD7 device is proportionally more pronounced than in the C3 device's case.

4.2 LCC efficiency

The efficiency of both design versions was evaluated in a setup to ensure an objective and unbiased analysis. The test setup is an automated bench, which applies 300 V AC at the input and 48 V at the output, and it varies the dimming input of the board to adjust the output power. The same settings and working points were applied to both the IDP90R1K2C3 version and the IPD95R450PFD7 version.

The system efficiency, both PFC and LCC together, is represented for the full load of the board. At the maximum LED current, the system efficiency is 91.07 for the C3 device, while it is 91.57 for the PFD7 device. That is an efficiency gain of 0.5 percent by updating the MOSFET to the 950 V CoolMOS™ PFD7 product.

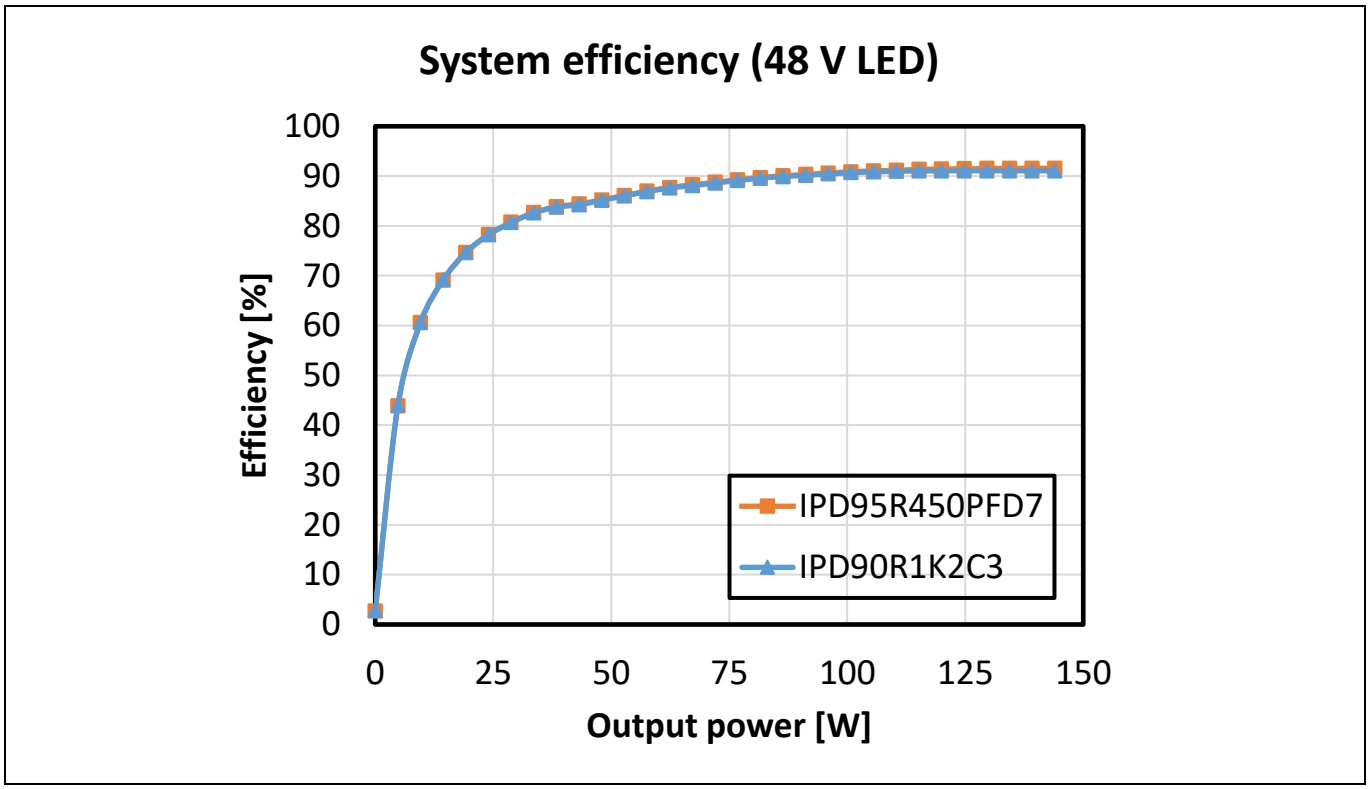

Figure 12 **Comparison of system efficiency of REF-ICL5102HV-U150W with IPD95R450PFD7 (orange), IPD90R1K2C3 (blue)**

There is an efficiency gain across the board from 16 percent load to 100 percent load, with an average efficiency gain of 0.16 percent. Note that this is the efficiency of not only the LCC converter, but the efficiency of the rectifier, PFC and LCC stages combined.

4.3 Thermal evaluation

The temperature profile of the board with both devices is given below. The measurements were carried out at 300 V AC/50 Hz input with 48 V LED at full load (3 A), at ambient temperature. In order to avoid possible temperature offsets produced by the thermal camera, an object with high thermal mass is used as reference to measure the room temperature of each test. The difference between the room temperature and the maximum MOSFET temperature is reported in **Table 6**.

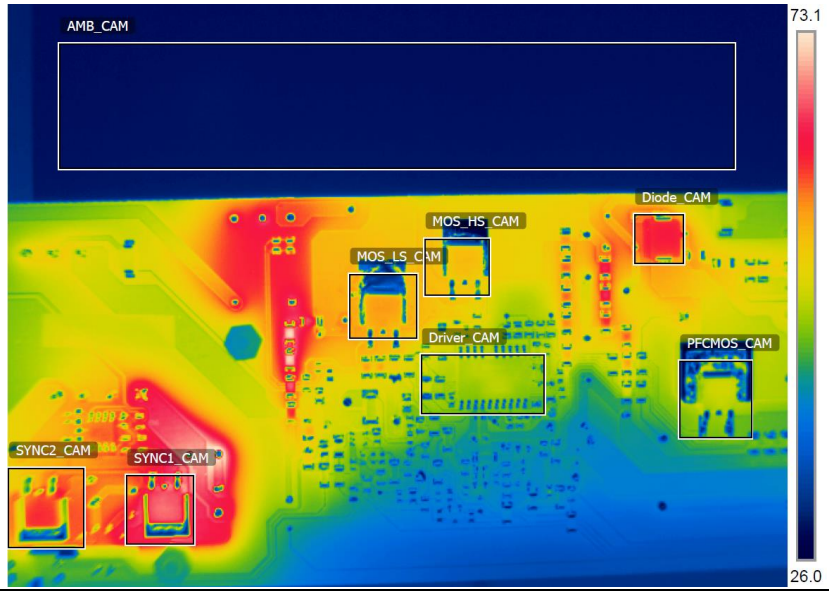

Figure 13 Board backside thermal image at 48 V 3 A output with IPD90R1K2C3

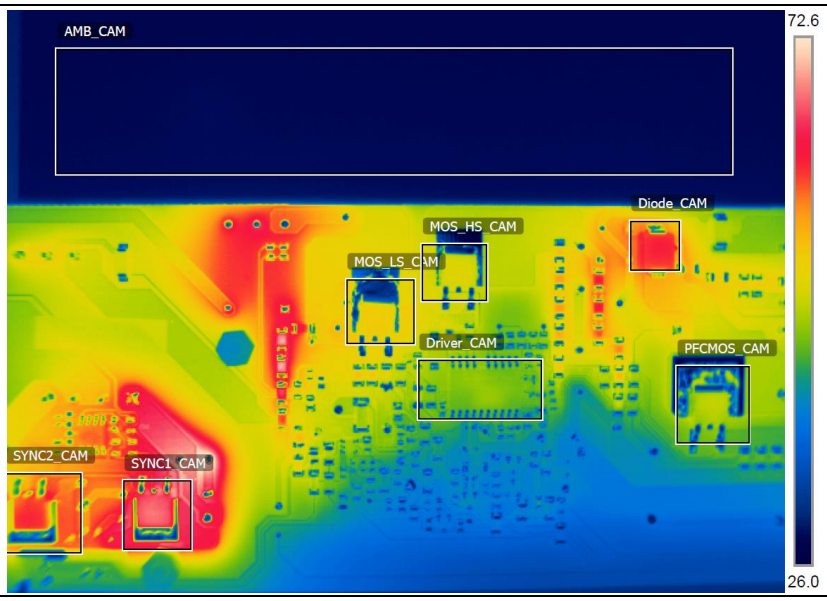

Figure 14 Board backside thermal image at 48 V 3 A output with IPD95R450PFD7

Table 6 Key figures from temperature test at 48 V and 3 A output

Product	Ambient	MOSFET maximum	Delta	Units
IPD90R1K2C3	29.3	59.9	30.6	°C
IPD95R450PFD7	28.5	56.0	27.5	

There is a difference of 3.1°C in favor of IPD95R450PFD7 due to the lower power loss reported in the efficiency comparison.

4.4 EMI performance

Finally, the conducted electromagnetic emissions are measured by a line impedance stabilization network (LISN) setup, and the results are compared to the EN 55015 standard, which applies to lighting loads. The blue trace is the quasi-peak measurement, while the orange is the average.

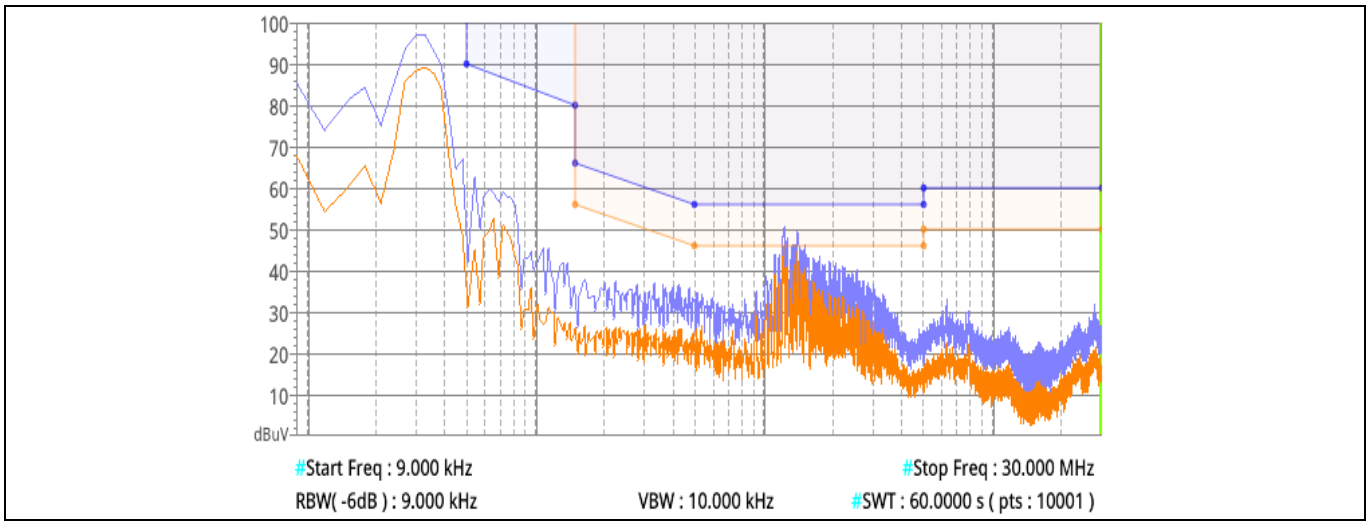

Figure 15 IPD90R1K2C3 EMI test result with EN 55015 limits

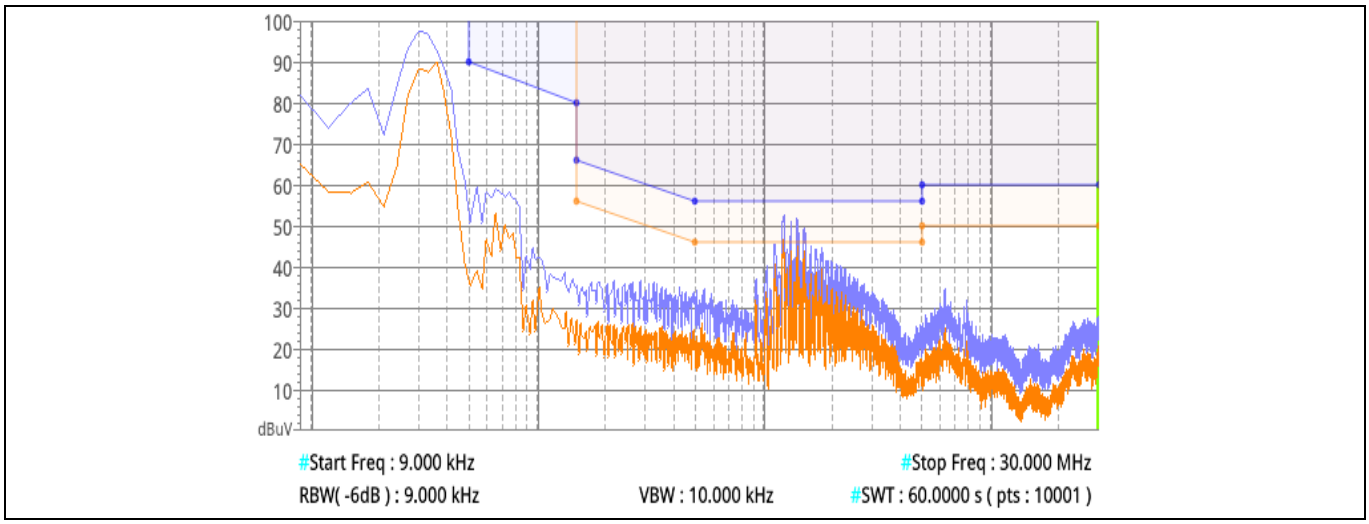

Figure 16 IPD95R450PFD7 EMI test result with EN 55015 limits

An increase of 2 dB is seen with the 950 V PFD7, which could be addressed with gate driving optimization.

5 Conclusion

This document explained the methodology behind replacing the 900 V CoolMOS™ C3 devices with the 950 V CoolMOS™ PFD7, and reported on the efficiency, thermals and EMI differences between the two. It was it shown that the 950 V CoolMOS™ PFD7 can be used in place of the older device with no loss in performance.

Revision history

Document revision	Date	Description of changes
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