# TLD6098-2DPVB2G_EVAL board

## User guide

**LITIX™ Power**
**Multitopology DC-DC controller**

## About this document

The TLD6098-2ES device used in this evaluation board, is an AEC qualified dual channel DC-DC controller, especially designed to be used as voltage regulator such as power supply or current regulator such as an LED driver. Its main features are:

- Wide input voltage up to 58 V and output voltage range up to 70 V
- EMC optimized device
- Overvoltage, short to ground, overcurrent, open feedback and overtemperature diagnostic output
- Configurable control as constant voltage or constant current

### Scope and purpose

The scope of this user guide is to provide instructions on the use of TLD6098-2ES Power dual phase boost-to-ground TLD6098-2DPVB2G_EVAL board.

### Intended audience

This document is intended for engineers who perform measurements and check performances with TLD6098-2EP Power dual phase boost to ground TLD6098-2DPVB2G_EVAL board.

### Evaluation Board

This TLD6098-2DPVB2G_EVAL board is to be used during the design-in process for evaluating and measuring multiphase topology with TLD6098-2ES.

*Note: PCB and auxiliary circuits are NOT optimized for final customer design.*

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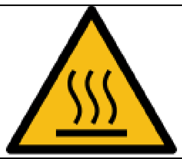
## Safety precautions

*Note:* *Please note the following warnings regarding the hazards associated with development systems.*

**Table 1 Safety precautions**

| | |
|---|---|
|  | **Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.* |
|  | **Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.* |
|  | **Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.* |
|  | **Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.* |
|  | **Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.* |
|  | **Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.* |
|  | **Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.* |

# Table of contents

# 1 The board at a glance

The TLD6098-2DPVB2G_EVAL dual phase boost-to-ground evaluation board is a switching power supply that, under nominal conditions, can deliver a constant voltage at the output between 43 V and 52 V and a current up to 7 A.

This power-supply can be set in constant voltage and in constant current: the output will maintain the desired voltage until the current sourced is higher than the threshold set. At this point it starts to regulate by keeping the current constant.

If compared to a similar power supply with only one channel; thanks to the phase shift applied between the switching signal of channels, ripple on input and output is reduced and so the frequency can be lowered, decreasing the commutation losses and thereby efficiency is maximized.

The power-supply is equipped with an output overvoltage protection.

Both channels are constantly monitored by the built-in diagnosis features of the TLD6098-2ES. Two LEDs are provided to signal any possible fault.

***Attention:*** ***This board requires protection against short circuits on input. A 50 A automotive fast blade fuse can provide protection or by setting the maximum current of the external power supply which is used to power the board to 50 A.***

***Attention:*** ***Please be aware that it is up to the user to provide protection and that the 50 A fast blade fuse is not included in this kit or on the board***

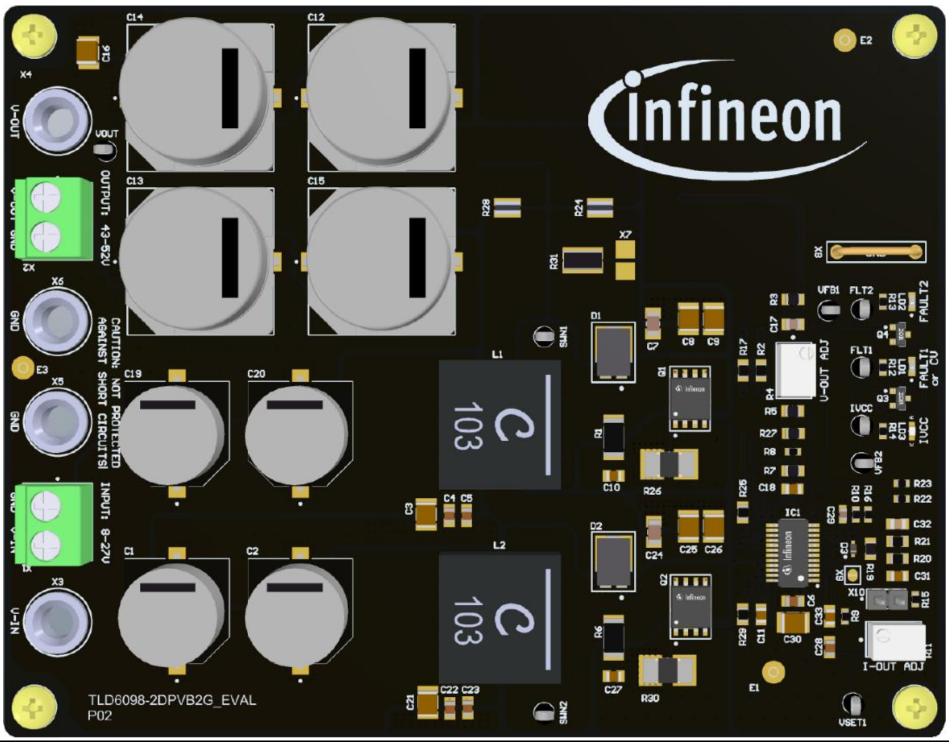



**Figure 1 TLD6098-2DPVB2G_EVAL board**

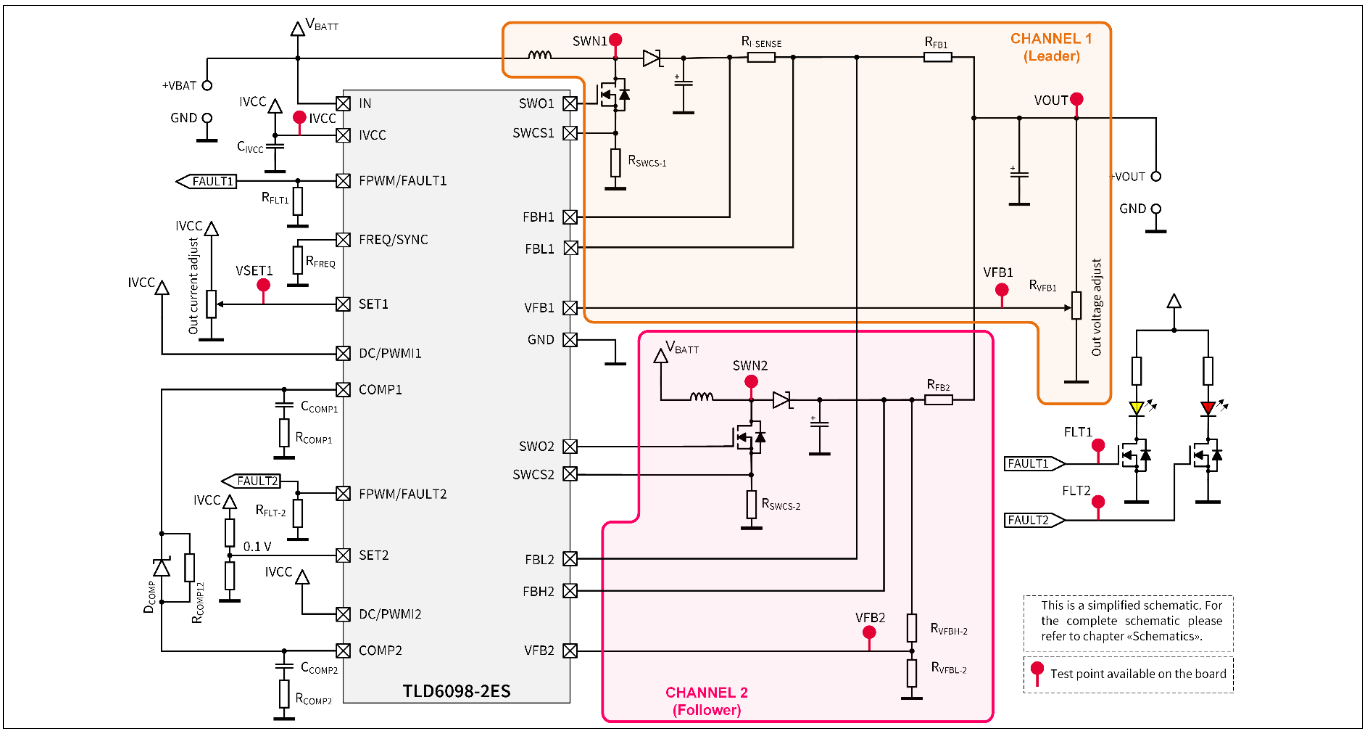



Figure 2 Simplified schematic

## 1.1 Main features

- Ripple on input and output is reduced
- Phase shift applied between the switching signal of channels
- Frequency can be lowered which decreases the commutation losses

## 1.2 Board parameters and technical data

Table 2 Performance summary

| Parameter | Conditions | Value |
|---|---|---|
| Input supply voltage | – | 8 to 27 V |
| Output voltage range | – | 43 to 52 V |
| Continuous output current | Voltage on pin VSET1 ≥ 2.2 V<br>$V_{BATT}$ ≥ 14 V<br>Output current derating for $V_{BATT}$ < 14 V (see Chapter 2.5)<br>$T_A$ ≤ 25°C | 7 A |
| Peak output current | Less than 2 s | 10 A (limited by $R_{I\text{-}SENSE}$) |
| Switching frequency | Set by $R_{FREQ}$ = 4.53 kΩ | 200 kHz |
| Efficiency | $V_{BATT}$ = 14 V, $V_{OUT}$ = 48 V, $I_{OUT}$ = 7 A | > 94% |
| Output overvoltage protection | Set by $R_{VFBH\text{-}2}$ = 68 kΩ and $R_{VFBL\text{-}2}$ = 1.8 kΩ | 62 V |
| Maximum ambient temperature | – | 35°C |

# 2 System and functional description

The power supply is composed of two DC-DC channels that work in parallel. Channel 1 leads the output voltage, channel 2 follows channel 1. Channel 1 works as a constant voltage source, whereas channel 2 works as a current source. The behavior of each channel depends on the resistor values used to tie to ground the pins FPWM/FAULT1 and FPWM/FAULT2 (resistors $R_{FLT1}$ and $R_{FLT2}$ on simplified schematics and refers to TLD6098-2ES datasheet [2] for more information).

Channel 1 senses the output voltage with pin VFB1 through the potentiometer $R_{VFB1}$ and regulates the duty-cycle of its power MOSFET to keep on VFB1 the voltage loop reference $V_{VFB1\_REF}$ at 1.6 V. The voltage loop on channel 1 is enabled when the voltage on VFB1 is higher than 1.5 V and disabled when it is lower than 1.35 V. The sourced current is measured through the sensing pins FBH1 and FBL1 across the shunt resistor $R_{I\text{-}SENSE}$. When the drop voltage on $R_{I\text{-}SENSE}$ goes above the current loop reference $V_{REF1}$ (typically 150 mV when the voltage on pin VSET1 is higher than 2.2 V), a current loop takes over the DC-DC control and limits the output current in order to keep the drop voltage on the shunt constant. $V_{REF1}$ is not fixed but it can be adjusted by varying the voltage on pin SET1: thus, it is possible to set the desired maximum output current by means of a trimmer connected to this pin (see Chapter Output current regulation).

Channel 2 is identical to channel 1 but it works as a constant current source. The signal used to drive MOSFET is 180° out of phase with respect to channel 1. This minimizes the current ripple at the input and output.

The most important requirement that channel 2 must fulfil, is to supply the same voltage and current of channel 1, in order to get an almost ideal parallel of both converters. This goal is achieved by connecting the FBL2 pin to the channel 1 output, FBH2 to the channel 2 output and by reducing the voltage on pin SET2 to 0.1 V with a voltage divider. This operation drives the channel 2 current loop reference $V_{REF2}$ to zero and thus forces channel 2 to increase or decrease its output voltage until the voltage difference between pins FBH2 and FBL2 is zero. Since $R_{FB1}$ is equal to $R_{FB2}$, this equilibrium condition is reached only when the channel 2 voltage (and thus the current) is identical to channel 1.

Looking at the compensation networks, it is clearly visible that they are different. In particular, the capacity is higher on the channel 2 compensation network, so it means that the channel 2 response is a little bit slower than channel 1. This is due to the different loop of the two channels and thus to a different transfer function that characterizes both converters. Indeed, as already mentioned, if the output current is lower than the maximum value allowed, channel 1 works as a constant voltage source, whereas channel 2 works as a current source.

Furthermore, since channel 2 follows the channel 1, when a load is connected to the output channel 1 is ready to supply the sudden demand of current in less time than channel 2. On pins COMP1 and COMP2 there is a similar delay. It is possible to mitigate this effect by placing a resistor $R_{COMP12}$ between pins COMP1 and COMP2. Indeed, after the current demand, the output voltage tends to decrease. Both channels respond by increasing the respective COMP voltages, however channel 2 is a little bit slower due to the higher value of compensation capacitance. A helping action in speeding up the voltage rising of COMP2 is given by the COMP1 pin and the resistor $R_{COMP12}$, that shows a steeper response to the output load increase. $R_{COMP12}$ may cause a slight output voltage increase when loading the output.

Diode $D_{COMP}$ acts as a clamping device to avoid excessive unbalance between channels. If channel 2 duty cycle (and therefore the energy transferred by the corresponding power stage) were to get significantly higher than channel 1, voltage loop of channel 1 will turn the channel off. In this case, the IC could find itself stuck in an operating point where all the current is delivered by channel 2. If the diode $D_{COMP}$ is present, then as soon as the channel 1 tends to turn off, COMP1 decreases and forces COMP2 also to decrease and consequently decreases the activity of channel 2.

## 2.1 Input connection

The board is equipped with a double type connector both in the input and in the output: screw terminal blocks and 4 mm female bananas.

***Attention:*** ***The screw terminal blocks have a limited current capability of up to 20 A. If the input current is higher than 20 A or it is unknown, connect the input power supply by using female bananas connectors. To have a rough estimation of the input current, use the following relation:***

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{0{,}9 \cdot V_{IN}} \; [A]$$

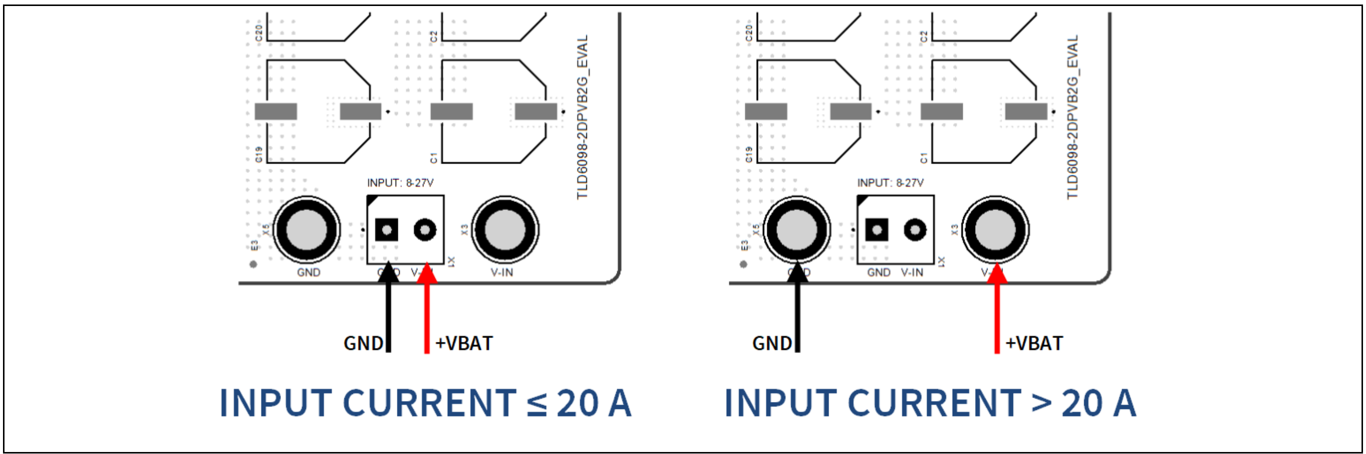



**Figure 3 Input connector selection**

Once the input power has been connected, if no fault is present on the circuit, the IVCC blue LED, LD3 will turn on and if the constant voltage mode is active, the FAULT1/CV yellow LED LD1 will also turn on.

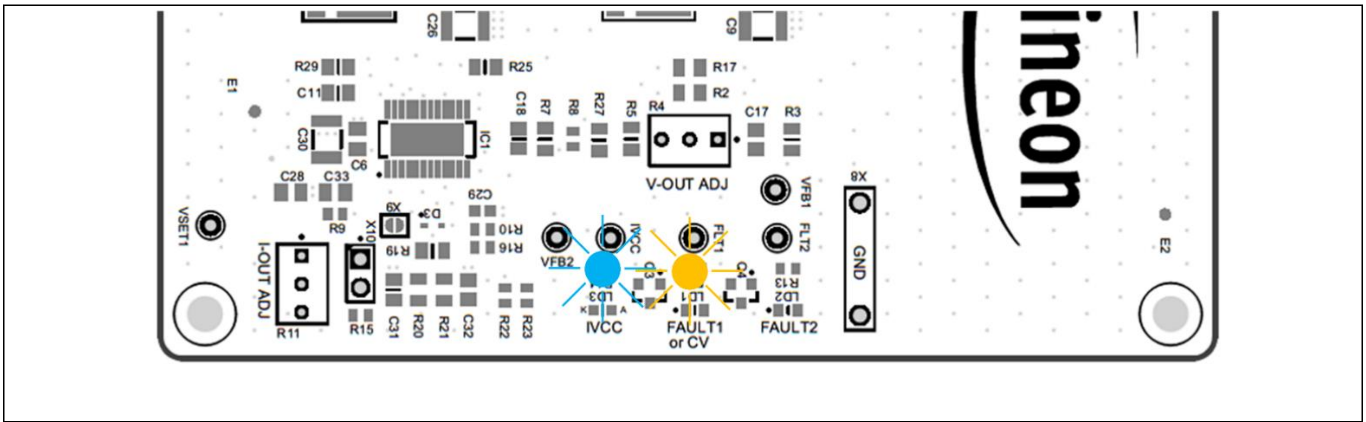



**Figure 4 Constant voltage mode active**

## 2.2 Output current regulation

This power supply behaves as a constant voltage supply if the output current is lower than a certain threshold and it becomes a constant current source when this threshold has been overcome. It is possible to regulate this threshold to set a maximum output current that satisfies the output needs.

As already mentioned in Chapter 2.1, above, when the output current of channel 1 causes a drop voltage on the shunt resistor $R_{I\text{-}SENSE}$, higher than a certain threshold called $V_{REF1}$, a current loop takes over the DC-DC control and limits the output current in order to keep the drop voltage on the shunt to $V_{REF1}$, constant.

$V_{REF1}$ is not fixed but it can be adjusted by setting the voltage on pin VSET1. Thus, the maximum output current $I_{OUT\text{-}MAX}$ can be set, by adjusting the voltage on pin VSET1 as described by the following relation:

$$I_{OUT-MAX} = 2 \cdot \frac{V_{REF1}(V_{VSET1})}{R_{I-SENSE}} = \frac{2}{R_{I-SENSE}} \cdot \frac{V_{VSET1} - 0.1}{14} \; [A]$$

Where $V_{VSET1}$ is the voltage on pin VSET1 [V], and $R_{I\text{-}SENSE}$ is the shunt resistor [Ω] of channel 1. In this schematic $V_{VSET1}$ can assume all the voltage values between 0.1 V and 2.4 V by means of trimmer $R_{VFB1}$.

Assuming a $R_{I\text{-}SENSE}$ of 30 mΩ as in this evaluation board (R31 in the schematics), $I_{OUT\text{-}MAX}$ can be set to the following values, depending on $V_{VSET1}$:

**Table 3 $I_{OUT\text{-}MAX}$ regulation**

| $V_{VSET1}$ [V] | $I_{OUT\text{-}MAX}$ [A] | Notes |
|---|---|---|
| 0 to 0.1 | 0 | – |
| 0.1 to 2.2 | 4.76 · ($V_{VSET1}$ – 0.1) | $R_{I\text{-}SENSE}$ = 30 mΩ |
| > 2.2 | 10 | $R_{I\text{-}SENSE}$ = 30 mΩ<br>Peak output current (less than 2 s) |

To adjust $V_{VSET1}$ and thus $I_{OUT\text{-}MAX}$, regulate trimmer R11, highlighted in Figure 5 by measuring the voltage on test point VSET1 and applying the above formula. By removing jumper X10, it is possible to rapidly set the maximum output current allowable (10 A peak), as can be seen in the figure.

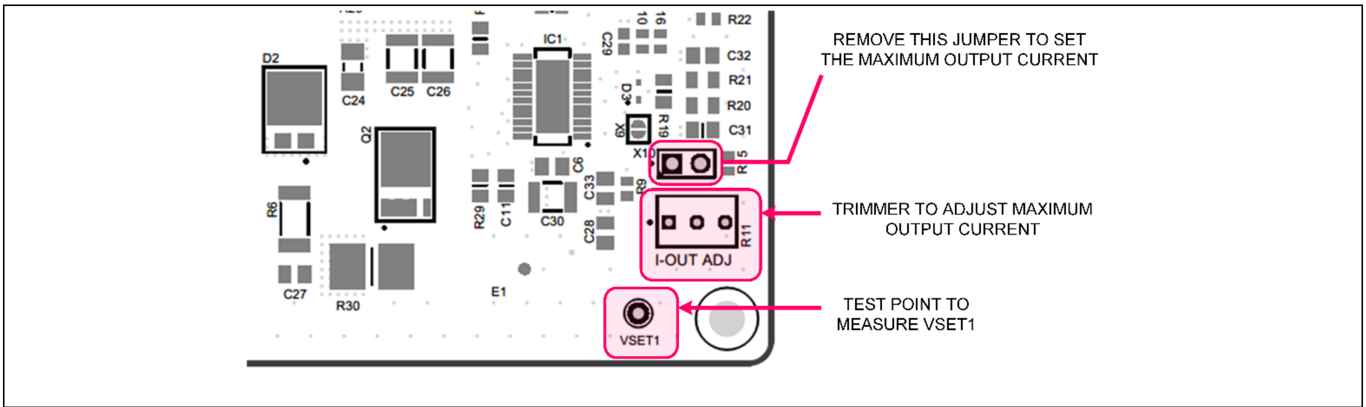



**Figure 5 Output current regulation**

Maximum current sourced from the output must be weighted on the input voltage, as described in this chapter.

A small capacitor on VSET1 can be used to slowly increase the output current during turn-on transient.

## 2.3 Output voltage regulation

Output voltage can be set between 43 V and 52 V.

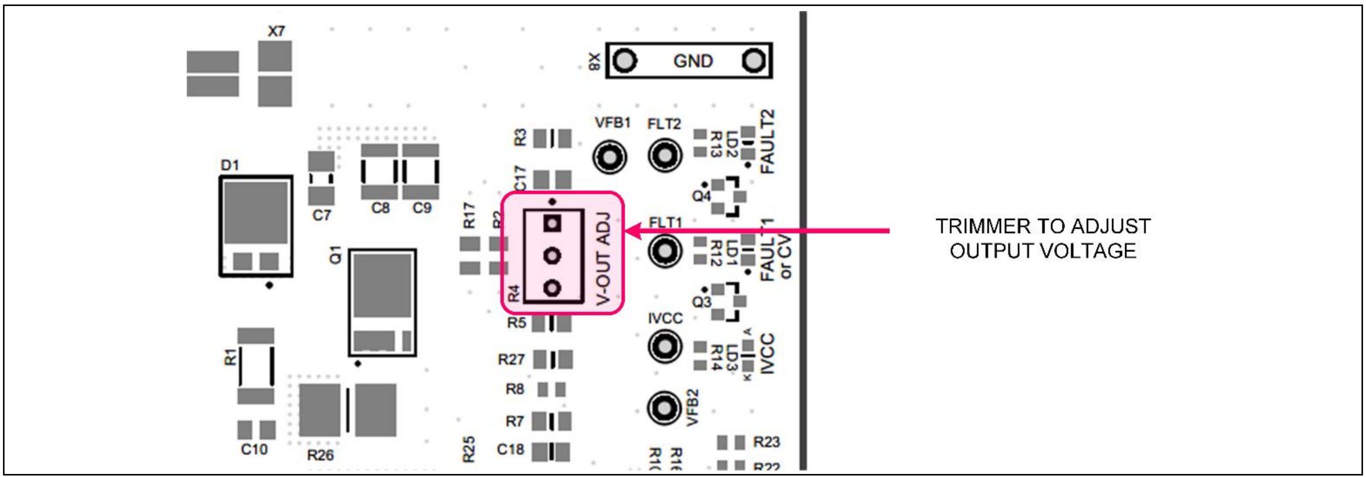



**Figure 6 Output voltage regulation**

Overvoltage protection is set by voltage divider $R_{VFBH-2}$ = 68 kΩ and $R_{VFBL-2}$ = 1.8 kΩ. If during a fault the output voltage goes higher than 62 V, on pin VFB2 the voltage is higher 1.6 V and the switching activity is stopped until the fault condition is removed.

FPWM/FAULT2 signals this fault with a specific squared waveform (see chapter Faults detection).

## 2.4 Faults detection

Depending on the resistor value connected to FPWM/FAULT1,2 pins, the controller shows different behavior during a fault. For more information, see datasheet [2] for TLD6098-2ES.

To ease the fault detection, two LEDs have been applied on the FPWM/FAULT1,2 pins:

- Yellow LED will light up when a fault occurs on channel 1 or the voltage loop of channel 1 is enabled
- Red LED will light up when a fault occurs on channel 2

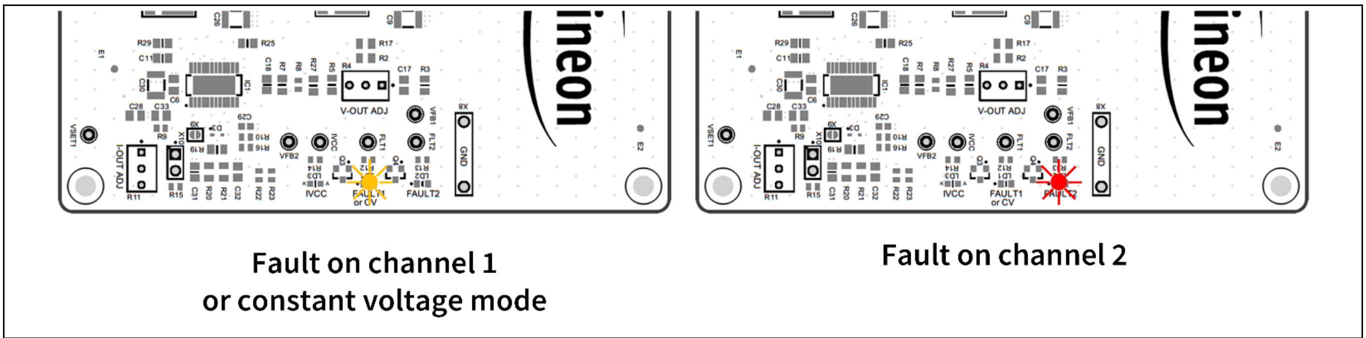



**Figure 7 Fault LED indication**

To understand what the fault FPWM/FAULT1,2 pins are signaling, connect two oscilloscope probes to the test points FLT1 and FLT2, as shown in Figure 8 and refer to the waveforms in Table 4 .

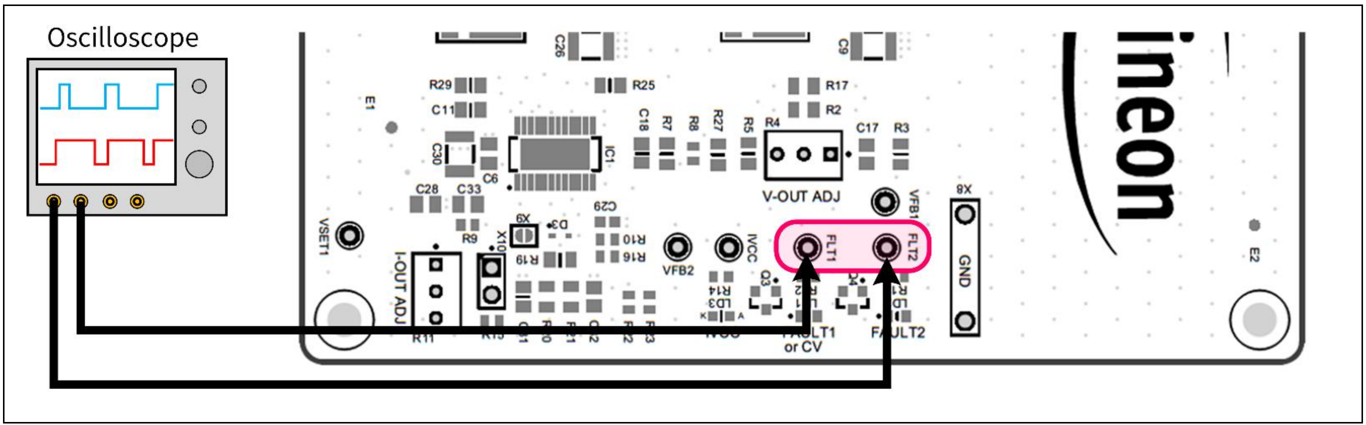
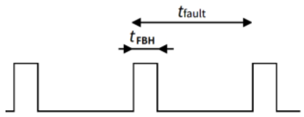
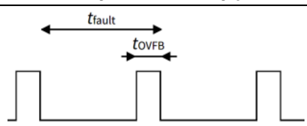
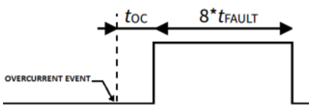



**Figure 8** **FLT1 and FLT2 test points**

In this board FPWM/FAULT1,2 pins react as follows, to a fault:

**Table 4** **Fault detection**

| Fault type | FPWM/FAULT1 (Yellow LED) | FPWM/FAULT2 (Red LED) |
|---|---|---|
| Constant voltage out enabled | Continuous high | N.A. |
| Constant current out enabled | Continuous low | N.A. |
| Overvoltage on pin FBH1 | High when $V_{FBH1}$ > 75 V (Max.)<br>Low when $V_{FBH1}$ < 65 V (Min.)<br>Device checks overvoltage every 10 ms (Typ.) | N.A. |
| Overvoltage on pin FBH2 | N.A. |  <br>$t_{fault}$ = 10 ms (Typ.)<br>$t_{FBH}$ = 6 ms (Typ.)<br>Device checks overvoltage every 10 ms (Typ.) |
| Output overvoltage or IVCC < 0.8 V | N.A. |  <br>$t_{FAULT}$ = 10 ms (Typ.)<br>$t_{OVFB}$ = 4 ms (Typ.) |
| Overcurrent: $I_{CH1}$ > 10 A |  <br>$T_{FAULT}$ = 10 ms (Typ.)<br>$t_{OC}$ = 4 ms (Typ.) | N.A. |

High voltage level on FPWM/FAULT1,2 pins is 4 V (Min.), low voltage level is 0.8 V (Typ).

The status of FPWM/FAULT1,2 pins can be also monitored by a microcontroller. In this case a series resistor of 10 kΩ minimum must be used between FPWM/FAULT1,2 and the input pin of the microcontroller.

## 2.5 Current derating

Input current increases with the decreasing of input voltage. Thus, in order to keep components within their safety temperature, output power must be limited, reducing the output current according to the safe operating area (SOA) showed in the figure below.

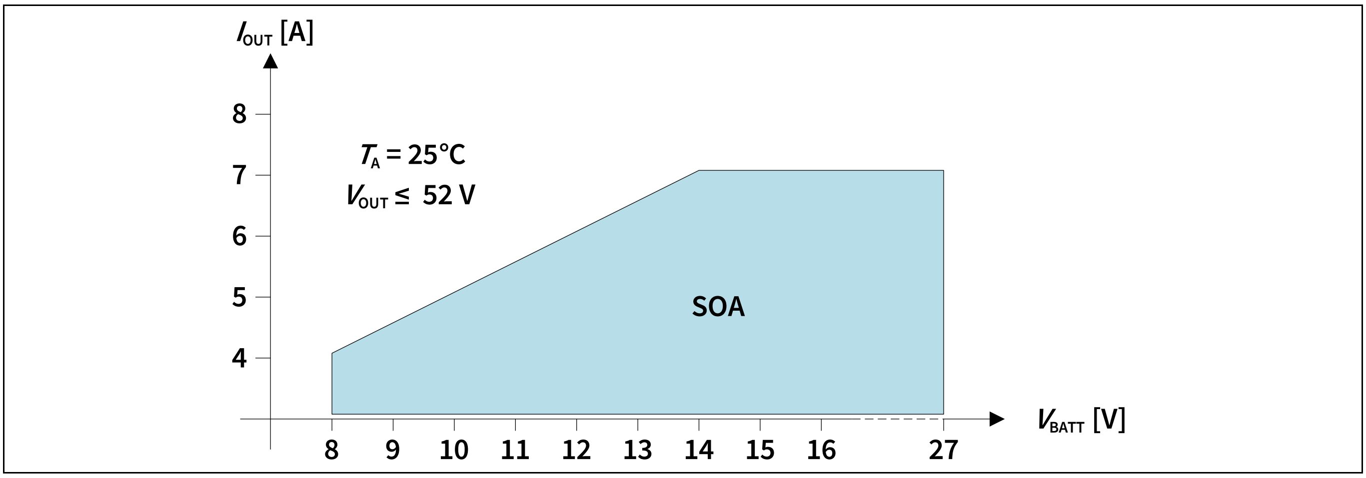



**Figure 9 Current derating**

# 3 System design

## 3.1 Schematics

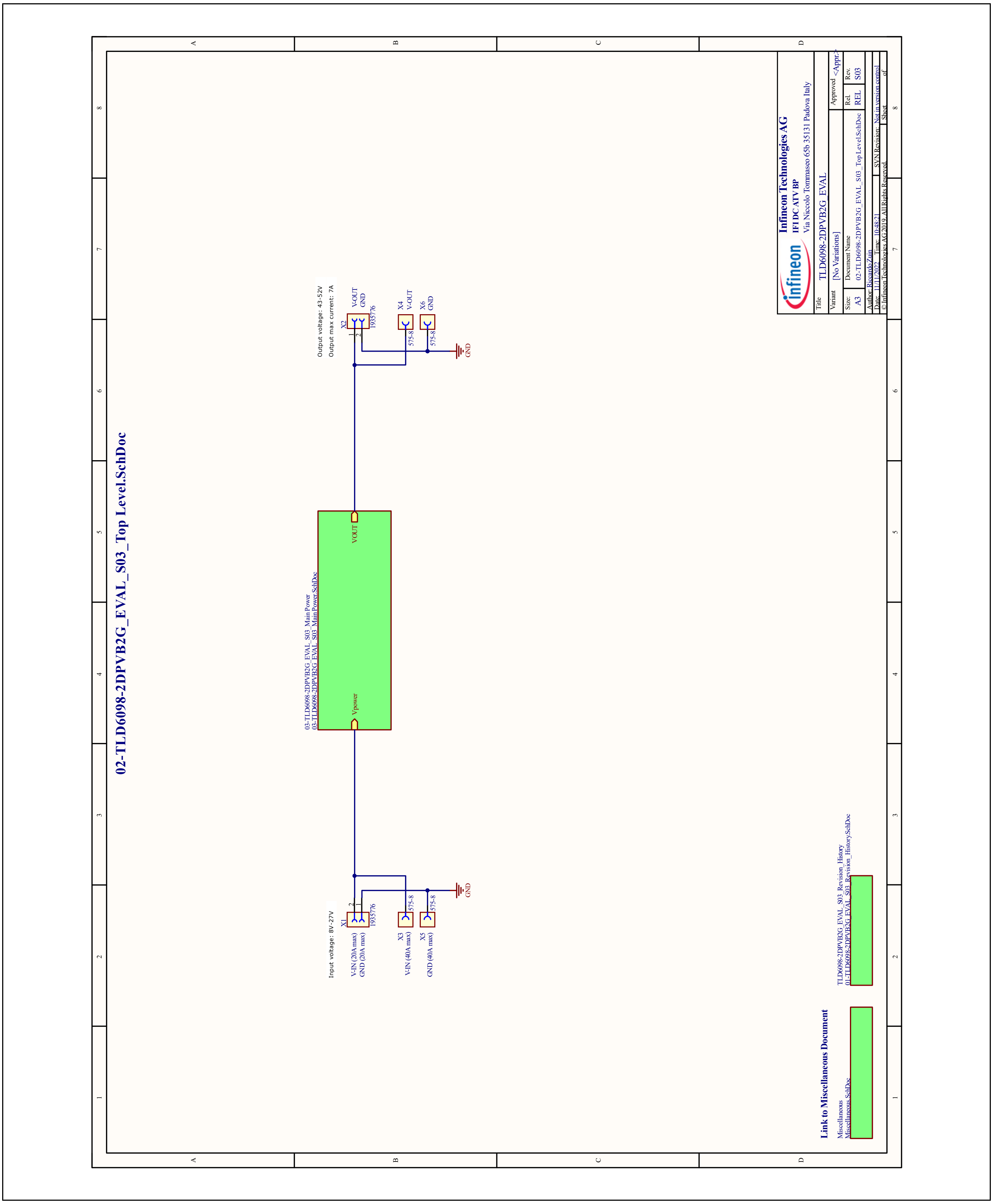



**Figure 10** Top Level

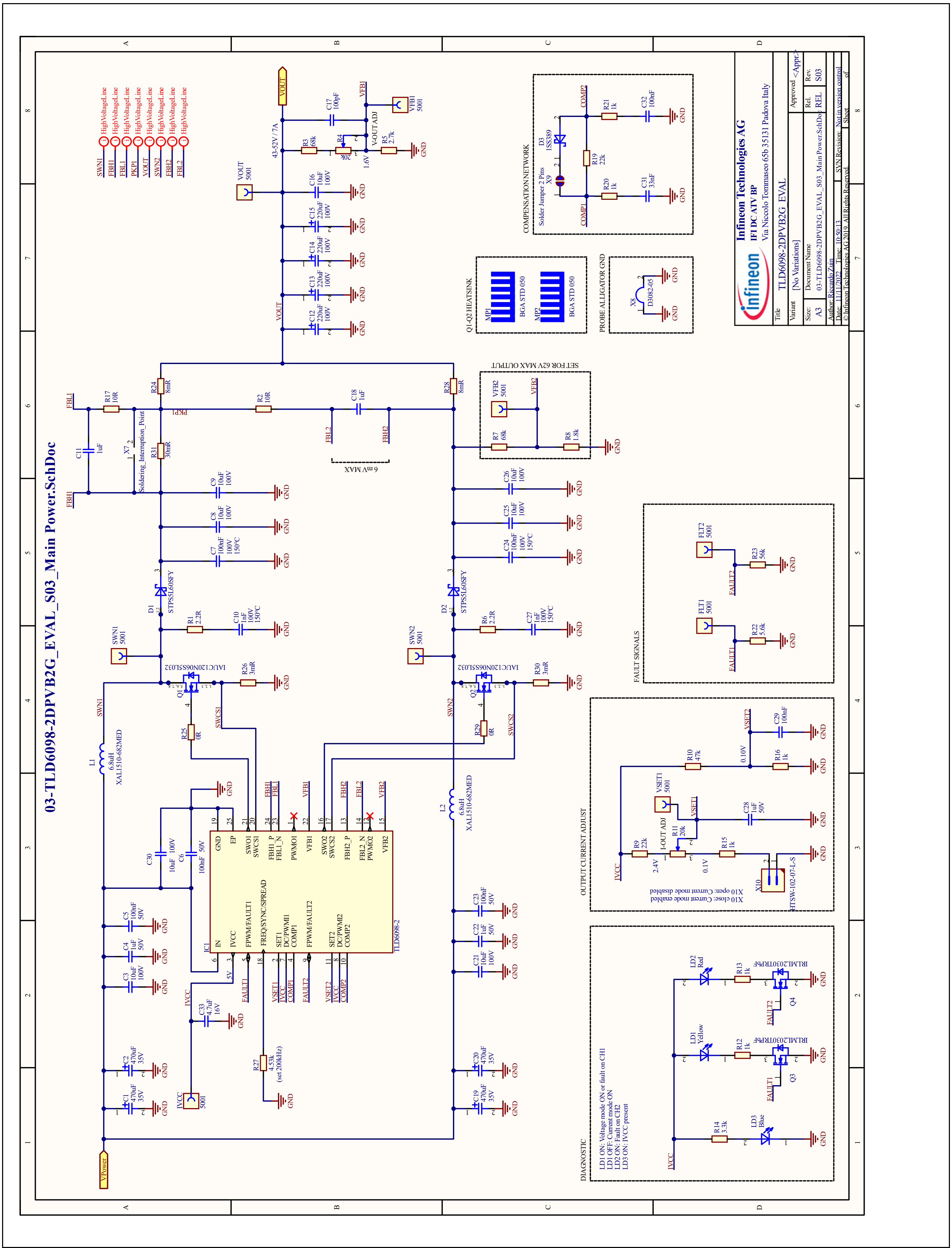


**Figure 11 Main power schematic**

## 3.2 PCB layout

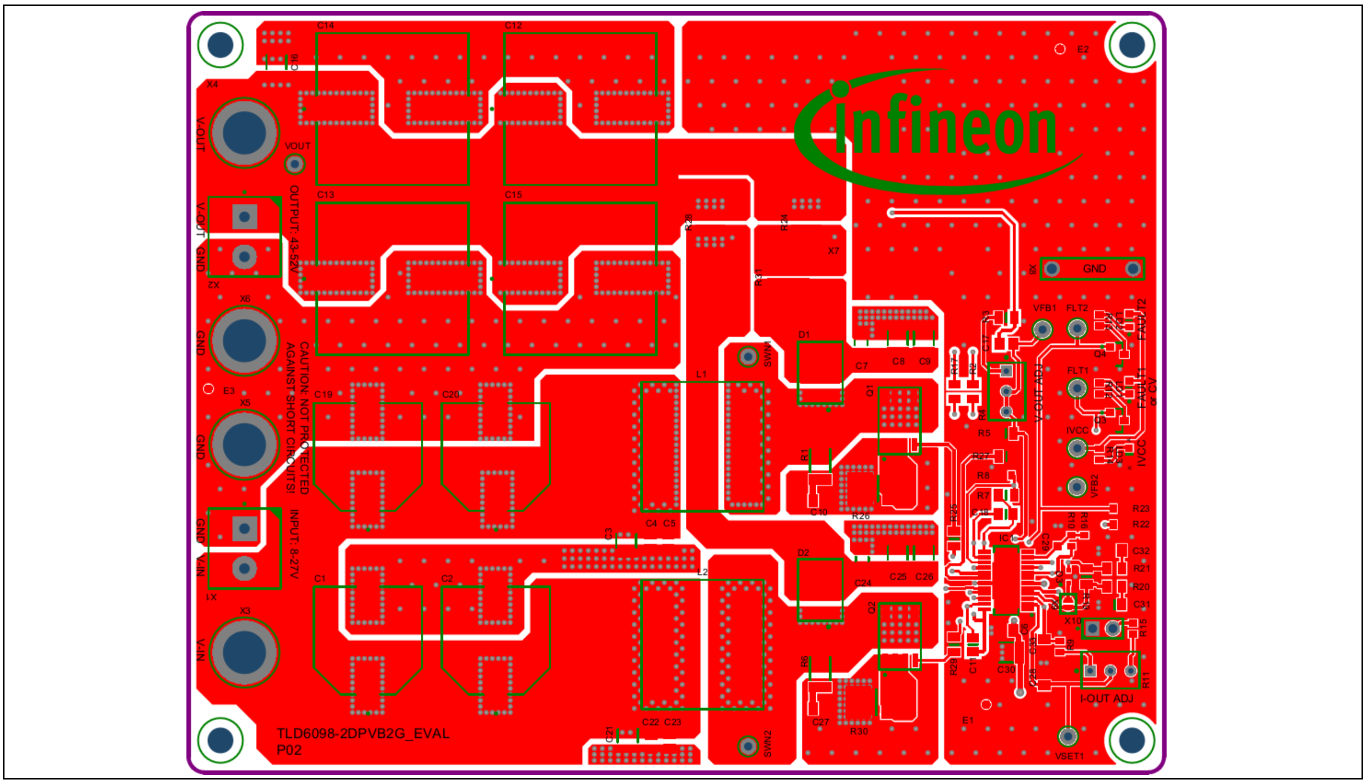



**Figure 12 Top overlay**

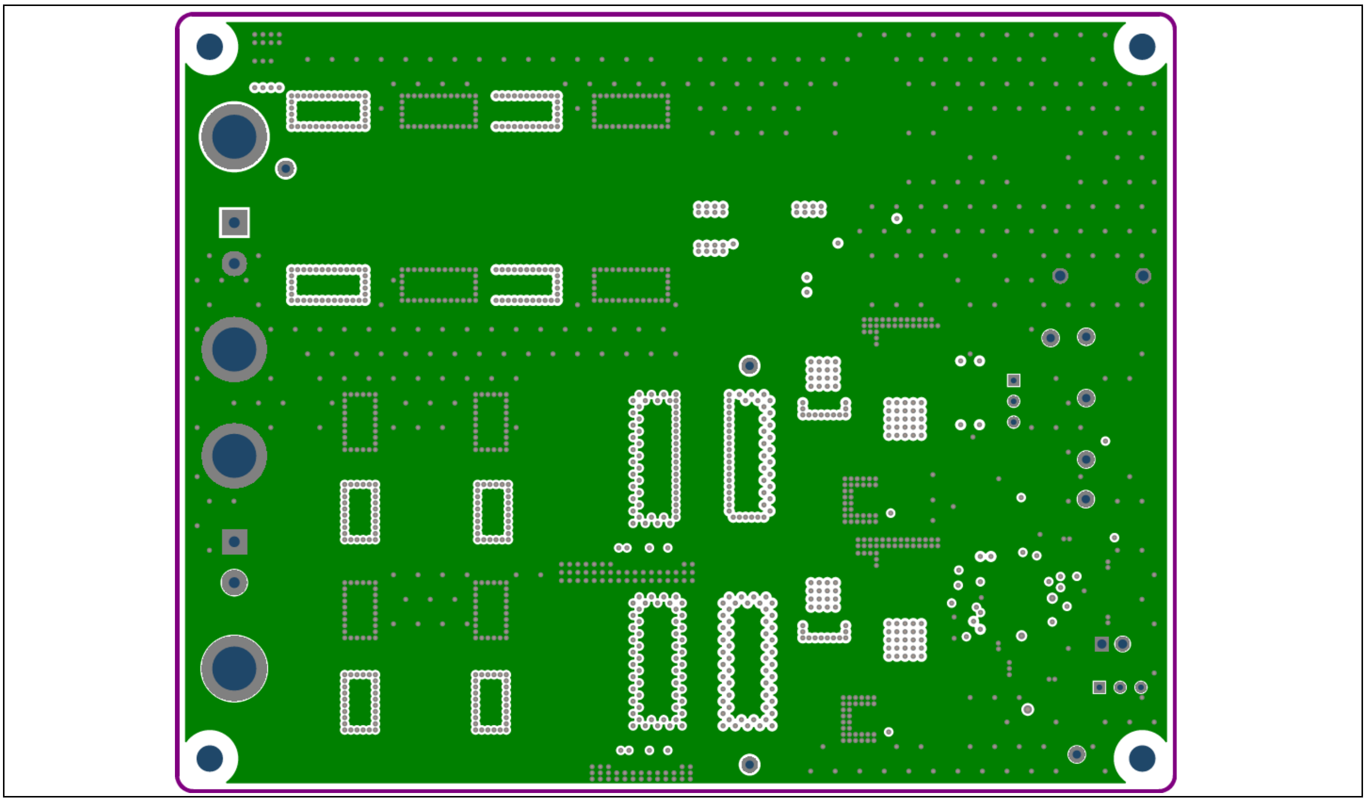


**Figure 13 Internal overlay 1 (GND ground plane)**

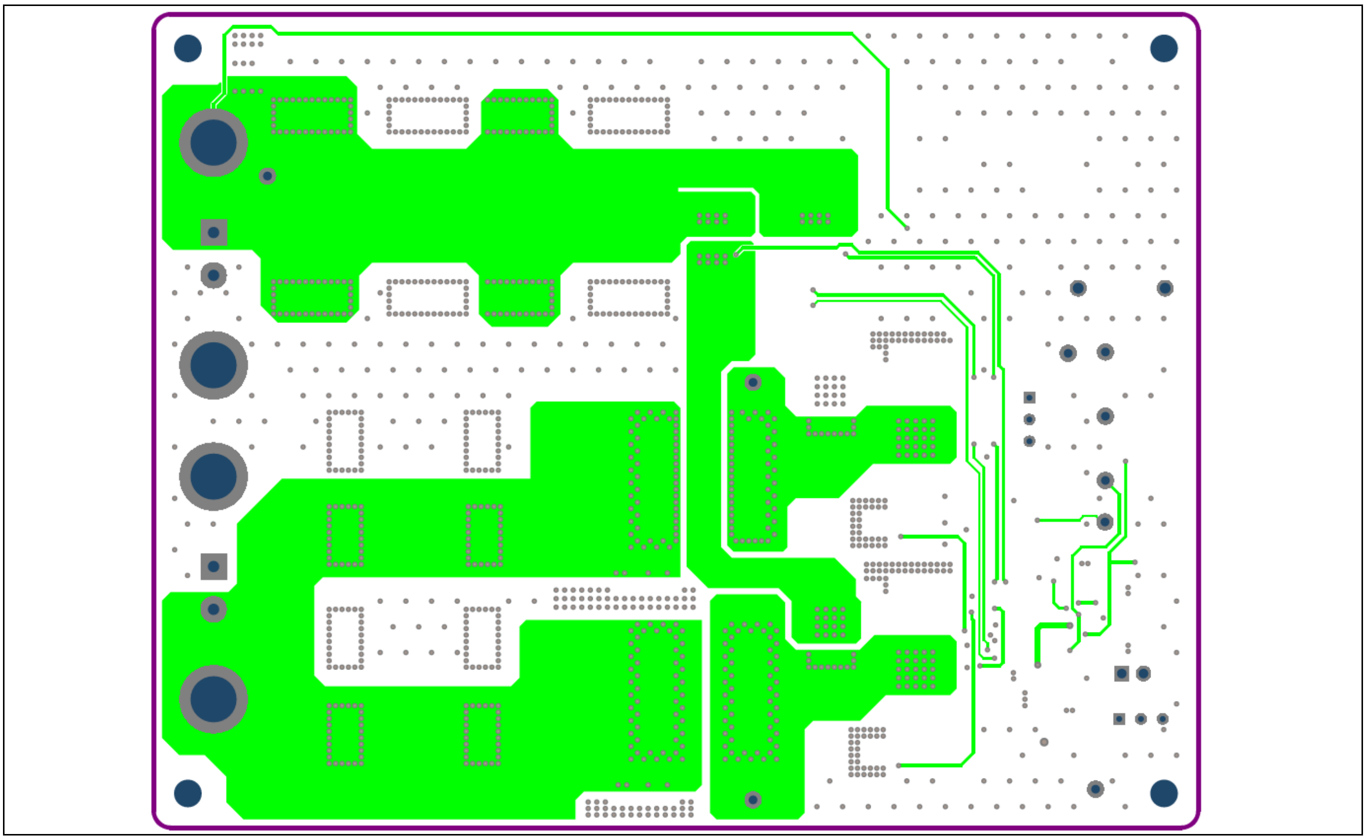


**Figure 14 Internal overlay 2**

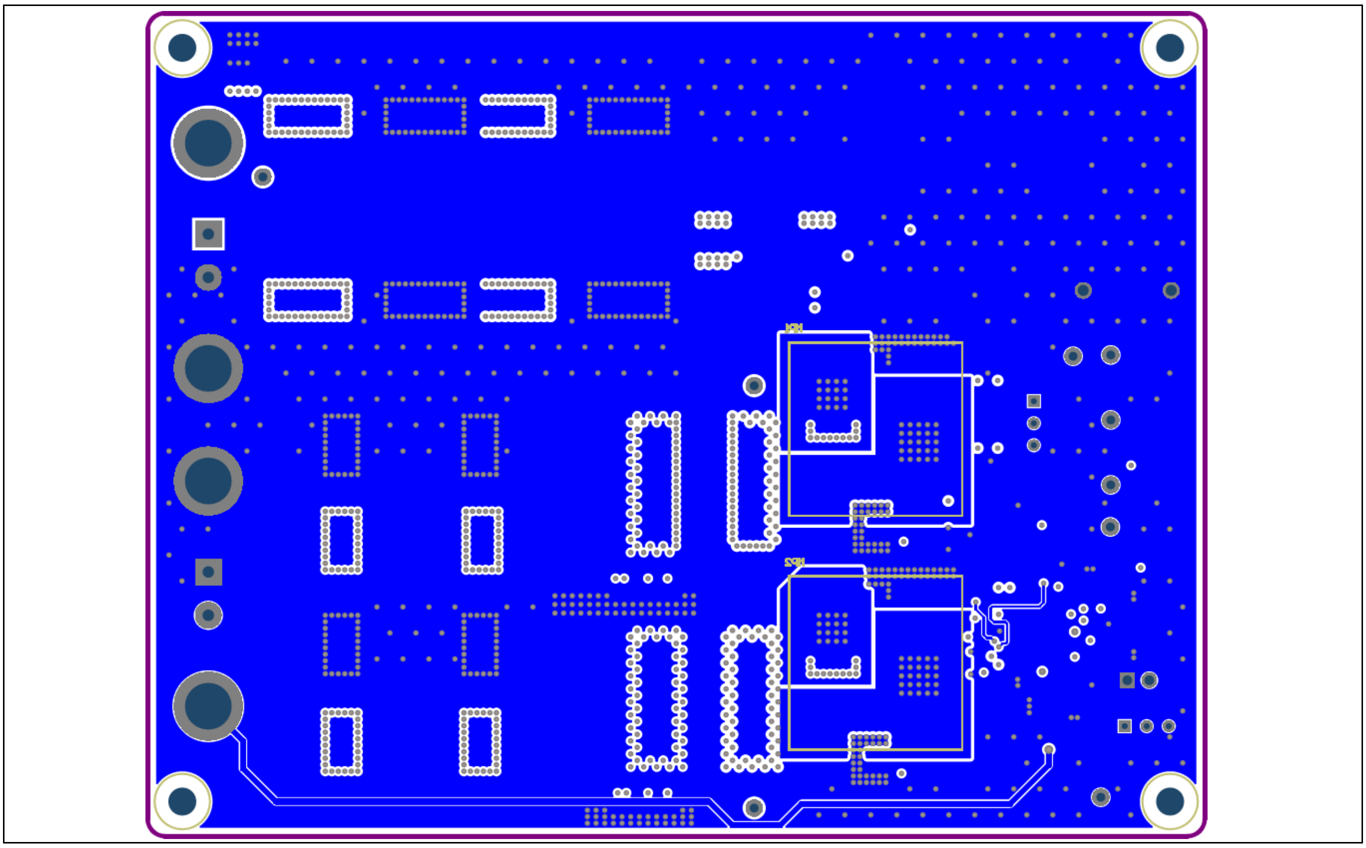


**Figure 15 Bottom overlay**

## 3.3 Bill of material

**Table 5 Bill of material**

| Designator | Value | Manufacturer | Manufacturer order number |
|---|---|---|---|
| C1, C2, C19, C20 | 470 µF | Panasonic | EEE-FK1V471AQ |
| C3, C8, C9, C16, C21, C25, C26, C30 | 10 µF | MuRata | GRM32EC72A106KE05L |
| C4, C22, C28 | 1 µF | TDK Corporation | CGA4J3X7R1H105K125AB |
| C5, C6, C23 | 100 nF | TDK Corporation | CGA4J2X8R1H104K125AA |
| C7, C24 | 100 nF | TDK Corporation | CGA5H2X8R2A104K115AA |
| C10, C27 | 1 nF | MuRata | GCM2195G2A102JA16 |
| C11, C18 | 1 µF | MuRata | GRM21BR71H105KA12L |
| C12, C13, C14, C15 | 220 µF | Panasonic | EEEFK2A221AM |
| C17 | 100 pF | AVX | 08051A101FAT2A |
| C29 | 100 nF | TDK Corporation | CGA3E2X8R1E104M080AA |
| C31 | 33 nF | MuRata | GRM21BR72A333MA01 |
| C32 | 100 nF | Kemet | C0805C104J5RAC |
| C33 | 4.7 µF | MuRata | GCM21BR71C475KA73 |
| D1, D2 | STPS5L60SFY | STMicroelectronics | STPS5L60SFY |
| D3 | 1SS389 | Toshiba | 1SS389 |
| FLT1, FLT2, IVCC, SWN1, SWN2, VFB1, VFB2, VOUT, VSET1 | - | Keystone Electronics Corp. | 5001 |
| IC1 | | Infineon Technologies | TLD6098-2ES |
| L1, L2 | 6.8 µH | Coilcraft | XAL1510-682MED |
| LD1 | Yellow | Vishay | TLMY1000-GS08 |
| LD2 | Red | Vishay | TLMS1100-GS08 |
| LD3 | Blue | Wurth Elektronik | 150060BS75000 |
| MP1, MP2 | BGA STD 050 | ABL Components | BGA STD 050 |
| MP3, MP4, MP5, MP6 | - | Multicomp | MP006555 |
| MP7, MP8, MP9, MP10 | - | Wurth Elektronik | 970300321 |
| Q1, Q2 | - | Infineon Technologies | IAUC120N06S5L032 |
| Q3, Q4 | - | Infineon Technologies | IRLML2030TRPbF |
| R1, R6 | 2.2 Ω | Vishay | CRCW20102R20FK |
| R2, R17 | 10 Ω | Yageo | RC0805FR-0710RL |
| R3, R7 | 68 kΩ | Vishay | CRCW080568K0FK |
| R4, R11 | 20 kΩ | Bourns | 3266Y-1-203LF |
| R5 | 2.7 kΩ | Vishay | CRCW08052K70FK |
| R8 | 1.8 kΩ | Vishay | CRCW06031K80FK |
| R9 | 22 kΩ | Vishay | CRCW060322K0FK |
| R10 | 47 kΩ | Vishay | CRCW060347K0FK |
| R12, R13, R15, R16 | 1 kΩ | Vishay | CRCW06031K00FK |
| R14 | 3.3 kΩ | Vishay | CRCW06033K30FK |
| R19 | 22 kΩ | Vishay | CRCW080522K0FK |
| R20, R21 | 1 kΩ | Yageo | AC0805FR-071KL |
| R22 | 5.6 kΩ | Vishay | CRCW06035K60FK |
| R23 | 56 kΩ | Vishay | CRCW060356K0FK |
| R24, R28 | 8 mΩ | Vishay | WFCP06128L000FE66 |

| Designator | Value | Manufacturer | Manufacturer order number |
|---|---|---|---|
| R25, R29 | 0 Ω | Vishay | CRCW08050000Z0EAHP |
| R26, R30 | 3 mΩ | Bourns | CRE2512-FZ-R003E-3 |
| R27 | 4.53 kΩ | Vishay | CRCW08054K53FK |
| R31 | 30 mΩ | Panasonic | ERJC1CFR03U |
| X1, X2 | - | Phoenix Contact | 1935776 |
| X3, X4, X5, X6 | - | Keystone Electronics Corp. | 575-8 |
| X8 | - | Harwin | D3082-05 |
| X9 | - | - | Solder Jumper 2 Pins |
| X10 | - | Samtec | HTSW-102-07-L-S |
| X11 | - | Harwin | M7583-05 |

## 3.4 Electrical performance

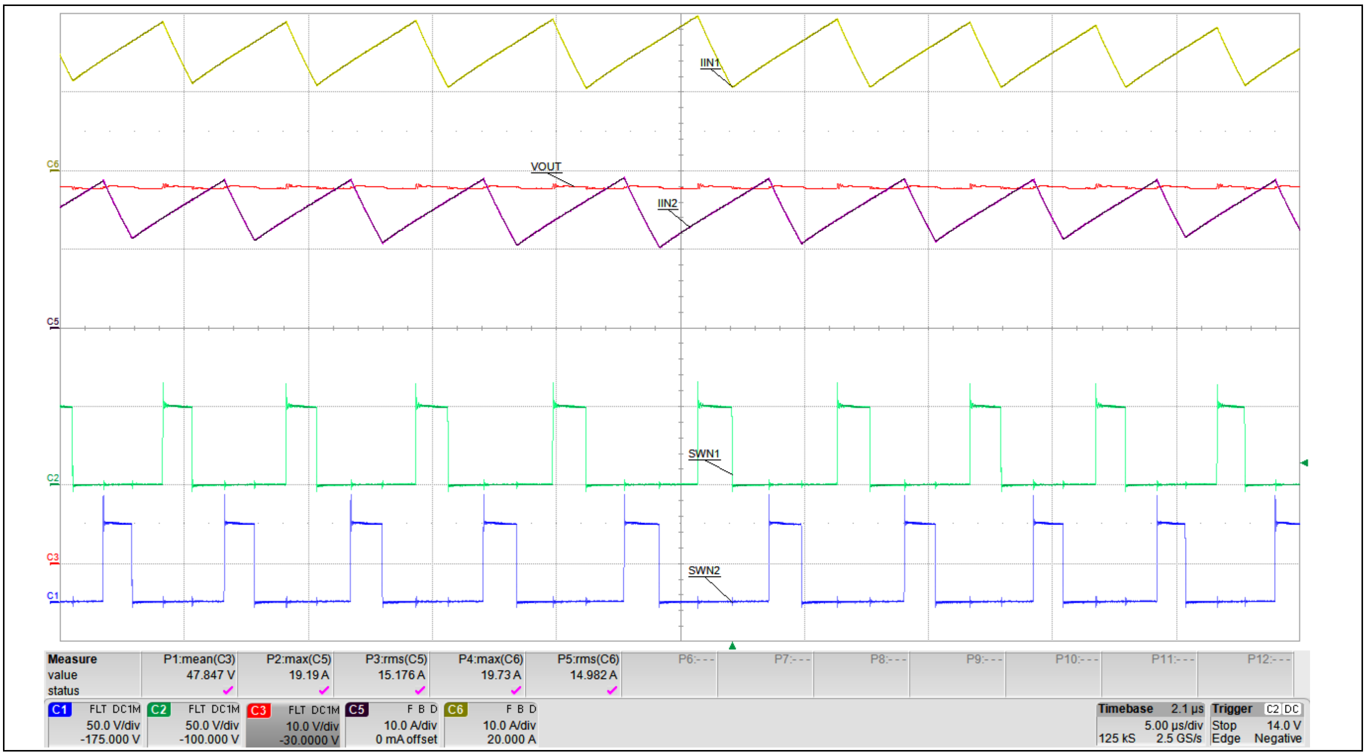



**Figure 16 Input currents, switching nodes, output voltage ($V_{IN}$ = 12 V, $V_{OUT}$ = 48 V, $I_{OUT}$ = 7 A)**

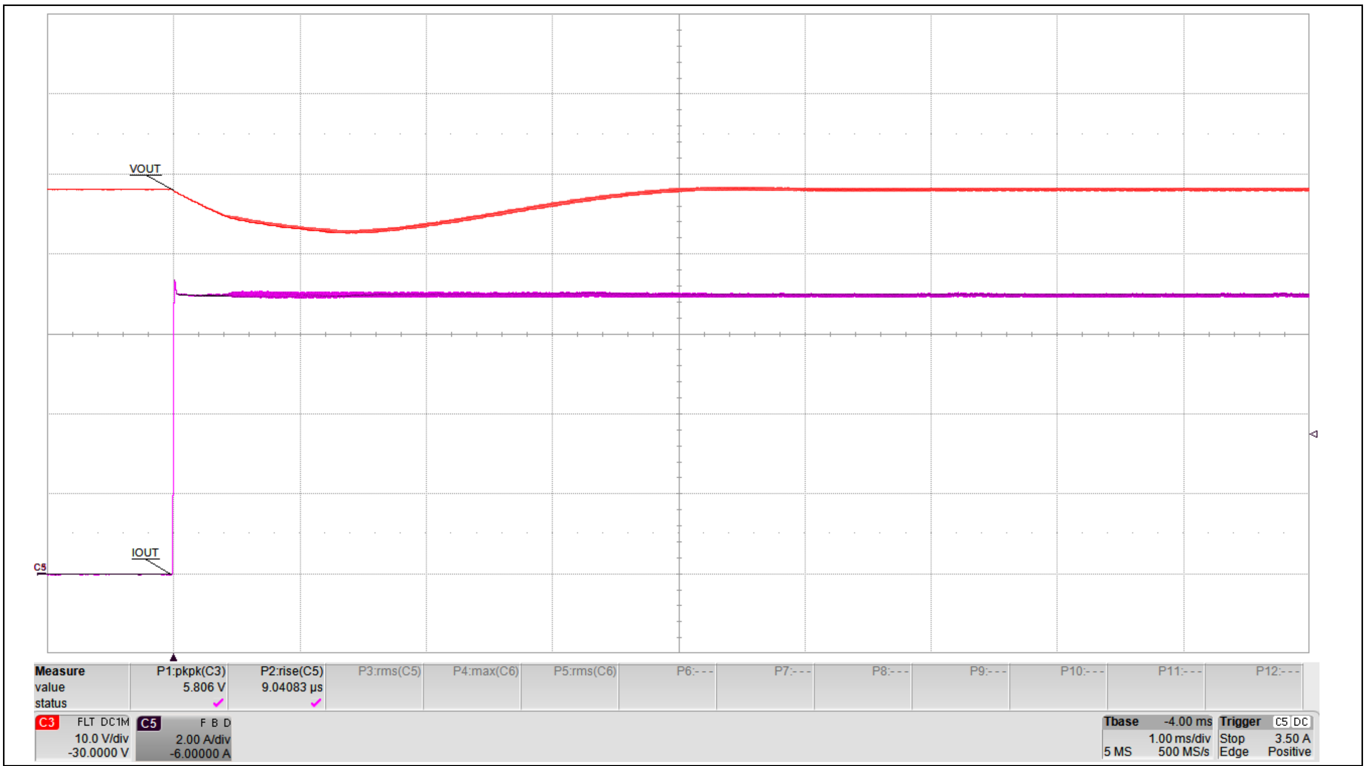



**Figure 17 Load dump ($V_{IN}$ = 14 V, $V_{OUT}$ = 48 V, $I_{OUT}$ = 0 A to 7 A, Rise time < 10 µs)**

## 3.5 Efficiency measurements

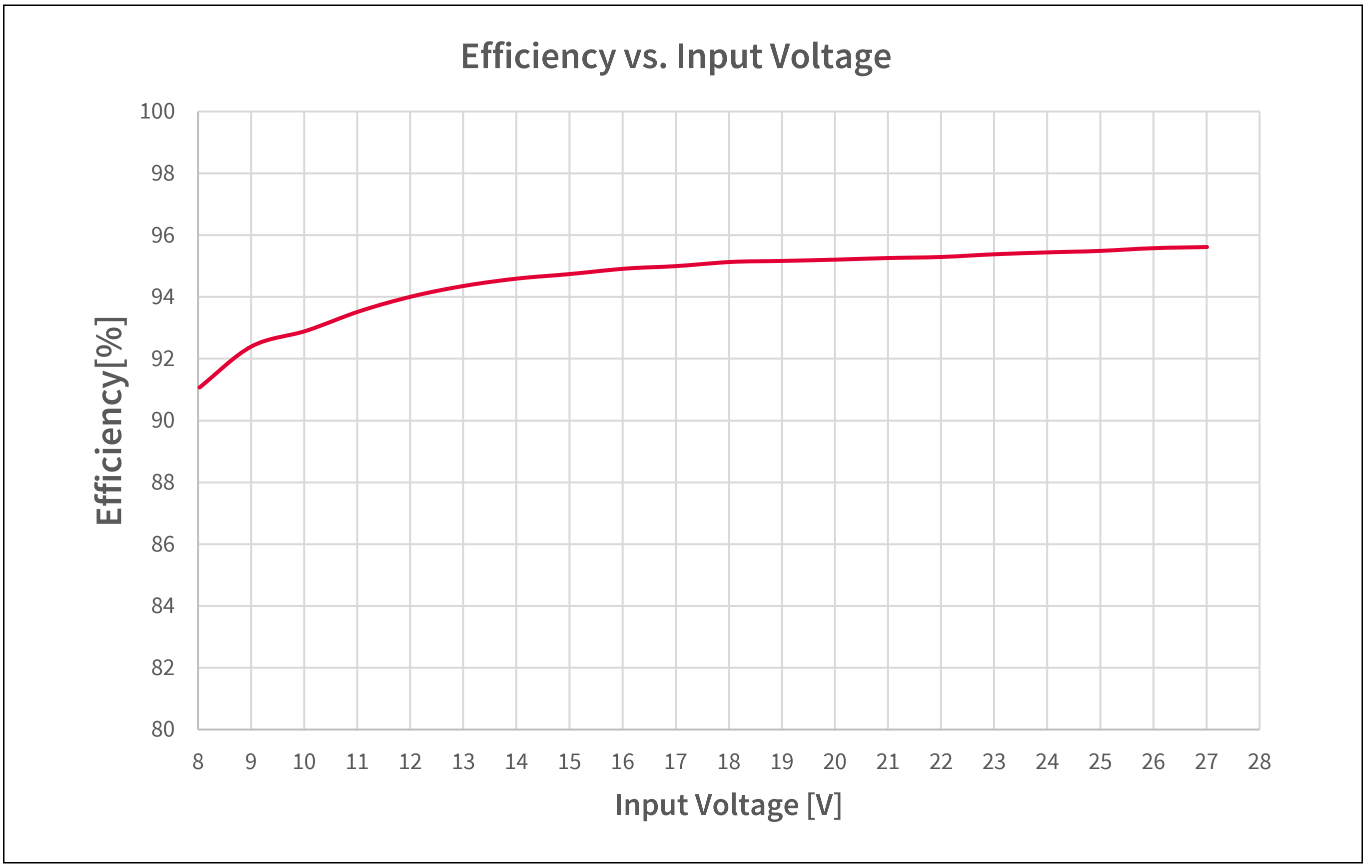



**Figure 18 Efficiency vs. input voltage performance**

This efficiency performance has been obtained with:

**Table 6 Efficiency measurement conditions**

| | |
|---|---|
| Output load: | Constant current sink set at 7 A |
| Output voltage: | 48 V |
| Ambient temperature: | 25°C |
| Current Mode: | Disabled (jumper X10 left open) |
| Current sensing resistor (R31): | Active (jumper X7 left open) |
| Compensation clamping diode (D3): | Active (jumper X9 closed) |

## 3.6 Thermal performances

Ideally, the output current should be generated equally by both channels. Unfortunately, since the controller inputs FBH2 and FBL2 are real and show a residual offset, the currents sourced by the two channels are not identical.

Referring to simplified schematic Figure 2, the current mismatch between the two channels $\Delta I_{12}$ can be calculated as following:

$$\Delta I_{12} = I_1 - I_2 = \frac{\Delta V_{FB2}}{R_{FB1,2}} = \frac{V_{FBL2} - V_{FBH2}}{R_{FB1,2}}$$

Where $I_1$ is the current sourced by channel 1, $I_2$ is the current sourced by channel 2 and $R_{FB1,2}$ is the value of balancing shunt resistors (8 mΩ).

Typically, the quantity $\Delta V_{FB2}$ is lower than 6 mV.

The current mismatch can generate different steady temperatures between the channels. An example is shown in Figure 19, where it is clearly visible that channel 1 shows a higher temperature than channel 2.

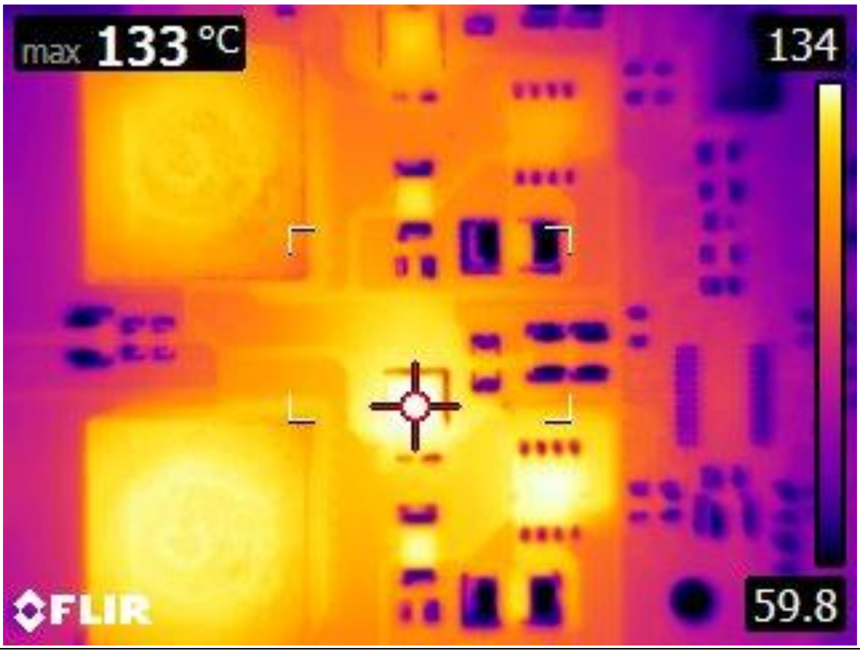



**Figure 19 Current mismatch ($V_{IN}$ = 14 V, $V_{OUT}$ = 52 V, $I_{OUT}$ = 7 A, $T_A$ = 25°C)**

# 4 References

[1] Infineon TLD6098-1EP Datasheet, https://www.infineon.com/cms/en/product/power/lighting-ics/litix-automotive-led-driver-ic/litix-power/tld6098-1ep/

[2] Infineon TLD6098-2ES Datasheet, https://www.infineon.com/cms/en/product/power/lighting-ics/litix-automotive-led-driver-ic/litix-power/tld6098-2es

## 5 Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| Rev.1.00 | 2022-12-22 | First release related to evalboard S03_P02 |
| | | |
| | | |

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