NAC1080/ NAC1081 Datasheet

Features

NAC1080 is an IC, suitable and optimized for NFC communication controlled actuation. It contains a NFC transceiver, an actuation interface, a microcontroller and wired communication interfaces. NAC1080 is available in a 16-pin package. NAC1081 is available in a 32-pin package. The functional pins in both package variants are identical.

The chip can operate in two different power supply modes:

- active supply mode:
  - The chip is supplied by an external 3V power supply source (e.g. battery).
- passive supply mode:
  - The chip is harvesting energy from the external NFC RF field. No additional external supply source is required. Of course, operation of the chip requires the presence of the NFC field in this use case. The chip can charge external capacitors, in order to store harvested energy. External storing capacitors can be used to store the required amount of energy to initiate an actuation action (e.g. to drive a motor).

Main product features are:

- contact-less communication interface NFC
  - PICC according to ISO/ IEC 14443 Type A
  - data rate 106 kBit/s
  - initialization and anti-collision protocol processed in firmware
  - proprietary and customizable application protocol optimized for end custom applications
- Integrated microcontroller
  - 32-bit ARM Cortex-M0 CPU operating at clock frequency of 28 MHz
  - nested vector interrupt controller with 18 interrupts
  - integrated system tick timer (SysTick)
  - MicroDMA with 8 DMA channels
  - 16 kByte integrated ROM containing start-up code and system development kit software library
  - 16 kByte integrated SRAM
  - 60 kByte integrated non volatile flash memory
  - Serial Wire Debug interface
  - multilayer AHB-Lite on chip interconnect
- Digital Peripherals
  - Up to 7 programmable and configurable General Purpose Input/ Outputs (GPIO)
  - System Timer Unit containing six independent timer channels and PWM generator
  - watchdog timer
  - arithmetic divide operation hardware accelerator
  - full duplex capable UART transceiver with Rx/ Tx FIFOs
  - SPI master/ slave transceiver with Rx/ Tx FIFOs
  - AES accelerator
  - Real Time Clock
- Actuation interface
  - integrated H-Bridge driver capable to direct drive a motor up to peak current of 250 mA
  - ability to control an external H-bridge driver IC by applying gate drive control signals to GPIO
- embedded Security
  - embedded AES hardware accelerator
  - True Random Number Generator (TRNG)

- Power Management
  - Ultra Low Power power saving Mode available
    - chip supply for almost all parts of the chip is switched off, except a small always-on power domain
    - entering power saving mode and configuring wake up sources is controlled by embedded software
    - chip can wake up by either detecting an external NFC RF field, expiration of an internal wake Up Timer or an external trigger event on a dedicated pin
  - software controlled CPU idle mode
  - CPU clock control by software
  - dedicated and software controlled switchable LDOs for sensing unit and flash memory
- Clock Generation
  - integrated 28MHz oscillator for operation clock generation
  - integrated ultra low power 32 kHz oscillator for always on clock generation
- Power Supply modes
  - passive supply Mode
    - energy is harvested from the external NFC RF field and the power supply of the chip is derived from the harvested energy
    - no external supply source apart from the NFC RF field required
  - active supply mode
    - the chip is supplied by an external supply source and operational, if no NFC field is applied
- Product qualified according to JEDEC Standard

Potential applications

Potential applications and application use cases of NAC1080/ NAC1081 are applications, which require embedded control together with a contact less communication interface, an actuation interface/ driver and optional passive supply mode operation based on RF field energy harvesting.

That might be:

- NFC activated smart lock
- NFC configured Time Relay
- solid state relay

An example application diagram for lock application in passive supply mode is given:

Potential applications

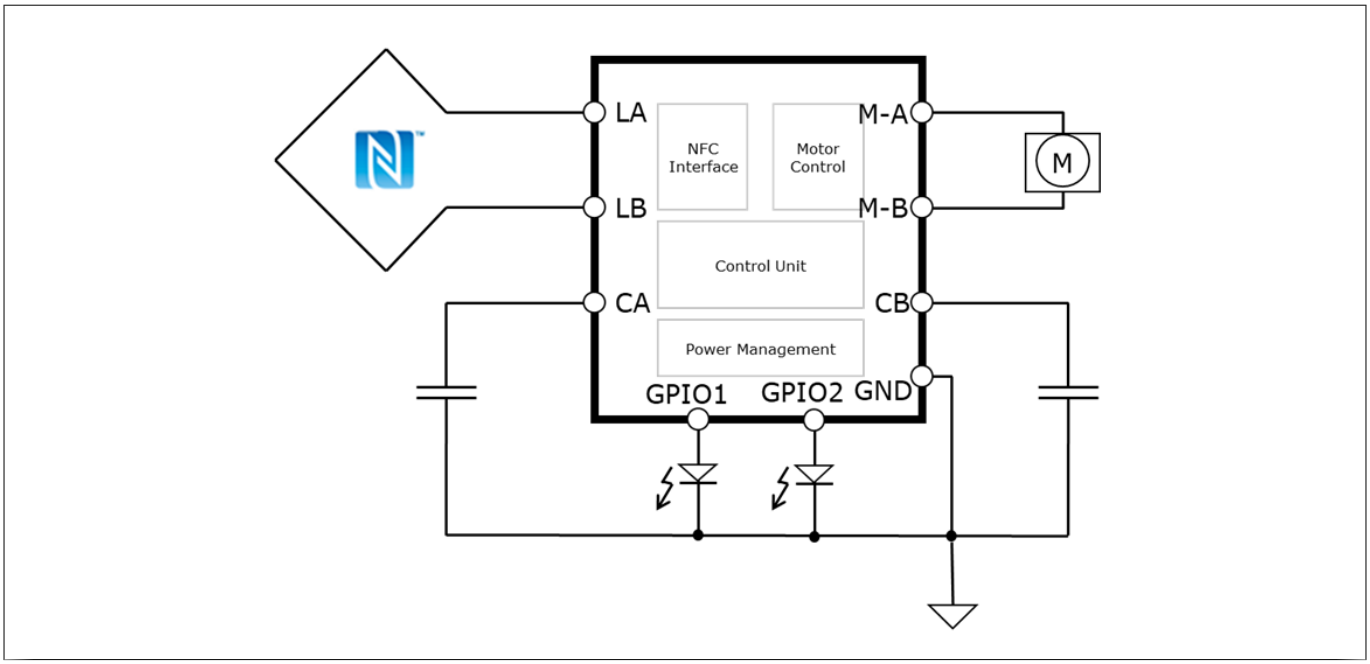

Figure 1 Smart Lock Example (Passive Supply Mode)

Table of contents

1 NAC1080/ NAC1081 Pin Description

This section provides the pin description of NAC1080/ NAC1081.

Table 1 NAC1080/ NAC1081 Pin Description

Name	Pin at PG-DSO-16 (NAC1080)	Pin at PG-VQFN-32 (NAC1081)	Characteristic	Direction	Comment
M_A	16	4	Analog	Input/ Output	Motor A (driven by internal H-Bridge)
M_B	1	5	Analog	Input/ Output	Motor B (driven by internal H-Bridge)
LA	7	18	Analog	Input/ Output (internally load modulated)	NFC Antenna Pin LA
LB	8	19	Analog	Input/ Output (internally load modulated)	NFC Antenna Pin LB
VCC	10	21	Supply	Input	- External supply (3.0V … 3.3V), if supplied in active supply mode - Open in passive supply mode
GND	15	3	Ground	Input	Ground Net
VCC_HB	2	6	Supply	Input/ Output	- Supply of H-Bridge output drivers - in passive supply mode to be connected to external energy storage element (capacitor); the energy is to be stored is harvested from the RF field - in active supply mode to be connected to the external supply (3.0 … 3.3V) *-if H-Bridge output driver is **not used** in application then:* • *in passive supply mode it should kept open or connect to an external capacitor (recommendation 1nF)* • *in active supply mode connect it to the external supply or GND*

(table continues...)

1 NAC1080/ NAC1081 Pin Description

Table 1 (continued) NAC1080/ NAC1081 Pin Description

Name	Pin at PG-DSO-16 (NAC1080)	Pin at PG-VQFN-32 (NAC1081)	Characteristic	Direction	Comment
VCC_CB	9	20	Supply	Input	- in active mode connect to external supply (3.0V … 3.3V) - in passive mode connect to external capacitor (recommendation 2.2 uF)
WAKE_UP	11	22	Analog	Input/ output	external Wake-Up - if not used in target application, then connect to GND
GPIO0	6	17	Digital 2.5V LVCMOS	Input/ Output	General Purpose Input/ Outputs with: • programmable direction and output value • configurable internal Pull Up/ Pull Down Resistors • programmable alternate functions
GPIO1	5	14			
GPIO2	4	10			
GPIO3	3	8			
GPIO4	14	1			
GPIO5	13	31			
GPIO6	12	28			

The unused pins of NAC1081 PG-VQFN-32 package are not bonded and can be considered as "Not Connected".

2 NAC1080/ NAC1081 General Architecture

The general architecture is illustrated by the following block diagram:

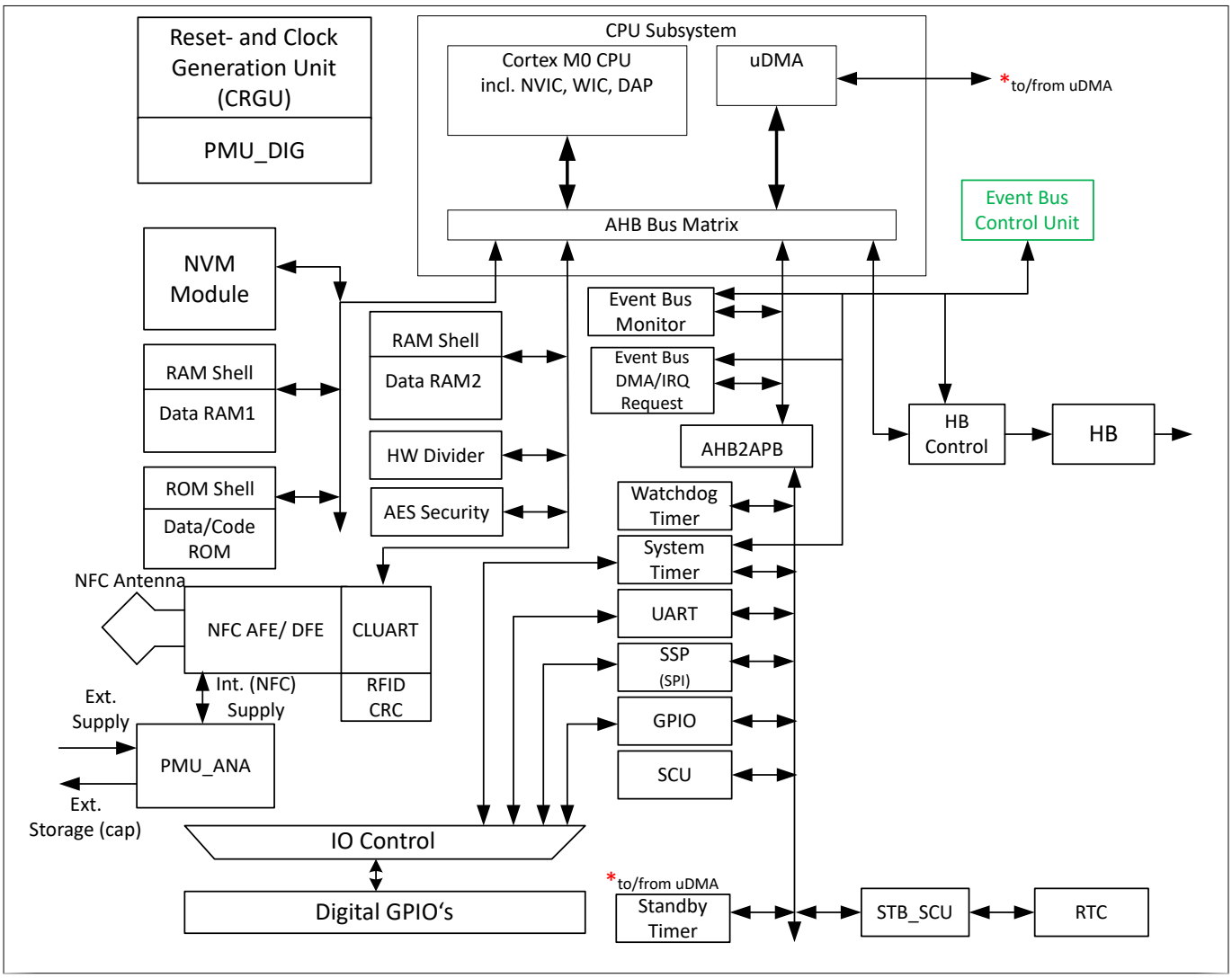

Figure 2 NAC1080/ NAC1081 Block Diagram

3 NAC1080/ NAC 1081 Functional Description

Topics:

ARM Cortex M0 CPU

Details of the ARM Cortex-M0 CPU can be derived from the ARM Cortex-M0 technical reference manual.

The Cortex-M0 is configured with the following parameters:

- Nested Interrupt Controller NVIC with 18 IRQ lines plus NMI
- System Timer Option (*Systick*) enabled
- Fast (Single Cycle) Multiplier
- Support of Wake Up Controller with 20 Wake-Up Sources (18 IRQ's + NMI + RX Event)
- Reset of all registers enabled
- Debugging Option Enabled
  - Serial Wire Debug Interface (*SWD*)
  - Support of one hardware break point comparator

Furthermore NAC1080/ NAC1081 integrates a direct memory access controller (*DMA*). Details of the DMA controller can be derived from the technical reference manual of the *"ARM PrimeCell DMA Controller (PL230)"*. In NAC1080 product the DMA controller is configured to serve ten independent DMA channels.

CPU Address Map

The CPU address space is used in NAC1080 as follows:

3 NAC1080/ NAC 1081 Functional Description

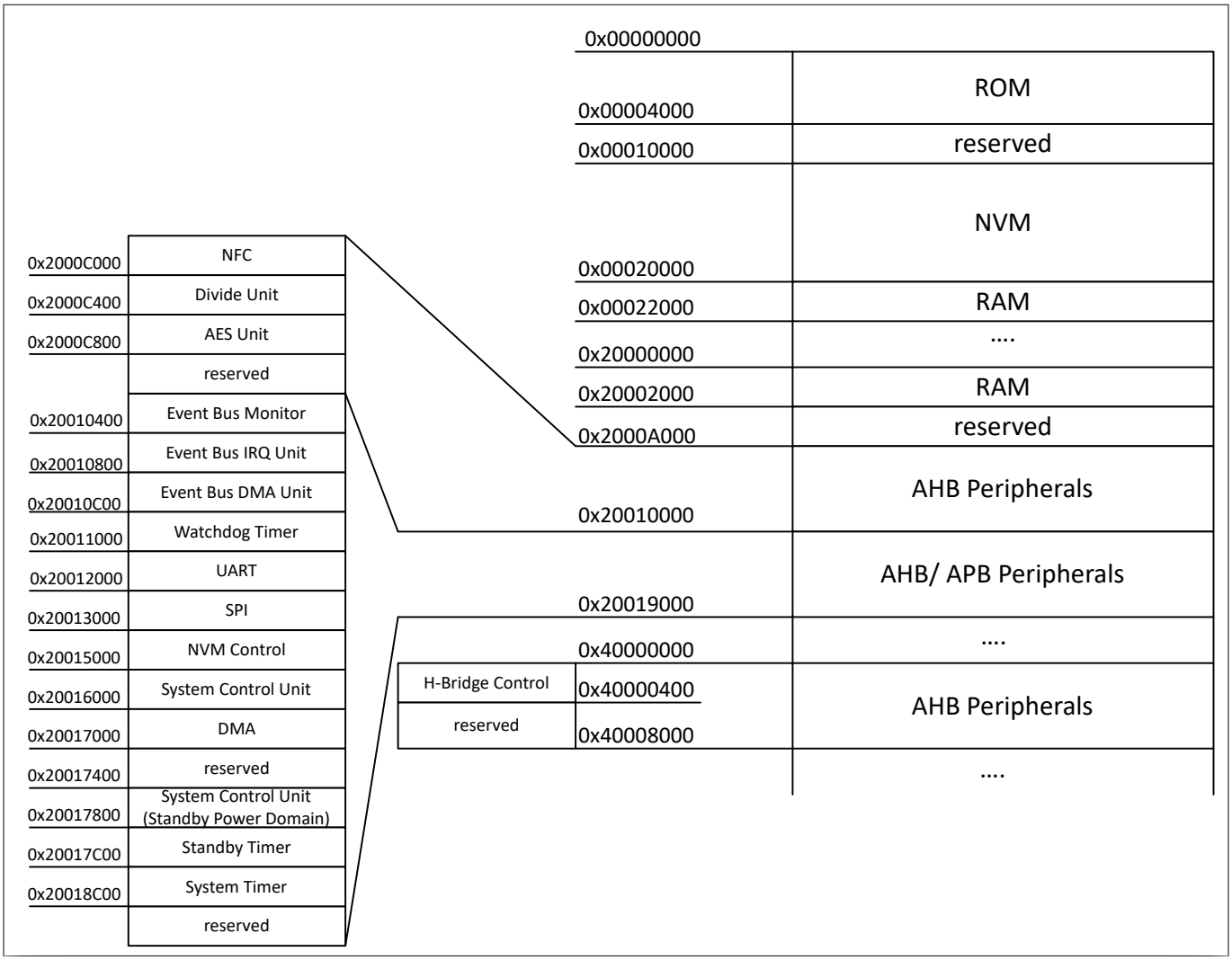

Figure 3 NAC1080/ NAC1081 Address Map

Interrupts

In NAC1080 eighteen IRQs plus non mask-able interrupt are available. Following IRQ sources are assigned to the interrupts:

Interrupt	IRQ Source
NMI	Event Bus Interrupt Request / NMI
IRQ0	NFC
IRQ1	Event Bus Interrupt Request
IRQ2	Event Bus Interrupt Request
IRQ3	Event Bus Interrupt Request
IRQ4	Event Bus Interrupt Request
IRQ5	Event Bus Interrupt Request
IRQ6	Event Bus Interrupt Request
IRQ7	Event Bus Interrupt Request
IRQ8	Event Bus Interrupt Request

Interrupt	IRQ Source
IRQ9	Event Switch Matrix
IRQ10	Event Switch Matrix
IRQ11	Event Switch Matrix
IRQ12	Event Switch Matrix
IRQ13	Event Switch Matrix
IRQ14	Event Switch Matrix
IRQ15	Watchdog Timer Unit
IRQ16	HW Divider
IRQ17	NVM busy

The event bus related interrupts have flexible IRQ sources, which are defined by the application run time software.

3.1 NAC1080/ NAC1081 Clock Generation

NAC1080/ NAC1081 integrates two clock oscillators.

One clock oscillator provides the fast clock of frequency of 28MHz and which is used in the core supply domain and is the CPU clock. The clock oscillator of fast clock is switched off in power saving mode. During operating mode the CPU clock is gated during CPU sleep mode. The fast clock can be divided by firmware programming

Another clock oscillator is generating a slow clock of 32kHz. This clock is always on and is used in the standby "always on" power domain. It clocks the power management unit and the standby timer. Hence the slow clock controls the power on start up, the transition into power saving mode and the wake up.

Furthermore a clock is extracted from the NFC carrier, in case an NFC RF field is present. This clock of 13.56MHz is used in the physical layer of the NFC transceiver and the related PHY layer digital logic.

3.2 NAC1080/ NAC1081 Power Management

NAC1080/ NAC1081 power management controls the power supply mode selection, the power on start-up and the power modes control.

NAC1080/ NAC1081 can be supplied in two different supply modes:

- active supply mode:
  - in active supply mode an external supply voltage of has to be provided at pin VCC. The internal power management detects the presence of a supply voltage at pin VCC at power on and controls the proper start-up and operation.
- passive supply mode:
  - In passive supply mode no external supply source is required. The device is supplied by the energy of the RF field of NFC. The NFC receiver is harvesting the required energy from the field and the power management is controlling a proper start-up and operation.

The device has different internal supply domains. Supply domains are internally separated from each other and are controlled by the power management. The purpose of separation of power supply domains are application dependent power saving and supply noise protection.

- core supply domain
  - This is a digital supply domain, which supplies the major part of digital logic and memories, including the CPU.
- standby supply domain
  - This is a supply domain, which supplies a small part of the chip. It is an "always on" power domain, which includes the power management unit . Since it is responsible for power mode and status control and wake up , it needs to be permanently "on". Beside the power management it contains a wake up timer and a real time clock counter.

  This is a
- NVM supply domain
  - This is a separate supply domain, which supplies the non volatile memory.
- I/O supply domain
  - This supply domain supplies the digital I/Os.
- H-Bridge Driver Supply domain
  - This is a separate supply domain, which supplies the switching transistors of the H-Bridge. It is sourced by the external pin VCC_HB. In active supply mode an external supply source has to be connected to pin VCC_HB. In passive supply mode, an external storage capacitor has to be connected to pin VCC_HB. In passive supply mode this external storage capacitor will be charged by the power management in a controlled way with harvested energy from the external RF-field.
- NFC Transceiver Power Domain
  - There is a small part of the NFC transceiver, which is sourced by the external RF field
-

The device integrates internal voltage regulators, which produce a stable output voltage in order to supply the domain specific circuitry. The internal voltage regulators are controlled by the power management and sourced by external supply at pin VCC in active supply mode or by supply harvested from RF field in passive mode. The pin VCC_CB is buffering the regulator input voltage by e.g. external capacitor. This is especially required in passive mode , when the RF field is low caused by NFC carrier modulation.

All chip internal supply domains, except the H-Bridge driver supply domain, are sourced by a dedicated internal voltage regulators.

The following figure gives an overview about the assignment of functions to power supply domains:

3 NAC1080/ NAC 1081 Functional Description

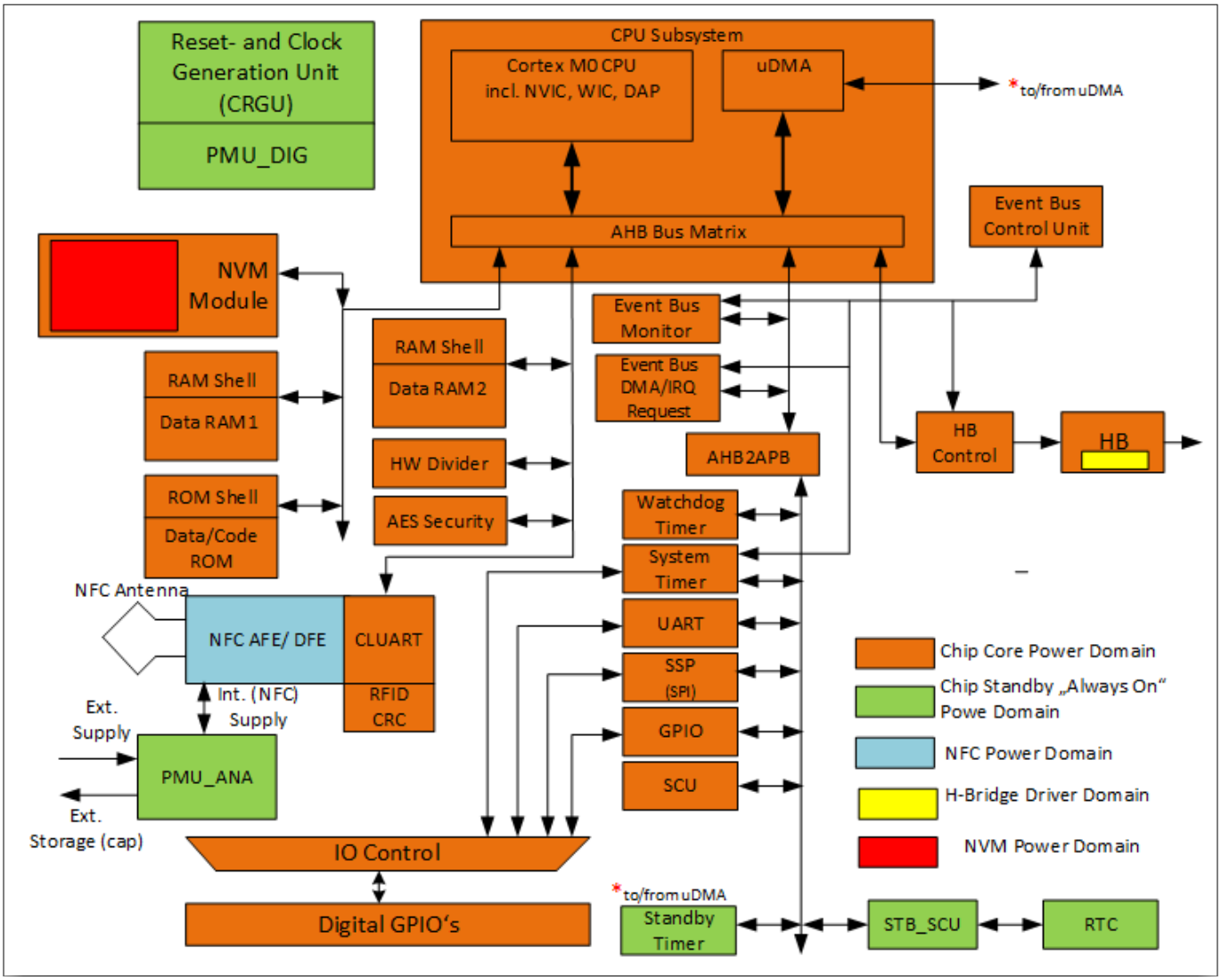

Figure 4 NAC1080/ NAC1081 Power Domains

The device is operating in two supply modes:

- operating mode
- power save mode

In power saving modes major parts of the device is switched off.

Table 2 Power Mode

	Power Save Mode	Operation Mode
Standby Power Domain	ON	ON
Core Power Domain	OFF	ON
NFC Power Domain	ON, if NFC field is present. Otherwise OFF	ON, if NFC field is present. Otherwise OFF
I/O Power Domain	OFF	ON
NVM Power Domain	OFF	Power State controlled by CPU. (Default: ON)

(table continues...)

Table 2 (continued) Power Mode

	Power Save Mode	Operation Mode
H-Bridge Power Domain	OFF	ON
Main Clock Oscillator	OFF	ON
Standby Clock Oscillator	ON	ON

After applying external supply (or RF field in passive mode) the device will enter the operation mode. The CPU software can request a transition into power save mode to the power management. The power management will serve this request and performn the transition into power save mode. The CPU software will configure and enable the desired wake up condition(s) to leave the power save mode and to re-enter operating mode. Possible wake up conditions are:

- presence detection of a NFC field
- Valid logical level on the pin WAKE_UP present. The polarity of the desired wake up level can be configured by CPU.
- Standby Timer Expired. The standby timer unit can be enabled, to trigger a wake up event after a configured number of slow oscillator clock ticks are counted. The counting of slow clock ticks will start after power save mode is entered.

In operating mode the system can enter a sleep mode state. The sleep mode will be entered, if the CPU is executing a *WFI (Wait For Interrupt)* or *WFE (Wait for Event)* instruction. The sleep mode is left, if an interrupt occurs. In sleep mode the clock of the CPU and memories is gated. Functional peripheral clocks are available. The clock gating of the CPU and memories provides a significant power save measure in operating mode. The fast clock of the system can be scaled as well by CPU software.

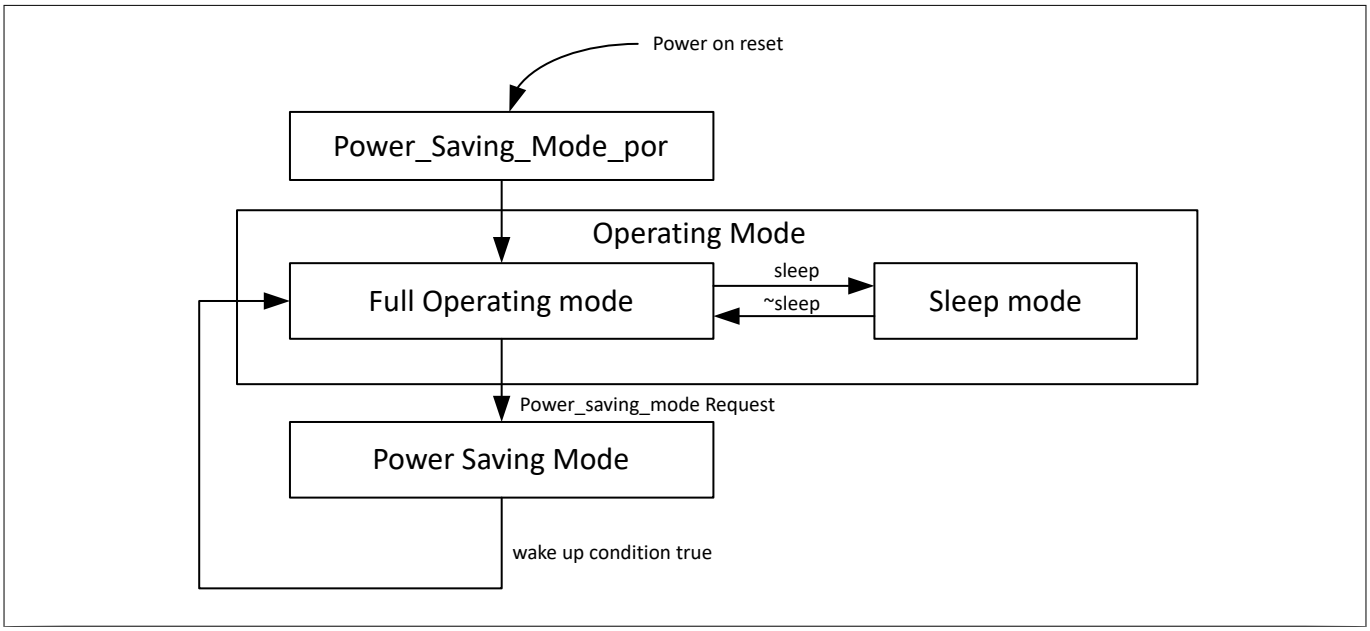

Figure 5 Power Management States

3.3 NAC1080/ NAC1081 Near Fields Communication

NAC1080/ NAC1081 supports Near Field Communication according to standard ISO/ IEC 14443 Type A (PICC).

A data Rate of 106 kBit/s is supported.

The device includes a transceiver, which processes the physical layer and parts of link layer function of near field communication. The upper layers of communication are processed in software. The NFC protocol stack is part of the ROM system library.

The NFC communication link initialization and anti collision is fully compliant to the PICC initialization Type A procedure as defined in standard ISO-14443-3. NAC1080 is using a fixed unique RFID UID with length of 7 bytes. NAC-1080 is using proprietary protocol state with proprietary protocol commands.

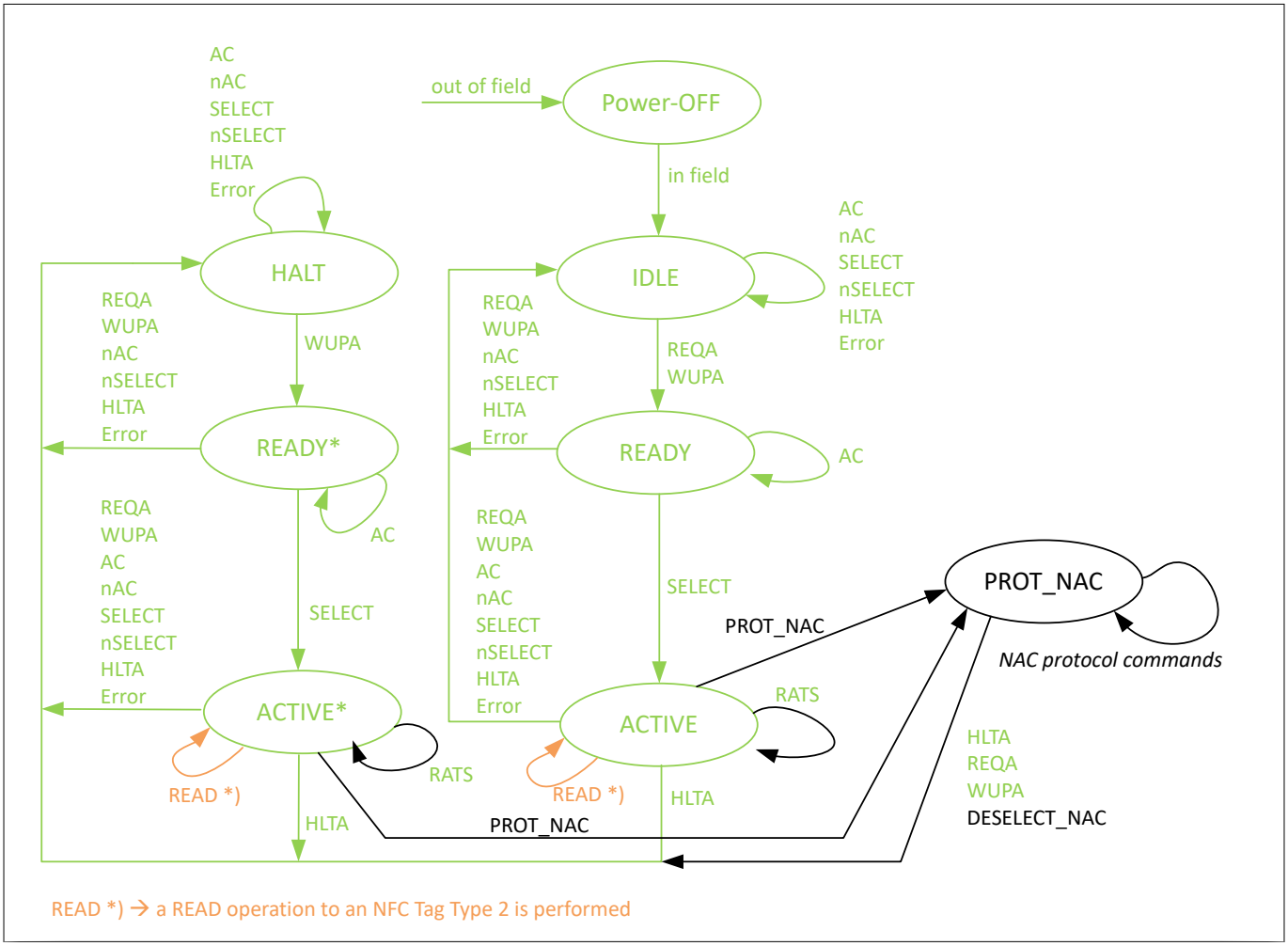

Figure 6 NAC1080/ NAC1081 PICC states

The states and transition drawn in *green* are according to ISO14443-3. The transitions and states are drawn in *black* are proprietary. The transition into the proprietary protocol state is triggered in *ACTIVE/ ACTIVE** state as the standard requires.

In protocol state *PROT_NAC* the NAC1080/ NAC1081 is able to react on external requests. Following types of requests are possible:

- Read/ Write Access to CPU address space.
  - A read/ write request to CPU address space is only granted, if the access to the specific address is authorized.
- Message Request
  - A message request will call a defined function of the ROM

- Call a CPU subprogram
  - A call of subprogram request will call an application specific subprogram located in the NVM
- Far End Loop back Test
  - NAC1080 will loop back received payload data of a loop back request frame.

In *ACTIVE/ ACTIVE** state the NAC1080/ NAC1081 accepts a NFC tag *READ* command. Using that command, a reserved area within the NVM can be read, which is considered to be compliant to an NFC tag type 2.

3.4 NAC1080/ NAC1081 H-Bridge

The H-Bridge provides an on chip interface to control an external actuation element, like an electrical motor. The H-Bridge driver is suitable to switch voltages up to 3.6V at a peak current of up to 250 mA.

A simplified functional diagram describes the H-bridge driver function.

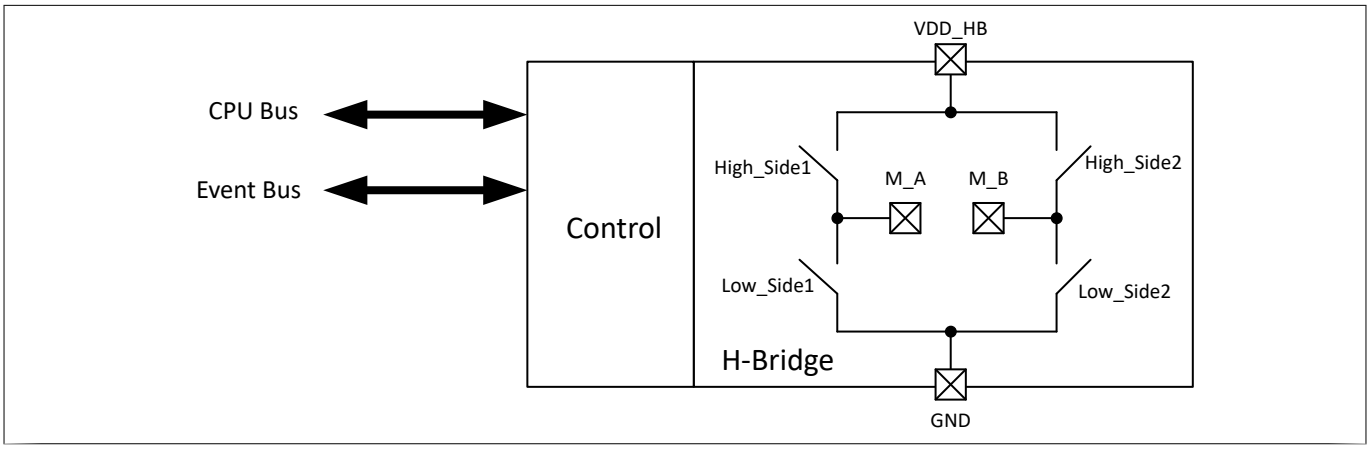

Figure 7 H-Bridge simplified functional view

Basically the H-bridge consists of 4 switching transistors, which are individually controlled by the CPU via the CPU bus or the event bus. An external load (e.g. a motor) will be connected to the pins M_A and M_B. In case the switches *High_Side1* and *Low_Side2* are closed and the other two switches are open, then a current will flow from *VDD_HB* via pin *M_A* to pin*M_B* to *GND*. In case *High_side2* and *Low_side1* are closed and the other two switches are open, the current will flow from pin *M_B* to pin *M_A*.

The system ROM library contains driver functions to configure and control the H-bridge.

3.5 NAC1080/ NAC1081 Security Support

NAC1080/ NAC1081 supports two security features by hardware:

- AES encryption and decryption
- True Random Number Generation

The AES accelerator hardware supports encryption and decryption operations with key length of 128-bit. The accelerator hardware encrypts or decrypts a 128-bit data gram within 16 clock cycles.

The True Random Number Generator generates a sequence of 128 random bits within 5 microseconds.

The system ROM library contains security driver functions to calculate the result of a data encryption or decryption operations and to generate a random number.

3.6 NAC1080/ NAC1081 System Timer Unit

The system timer unit consists of 6 independent programmable timer channels (16-bit).

A timer can operate in :

- continuous mode
- single shot mode

The timer per

If a timer expires, an IRQ request could be generated or an event could be sent to the event bus.

A timer can be started by CPU software access or by receiving an timer start event on the event bus.

System timer channels can be chained, in order to increase the timer length up to maximum 96 bit.

The system ROM library contains the necessary functions to configure and control the system timer unit.

3.7 NAC1080/ NAC1081 General Purpose Input/ Outputs

General Purpose Input and Outputs are bidirectional input/ output structures.

The output state of a GPIO can be set by the Cortex-M0 CPU. The input state of a GPIO can be read by the Cortex-M0 CPU.

Beside to the CPU read/write access to the GPIO, alternate port functions can be enabled . An alternate port function connects the GPIO port to the input or output of an internal hardware peripheral (e.g. to connect a selected GPIO to the TxD of UART).

A GPIO port consists of:

- input stage
- output driver
- internal Pull Up resistor
- internal Pull Down resistor

The input stage can be enabled or disabled by CPU software. In case of disabled input stage, the CPU will always read a logic *HIGH* level. The output driver can be enabled or disabled by CPU software or controlled by an alternate function control signal, if an alternate function is selected. The internal pull up resistor can be enabled or disabled by CPU software. The internal pull down resistor can be enabled or disabled by CPU software. The output characteristic can be set by CPU software to CMOS Push-Pull output or Open Drain output.

The system ROM library contains the required functions to configure and control the GPIOs and to select alternate port functions.

Table 3 Alternate GPIO Functions

	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6
Primary Output	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6
Alternate Output 1	SPI TxD	SPI Clock Out		SPI Frame Sync Out			Debugger Data
Alternate Output 2	UART TxD		UART TxD	reserved	reserved	reserved	reserved
Alternate Output 3	PWM Out	PWM Out	PWM Out	reserved	reserved	reserved	reserved
Primary Input	IN0	IN1	IN2	IN3	IN4	IN5	IN6
Alternate Input 1			SPI RxD		SPI CLKIN	SPI Frame Sync In	Debugger Data
Alternate Input 2	UART RxD		UART RxD			Debugger Clock	
Alternate Input 3	reserved	reserved	reserved	reserved	reserved	reserved	reserved

3.8 NAC1080/ NAC1081 SPI Controller Peripheral

The SPI controller peripheral provides compatibility to following interface types :

- Motorola SPI

- Texas instruments serial synchronous interface (SSI)
- National Semiconductor micro-wire interface

It can operate in master or in slave mode.

It contains a receive FIFO buffer and a transmit FIFO buffer, of eight entries of 16 bit width.

When operating in SPI mode, frame sizes of 4 to 16 bit are supported. It provides a full duplex synchronous data transfer utilizing 4 wires. Clock polarity and clock phase are programmable.

The SPI signals can be mapped to general purpose IOs using alternate input and output functions.

3.9 NAC1080/ NAC1081 UART

The product contains an UART transceiver peripheral.

Following features are included:

- full duplex capable UART
- Separate 32x8 transmit and 32x12 receive First-In, First-Out memory buffers (FIFOs) to reduce CPU interrupts.
- Programmable baud rate generator
- Programmable line characteristics:
  - one or two STOP bits
  - support of 5, 6, 7 or 8 data bits
  - even, odd, stick, or no-parity bit generation and detection

Start-bit, stop-bit and parity-bit are added prior to transmission within the transceiver in transmit direction and processed and removed in receive direction.

The UART ports can be mapped to general purpose IOs using alternate input and output functions.

The product does not support the modem control functions like CTS, RTS etc .

4 NAC1080/ NAC1081 Electrical Characteristics

Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input peak voltage between LA-LB	V_{Inpeak}			3.6	V_{Peak}	
Absolute Maximum Field Strength for indefinite exposure without damage. The chip functionality can be affected.	H_{absmax}			10	A/m	
Absolute Maximum Field Strength for exposure for up to 10 seconds without damage. The chip is not guaranteed to function	$H_{absmax12}$			12	A/m	Conditions: $T_{joperating}$ = 110°C
Input peak voltage at VCC, VCC_HB, VCC_CB	V_{CC}, V_{CC_HB}, V_{CC_CB}	0		3.6	V	
electrostatic discharge voltage Human Body model	V_{ESD_HB}			2	kV	ANSI/ESDA/JEDEC JS-001
electrostatic discharge voltage charged device model	V_{ESD_CDM}			500	V	ANSI/ESDA/JEDEC JS-002
Storage Temperature	$T_{Storage}$	-40		125	°C	
Operating Temperature	$T_{Ambient}$	-40		85	°C	Ambient temperature range, where device is operating. The operation in NFC system requires a NFC reader, which is operational within the $T_{Ambient}$ temperature range. All external system components need to support the full $T_{Ambient}$ range, if the full $T_{Ambient}$ range is used.

4 NAC1080/ NAC1081 Electrical Characteristics

Table 5 static characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The static parameters are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Supply Pins						
Supply Voltage	V_{CC}, V_{CC_HB}, V_{CC_CB}	2.8	3.0	3.3	V	
Supply Current	I_{CC}			5	mA	average value and operating mode dependent, CPU running at 27 MHz, NVM access enabled
Power Down Mode Supply Current	I_{CC_PD}		30		uA	Chip is in Power Down Mode and wait for Wake Up Event, RTC and Standby Timer active
GPIO Pins						
HIGH Level input Voltage	V_{IH}	1.75		3.6	V	
LOW Level input Voltage	V_{IL}	0		0.7	V	
HIGH Level Output Voltage	V_{OH}	2.2			V	load 1mA
Low Level Output Voltage	V_{OL}			0.2	V	load 1mA
Pull-Up Resistance	R_{PU}		200		kOhm	
Pull-Down Resistance	R_{PD}		200		kOhm	
Wake-Up Pin						
Wake Up Threshold HIGH Level	V_{WU_HIGH}	2			V	
Wake Up Threshold Low Level	V_{WU_LOW}			0.4	V	
Antenna Pins						
Resonance Capacitance between terminals LA and LB	C_{Chip}		23.5		pF	

Table 6 NVM characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The NVM are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Program/ Erase Cycles	NC	500k				Every Page, T =27°C

(table continues...)

Table 6 (continued) NVM characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Data Retention after 100 cycles	DR	15			a	

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The Dynamic characteristics are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
GPIO Pins						
Rise Time (output)	t_R	2		7	ns	capacitive load of 50pF
Fall Time (output)	t_F	2		7	ns	capacitive load of 50pF
Wake Up Pin						
Input Slope Low to High	t_{LH}	2		10	ns	
Input Slope High to Low	t_{HL}	2		10	ns	

Table 8 H-Bridge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The H_bridge characteristics are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Current between M_A and M_B	I_{HB}			250	mA	
Voltage at VCC_HB	VDDHB		3	3.6	V	VDDHB shall be smaller or equal to the voltage at pin VCC_CB. In passive supply mode this is guaranteed by chip internal control. In active supply mode pins VCC, VCC_HB, VCC_CB might be connected to the same supply source.

5 NAC1080/ NAC1081 Package Outline

NAC1080 is offered in PG-DSO-16 package. The geometry is provided in the subsequent figure.

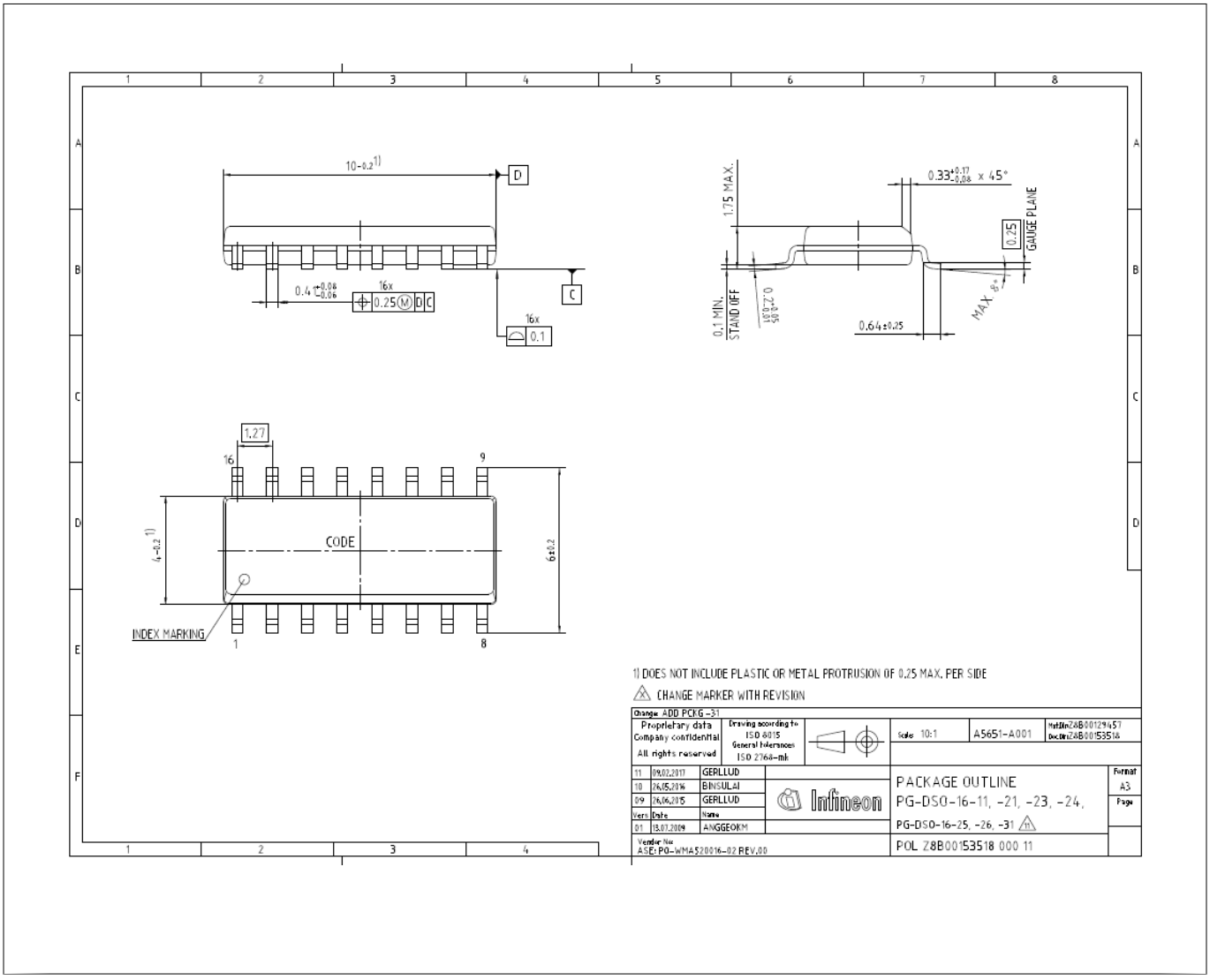

Figure 8 PG-DSO-16 Package Specification

NAC1081 is offered in PG-VQFN-32 package. The geometry is provided in the subsequent figure.

5 NAC1080/ NAC1081 Package Outline

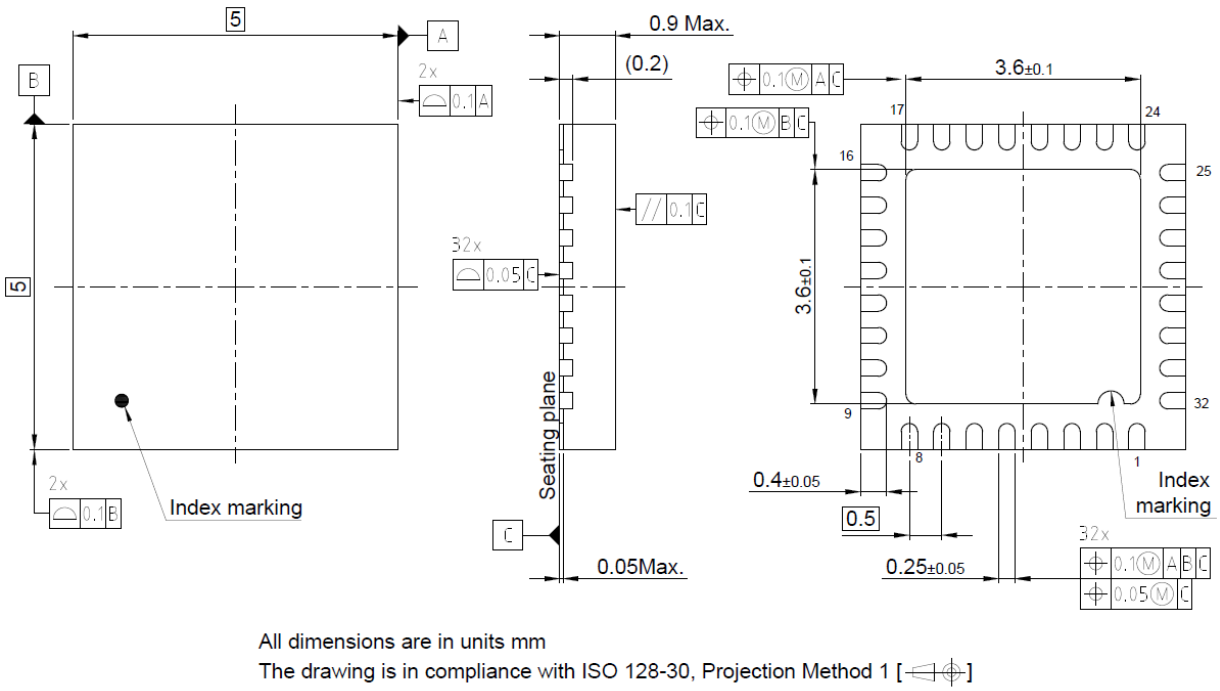

Figure 9 PG-VQFN-32 Package Specification

Revision history

Document version	Date of release	Description of changes
0.9	02-01-2021	• initial internal draft
1.0	12-01-2021	• initial release
1.1	05-30-2021	change recommendation of external capacitor at pin VCC_CB
1.2	01-11-2023	add Package Variant NAC1081
1.3	07-19-2023	add operating temperature range to Electrical Characteristics

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