

# ISOFACE™

## ISO2H823V2.5

### Overview

The 2nd generation of Infineon Technologies ISOFACE™ 8-channel high-side driver IC ISO2H823V2.5 offers a 2.5 kV galvanic isolation meeting the IEC 61131-2 requirements for reinforced isolation. Concurrently, the ISO2H823V2.5 sets a new standard for system-level diagnostics: each of the 8 channels is equipped with a 5-fold diagnostic monitoring capability: open load in active mode (channel “ON”), open load in inactive mode (channel “OFF”), short-circuit to V<sub>bb</sub>, short-circuit to GND and overtemperature.

With the ever increasing level of complexity and integration in industrial control systems comprehensive diagnostic monitoring is highly valuable in a vast range of industrial applications, both for preventive maintenance as well as to shorten or avoid costly un-scheduled down-times.



PG-VQFN-70

### Product Highlights

- 2.5 kV galvanic isolation integrated (UL508 & CSA22.2 certified) meeting IEC 61131-2 requirements for reinforced isolation
- 8 channel protected high-side switch with nominal current up to 600 mA per channel and 150 mΩ typ R<sub>ON</sub> (25°C)
- Comprehensive diagnostic feedback for each channel
- µController compatible 8-bit parallel/serial interface
- 12 mm x 12 mm PG-VQFN-70 package

### Key Features

- Interface 3.3 V CMOS operation compatible
- Parallel/Serial µC interface
- High common mode transient immunity
- Integrated diagnostics:
  - 5-fold diagnostic feedback per output channel: Open load in “ON”- and “OFF”-state, short circuit-to GND and short-circuit to supply, overtemperature
  - 5-fold diagnostic feedback in addition reported on global level
- Common output disable pin
- Common error indication pin
- Resynchronization to achieve low jitter when switching the high-side switch ON and OFF
- Active output current limitation for short circuit protection
- Reverse Output Voltage protection
- Undervoltage shutdown with auto-restart and hysteresis
- Integrated clamping to switch inductive loads up to 150 mJ energy per channel
- Thermal shutdown and diagnostics per channel with auto-restart
- V<sub>BB</sub> range from 11 V to 35 V designed for 24 V systems

Type	Package
ISO2H823V2.5	PG-VQFN-70

- ESD protection
- RoHS compliant

## Overview

### Typical Application

- Isolated switch for industrial applications:  
PLC, distributed control systems, industrial PCs, robotics, etc.
- All types of resistive, inductive and capacitive loads
- $\mu$ Controller compatible power switch for 24 V DC applications
- Driver for solenoid, relays and resistive loads

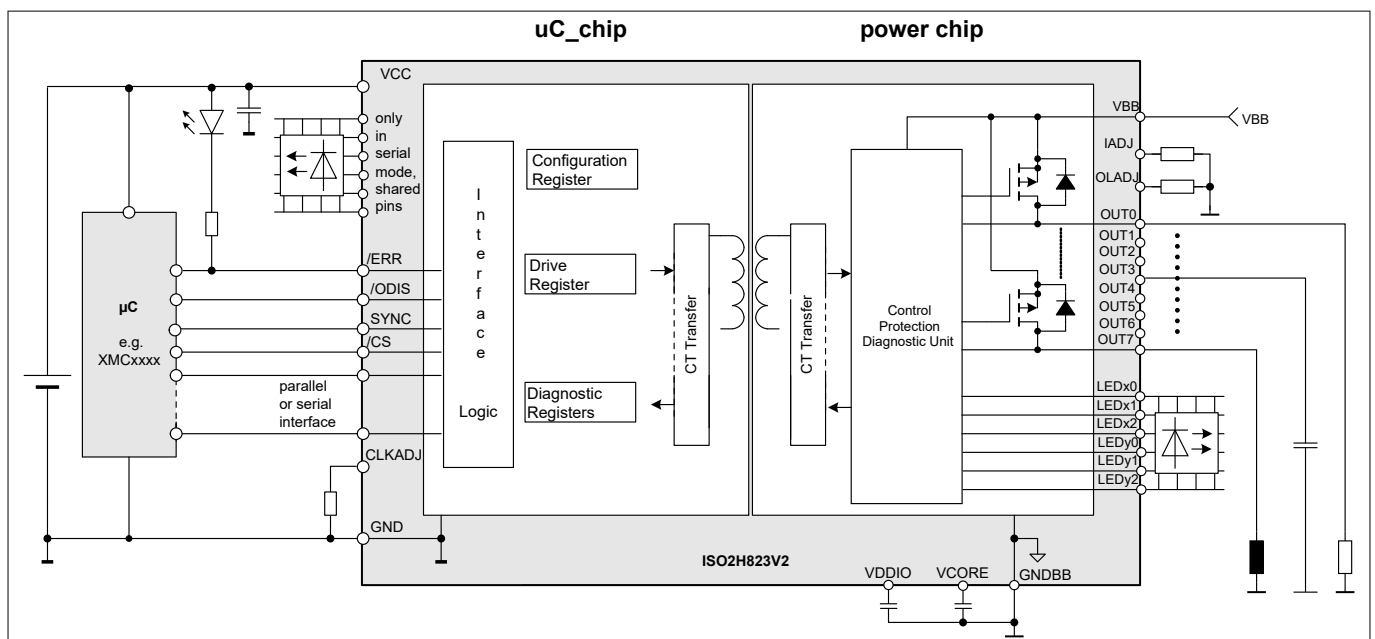
### Description

The ISO2H823V2.5 is a galvanically isolated 8-bit data interface in PG-VQFN-70 package that provides 8 fully protected high-side power switches that are able to handle currents up to 730 mA per channel.

An 8-bit parallel  $\mu$ Controller compatible interface or a serial SPI-interface allows to connect the IC directly to a  $\mu$ Controller system. The input interface supports also a direct control mode for writing driver information and is designed to operate with 3.3 V CMOS compatible levels.

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

This product is the second generation of isolated 8 channel digital output device (ISO2H823V2.5) and provides a robust integrated diagnosis for switches with low  $R_{ON}$  as well as an upgraded  $\mu$ Controller interface.



**Figure 1** Typical Application

### Infineon Ordering Code :

SP001225470

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## 1 Pin configuration and functionality



Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl <i>1)</i>	Type <i>2)</i>	Function	Symbol	Ctrl	Type	Function
top side pins								
1	<i>GNDBB</i>		A	Output Stage Ground	<i>GNDBB</i>			
2	<i>VBB</i>		A	Output Stage Positive Supply	<i>VBB</i>			
3	<i>VBB</i>		A	Output Stage Positive Supply	<i>VBB</i>			
4	<i>OUT6</i>		A	Switch Output 6	<i>OUT6</i>			
5	<i>OUT6</i>		A	Switch Output 6	<i>OUT6</i>			

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## 1 Pin configuration and functionality

**Table 1** (continued) Pin configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl <sup>1)</sup>	Type <sup>2)</sup>	Function	Symbol	Ctrl	Type	Function
6	VBB		A	Output Stage Positive Supply	VBB			
7	OUT5		A	Switch Output 5	OUT5			
8	OUT5		A	Switch Output 5	OUT5			
9	OUT4		A	Switch Output 4	OUT4			
10	OUT4		A	Switch Output 4	OUT4			
11	VBB		A	Output Stage Positive Supply	VBB			
12	VBB		A	Output Stage Positive Supply	VBB			
13	OUT3		A	Switch Output 3	OUT3			
14	OUT3		A	Switch Output 3	OUT3			
15	OUT2		A	Switch Output 2	OUT2			
16	OUT2		A	Switch Output 2	OUT2			
17	VBB		A	Output Stage Positive Supply	VBB			
18	OUT1		A	Switch Output 1	OUT1			
19	OUT1		A	Switch Output 1	OUT1			
20	VBB		A	Output Stage Positive Supply	VBB			
21	VBB		A	Output Stage Positive Supply	VBB			
22	GNDBB		A	Output Stage Ground	GNDBB			
23	n.c.	not connected			n.c.	not connected		
24	OUT0		A	Switch Output 0	OUT0			
25	OUT0		A	Switch Output 0	OUT0			
26	VBB		A	Output Stage Positive Supply, Supply of Reference Voltages	VBB			
27	GNDBB		A	Output Stage Ground	GNDBB			
28	OLADJ		A	Open Load Adjust	OLADJ			
29	IADJ		A	Current Reference Adjust	IADJ			
30	VDDIO		A	CT Blocking Capacitor	VDDIO			
31	VCORE		A	Digital Core Supply	VCORE			

(table continues...)

**1 Pin configuration and functionality**
**Table 1 (continued) Pin configuration**

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl 1)	Type 2)	Function	Symbol	Ctrl	Type	Function
32	<i>GNDBB</i>		A	Output Stage Ground	<i>GNDBB</i>			
gap used for creepage distance								
33	<i>GND</i>		A	Logic Ground	<i>GND</i>			
34	<i>GND</i>		A	Logic Ground	<i>GND</i>			
35	<i>GND</i>		A	Logic Ground	<i>GND</i>			
36	<i>SEL</i>	I	PD	Serial / Parallel Mode Select	<i>SEL</i>			
37	<i>VCC</i>		A	Positive 3.3 V logic supply	<i>VCC</i>			
38	<i>CLKADJ</i>		A	Clock Frequency Adjustment	<i>CLKADJ</i>			
39	<i>GND</i>		A	Logic Ground	<i>GND</i>			
40	<i>ODIS</i>	I	PD	Output Disable	<i>ODIS</i>			
41	<i>SYNC</i>	I	PU	Synchronize and Freeze Diagnostics	<i>SYNC</i>			
42	<i>WR</i>	I	PU	Data Write Input	n.c.			high impedance "Z"
43	<i>ALE/RST</i>	I	PD	Address Latch Enable / Reset	<i>RST</i>	I	PD	Reset
44	<i>RD</i>	I	PU	Data Read Input	<i>MS0</i>	I	PD	SPI Mode Select bit 0
45	n.c.			not connected	<i>MS1</i>	I	PD	SPI Mode Select bit 1
46	<i>GND</i>		A	Logic Ground	<i>GND</i>			
47	<i>GND</i>		A	Logic Ground	<i>GND</i>			
48	<i>CS</i>	I	PU	Chip Select	<i>CS</i>			
49	<i>AD0</i>	IO	PPZ	Addr-Data in/output bit0	<i>SDI</i>	I	PD	SPI Data input
50	<i>AD1</i>	IO	PPZ	Addr-Data in/output bit1	n.c.			high impedance "Z"
51	<i>AD2</i>	IO	PPZ	Addr-Data in/output bit2	n.c.			high impedance "Z"
52	<i>AD3</i>	IO	PPZ	Addr-Data in/output bit3	n.c.			high impedance "Z"
53	<i>AD4</i>	IO	PPZ	Addr-Data in/output bit4	<i>CRCERR</i>	OD	PU	CRC Error output
54	<i>AD5</i>	IO	PPZ	Addr-Data in/output bit5	<i>SCLK</i>	I	PD	SPI Shift Clock input
55	<i>AD6</i>	IO	PPZ	Addr-Data in/output bit6	n.c.			high impedance "Z"
56	<i>AD7</i>	IO	PPZ	Addr-Data in/output bit7	<i>SDO</i>	O	PPZ	SPI Data Output
57	<i>ERR</i>	OD	PU	Fault indication	<i>ERR</i>			

**(table continues...)**

## 1 Pin configuration and functionality

**Table 1** (continued) Pin configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl <sup>1)</sup>	Type <sup>2)</sup>	Function	Symbol	Ctrl	Type	Function
58	GND		A	Logic Ground	GND			
59	GND		A	Logic Ground	GND			
60	GND		A	Logic Ground	GND			
gap used for creepage distance								
61	GNDBB		A	Output Stage Ground	GNDBB			
62	LEDX0		A	LED Output Row 0	LEDX0			
63	LEDX1		A	LED Output Row 1	LEDX1			
64	LEDX2		A	LED Output Row 2	LEDX2			
65	LEDY0		A	LED Output Column 0	LEDY0			
66	LEDY1		A	LED Output Column 1	LEDY1			
67	LEDY2		A	LED Output Column 2	LEDY2			
68	OUT7		A	Switch Output 7	OUT7			
69	OUT7		A	Switch Output 7	OUT7			
70	n.c.	not connected			n.c.	not connected		

1) Direction of the digital pins : I = input, O = output, IO = Input/Output

2) Type of the pin: A = analog, OD = Open-Drain, PU = internal Pull-Up resistor, PD = internal Pull-Down resistor, PPZ = Push-Pull pin with High-Impedance functionality

In case of serial mode six pins can be used to drive a LED-matrix on the uC-side (Table 2). For this purpose the bit LEDON in register GLCFG has to be set to "1".

**Table 2** Pin Configuration for LED-Application on the uC-Side

Pin	Serial Interface Mode			
	Symbol	Ctrl	Type	Function
top side pins				
55	AD6		OD	LEDR0
52	AD3		OD	LEDR1
51	AD2		OD	LEDR2
42	WR		OD	LEDC0
43	ALE/RST		OD	LEDC1
50	AD1		OD	LEDC2



## 1 Pin configuration and functionality

### 1.1 Pin functionality

This section describes the pins of the  $\mu$ Controller Interface as well as the Process Interface.

#### 1.1.1 Pins of power interface

##### VBB (Positive supply 11-35 V output stage)

$V_{BB}$  supplies the output stage. An external circuitry for reverse polarity protection is required (see Electrical Characteristics).

A ceramic capacitor of minimum 2.2  $\mu$ F must be connected between VBB and GNDBB.

##### GNDBB (Ground for VBB domain)

This pin acts as the ground reference for the output stage that is supplied by  $V_{BB}$ .

##### OUT0... OUT7 (Output channel 0 ... 7)

Due to EMI-requirements (Radio-Frequency-Common-Mode and burst-application) a capacitor of min.10 nF ( $\pm 10\%$ , recommended value 12 nF  $\pm 10\%$ ) for each output pin has to be connected to GNDBB.

##### LEDx0,1,2 (LED Row output channel 0,1,2)

Low side switches

##### LEDy0,1,2 (LED Column output channel 0,1,2)

High side drivers

##### IADJ (Current Adjust)

Reference current input, must be connected to GNDBB through a reference resistor of typ. 6.81 K $\Omega$  (E96 series). The DC-level  $V_{IADJ}$  is 1.215 V.

##### OLADJ (Open Load Adjust)

The current for the Open load detection can be adjusted by connecting a resistor between this pin and GNDBB (from the E96 series : 25 k $\Omega$  - 2.3 k $\Omega$ ). The DC-level  $V_{OLADJ}$  is 1.215 V.

##### VDDIO (3.3 V Supply Blocking Capacitor)

A 1  $\mu$ F ceramic capacitor must be connected between VDDIO and GNDBB.

##### VCORE (Blocking Capacitor for 1.5 V Digital Core)

A 470 nF ceramic capacitor must be connected between VCORE and GNDBB.

#### 1.1.2 Pins of serial and parallel logic interface

Some pins are common for both interface types, some others are specific for the parallel or serial access.

##### VCC (Positive 3.3 V logic supply)

$V_{CC}$  supplies the output interface that is electrically isolated from the output power stage. The interface can be supplied with 3.3 V. A ceramic capacitor of minimum 2.2  $\mu$ F must be connected between VCC and GND.

## 1 Pin configuration and functionality

### GND (Ground for VCC domain)

This pin acts as the ground reference for the uC-interface that is supplied by  $V_{CC}$ .

### CLKADJ (Clock Adjust)

A high precision resistor of 10 K $\Omega$  has to be connected between CLKADJ and GND. The DC-level  $V_{CLKADJ}$  is 0.5 V.

### $\overline{ERR}$ (Fault Indication)

The low active  $\overline{ERR}$  signal contains the OR-wired diagnostic information depending on chosen serial or parallel mode (VBB undervoltage or missing voltage detection, the internal data transmission failure detection unit and the fault(s) of the output switch). The output pin  $\overline{ERR}$  provides an open drain functionality. This pin has an internal Pull-Up resistor. In normal operation the signal  $\overline{ERR}$  is high.

### $\overline{ODIS}$ (Output Disable)

The low active  $\overline{ODIS}$  signal immediately switches off the output channels OUT0-OUT7. This pin has an internal Pull-Down resistor. In normal operation the signal  $\overline{ODIS}$  is high. Setting  $\overline{ODIS}$  to Low clears the **DRIVE** register as well. The minimum width of the  $\overline{ODIS}$  signal is 5  $\mu$ s.

### SEL (Serial or Parallel Mode Select)

When this pin is in a logic Low state, the IC operates in Parallel Mode. For Serial Mode operation the pin has to be pulled into logic High state. During Start Up the IC is operating in Parallel Mode. This pin has an internal Pull-Down resistor and a 200 ns blanking time<sup>1)</sup>.

### SYNC

In isochronous mode (clock-sync-mode) the transfer of the latched output data register into the output-stages is controlled by the SYNC signal. When the SYNC-signal is in low state, the output-stage won't be updated any longer, the last value is frozen. With the rising edge of SYNC the information of the latched output data registers will be transferred to the output stages. It can be chosen by a configuration bit whether all the channel diagnostic bits will be latched into the DIAG channel register every data cycle or only when the SYNC-signal is in high state. In the last case when the SYNC-signal is in low state, the DIAG channel register wouldn't be updated any longer, the last value would be frozen. SYNC is also used for resynchronization of the data transmission with the target to achieve a low jitter. This pin has an internal Pull-Up resistor and a 20 ns blanking time<sup>1)</sup>.

### $\overline{CS}$ (Chip Select)

When this pin is in a logic Low state, the IC interface is enabled and data can be transferred. This pin has an internal Pull-Up resistor and a 20 ns blanking time<sup>1)</sup>.

When the  $\overline{CS}$  pin is held Low whereas the ALE pin is High for at least 100  $\mu$ s, the device is reset.

## The following pins are provided in the parallel interface mode

### AD7:AD0 (AddressData input / output bit7 ... bit0)

The pins AD0 .. AD7 are the bidirectional input / outputs for data write and read. Depending on the state of the ALE pin and the AD7 pin, register addresses or data can be transferred between the internal registers and e.g. the micro-controller. By connecting  $\overline{CS}$  and  $\overline{WR}$  and ALE/RST pins to GND and  $\overline{RD}$  to VCC, the parallel direct mode is activated.

<sup>1)</sup> the signal must be stable for the duration of the blanking time before it is accepted as valid

## 1 Pin configuration and functionality

### $\overline{WR}$ (Write)

By pulling this pin down, a write transaction is initiated on the AddressData bus and the data has to be valid on the rising edge of  $\overline{WR}$ . The AD7-bit of the register address has to be set to '1'. This pin has an internal Pull-Up resistor and a 20 ns blanking time<sup>1)</sup>.

### $\overline{RD}$ (Read)

By pulling this pin down, a read transaction is initiated on the AddressData bus and the data becomes valid on the rising edge of  $\overline{RD}$ . The AD7-bit of the register address has to be set to '0'. This pin has an internal Pull-Up resistor and a 20 ns blanking time<sup>1)</sup>.

### ALE (Address Latch Enable)/RST

The pin ALE is used to select between address (ALE is in a logic High state) or data (ALE is in a logic Low state). Furthermore, a read or write transaction can be selected with the  $\overline{RD}$  and  $\overline{WR}$  pin. When ALE is pulled high, address is transferred and latched over the bit AD0 to AD7. During the time interval where ALE = High  $\overline{RD}$  or  $\overline{WR}$  has to be pulled to High. During the Low State of ALE all transactions hit the same address. This pin has an internal Pull-Down resistor and a 20 ns blanking time<sup>1)</sup>. For the reset-function see comment under the item:  $\overline{CS}$ .

### The following pins are provided in the serial interface mode

#### MS0, MS1 (Serial Mode Select)

By driving these pins to Logic High or Low the Serial Interface Mode (number of bits - 8, 16, 24 - to be transferred, CRC) can be selected. These pins have both an internal Pull-Down resistor and a 200 ns blanking time<sup>1)</sup>.

#### SCLK (Serial Interface Shift Clock)

Input data are sampled with rising edge and output data are updated with the falling edge of this input clock signal. This pin has an internal Pull-Down resistor and a 20 ns blanking time<sup>1)</sup>.

#### SDI (Serial Interface Input Data)

SDI is put into a dedicated FIFO (clocked by SCLK) to program the DRIVE register and the internal address and the write data. This pin has an internal Pull-Down resistor and a 20 ns blanking time<sup>1)</sup>.

#### SDO (Serial Interface Data Output)

SDO provides the serial output data bits.

#### $\overline{CRCERR}$ (CRC Error Output)

This pin is in a logic Low state when CRC errors or Shift-Clock errors are detected internally. This pin has an open drain functionality and an internal Pull-Up resistor.

<sup>1)</sup> the signal must be stable for the duration of the blanking time before it is accepted as valid

## 2 Block diagram

### 2 Block diagram

The IC is divided into an uC\_chip and into a power chip due to the galvanical isolation. The uC\_chip contains the uC-interface and the power chip the power switches.

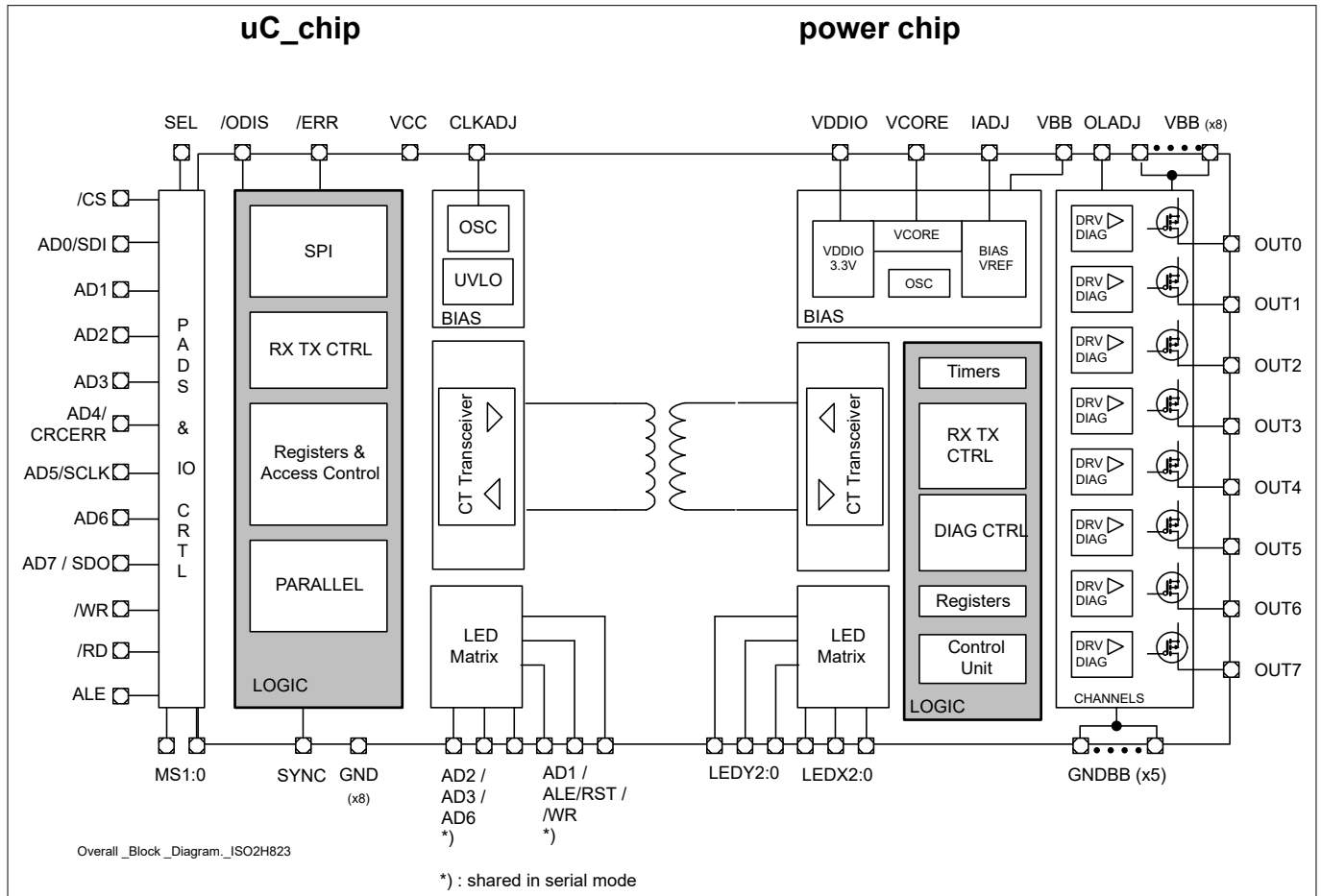


Figure 3 Block diagram

## 2 Block diagram

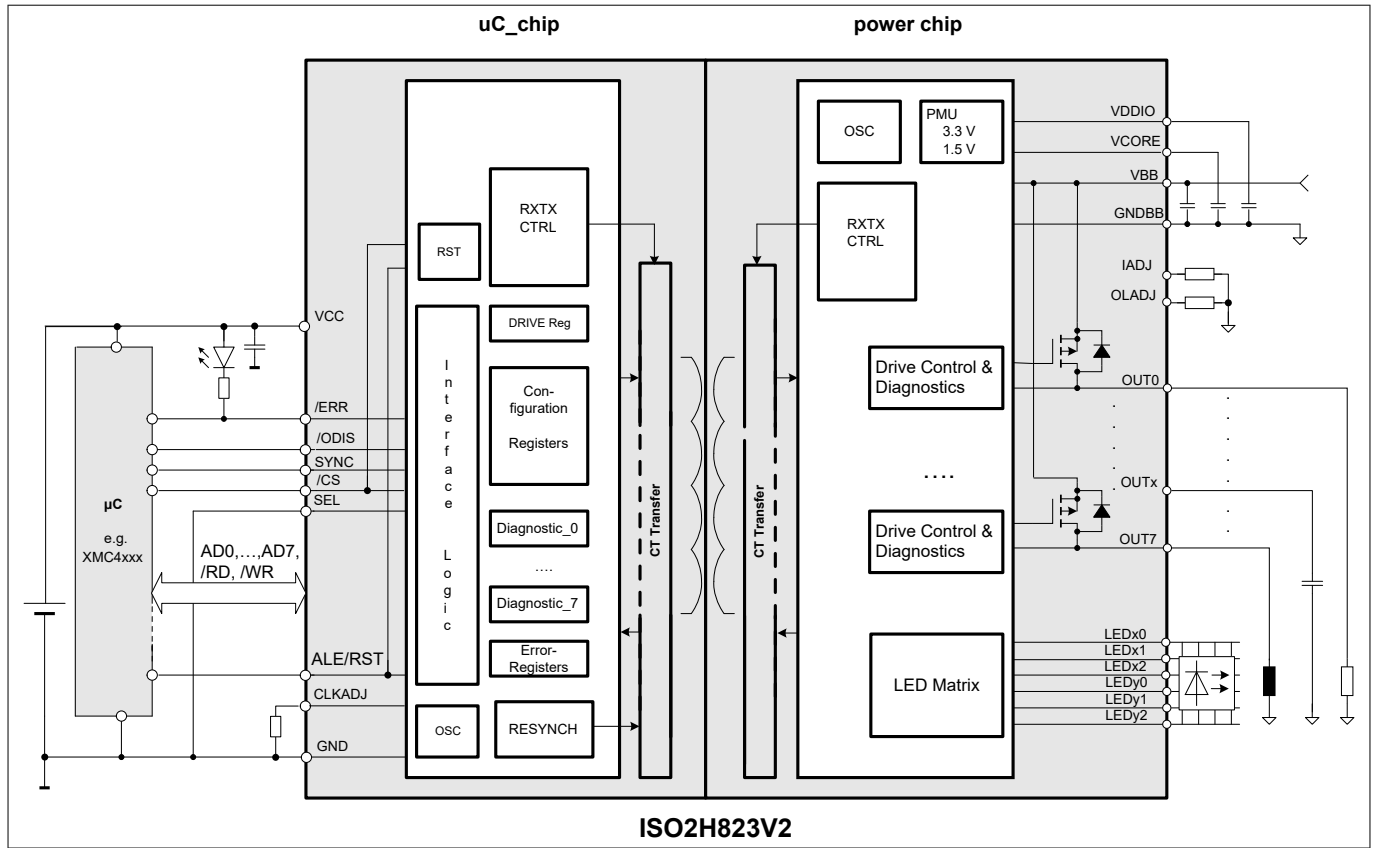


Figure 4 Application with parallel interface

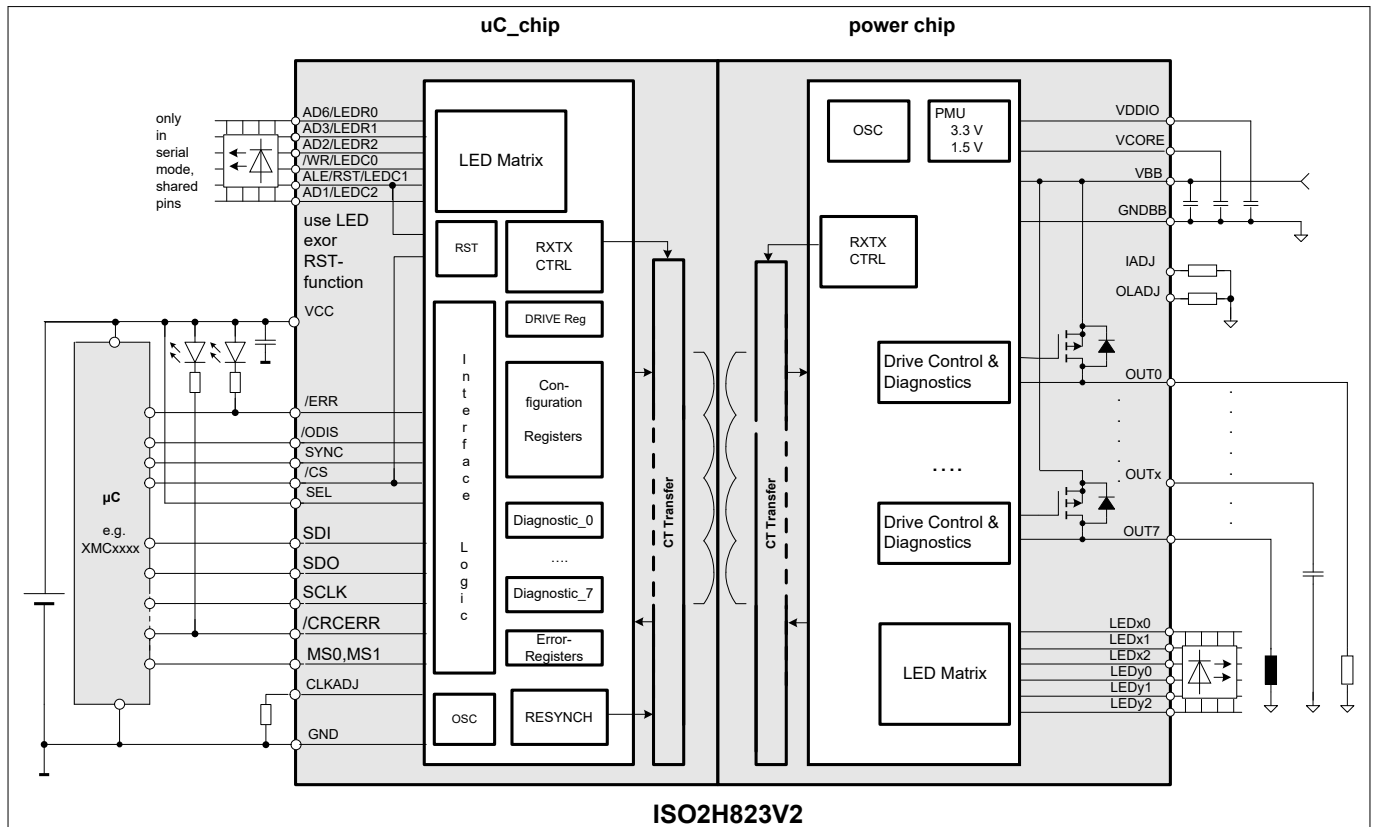


Figure 5 Application with serial interface

## 3 Functional description

### 3 Functional description

#### 3.1 Introduction

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface ( $\mu$ C-chip) is supplied at  $V_{CC}$  and the output stage (power chip) is supplied at  $V_{BB}$ . The different voltage domains can be switched on at different times. The output stage is only enabled once the input stage enters a stable state. The power chip generates out of  $V_{BB}$  two internal voltages  $V_{DDIO} = 3.3\text{ V}$  ( $\pm 10\%$ ) and  $V_{CORE} = 1.5\text{ V}$  ( $\pm 10\%$ ) which have to be buffered externally.

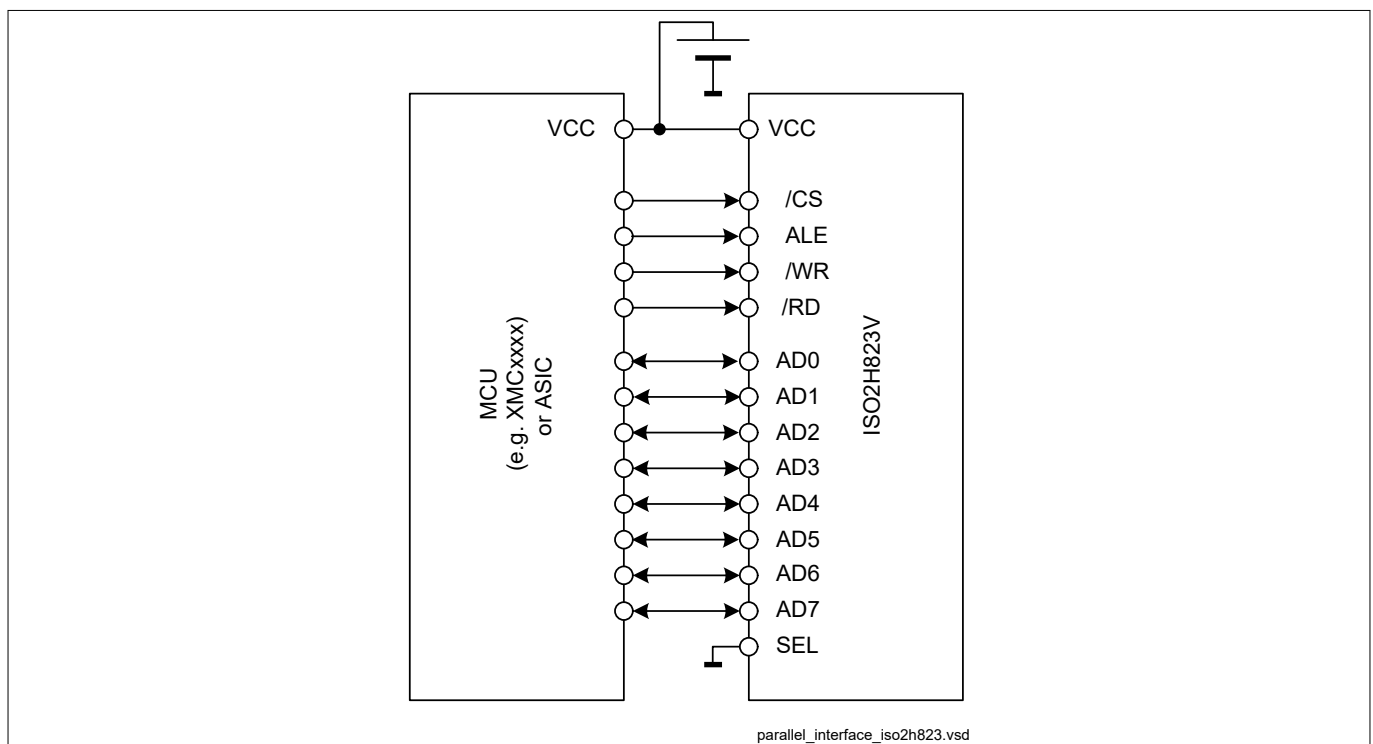
The ISOFACE™ ISO2H823V2.5 includes 8 high-side power switches that are controlled by means of the integrated parallel/serial interface. The interface is 8-bit  $\mu$ Controller compatible. Furthermore a direct control mode can be selected that allows the direct control of the outputs OUT0 ... OUT7 (power chip) by means of the inputs AD0 ... AD7 ( $\mu$ C-chip) without any additional logic signal. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The  $\mu$ Controller compatible interface allows a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against overload, overtemperature and against overvoltage by an active zener clamp.

#### 3.2 Microcontroller interface

The microcontroller interface can be configured as a parallel or serial interface via the SEL pin.

##### 3.2.1 Parallel interface mode

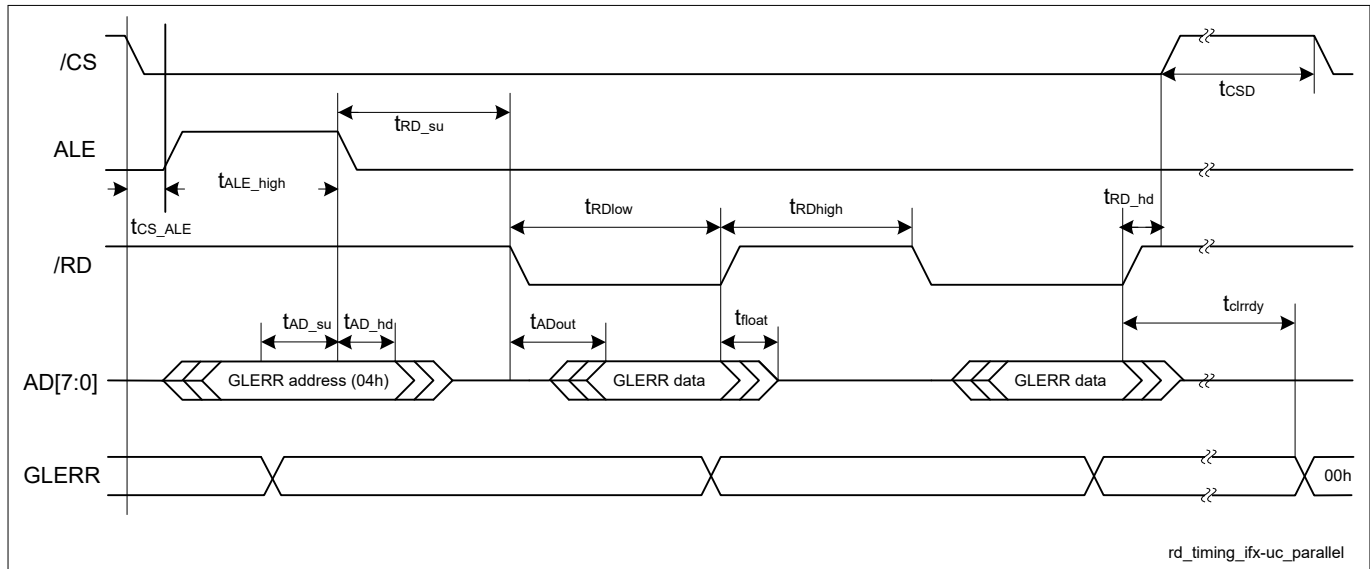
The ISO2H823V2.5 device contains a parallel interface that can be selected by pulling the SEL Pin to logic Low state. The interface can be directly controlled by the  $\mu$ Controller output ports (see Figure 6). The output pins AD7:AD0 are in state "Z" as long as  $\overline{CS} = 1$ ,  $\overline{RD} = 1$  and  $\overline{WR} = 1$ .



**Figure 6** Bus configuration for parallel mode

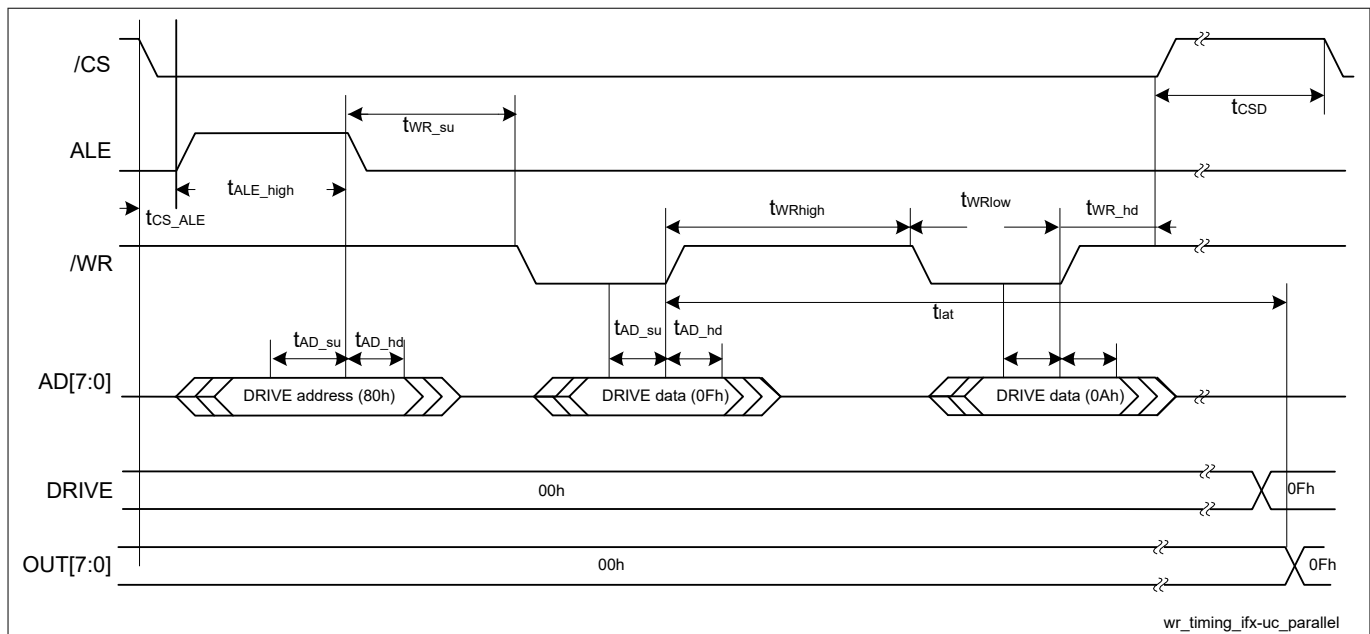
### 3 Functional description

The timing requirements for the parallel interface are shown in [Figure 7](#) (Read), [Figure 8](#) (Write) and [Table 23](#).



**Figure 7** Timing by parallel read access (e.g. [GLERR](#) register)

For a reading access to internal registers the MSB of the address register has to be set to “0”.



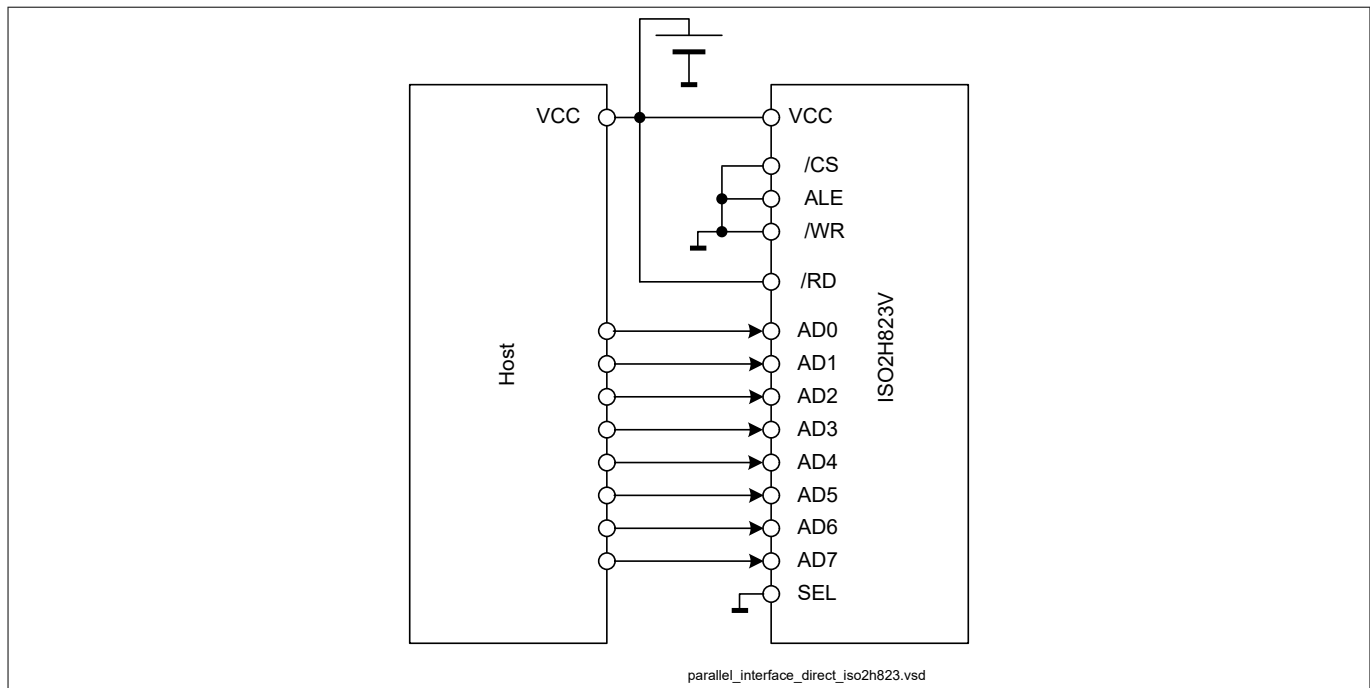
**Figure 8** Timing by parallel write access (e.g. [DRIVE](#) register)

For a writing access to internal registers the MSB of the address register has to be set to “1”.

#### 3.2.1.1 Parallel direct mode

The parallel interface can be also used in a direct mode that allows direct changes of the output OUT0...OUT7 by means of the corresponding inputs D0-D7 without additional logic signals. To activate the parallel direct mode  $\overline{CS}$ ,  $\overline{WR}$  and ALE pins have to be wired to ground and  $\overline{RD}$  has to be wired to VCC as shown in the [Figure 9](#). Although the diagnostics cannot be read in this operation mode, the faults as specified in [Table 3](#) are still reported at the  $\overline{ERR}$  pin (volatile).

### 3 Functional description



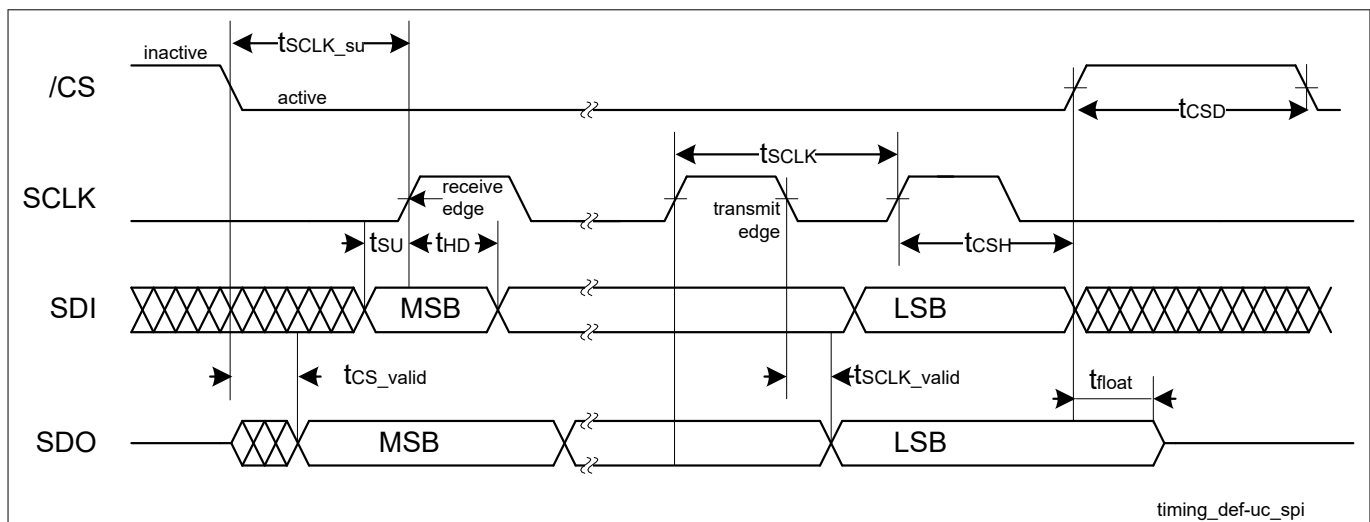
**Figure 9** Parallel direct mode

The direct mode is intended to be an additional parallel mode which is invoked directly after reset. In this case internal settings have already been realized (e.g. MSB of the address register is set to “1”).

#### 3.2.2 Serial interface mode

The ISO2H823V2.5 device contains a serial interface that can be activated by pulling the SEL pin to logic High state. The interface can be directly controlled by the  $\mu$ Controller output ports. The output pin SDO is in state “Z” as long as  $\overline{CS} = 1$ . Otherwise, the bits at the SDI input are sampled with the rising edge of SCLK and registered into the input FIFO buffer of length dependent on the selected SPI-mode (8, 16, 24 bits, [Figure 12](#), [Figure 13](#), [Figure 14](#), [Figure 15](#)). With every falling edge of SCLK the bits to be read are provided serially to the pin SDO.

The timing requirements for the serial interface are shown in [Figure 10](#) and in [Table 24](#).



**Figure 10** Serial bus timing



3 Functional description

Several SPI topologies are supported: pure bus topology, daisy chain and combinations (Figure 11). Of course independent individual control with a dedicated SPI controller interface for each slave IC is possible as well.

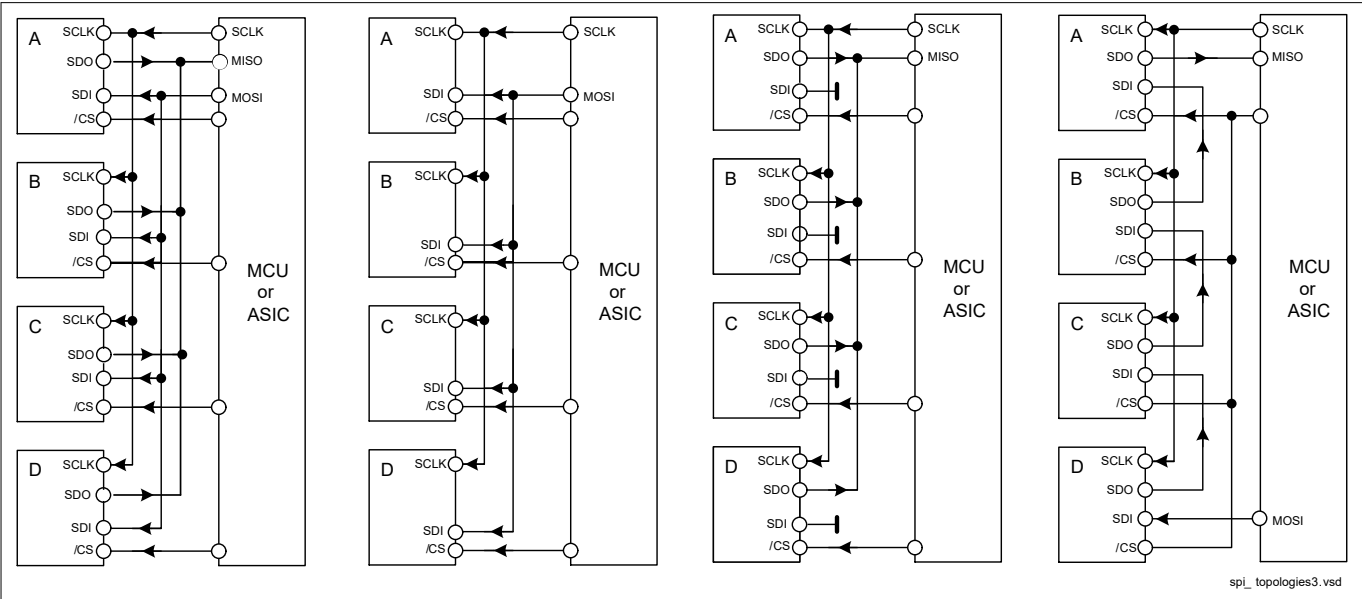


Figure 11 Example SPI topologies

3.2.2.1 SPI modes

Four different SPI-modes can be selected by means of MS0 and MS1 (Figure 12 - Figure 15).

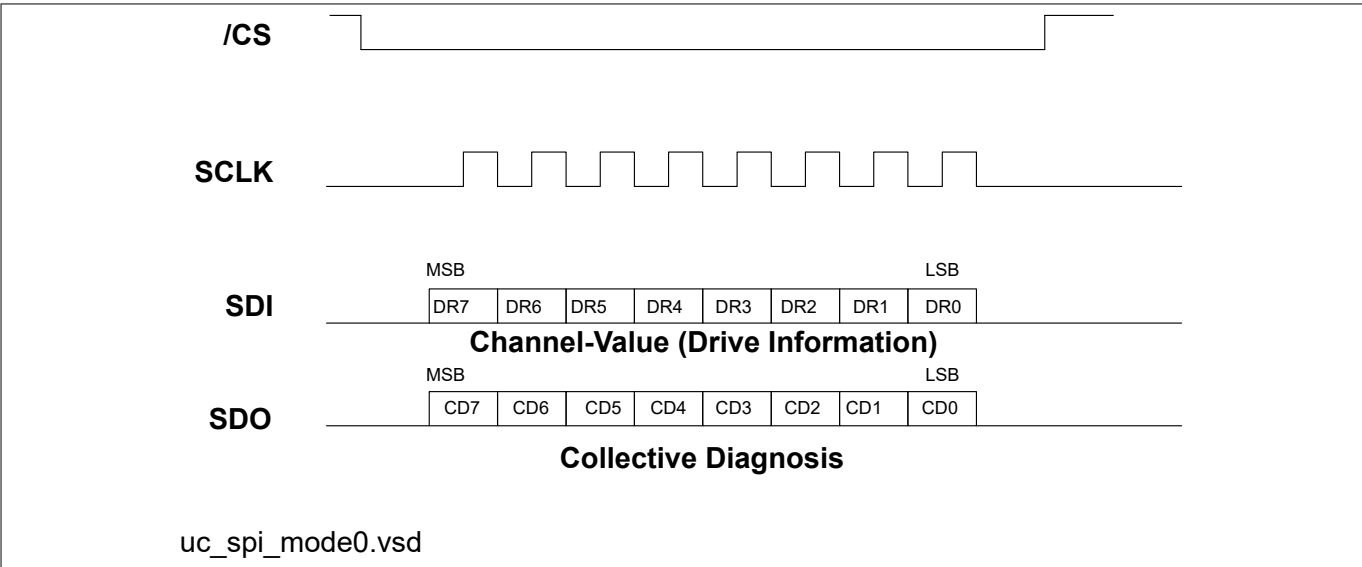


Figure 12 SPI mode 0, MS0 = 0, MS1 = 0, daisy chain supported

3 Functional description

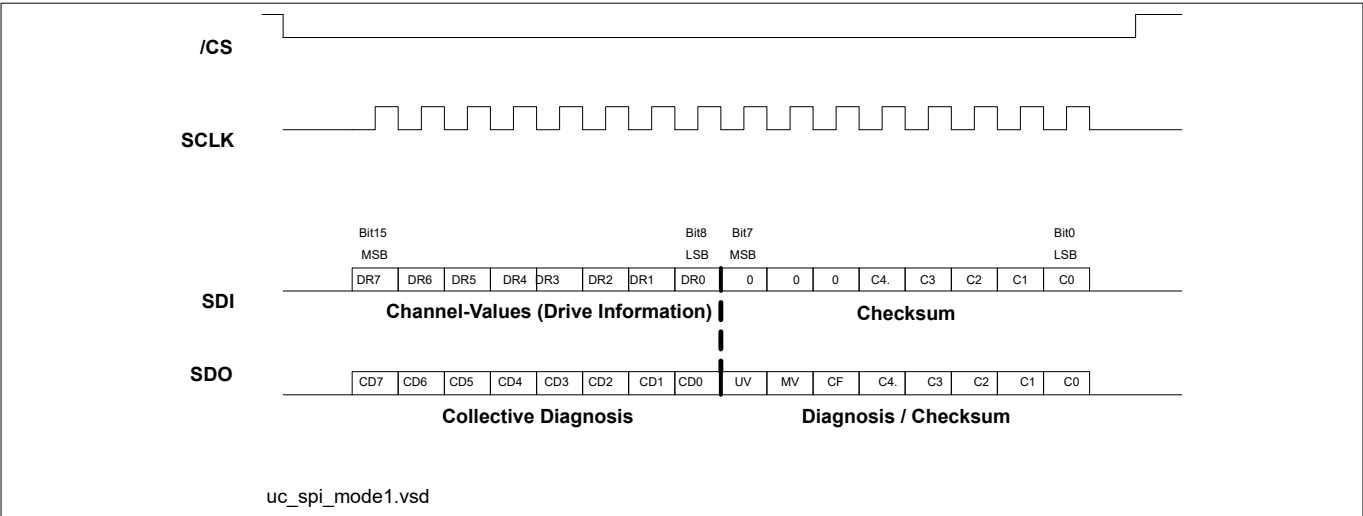


Figure 13 SPI mode 1, MS0 = 1, MS1 = 0, daisy chain supported

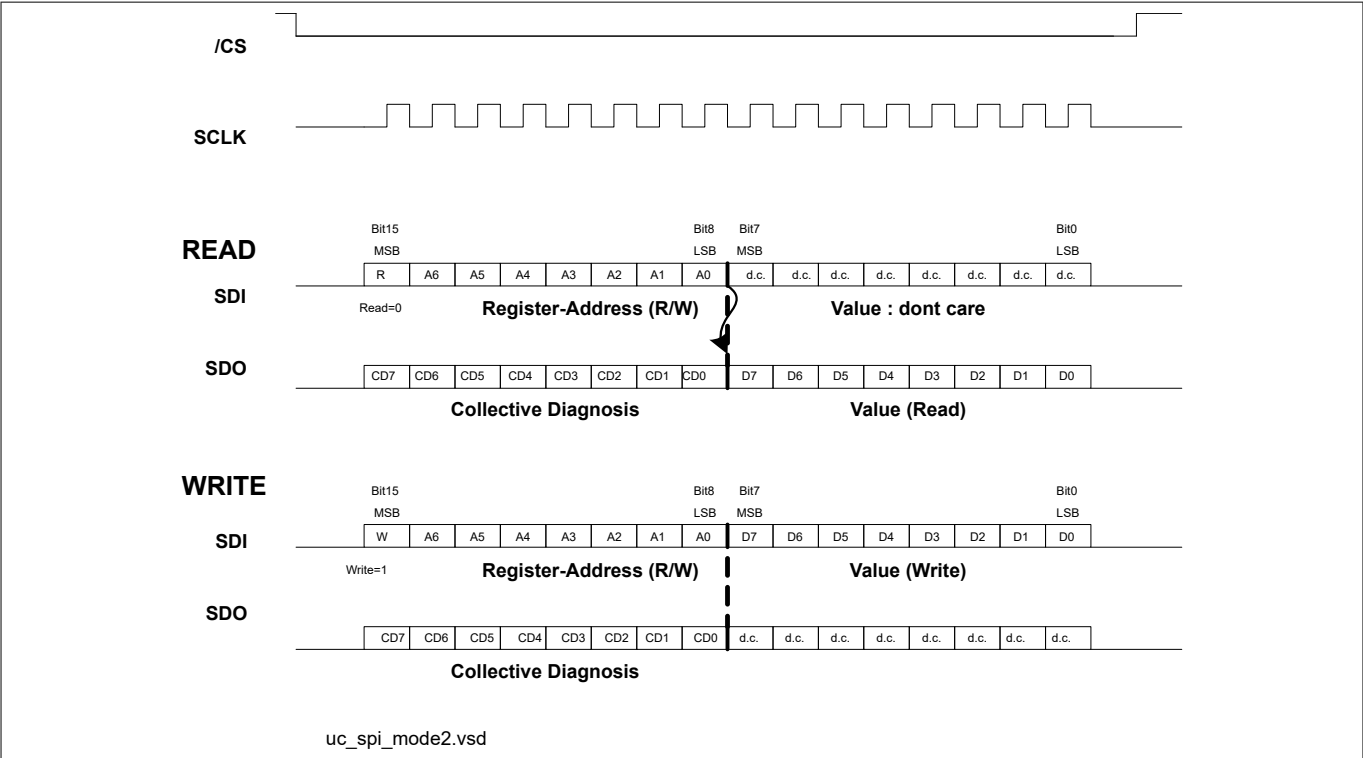


Figure 14 SPI Mode 2, MS0 = 0, MS1 = 1

### 3 Functional description

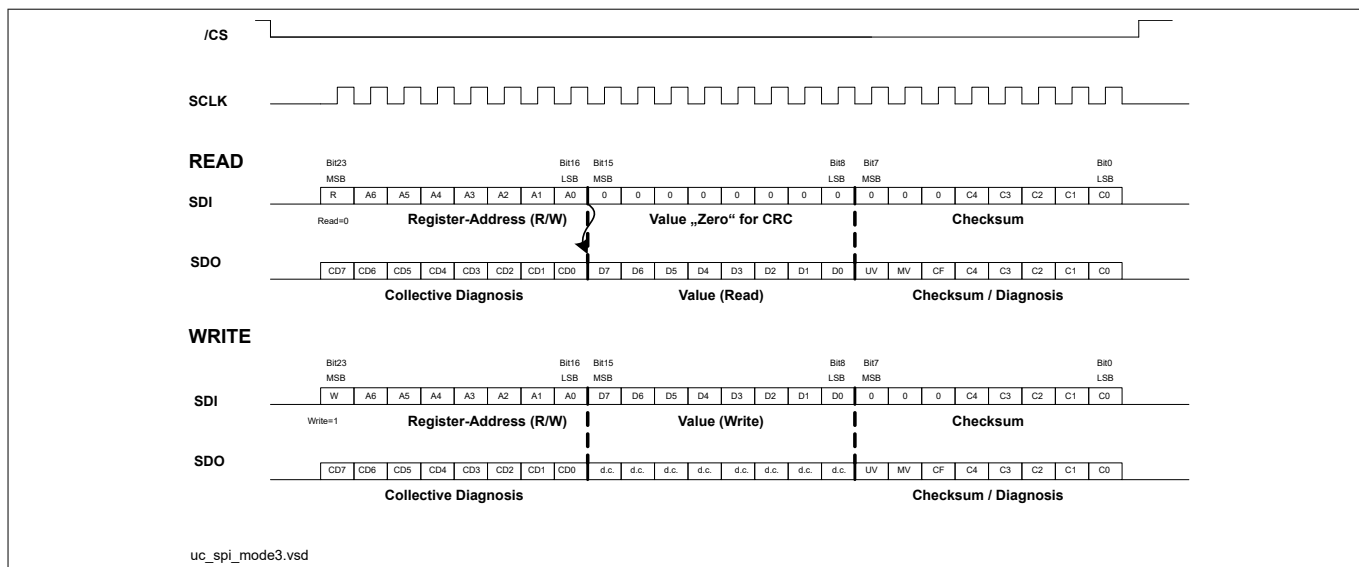


Figure 15 SPI mode 3, MS0 = 1, MS1 = 1

#### 3.2.2.2 Daisy chain mode

Up to 4 devices can be connected together as shown in the Figure 16 to operate in the daisy chain mode. Serial modes 0 and 1 can be operated in daisy chain mode. In this case, the SDO output of one device is directly connected to the SDI input of the next device. The SPI chain has to be connected to the  $\mu$ C or Bus ASIC (MOSI, MISO and common SCLK and  $\overline{\text{CS}}$  signals). If the received SCLK pulses are not fulfilling the modulo(8)-condition the CRCERR pin will be activated.

In serial mode 1 the CRC-generation has to be reset after 16 SCLK-cycles. At the rising edge of  $\overline{\text{CS}}$  each connected daisy-chain-device checks its related 16 bit-stream concerning CRC-consistency.

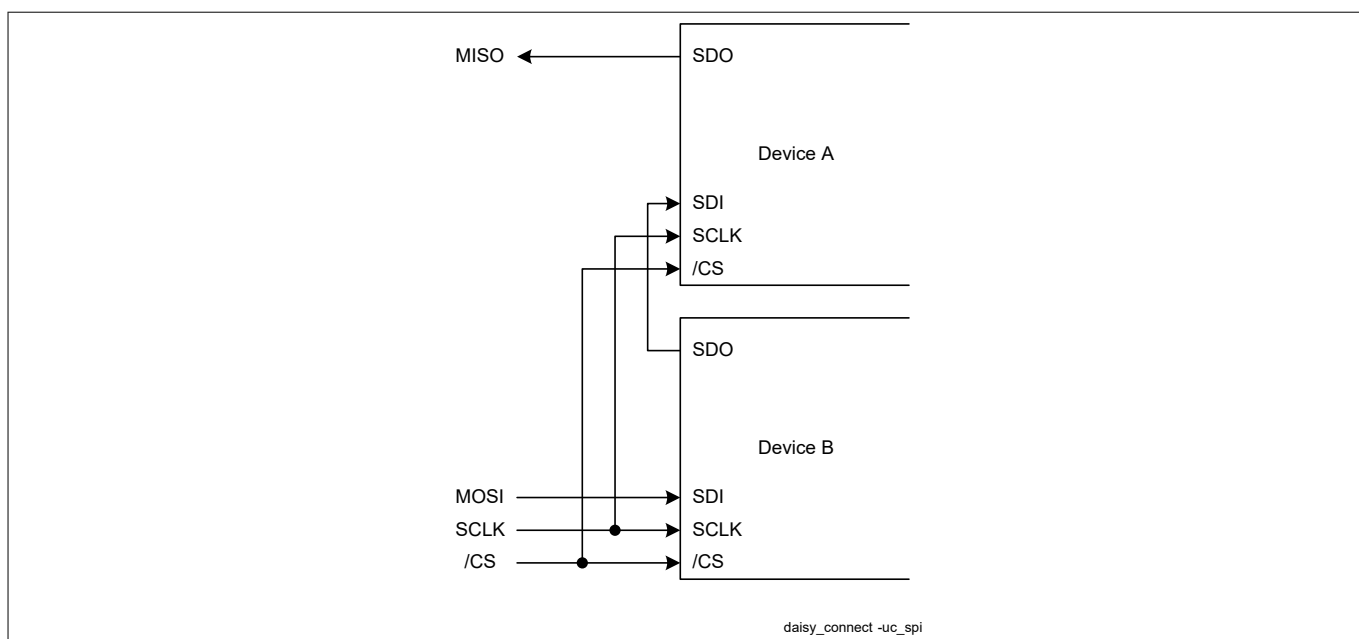
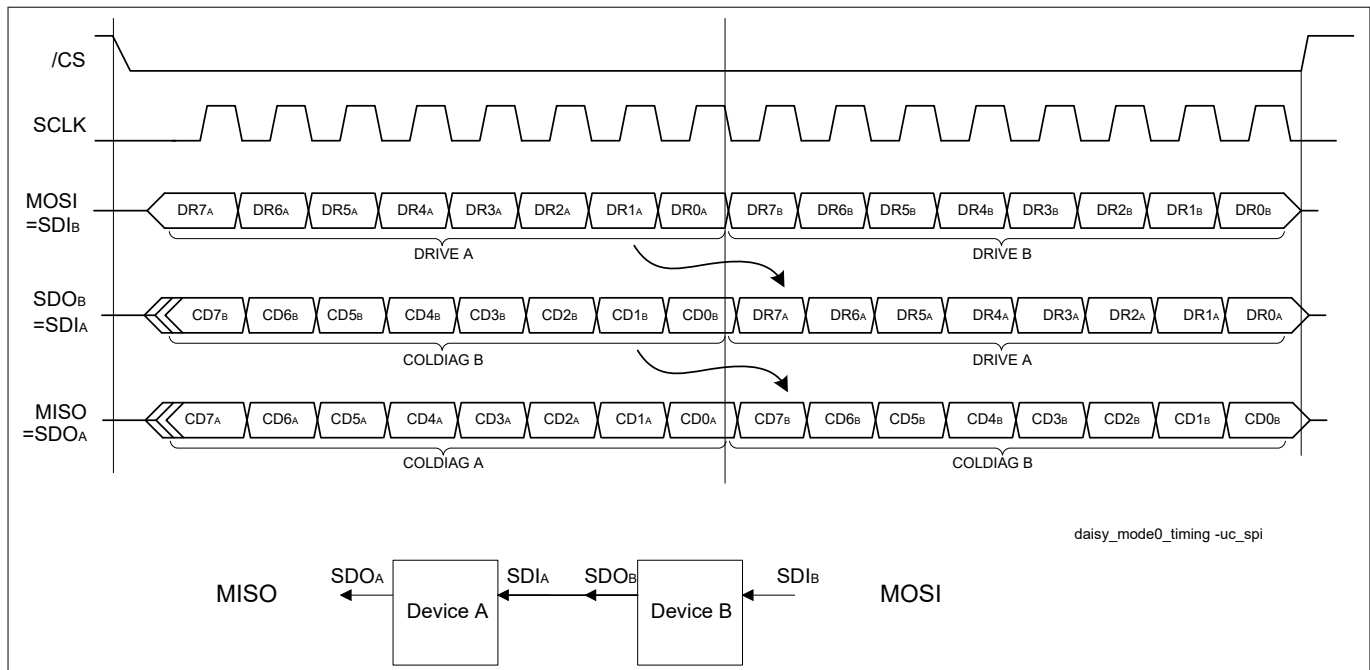


Figure 16 Connecting two devices for daisy chain mode

The data shifted in the first device SDI input is shifted out at the SDO output after the first byte for the serial mode 0 (after the second byte for the mode 1) while  $\overline{\text{CS}}$  remains Low as shown in the Figure 17.

### 3 Functional description



**Figure 17** Typical timing diagram of daisy chain operation (Serial mode 0)

#### 3.2.2.3 Cyclic Redundancy Check CRC

To detect errors inside SPI data transmission two SPI-Modes are provided with integrated Cyclic Redundancy Check.

The 5-Bit-CRC checksum will be calculated with the polynom  $X^5 + X^4 + X^2 + 1$ . The bit length used for the calculation is 11 bits for SPI-mode 1 and 19 bits for SPI-mode 3. The internal CRC-working register is loaded with "11111" before start of the CRC-calculation.

The SPI-mode 1 supports only the write procedure for the **DRIVE** register (SPI-mode 1, MS1, MS0 = 01). Eight bits of drive-information plus 3 dummy bits and the related CRC-information (5 bits based on the fed-in 11 bits) are delivered to the CRC-engine. At the same time the **COLDIAG**-information in combination with the **UV**, **MV**, **CF**-bits and the related CRC-information (based on these 11bits: COLDIAG, UV, MV, CF) are fed out of SDO. The bit stream format is shown in [Figure 13](#).

SPI-mode 3 provides register based access to the ISO2H823V2.5 with implemented CRC. The bit stream for a write access to a register consists of the register address (8 bits), register data (8 bits), 3 dummy bits and the CRC signature (5 bits) as shown in [Figure 15](#). The total bitstream is fed into the CRC-input engines and processed according to the underlying CRC-algorithm serially. At the same time the COLDIAG-information in combination with the UV, MV, CF-bits and the related CRC-information (based on these 19 bits: COLDIAG, 8 dummy bits, UV, MV, CF) are fed out of SDO.

The bit stream for a read access to a register consists of the register address (8 bits), 11 dummy bits and the CRC signature (5 bits) as shown in [Figure 15](#). The total bitstream is fed into the CRC-input engines and processed according to the underlying CRC-algorithm serially. At the same time the COLDIAG-information, register data in combination with the UV, MV, CF-bits and the related CRC-information (based on these 19 bits: COLDIAG, 8 bits register data, UV, MV, CF) are fed out of SDO.

After processing the 24 in-bits (including the CRC-signature) the result of the CRC-algorithm processing has to be zero. In the case of another result different from zero the delivered signature is not consistent with the delivered bit stream. This will be indicated by driving the **CRCERR** Pin to Low.

In both cases (SPI-mode 1 and SPI-mode 3) the status of the CRCERR pin is evaluated not at the end of the bit sequence but with rising edge of  $\overline{CS}$ . The procedure is consistent with the daisy-chain application where each

### 3 Functional description

partner of the daisy chain checks its own contribution with the rising edge of  $\overline{CS}$  when it is confirmed that the chain is completely filled.

$\overline{CRCERR}$  reflects both the fulfillment of the modulo-8-condition for the number of SCLK-signals and the correctness of the CRC-signature. Both kinds of information are evaluated only during  $\overline{CS}$  is Low and reported with the rising edge of  $\overline{CS}$ . Therefore it is assured that non-active ICs ( $\overline{CS}$  = High) does not report a  $\overline{CRCERR}$  = Low signal in case SCLK is toggling.

The signal  $\overline{CRCERR}$  has an internal pull-up-resistor of 50 kΩ. When releasing  $\overline{CRCERR}$  the internal pull-up resistor determines the rise time, which is about 3 μs. It is possible to reduce the rise time to around 1 μs by adding an external pull-up resistor of 10kΩ at the  $\overline{CRCERR}$  pin.

#### 3.2.3 Common error indication output

The dedicated  $\overline{ERR}$  pin signalizes a common fault. This low-active pin has an open drain functionality with a pull-up resistor.

Depending on the μController-interface mode in use, several internal status signals are OR-wired to drive the  $\overline{ERR}$  pin:

- In direct mode, the **OTC** flag (LEDGx-bit-field of CT-transmission, OR-wired, volatile) and the volatile **W4P**-information are routed to the  $\overline{ERR}$  pin
- The output stage undervoltage (**UV**) and missing voltage (**MV**) of the power-chip which are transmitted via the integrated coreless transformer are provided at the  $\overline{ERR}$  pin
- The internal data transmission error (**TE**) over the galvanic isolation is available as well at the  $\overline{ERR}$  pin
- The signal Wait-for-Power chip (**W4P**) is also provided. It detects that a continuous transmission error over a longer time has occurred e.g. when the process side is not supplied properly and that no diagnostic data are received on the μController-interface side
- The common fault error signal (**CF**) is routed out to the  $\overline{ERR}$  pin in parallel mode. This signal is the OR-combination of the **COLDIAG** register bits (sticky)
- **CF** is not routed out to the  $\overline{ERR}$  pin in any serial mode. In serial modes 1 and 3 the CF-bit is contained in the serial telegram

**Table 3** provides the overview of the signals provided at the  $\overline{ERR}$  pin and the behaviour of the bits used. The prefix "S" specifies the bits as sticky.

During UVLO, all status signals and register bits are reset. The flags UV, MV, TE and W4P have a reset value of 1, so that by default these errors are active. As a consequence after power-up the  $\overline{ERR}$  pin is by default driven Low. The  $\overline{ERR}$  pin returns to High logic level once all the signals OR-wired at this pin are Low i.e. once all the fault conditions are not detected anymore and the bits have been cleared. This behaviour requires the external controller to read the **GLERR** and **INTERR** to "clear" the  $\overline{ERR}$  pin (except in parallel direct mode where the error bit is simply OTC of type: volatile bit generated by oring the volatile gated-LEDGx-information of each channel and W4P). In some operation modes the update and the clearing of the status bits are done automatically after every access (serial mode 0 and 1). For the other operation modes, the error bits need to be read with direct addressing to be updated and cleared (parallel mode and serial modes 2,3).

The  $\overline{ERR}$  signal differs between serial modes and parallel modes since in serial modes 1 and 3 the CF bit is already shifted out when CRC is used. The serial or parallel mode is selected with the SEL signal whereas the serial submodes are controlled with the SPI\_MODE 2-bit signal.

### 3 Functional description

**Table 3** Bits composing the  $\overline{\text{ERR}}$  signal

Status bits	Serial communication				Parallel communication		
	Mode-0	Mode-1	Mode-2	Mode-3	Single access	Repeated read	Direct mode
SUV	X	X	X	X	X	X	
SMV	X	X	X	X	X	X	
CF					X	X	
STE	X	X	X	X	X	X	
SW4P	X	X	X	X	X	X	X <sup>1)</sup>
OTC							X

1) Bit is volatile in direct mode

Upon reset most of the bits used in the  $\overline{\text{ERR}}$  generation are reset to High, the  $\overline{\text{ERR}}$  pin is pulled down on startup and will remain Low as long as the external controller does not clear the corresponding bits (and as long as the fault exists).

#### 3.2.4 Update of the diagnostic registers

The following list describes the handling of appearing and disappearing failures and therefore the diagnostics.

- Appearing diagnostic/failure: appearing diagnostics are stored internally within sticky registers and are OR-ed into the register **COLDIAG** (except **LEDGx**). Therefore the appearing diagnostic/failure bit can be seen immediately. After reading **COLDIAG** the diagnostic bits are transferred from the internal sticky registers to **DIAG0**,..., **DIAG7** from which these can be read now in detail
- Disappearing diagnostic/failure: the diagnostic bits are stored internally as sticky bits and therefore also or-ed in **COLDIAG**. In the case the source for the diagnostic bits has disappeared the diagnostic bits are still available internally and in **COLDIAG** until the user has read **COLDIAG**. Therefore the diagnostic bits never disappear with vanishing of the source for setting the bits alone. Both conditions have to be fulfilled: vanishing of the source of the occurrence and reading of **COLDIAG**
- In the case the isochronous mode for the channel diagnostic values is activated with the bit **FRZSC** in register **GLCFG** (see [Chapter 3.2.5.2](#)) the diagnostic bits are transferred from the internal sticky registers to **DIAG0**,..., **DIAG7** with each edge of the SYNC-signal

#### 3.2.5 SYNC operation

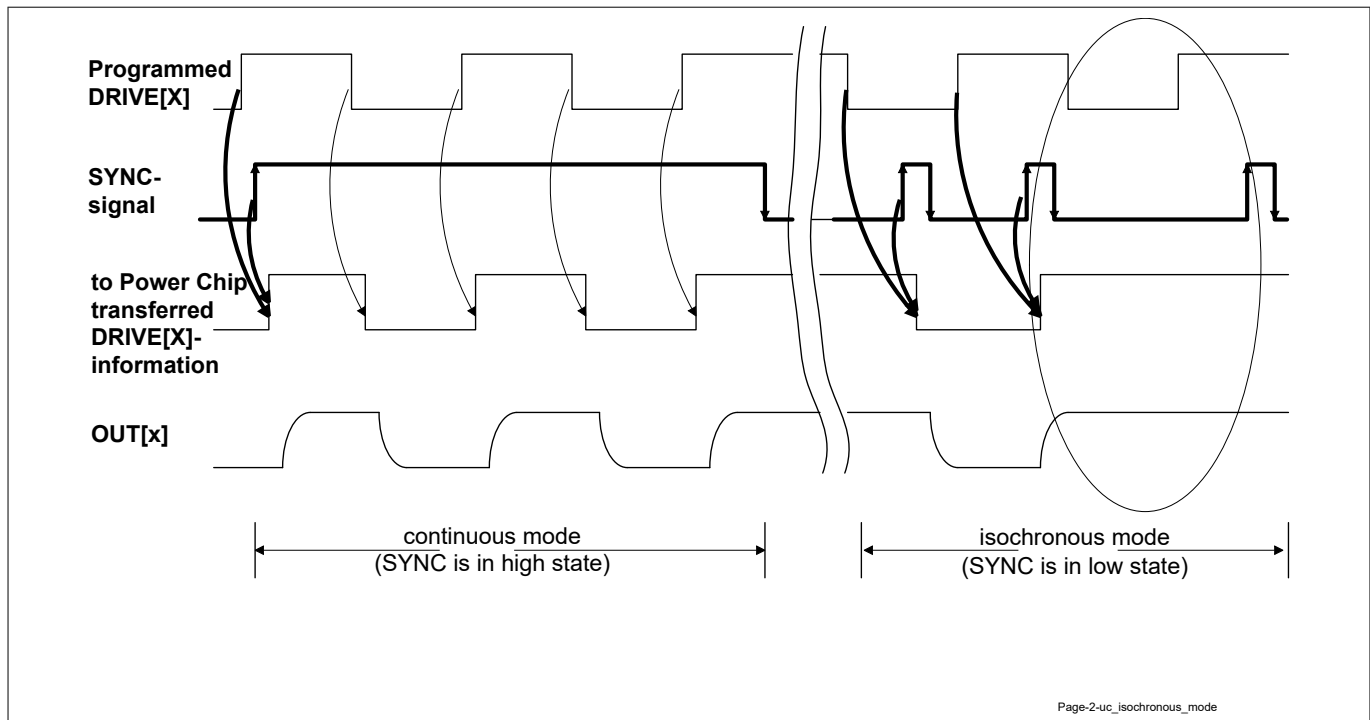
The Isochronous Mode enables the synchronization of several devices (e.g. to provide 32 channels when 4 devices are grouped in parallel). In this way the update of all the output channels as well as their diagnostics can be synchronized and held such that the Bus ASIC or microcontroller can program a new control word of the output channels and read the diagnostic status. In continuous mode, each device with its own built-in oscillator is updated independently.

The Isochronous Mode is controlled by the SYNC pin and independent of the selected serial or parallel interface (with the SEL pin). It concerns only the update of user registers in the system.

##### 3.2.5.1 SYNC-signal for drive-signals

[Figure 18](#) explains in detail the mechanism for SYNC = High, SYNC = Low and the rising and falling edges of SYNC for transferring the drive-information from the uC-Chip to the Power Chip.

### 3 Functional description



**Figure 18** SYNC operation timing

#### SYNC = High, normal mode:

The **DRIVE**-register can be written with new data and the contents of it is also transferred to the power chip.

#### SYNC = Low, isochronous-mode:

In isochronous mode the user can write the **DRIVE**-register but this value will not be transferred to the Power Chip. Therefore the driver configuration (activation of drivers in the Power Chip) is frozen. In **Figure 18** it can be clearly seen that the toggling of the **DRIVE[x]**-information (SPI-data-cycle) at the right side had not been transferred to the process side (see oval area in **Figure 18**).

### 3.2.5.2 SYNC-signal for diagnostics

Independent from the level of the SYNC-signal always the same reading-sequence of the diagnostics shall be obeyed: read **COLDIAG** register first and identify which channel x shows the setting of the diagnostic bit and then read the corresponding registers **DIAG0**,..., **DIAG7** for which the diagnostic has been reported (in **Table 4** and **Table 5** this is illustrated exemplary for channel 0). Reading **COLDIAG** first assures that the **DIAG0**,..., **DIAG7**-registers are loaded from the internal sticky registers.

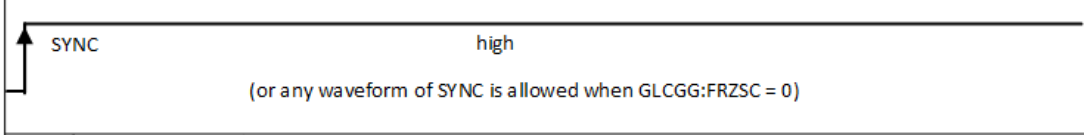
#### SYNC = High, continuous mode:

When the signal SYNC is High (default), the continuous mode is selected and the diagnostic registers **DIAG0**,..., **DIAG7** are always updated after read access to **COLDIAG**.

**Table 4** shows the typical scenario where an external disturbance (open load or short-circuit-to VBB) causes the setting of the diagnostic registers **DIAG0**,..., **DIAG7** (here exemplary **DIAG0**) and the collective diagnostic register **COLDIAG**. After vanishing of the disturbance and reading of **COLDIAG** the internal diagnostic registers are reset. The SYNC-waveform is sketched in the 1<sup>st</sup> row of **Table 4** (please note that in case of continuous mode any waveform of SYNC is allowed).

### 3 Functional description

**Table 4** Continuous Mode (GLCFG : FRZSC = 0), Disturbance (to Channel 0) Scenario

Waveform of SYNC (permanently high)						
Scenario #						
#1		disturbance				
Read results #1 COLDIAG DIAG0			READ=yes 0x01 0xvalue		READ=yes 0x00 0x00	
#2		disturbance				
Read results #2 COLDIAG DIAG0			READ=yes 0x01 0xvalue		READ=yes 0x01 0xvalue	READ=yes 0x00 0x00

#### SYNC = Low, isochronous-mode:

The isochronous mode for the channel diagnostic values is activated with the bit **FRZSC** in register **GLCFG**. If **FRZSC** = 1 (**RESYN** = 0) the isochronous mode for diagnostics is enabled.

When **SYNC** is Low, the **DIAG0-7** and **COLDIAG** (including **CF**) are not updated anymore (frozen). At the falling edge of **SYNC** the information of the internal sticky registers is transferred to **DIAG0,..., DIAG7**. During **SYNC** = High the information of the internal sticky registers has been mirrored and OR-ed to **COLDIAG**. When isochronous mode is activated the **DIAG0,..., DIAG7**-registers and **COLDIAG** freeze the diagnostic data. But the internal sticky registers collect the diagnostic information independently from **SYNC**. With rising edge of **SYNC** the **DIAG0,..., DIAG7** registers and **COLDIAG** are updated on base of the contents of the internal sticky registers.

**Table 5** shows some scenarios where an external disturbance (open load or short-circuit-to VBB) cause the setting of the diagnostic registers **DIAG0,..., DIAG7** (here **DIAG0**) and the collective diagnostic register **COLDIAG**. In all scenarios the same procedure is sketched where a disturbance occurs and the diagnostic registers are read in the following. The **SYNC**-waveform is sketched in the 1<sup>st</sup> row of **Table 5** for isochronous mode with low and high periods), the disturbance is drawn in light shaded grey (please note that the disturbances in this examples are strictly time-limited with respect to the corresponding read-accesses at different time stamps. Examples of possible read-access events and the related read results are visualized as blocks in the corresponding rows of **Table 5**. The occurrence of the disturbances in relation to the edges of the **SYNC**-signal is altered for some of the displayed examples. The Read procedures may take place during the phase where **SYNC** is Low (=0) or High (=1). Depending on the occurrence of the disturbance in relation to the **SYNC**-edges and the read-process the diagnostic values have been already set in **COLDIAG** and **DIAG0,..., DIAG7** or the old ( i.e. previous) values have been frozen. In the second case the new values will be updated in **COLDIAG** and **DIAG0,..., DIAG7** with the next rising edge of **SYNC** and can be read with the next read-cycle. Due to the sticky registers no diagnostic value is lost. After vanishing of the disturbance and reading the diagnostic values are reset.

Entries in **COLDIAG** can be reset during **SYNC** = Low after a reading procedure when the disturbance had been registered before the falling edge of **SYNC** and is therefore securely delivered. But **DIAG0,..., DIAG7** remains unaffected from this reading procedure.



### 3 Functional description

**Table 5** Isochronous Mode (GLCFG : FRZSC = 1 (RESYN = 0)), Channel 0 Disturbed, Scenarios

Waveform of SYNC (alternating high/low)										
Scenario #										
#1	disturbance									
Read results #1 COLDIAG DIAG0			READ=yes 0x01 0xvalue				READ=yes 0x00 0x00			
#2	disturbance									
Read results #2 COLDIAG DIAG0			READ=yes 0x01 0xvalue	=yes 0x00 0xval			READ=yes 0x00 0x00			
#3	disturbance									
Read results #3 COLDIAG DIAG0			READ=yes 0x00 0x00				READ=yes 0x01 0xvalue	READ=yes 0x00 0x00		
#4	disturbance									
Read results #4 COLDIAG DIAG0			READ=yes 0x00 0x00				READ=yes 0x01 0xvalue	READ=yes 0x00 0x00		
#5	disturbance									
Read results #5 COLDIAG DIAG0			READ=yes 0x01 0xvalue					READ=yes 0x00 0x00		
#6	disturbance									
Read results #6 COLDIAG DIAG0			READ=yes 0x00 0x00					READ=yes 0x01 0xvalue	READ=yes 0x00 0x00	
#7	disturbance									
Read results #7 COLDIAG DIAG0			READ=yes 0x00 0x00					READ=yes 0x01 0xvalue	READ=yes 0x00 0x00	

#### 3.2.6 $\overline{\text{ODIS}}$ output disable

The low active  $\overline{\text{ODIS}}$  signal immediately switches off the output channels OUT0-OUT7. This pin has an internal Pull-Down resistor. In normal operation the signal  $\overline{\text{ODIS}}$  is High. Setting  $\overline{\text{ODIS}}$  to Low clears the registers as well. The minimum width of the  $\overline{\text{ODIS}}$  signal is 5  $\mu\text{s}$ .

#### 3.2.7 LEDGOFF

The gated-LED-signal  $\text{LEDG}_x$ ,  $x = 0, \dots, 7$  is per default reported in the diagnostic registers  $\text{DIAG}_0, \dots, \text{DIAG}_7$  (not or-ed in the  $\text{COLDIAG}$ -register).  $\text{LEDG}_x$  is updated with a long time constant every 100 ms. Therefore the bit  $\text{LEDGOFF}$  in  $\text{GLCFG}$  offers the possibility to suppress the reporting in the diagnostic registers  $\text{DIAG}_0, \dots, \text{DIAG}_7$ .

### 3 Functional description

#### 3.2.8 OLOFF

The bit **OLOFF** in **GLCFG** offers the possibility to suppress the reporting of **OLIx**, **OLAx** in the diagnostic registers **DIAG0**,..., **DIAG7**.

#### 3.2.9 RESET (Hard and Soft)

##### 3.2.9.1 Hardware reset

The external hardware reset command (triggered via pins CS and ALE) can be enabled or disabled by the bit **RSTOFF** in the register **GLCFG**, by default the external hardware reset function is enabled. The external hardware reset forces the logic asynchronous reset for the uC\_chip (acts like a power-on-reset), all registers are loaded with the default values. It is triggered when the signal ALE is set High whereas the  $\overline{\text{CS}}$  signal is set Low for at least 100  $\mu\text{s}$ . Once an internal timer reaches the end value of 100  $\mu\text{s}$  then the hardware reset condition is fulfilled and “latched”. At the point where one of the signals ALE and  $\overline{\text{CS}}$  returns to its default value, the reset is processed. With resetting the **DRIVE**-register and restarting the CT-transmission the output switches are turned off.

##### 3.2.9.2 Soft reset

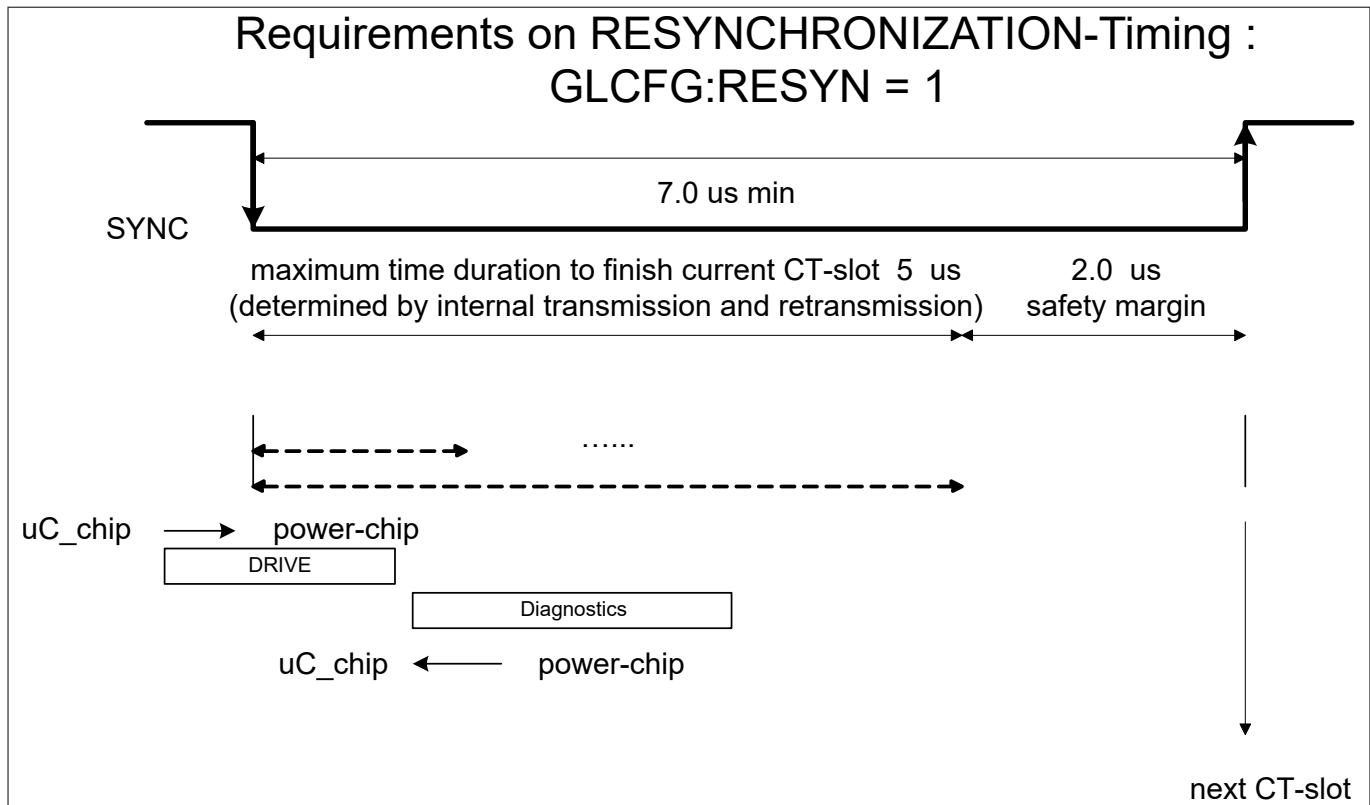
The soft reset for the uC\_chip is triggered by the bit **SWRST** (self clearing after performing the soft reset) in the register **GLCFG**. If the soft reset is triggered the **DRIVE**, **INTERR**, **GLERR**, **DIAG0**,..., **DIAG7**, **COLDIAG**, **DIAGCFG** register are set to their reset values synchronously. In addition the internal flags are cleared. The CT-transmission is restarted. The actual transmission cycle is not disturbed. With resetting the **DRIVE**-register and restarting the CT-transmission the output switches are turned off.

#### 3.2.10 Resynchronization of CT-Transmission

During the CT-transmission the drive-information **DRIVE** for the 8 power switches is sent from the uc-Chip to the Power-Chip. Subsequently one of the diagnostic informations (status-information, **OTx**, **OLIx**, **OLAx**, **OCx**, **SCVx** or **LEDGx**-information for the 8 power switches) is sent back. The duration of a CT-time slot with transmission of drive - information and back-transmission of one of the diagnostic information lasts about 5  $\mu\text{s} \pm 20\%$ . (internal operating frequency : 10 MHz, resistor at pin CLKADJ : 10 k $\Omega$ ). When the user programs the drive register a timing uncertainty arises when the specific programmed switch is activated or deactivated in the power chip. The data of the drive register can be transferred to the power chip only in the next free CT-time slot.

The goal of resynchronization is to limit the timing uncertainty due to transmission and retransmission to a value below  $\pm 1.5\text{ }\mu\text{s}$  but with a fixed latency of minimum 7.0  $\mu\text{s}$ . For triggering the transmission the signal SYNC is used when **GLCFG:RESYN** = 1. A timing difference between switching on and off of the power transistors exists which is already included in the timing uncertainty value above. Switching off a power transistor is delayed by up of 0.5  $\mu\text{s}$  max relative to the SYNC-rising edge compared to switching on a power transistor

### 3 Functional description



**Figure 19** Timing of resynchronization

#### Transmission without resynchronization:

- **GLCFG:RESYN** = 0 or 1
- signal SYNC = 1
- write the drive information into **DRIVE**
- the contents of DRIVE is transferred via the CT to the power-chip

#### Transmission with resynchronization:

- signal SYNC = 1
- **GLCFG:RESYN** = 1
- write the drive information into **DRIVE\_RESYNCH**
- signal SYNC = 0
- the duration of the signal SYNC = 0 (minimum 7.0 us) determines the time for resynchronization and the time until the next CT-transfer
- In the meantime the pending transmission and retransmission has been finished and the contents of **DRIVE\_RESYNCH** has been transferred to **DRIVE**
- set signal SYNC = 1, the CT-transfer is started from DRIVE with the rising edge of SYNC

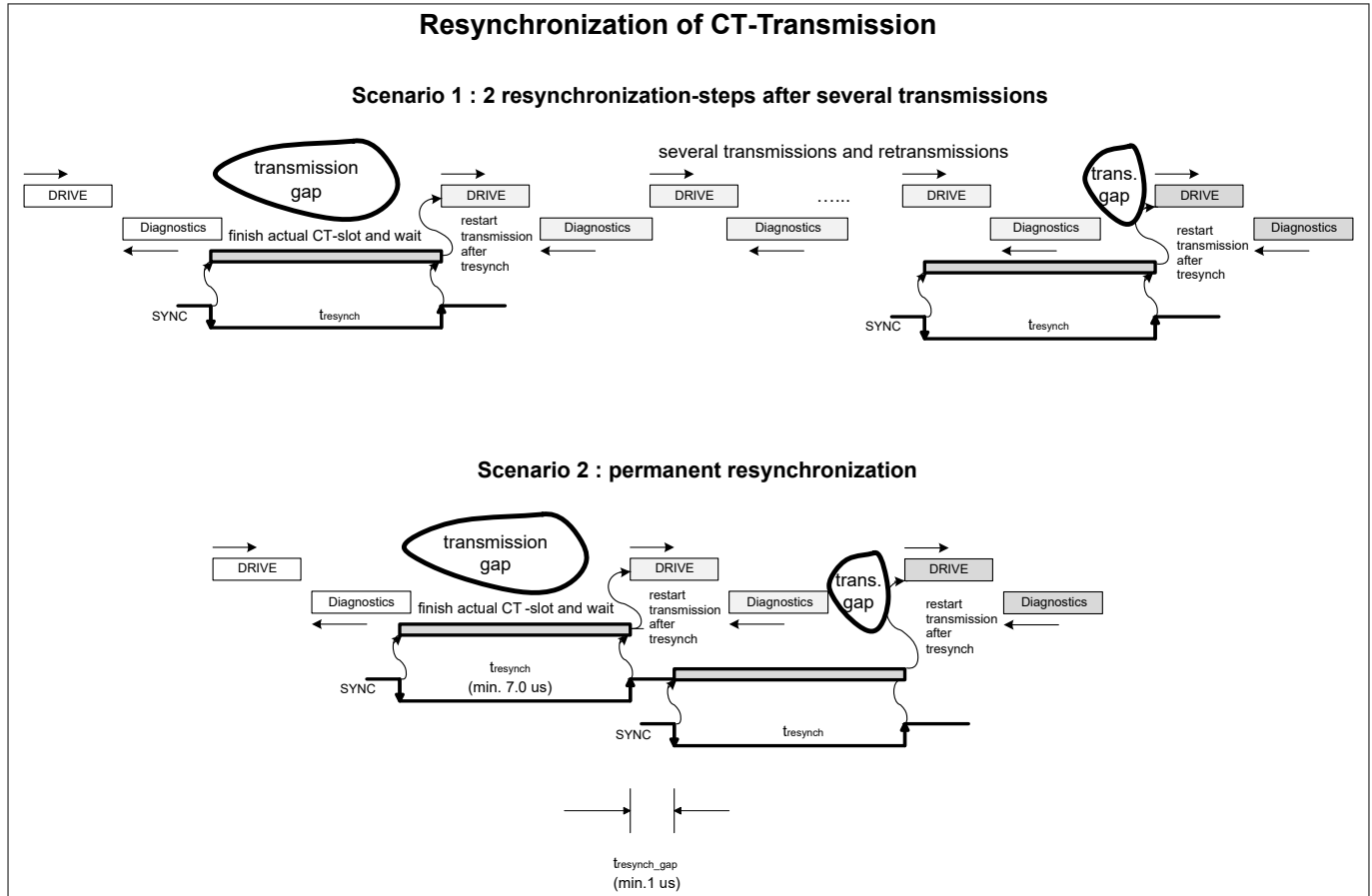
Without any negative pulses on SYNC the CT-transfer is operated permanently from DRIVE; the negative pulses on SYNC are solely used for resynchronization, the isochronous mode for drive-information and for diagnostics is inactive when GLCFG:RESYN is set to "1".

Information for the **DRIVE\_RESYNCH**-register can be written long before the resynchronization trigger with falling and rising edge of SYNC.

The user has to obey the timing requirements of the SYNC-signal. For a duration longer than 300 us ± 20% the watchdog in the power chip disables the output drivers. For a duration of the SYNC-signal shorter than recommended the resynchronization is not guaranteed and the normal transmission fed by the register DRIVE can be performed.

### 3 Functional description

Figure 20 shows 2 different applications of resynchronization. The timing gap between two synchronizations can be as low as 1 us. In this way the customer can decide between single synchronization steps and permanent synchronized transmission with the drawback of reduced CT throughput (waiting time for new transmission).



**Figure 20** Examples of application of resynchronization

Application hint: It is not possible to select `GLCFG:RESYN = 1` and isochronous mode of drive information or/and isochronous mode of diagnostics at the same time. That means resynchronization and isochronous mode of driver information and diagnostics at the same time is not possible. With `GLCFG:RESYN = 1` edges on SYNC are used solely for resynchronization.

### 3.3 Output stage

Each channel contains a high-side power FET that is protected by embedded protection functions. The continuous current for each channel is 600 mA nominal, which depends on the cooling conditions and the total power dissipation.

#### 3.3.1 Output stage control

Each output is independently controlled by an output latch and a common reset line via the pin  $\overline{\text{ODIS}}$  that disables all eight outputs and resets the latches.

### 3 Functional description

#### 3.3.2 Protection functionality

##### 3.3.2.1 Power transistor overvoltage protection

Each of the eight output stages has its own zener clamp that limits the voltage over the power stage at the power transistor when solenoid loads are switched off.  $V_{ONCL}$  is then clamped to 52 V (typ.).

##### 3.3.2.2 Power transistor overload protection

The outputs are provided with a linear current limitation, which regulates the output current to the current limit value in case of overload. The electrical operation point does not lead to a shutdown.

The excess power dissipation in the power transistor during current limitation will lead to a rapid increase of the junction temperature. When the junction temperature exceeds 150 °C (typ.) the output will switch off and will switch on again when the junction temperature has cooled down by a temperature hysteresis of 15 K (typ.). Therefore during persisting overload a thermal on-off toggling may occur.

The thermal hysteresis is reset during inactive mode. Therefore when switching to the active mode the power transistor is first switched on if the junction temperature is below 150 °C.

##### 3.3.2.3 Current sense and limitation

To achieve an excellent accuracy for the current limitation and current referred diagnostic (OCLx) an external reference resistor is used. The resistor must be connected between the pins IADJ (as close as possible) and GNDBB. The nominal resistor value is 6.81 kΩ (E96; current drawn out of IADJ typ. 178 μA), the tolerance should be within 2% to meet an overall current limit tolerance from 0.73 A to 1.3 A.

Operation with other resistor values than 6.8 kΩ ±5% is not allowed and may lead to insufficient short circuit protection.

To offer open load diagnostics in active mode, a part of the power transistor is driven down when the drain-source-voltage drops below a certain limit (low load condition). The voltage drop across the remaining part is used to evaluate an open load diagnostic.

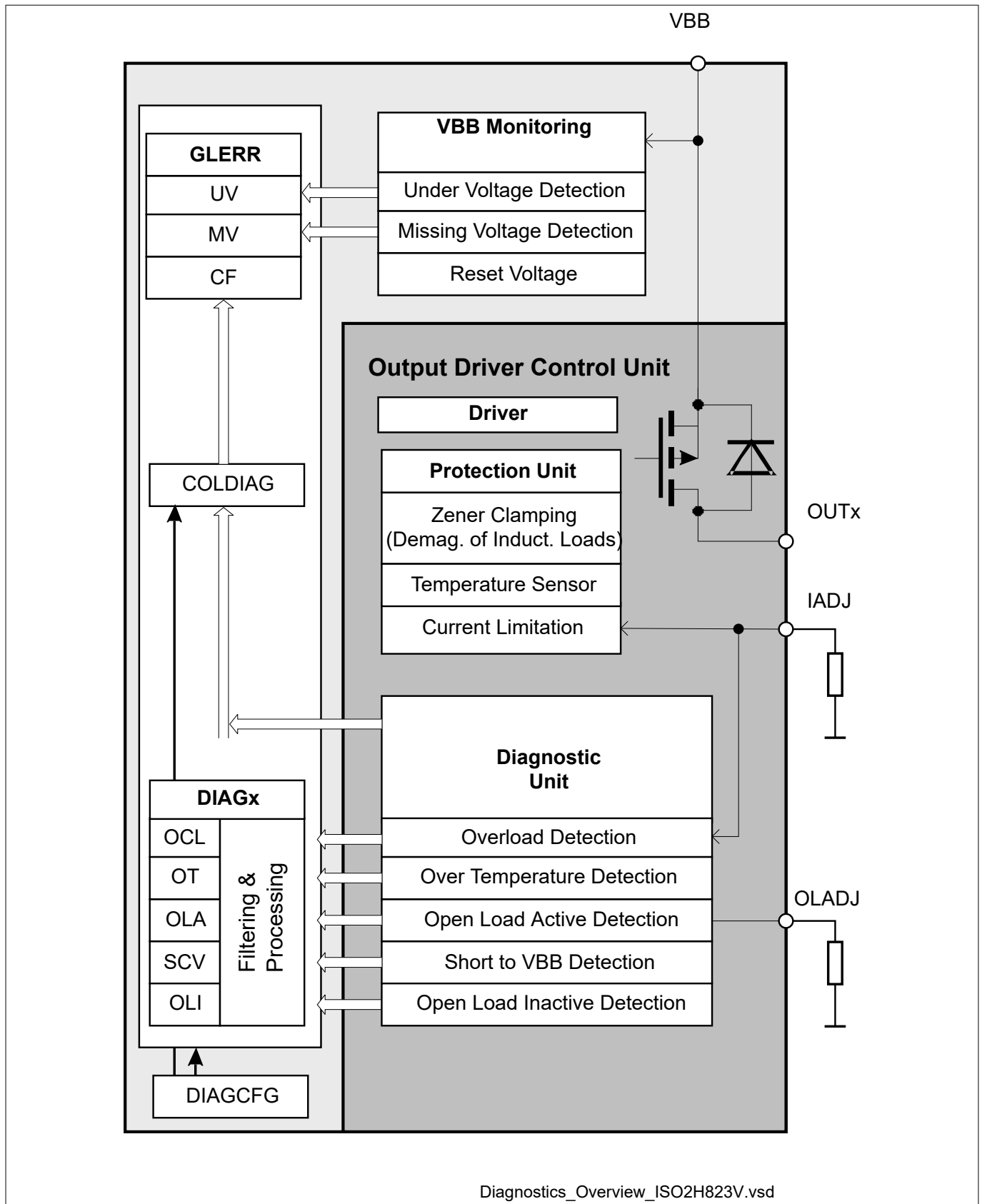
#### 3.3.3 Diagnostic functions

For each of the output stages 5 different types of diagnostics are available. Table 6 specifies the diagnostics. Some of the diagnostics are available only in active mode, others only in inactive mode. The diagnostics OLx, OLAx, SCVx can be prolonged within the complementary mode. Overtemperature in inactive mode is not reported (set to zero).

**Table 6** Diagnostic

Item	Diagnostic type	Inactive mode	Active mode
OTx	Overtemperature	no	yes (OTx Active)
OLx	Open Load/Wire Break, "inactive"	yes	no
OLAx	Open Load/Wire Break, "active"	no	yes
OCLx	Current Sense, Overload Detection	no	yes
SCVx	Short Circuit to $V_{BB}$	yes	not distinguishable from OLAx

### 3 Functional description



**Figure 21**      **Diagnostics overview**

The diagnostics OL<sub>ix</sub>, SCV<sub>x</sub> are reported in inactive mode and OL<sub>Ax</sub> is reported in active mode. When the duration of the disturbance was not sufficient to guarantee a 6 ms blanking/filtering time these diagnostics are

### 3 Functional description

at least reported when switching from one mode into the other mode. The diagnostics OLlx, OLAx and SCVx, OLAx appear in pairs one component for the inactive mode and one component for the active mode with a delay for the filtering. In order not to allow reporting gaps the diagnostics are prolonged until the complementary part is occurring or until a time-out counter has expired (i.e. the diagnostic OLlx (SCVx) is prolonged also during the active time period until the filter delivers a reliable OLAx- (OLAx-) diagnostics and vice versa).

#### 3.3.3.1 Diagnostics in inactive mode

When the output is in inactive mode a diagnostic current is fed to the output. If the load is connected and the load resistance is less than 12 kΩ, the output voltage will be 300 mV or less.

If no load is connected a voltage drop of 7 V is present at the output. A voltage in the range of 5.5 V up to 9.2 V at the output OUTx is detected and reported as open load inactive (OLlx) after filtering.

If the output is shorted to  $V_{BB}$  the output voltage will be close to  $V_{BB}$  level even in inactive mode, this depends upon the type of the short circuit. A voltage level above 9.2 V at the output is detected and reported as short circuit to  $V_{BB}$  (SCVx) after filtering.

The window comparator for OLlx (5.5 V - 9.2 V) is realized with the analog level comparators for 5.5 V and 9.2 V and the digital filters for OLlx and SCVx. After filtering SCVx has the priority against OLlx. By means of the digital filters EMI-contributions shall be filtered before deciding about OLlx or SCVx.

If a capacitive load with a long RC time constant is connected to the ISO2H823V2.5 (like a 12 kΩ resistor through a long cable with 100 nF capacitance) when switching off, the output voltage sequentially passes through the windows of short to VBB detection and broken wire detection. During a blanking time of 6 ms (typ.) the diagnostic signals are ignored to avoid false triggering of diagnostic registers.

If the corresponding channel is switched on again before the end of the blanking time (6 ms), the state of the diagnostic signals present before switching on is transferred to the diagnostic registers, bypassing the blanking window of 6 ms and filtered instead with a filtering time of 100 μs, 0.5 ms, 1 ms depending on the switching frequency.

**Table 7 Filter time in inactive mode for OLlx and SCVx**

Duration of inactive time $t_{OFF}$ before switching	Filter time
$0 \text{ ms} < t_{OFF} < 1.5 \text{ ms}$	100 μs
$1.5 \text{ ms} < t_{OFF} < 3 \text{ ms}$	0.5 ms
$3 \text{ ms} < t_{OFF} < 6 \text{ ms}$	1 ms
$t_{OFF} > 6 \text{ ms}$	6 ms (OLlx), 2 ms (SCVx)

For the largest SCVx-filter a filter-length of 2.0 ms is chosen but a setting of SCVx is only possible after the blanking window of 6 ms. No single channel over temperature diagnostics is given during inactive mode to avoid false triggering when switching inductive loads.

#### 3.3.3.2 Diagnostics in active mode

During active mode operation the remaining voltage drop of a low load condition is compared to the voltage drop across a reference transistor biased with a reference current. The reference current can be set by the value of a resistor connected between OLADJ and GNDBB defining the threshold for open load diagnostics. The resulting open load threshold is inversely proportional to the connected resistor (25 kΩ - 2.3 kΩ, E96 series; current out of the OLADJ-pin 48.6 μA - 528 μA) and can be set within 0.5 mA to 5 mA.

Like the diagnostics in inactive mode the open load diagnostics in active mode (OLAx) is ignored during a 6 ms blanking window after switching on. If the channel is switched off before the end of the blanking window the current state of the open load diagnostics is transferred to the diagnostic registers, bypassing the blanking

### 3 Functional description

window of 6 ms and filtered instead with a filtering time of 100 µs, 0.5 ms or 1.0 ms (depending on the switching frequency).

The over load diagnostic (OLx) occurs generally if the output stage limits the load current. Therefore the diagnostic threshold is equal to the current limiting value. An overload may and a short to GNDBB will very likely lead to a thermal shutdown. The shutdown is indicated separately by the diagnostics OTx. The standard filter time for overload (OLx) and overtemperature (OTx) is 50 µs (for a thermal shutdown).

**Table 8** Filter time in active mode for OLx

Duration of active time $t_{ON}$ before switching	Filter time
$0 \text{ ms} < t_{ON} < 1.5 \text{ ms}$	100 µs
$1.5 \text{ ms} < t_{ON} < 3 \text{ ms}$	0.5 ms
$3 \text{ ms} < t_{ON} < 6 \text{ ms}$	1 ms
$t_{ON} > 6 \text{ ms}$	6 ms

Some loads like incandescent lamps or DC motors show an inrush current, which is normal and should not trigger an overload diagnostic. In some cases even a transient thermal shutdown can not be avoided but an OTx-message is avoided, e.g. for the time duration of lighting up a cold lamp (max. 200 ms). In this case and only for this short time duration the current limiting threshold can be set to 1.5 A and the temperature threshold to 200°C by the internal finite state machine.

The ISO2H823V2.5 adapts filtering of over load and thermal shutdown diagnostics as well as shutdown temperature and current limit level by evaluating the previous turn off time and the load resistance.

#### 3.3.3.3 Diagnostic scenarios in dependence of switching frequency

The Table 9 explains the occurrence of diagnostics dependent on the switching frequencies for the disturbance "Short-Circuit-to-VBB".

**Table 9** Occurrence of diagnostics during the disturbance : Short-Circuit-to-VBB

	Reported diagnostic	Unwanted diagnostics at onset of SCV-diagnostics	Unwanted diagnostics when resolving SCV-diagnostics
<b>Stable switching frequency : f</b>			
permanently "low" : $f \leq 62,5 \text{ Hz}$	SCVx, OLx		OLx <sup>1)</sup>
permanently "intermediate" $62,5 \text{ Hz} < f < 2 \text{ kHz}$	SCVx, OLx	OLx <sup>2)</sup>	
permanently "high" $f \geq 2 \text{ kHz}$	SCVx, OLx	OLx <sup>2)</sup>	
<b>Transitions in the switching frequency : f</b>			
permanently "low" --> permanently "high" $f \leq 62,5 \text{ Hz} \rightarrow f \geq 2 \text{ kHz}$	SCVx, OLx	OLx <sup>1) 2)</sup> : depends on the time of onset and resolving of SCVx-disturbance	
permanently "high" --> permanently "low" $f \geq 2 \text{ kHz} \rightarrow f \leq 62,5 \text{ Hz}$	SCVx, OLx	OLx <sup>1) 2)</sup> : depends on the time of onset and resolving of SCVx-disturbance	

1) In Table 9 an additional OLx-signal can be generated when 1. the SCVx-disturbance has been resolved in the inactive phase and 2. the inactive phase is longer than 8 ms ( $f < 62,5 \text{ Hz}$ ) and 3. the SCVx-disturbance has been existing for  $\geq 6 \text{ ms}$  in the inactive phase.



### 3 Functional description

The occurrence of the additional OLIX-signal depends on the relative duration of the inactive mode and the SCVx-disturbance. It disappears at least after 4 ms or with continued switching of the power transistor. As the user himself has caused the additional OLIX-signal by resolving the SCVx-disturbance the user can ignore this signal for the next 4 ms or can continue switching the power transistor.

- 2) Depending on the onset of the SCVx-disturbance in scenarios with high or intermediate switching frequency one time an unwanted OLIX-reporting can occur which vanishes during further switching. As in the upper case 1) the user can ignore it as in the sequel the correct signaling occurs.

Table 10 explains the occurrence of diagnostics dependent on the switching frequencies for the disturbance "Open load".

Prerequisite : an external capacitor of  $C = 10 \text{ nF}$  (minimum value) for enhancing the EMI-robustness is attached to the output;  $V_{BB} = 24 \text{ V}$ .

In Table 10 the additional SCVx-diagnostic reflects the transition from active to inactive mode when the external capacitor (EMI-robustness) has to be discharged via a high ohmic internal resistor. During the discharging process the output voltage is in the region of reporting SCVx.

**Table 10 Occurrence of diagnostics during the disturbance : Wirebreak**

Stable switching frequency : $f$	Reported diagnostic	Comment
permanently "low" : $f \leq 50 \text{ Hz}$	OLIX, OLAX, SCVx	additionally SCVx <sup>1)</sup>
permanently "intermediate" $50 \text{ Hz} < f < 2 \text{ kHz}$	SCVx, OLAX	instead of OLIX : SCVx <sup>2)</sup>
permanently "high" $f \geq 2 \text{ kHz}$	SCVx, OLAX	instead of OLIX : SCVx <sup>2)</sup>
<b>Transitions in the switching frequency : <math>f</math></b>		
permanently "low" --> permanently "high" $f \leq 50 \text{ Hz} \rightarrow f \geq 2 \text{ kHz}$	OLIX, OLAX, SCVx --> SCVx, OLAX	additionally SCVx <sup>1)</sup>
permanently "high" --> permanently "low" $f \geq 2 \text{ kHz} \rightarrow f \leq 50 \text{ Hz}$	SCVx, OLAX --> OLIX, OLAX, SCVx	additionally SCVx <sup>1)</sup>

1) additionally SCVx reported, diagnostic due to discharging of the external capacitor (EMI-robustness)

2) instead of OLIX is SCVx reported, diagnostic due to discharging of the external capacitor (EMI-robustness)

#### 3.3.3.4 Global diagnostics

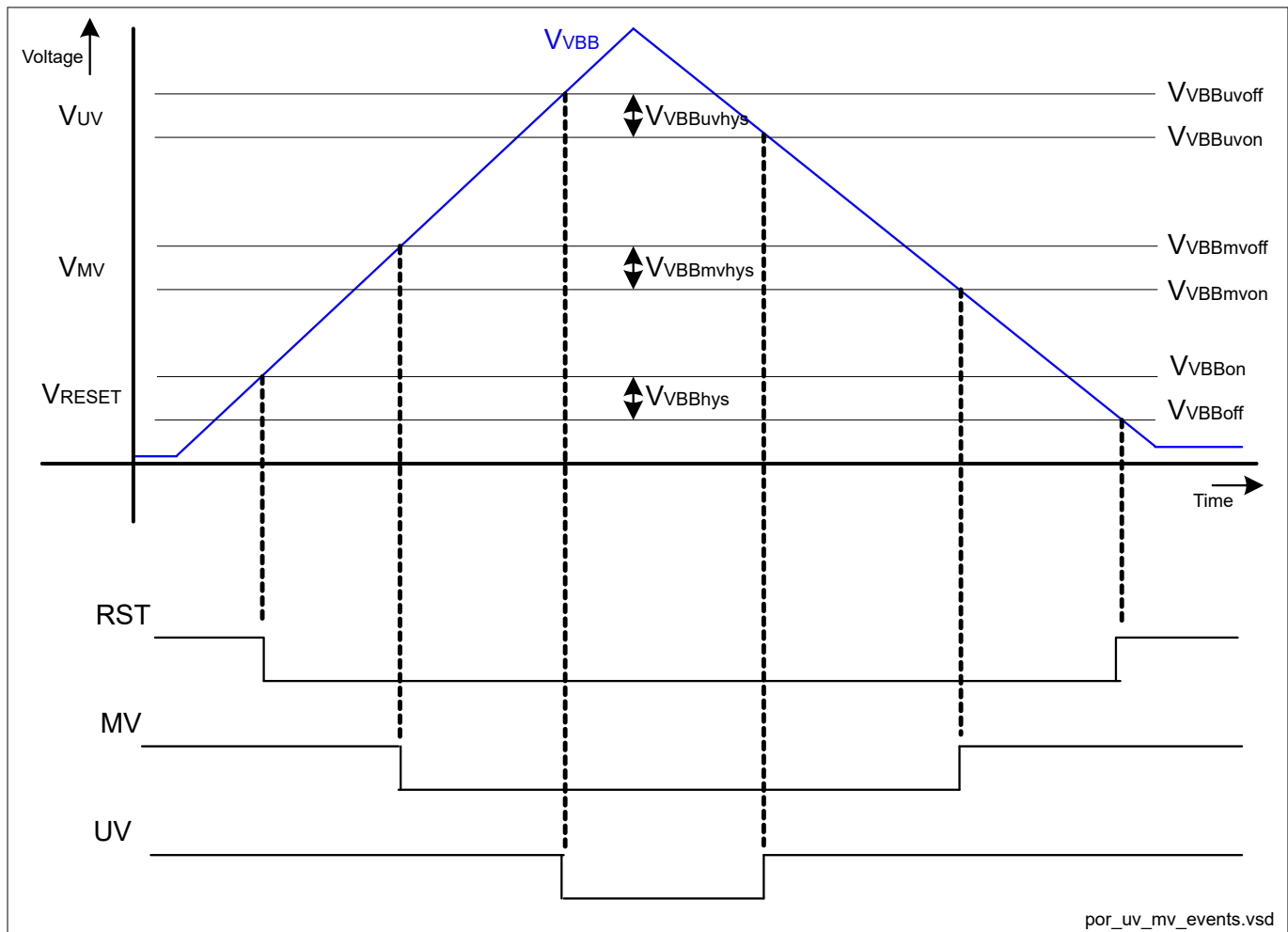
The global diagnostics include:

- **UV**: undervoltage supply condition when  $V_{BB}$  is below 16 V with 0.5 V hysteresis
- **MV**: missing voltage supply condition when  $V_{BB}$  is below 13 V with 0.5 V hysteresis
- **OTP**: global overtemperature (chip temperature outside the switch area triggers above 125 °C), the global over temperature does not lead to thermal shutdown
- **ALLOFF**: all drivers in the power chip are disabled either by DRIVE-programming,  $\overline{\text{ODIS}}$ -setting or temperature shutdown of all channels
- **LAMP**: the load of one of the drivers behaves like a cold lamp

### 3 Functional description

#### 3.3.3.5 Power supply

The startup procedure of the power chip is explained in Figure 22.



**Figure 22** Start up procedure of the power chip

During UVLO, all registers of the power chip are reset to their reset values as specified in the register description (Chapter 5). As a result, the flags **TE**, **UV** as well as **MV** are High and the  $\overline{ERR}$  pin is Low (error condition). Immediately after the reset is released, the chip is first configured by “reading” the logic level of the SEL, MS1, MS0 - pins. The IC powers up as a parallel device i.e. the AD0-7 pins are high-impedance until the IC configuration is completed.

The supply voltage VBB is monitored during operation by two internal comparators (with typ. 2 ms blanking time) detecting:

- **VBB Undervoltage:** If the voltage drops below the UV threshold, the UV-bit in the **GLERR** register is set High. The IC operates normally
- **VBB Missing Voltage:** If the voltage further drops below the MV threshold, lower than the previous threshold, the MV-bit in the GLERR is set. The Power Side of the chip is finally turned off when VBB is reaching the VReset-threshold whereas the Micro-Controller Side remains active

**Note:** The driver stage is self protected in overload condition: the internal switches will limit the current if an overload condition is detected and finally be turned off if the current limitation is leading to an overtemperature event. The affected channel will automatically re-start once it has cooled down (thermal toggling). By this implicitly affected channels re-start if the overload condition disappears.

### 3 Functional description

**Attention:** The UV- and MV-bits (as well as the TE-bit) are used for generating the  $\overline{ERR}$  signal. As the mentioned bits UV, MV are preset to High during UVLO the  $\overline{ERR}$  pin is Low after re-powering up. Therefore the  $\overline{ERR}$  requires to be explicitly cleared after power-up. At least one read access to GLERR and INTERR registers or one default read access for certain access-modes (see Chapter 3.2.3) is needed to update those status bits and thus release the  $\overline{ERR}$  pin.

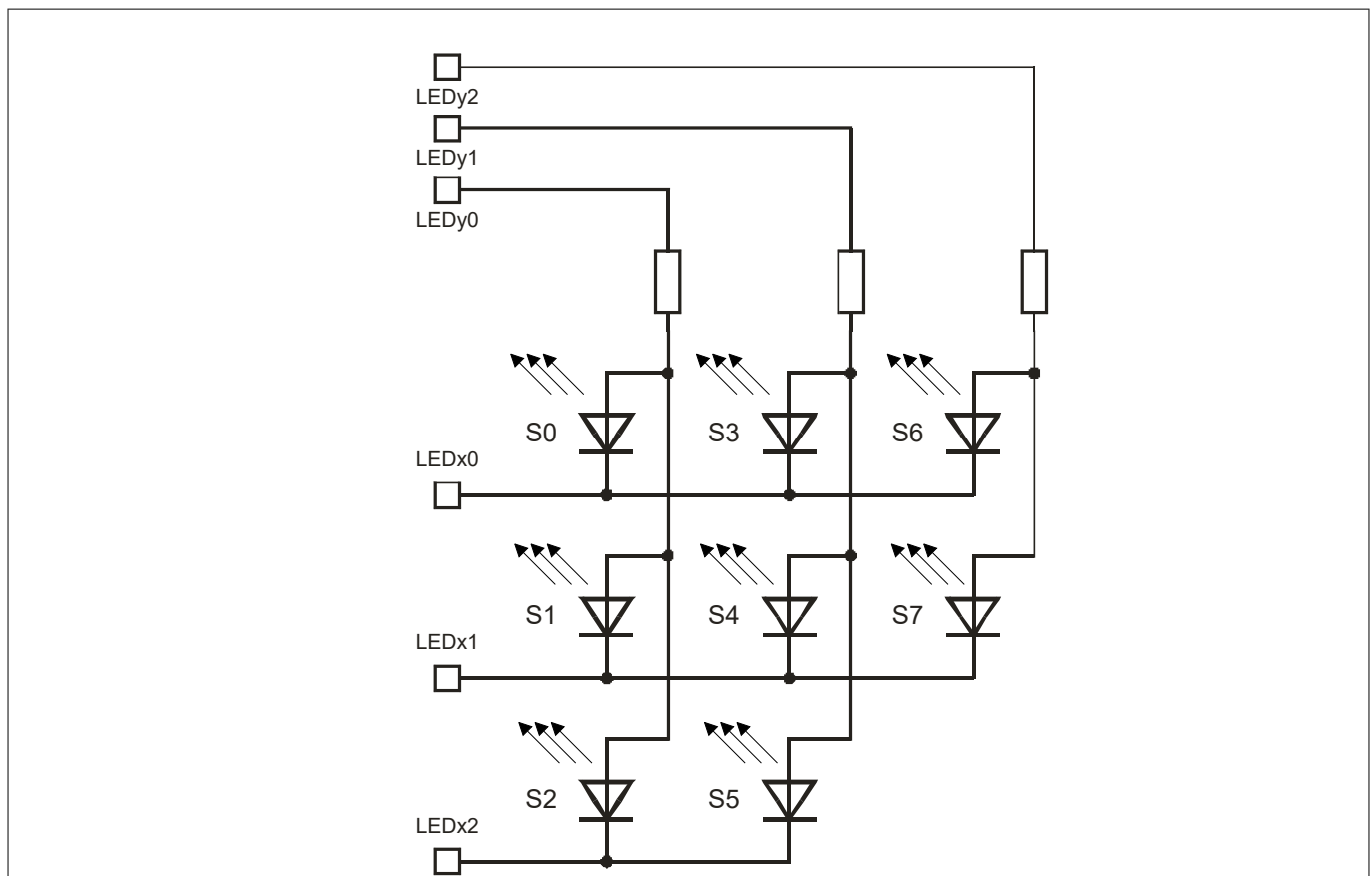
#### 3.3.4 LED matrix

The driving signal for the LED-matrix is the drive-signal of the register DRIVE gated with the signal LEDGx of the registers DIAG0,..., DIAG7. This signal is generated in the power chip and transferred via the CT-interface to the uC-Chip. To avoid that thermal toggling events (triggered by overcurrent and resulting thermal shutdown) become visible on the LED-matrix LEDGx disables the related LED for at least 100ms when an overtemperature (OTx) or overcurrent condition (OCLx) has occurred.

##### 3.3.4.1 LED matrix on the process side

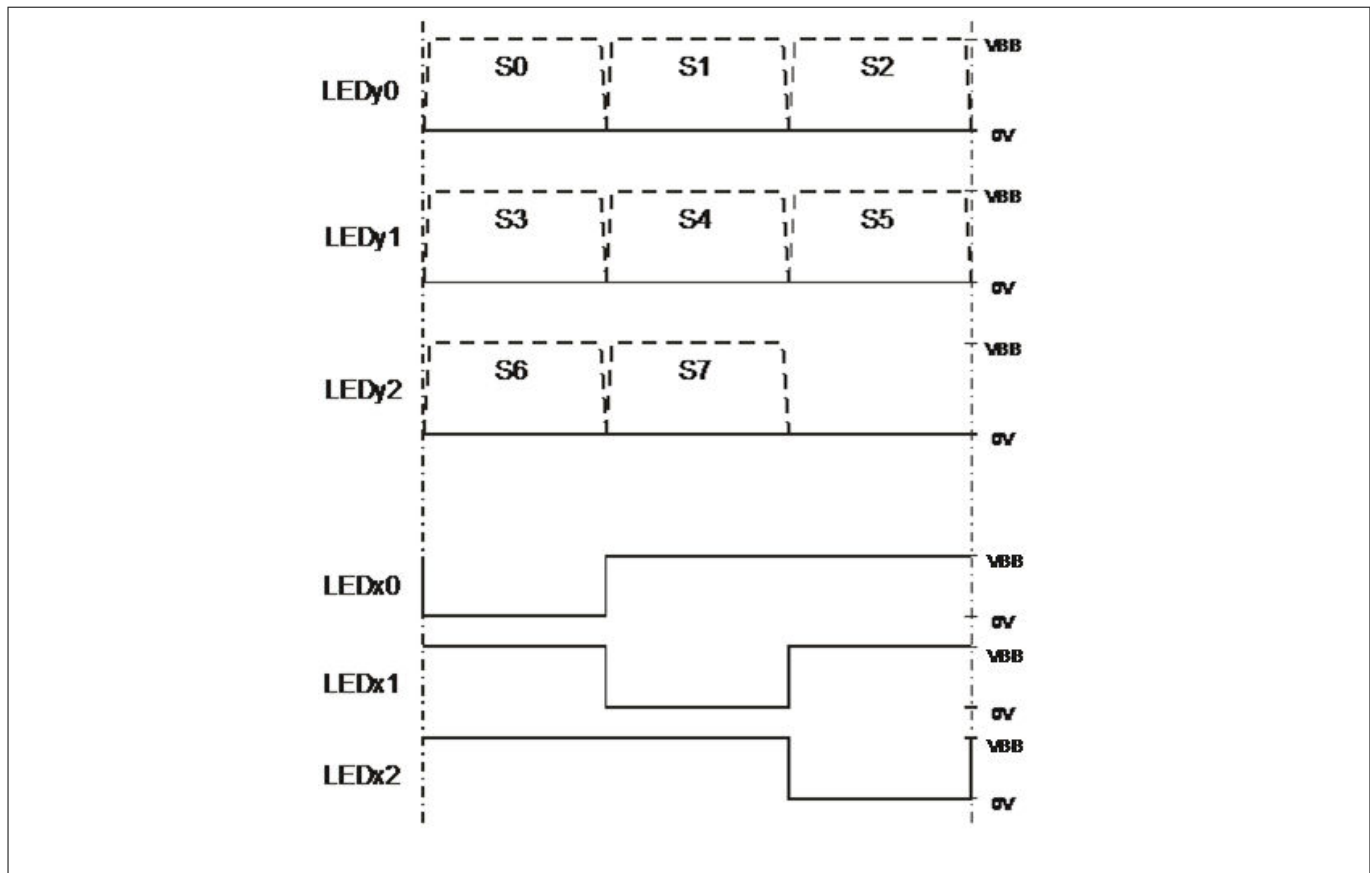
Eight LEDs arranged in a 3x3 matrix can be driven through the outputs LEDx0,1,2 and LEDy0,1,2 of the Power Chip. Each output channel has a corresponding status LED in the matrix showing the actual status of the channel. When the LED lights up, the corresponding channel is in the active mode and has no thermal shutdown and no overcurrent condition.

Series resistors must be inserted in each column line LEDy0,1,2 to set the LED current. The driving level on the column lines is the  $V_{BB}$  voltage level. The row lines are driven alternately with 1/3 duty cycle at 1000 Hz. The resulting average current for each LED is  $1/3 \cdot (V_{BB} \text{ minus diode forward voltage}) / \text{series resistance}$ . If the diode matrix is used, all 8 LEDs must be connected for a correct function of the matrix.



**Figure 23** LED matrix connected to the power chip

### 3 Functional description



**Figure 24** LED pulse diagram

If no LEDs are used at all it is possible (by reasons of EMI) to connect all column signals LEDy0,1,2 together and all row-signals LEDx0,1,2 together but a connection among columns and rows is not allowed. In the case of paralleling of channels it is possible to substitute the unused LEDs by resistors which have the only function to dissipate the current which is delivered in case the not existing diode is accessed. If no limiting element is used (i.e. resistor) the voltage at the LEDs of the non-activated rows can rise up to VBB if the non-existing element is activated (the related row activated and the corresponding column activated).

#### 3.3.4.2 LED matrix on the uController side (only in serial communication mode)

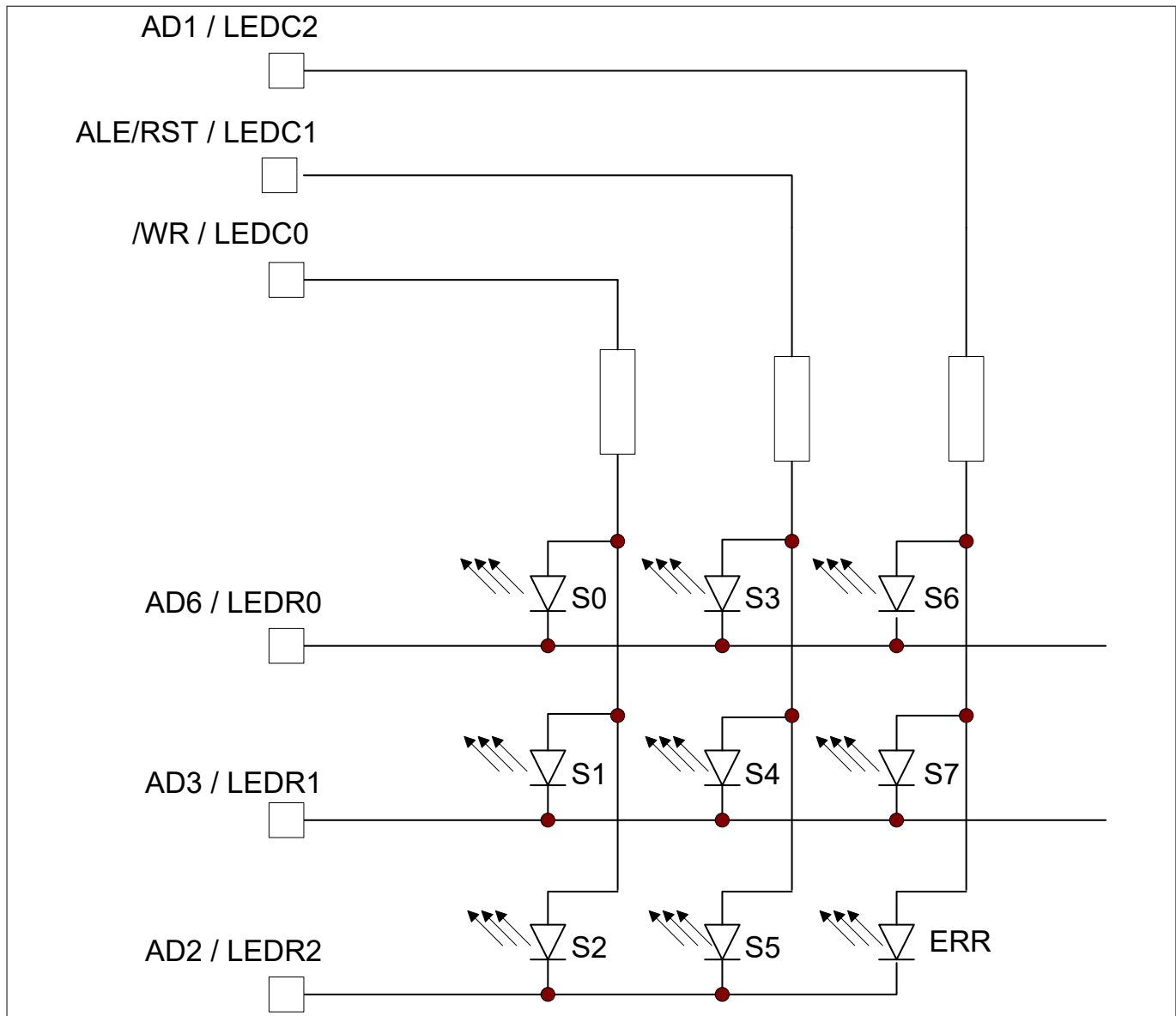
For the driving signals on the uController-side the following pins are used for the column signals : AD1/LEDC2, ALE/RST/LEDC1,  $\overline{WR}$ /LEDC0 and for the row-signals : AD2/LEDR2, AD3/LEDR1, AD6/LEDR0. For enabling the LED-function on the uC-Chip side the bit **LEDON** in the **GLCFG**-register has to be set. LED-operation is only possible in serial communication mode. If LEDON = 1 the hardware reset function is disabled.

As in the case for the LED on the power chipside a 3x3 matrix can be driven. Each output channel has a corresponding status LED in the matrix showing the actual status of the channel. When the LED lights up, the corresponding channel is in the active mode and has no thermal shutdown and no overcurrent condition. The 9.th LED is connected with the ERR-signal.

Series resistors must be inserted in each column line LEDC0...LEDC2 to set the LED current. The driving level on the column lines is the  $V_{CC}$  voltage level. The row lines are driven alternately with 1/3 duty cycle at 1000 Hz. The resulting average current for each LED is  $\frac{1}{3} \cdot (V_{CC} \text{ minus diode forward voltage}) / \text{series resistance}$ .

If the diode matrix is used (LEDON = 1) , all 9 LEDs must be connected for correct function of the matrix.

### 3 Functional description



**Figure 25 LED matrix connected to the uC-Chip**

In the case of paralleling of channels it is possible to substitute the unused LEDs by resistors which have the only function to dissipate the current which is delivered in case the not existing diode is accessed.

The minimum value of the VCC-voltage is 2.75 V. But this low voltage will limit the choice of the used LEDs (in the worst case only LEDs with a lower forward voltage of around 2.2 V are possible).

### 3.4 EMI-Robustness

Care has been taken to increase the Burst- and RFCM-robustness according to the standardization requirements referenced in

- DIN EN 61131-2 (Programmable Controllers , Part 2 : Equipment Requirements and Tests)
- IEC 61000 -4-4 (Testing and measurement techniques - electrical fast transient/burst immunity test)
- IEC 61000 -4-6 (Testing and measurement techniques - immunity to conducted disturbances, induced by radio-frequency fields)

respectively.

### 3 Functional description

As the standardization document DIN EN 61131-2 provides a system-requirement we can give only recommendations for the application with ISO2H823V2.5 for improving the EMI-robustness. Exact values have to be evaluated with the total system including external components and PCB-layout and wiring.

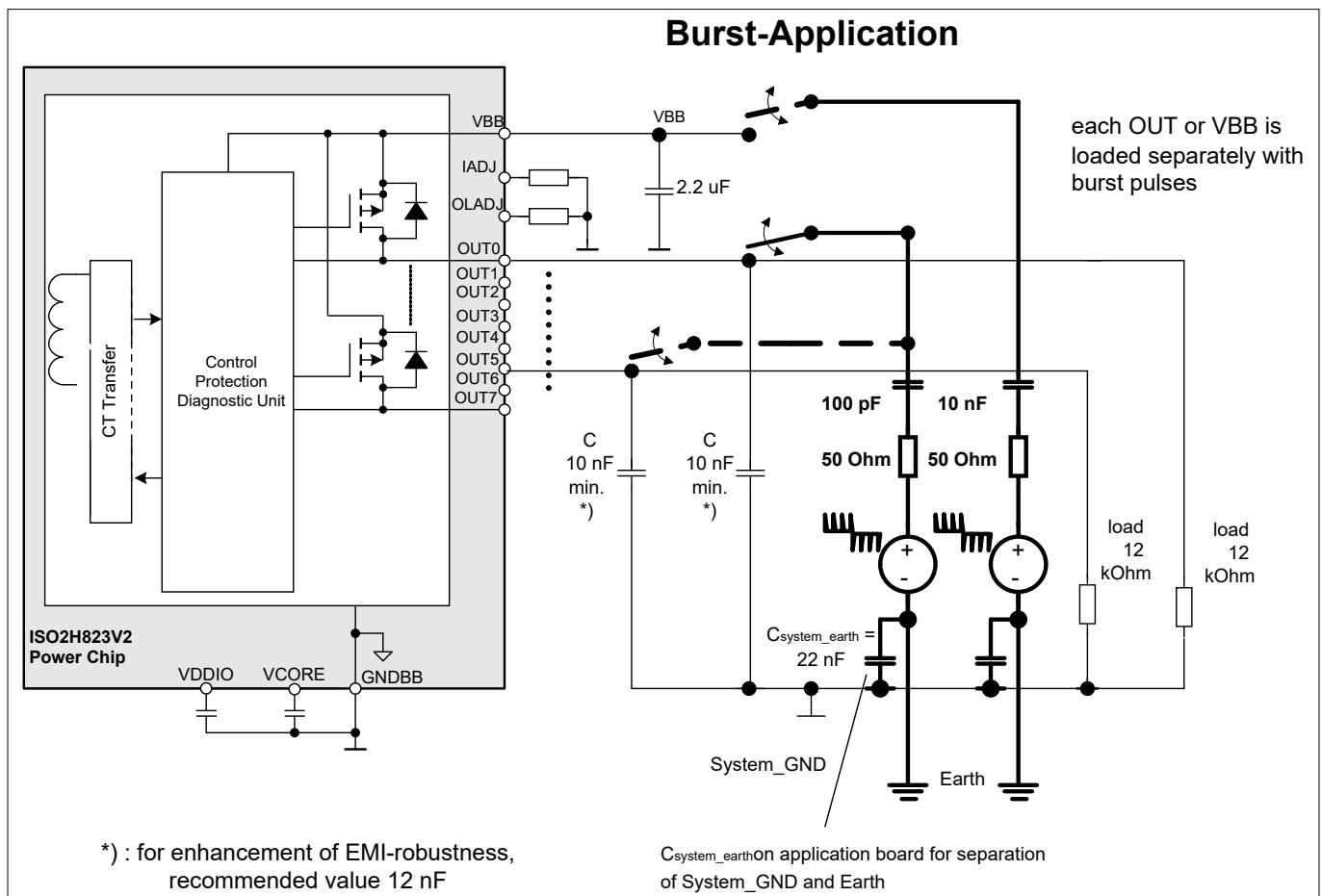
For Burst- and RFCM-robustness we consider only the driver-pins OUTx and VBB as these pins are exposed to external disturbances. Other pins of ISO2H823V2.5 are encapsulated within the housing of the control equipment (e.g. PLC).

The influence of HF-signals is eliminated internally with assistance of the external capacitors of min.10 nF ( $\pm 10\%$ ) at the output OUTx of each power transistor. To increase the safety margin if higher test voltages are applied it is possible to increase the capacitor up to  $12 \text{ nF} \pm 10\%$ . The purpose is to suppress frequency contributions of the external disturbance greater than 2 MHz.

Investigations have been done with an external load of a high value of 12 k $\Omega$ . Other critical loads consisting of a high inductive value combined by a high resistive value (e.g. 0.8 H, 1.4 k $\Omega$ ) have also been examined.

#### 3.4.1 Burst robustness

Figure 26 shows the test circuitry for applying burst pulses. The fat drawn equipment symbolizes the burst-generator and the coupling of burst pulses to the OUTx-pins and/or to the VBB-pin (see the different coupling network for OUTx, VBB as specified in IEC 61000).



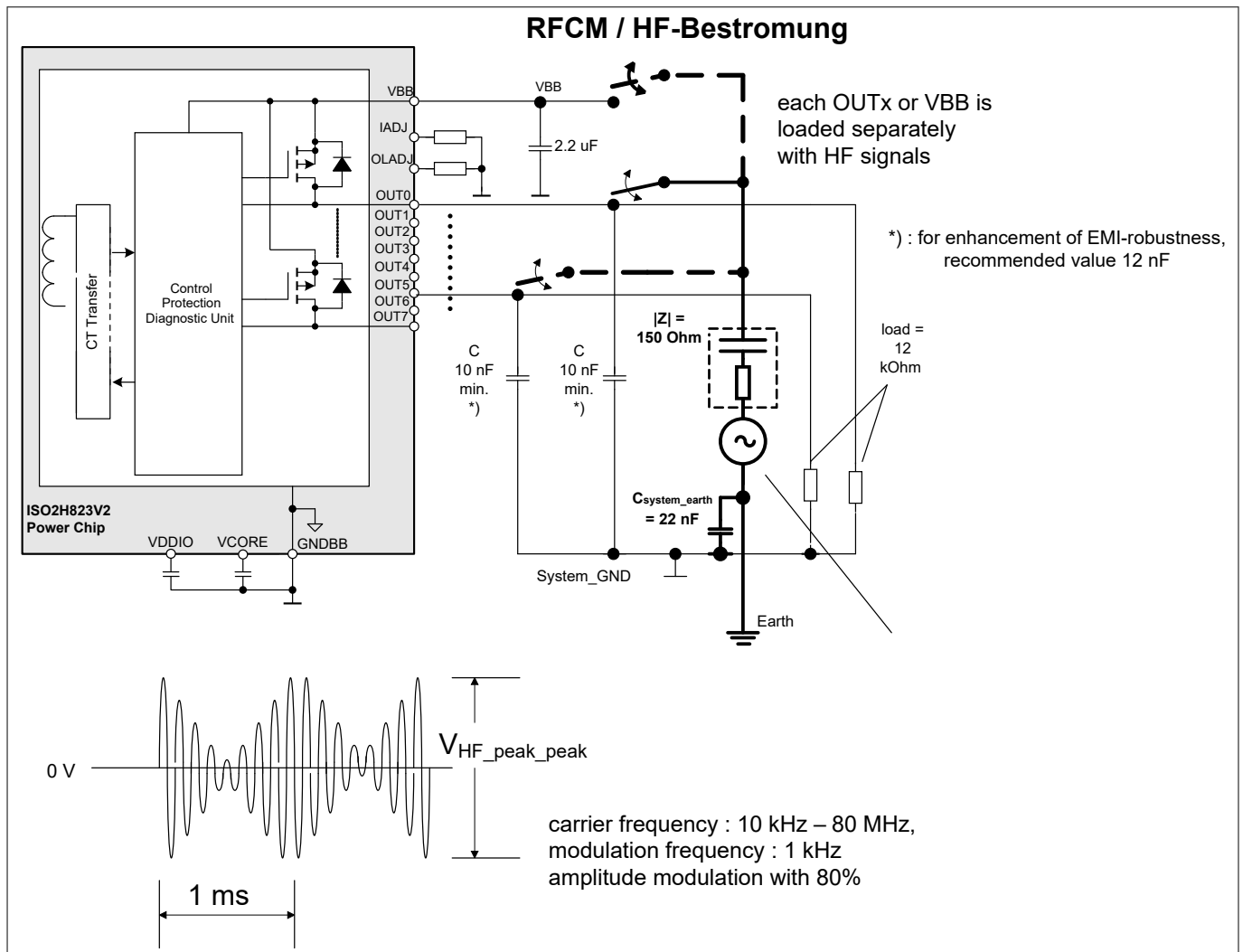
**Figure 26 Burst-Application**

For burst-disturbance the standard foresees 2 repetition frequencies : 5 kHz and 100 kHz. For the repetition frequency of 5 kHz the target is to achieve a burst-robustness of min.  $\pm 2500 \text{ V}$  within the system with external elements. For a repetition frequency of 100 kHz it is much harder to give an estimation without the knowledge of external elements. For this case no statement is given here.

## 3 Functional description

### 3.4.2 RFCM-Robustness

Figure 27 shows the test circuitry for applying RFCM frequencies. The fat drawn equipment symbolizes the HF-generator and the coupling of HF frequencies to the OUTx-pins and/or to the VBB-pin (the drawn coupling network shall symbolize an effective impedance of 150  $\Omega$  regardless of the frequency as specified in IEC 61000). The HF-disturbance is an 80%-amplitude modulated signal with the carrier frequency of 10 kHz - 80 MHz and the modulation frequency of 1 kHz.



**Figure 27 RFCM-Application**

The 80 % amplitude modulated signal is shown in Figure 27 in the lower half. With external elements on the user-PCB-board it is targeted to achieve a RFCM-robustness against the defined HF-signals of  $V_{HF\_peak\_peak} = \pm 25$  V.

## 3.5 Application hints

### 3.5.1 Layout recommendations

The reference resistor for CLKADJ must be placed close to the pin 38 (CLKADJ) and pin 39 (GND). Decoupling capacitors should be close to VCC terminal pin 37 and directly connected to the GND plane on the PCB.

GND and GNDBB must be totally isolated in the PCB layout. A separation distance of min. 3.2mm is recommended.

---

### **3 Functional description**

The reference resistors for OLADJ, IADJ must be placed close to their terminals of the ISO2H823V2.5 and the connection to the referring ground plane should be as short as possible. The capacitors for  $V_{CORE}$  and  $V_{DDIO}$  must be placed close to the pins and directly connected to the GNDBB plane.



## 4 Electrical characteristics

### 4 Electrical characteristics

**Note:** All voltages at pins 1 to 32 as well as 61 to 70 are measured with respect to GNDBB. All voltages at pins 33 to 60 are measured with respect to GND. The voltage levels are valid if other ratings are not violated. The two voltage domains  $V_{CC}$  and  $V_{BB}$  are internally galvanic isolated.

**Note:** All Typical Values are defined for  $T_j = 25^\circ\text{C}$ ,  $V_{BB} = 24\text{ V}$ ,  $V_{CC} = 3.3\text{ V}$ .

**Note:** Electrical Values are defined in the range  $T_j = -40 \dots 125^\circ\text{C}$ ,  $V_{BB} = 11 \dots 35\text{ V}$ ,  $V_{CC} = 2.75 \dots 3.6\text{ V}$ , unless otherwise specified, [Table 13](#) to [Table 26](#).

#### 4.1 Absolute maximum ratings

(at  $T_j = -40 \dots 135^\circ\text{C}$ , unless otherwise specified)

**Note:** Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 37 ( $V_{CC}$ ) is discharged before assembling the application circuit. Operating at absolute maximum ratings can lead to a reduced lifetime.

Absolute maximum ratings are not subject to production test.

**Table 11 Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage input interface	$V_{CC}$	-0.5	–	3.6	V	–
Supply voltage output interface	$V_{BB}$	-1 <sup>1)</sup>	–	45	V	–
Continuous voltage at data inputs (AD0 ... AD7)	$V_{Dx}$	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{CS}$	$V_{CS}$	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{ALE}$	$V_{ALE}$	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{RD}$	$V_{RD}$	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{WR}$	$V_{WR}$	-0.5	–	3.6	V	–
Continuous voltage at pin SYNC	$V_{SYNC}$	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{ODIS}$	$V_{ODIS}$	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{ERR}$	$V_{ERR}$	-0.5	–	3.6	V	–
Continuous voltage at pin SEL	$V_{SEL}$	-0.5	–	3.6	V	–
Continuous voltage at pin MSx	$V_{MSx}$	-0.5	–	3.6	V	–
Continuous voltage at pin CLKADJ	$V_{CLKADJ}$	-0.5	–	3.6	V	–
Continuous voltage at pin VCORE	$V_{VCORE}$	-0.5	–	1.65	V	–
Continuous voltage at pin VDDIO	$V_{VDDIO}$	-0.5	–	3.6	V	–
Continuous voltage at pin IADJ	$V_{IADJ}$	-0.5	–	3.6	V	–
Continuous voltage at pin OLADJ	$V_{OLADJ}$	-0.5	–	3.6	V	–
Continuous voltage at pin OUTx	$V_{OUTx}$	$V_{BB} - 55$	–	$V_{BB}$	V	–

(table continues...)

## 4 Electrical characteristics

**Table 11 (continued) Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Continuous voltage at pin LEDXx	$V_{LEDXx}$	-0.5	–	$V_{BB}$	V	–
Continuous voltage at pin LEDYx	$V_{LEDYx}$	-0.5	–	$V_{BB}$	V	–
Load current (short-circuit current)	$I_L$	–	–	Self limited	A	–
LED matrix driver current	$I_{LED}$	-20		20	mA	Peak current each LED
Static operating temperature	$T_{j\text{stat}}$	-40		Internal limited	°C	Static operation
Peak junction temperature	$T_{j\text{per}}$	–		175	°C	Periodic duty cycle <1%
Peak junction temperature	$T_{js}$	–		200	°C	Non periodic
Periodic temperature cycling	$\Delta T_{j\text{per}}$	–		75	K	$f = 2\text{ Hz}$
Transient thermal impedance all 8 channels	$Z_{th}$	–	0.375	–	K/W	12 ms sawtooth pulse, all channels equally loaded
Transient thermal impedance single channel	$Z_{th}$	–	3.5	–	K/W	50 ms sawtooth pulse 1 channel loaded
Storage Temperature	$T_{stg}$	-50	–	150	°C	–
Power Dissipation <sup>2)</sup>	$P_{tot}$	–	–	1.5	W	–
Inductive load switch-off energy dissipation for each channel, single pulse <sup>3)</sup> , all channels are switching simultaneously, $T_j = 125^\circ\text{C}$ , $I_L = 0.6\text{ A}$	$E_{AS}$	–		150	mJ	
Electrostatic discharge voltage (Human Body Model) according to JESD22-A114	$V_{ESD}$	–	–	2	kV	–
Electrostatic discharge voltage (Charge Device Model) according to JESD22-C101	$V_{ESD}$	–	–	0.5	kV	–

1) Defined by  $P_{tot}$ .

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip + Package) was simulated on a  $76.2 \times 114.3 \times 1.5\text{ mm}$  board with 2 inner copper layers ( $2 \times 70\text{ mm Cu}$ ,  $2 \times 35\text{ mm Cu}$ ). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Single pulse means that the thermal recovery time is sufficient so that an increase of the chip temperature is avoided or at least limited (depends on the thermal connection of chip with PCB-board, [Figure 34](#) - [Figure 36](#)).

## 4.2 Operating conditions and power supply

For proper operation of the device, absolute maximum rating ([Table 11](#)) and the parameter ranges in [Table 12](#) must not be violated. Exceeding the limits of operating condition parameters may result in device malfunction or spec violations. The power supply pins  $V_{BB}$  and  $V_{CC}$  have the characteristics given in [Table 14](#).

#### 4 Electrical characteristics

**Table 12** Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply Voltage Logic $V_{CC}$	$V_{VCC}$	2.75	–	3.6	V	Related to GND
Supply Voltage Power $V_{BB}$	$V_{VBB}$	11	–	35	V	Related to GNDBB
Ambient Temperature	$T_A$	-40	–	85	°C	–
Junction Temperature	$T_J$	-40	–	150	°C	–
Package Temperature	$T_{pack}$	-40	–	125	°C	Exposed Pad
Common Mode Transient	$dV_{ISO}/dt$	-25	–	25	kV/μs	<sup>1)</sup>
Magnetic Field Immunity	$ HIM $	30	–	–	A/m	IEC61000-4-8 <sup>1)</sup>
Bias Resistor for Current Limit	$R_{IADJ}$	6.46	6.81	7.14	kΩ	$C_{IADJ} < 25$ pF
Bias Resistor for Open Load	$R_{OLADJ}$	2.3	–	25	kΩ	$C_{OLADJ} < 25$ pF
Bias Resistor for CLKADJ	$R_{CLKADJ}$	9.9	10	10.1	kΩ	E96-resistor, $C_{CLKADJ} < 25$ pF

1) Not subject to production test, specified by design.

**Table 13** Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - case top <sup>1)</sup>	$R_{thJC\_Top}$	–	–	10.5	K/W	Measured on top side
Thermal resistance junction - case bottom <sup>1)</sup>	$R_{thJC\_Bot}$	–	–	0.5	K/W	–
Thermal resistance junction - pin <sup>1)</sup>	$R_{thJP}$	–	–	26	K/W	–
Thermal resistance <sup>1) 2)</sup>	$R_{th(JA)}$	–	23	–	K/W	–

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

**Table 14** Electrical Characteristics of the power supply pins

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
$V_{BB}$ UVLO startup threshold	$V_{VBBon}$	–	8.9	9.35	V	–
$V_{BB}$ UVLO shutdown threshold	$V_{VBBoff}$	7.5	7.9	–	V	–
$V_{BB}$ UVLO Hysteresis	$V_{VBBhys}$	–	1	–	V	–
$V_{BB}$ missing voltage OFF (MV) threshold	$V_{VBBmvoff}$	–	13.3	14.0	V	–

(table continues...)

#### 4 Electrical characteristics

**Table 14** (continued) Electrical Characteristics of the power supply pins

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
$V_{BB}$ missing voltage ON (MV) threshold	$V_{VBBmvon}$	12.1	12.8	–	V	–
$V_{BB}$ undervoltage OFF (UV) threshold	$V_{VBBuvoff}$	–	16.2	17.0	V	–
$V_{BB}$ undervoltage ON (UV) threshold	$V_{VBBuvon}$	14.9	15.7	–	V	–
Glitch filters for $V_{BB}$ missing voltage and undervoltage <sup>1)</sup>	$T_{VBBfil}$	–	2	–	ms	–
Undervoltage Current for $V_{BB}$	$I_{VBBuv}$	–	1.7	–	mA	$V_{VBB} < 7.0\text{ V}$
Quiescent Current $V_{BB}$	$I_{VBBq}$	–	9	–	mA	$V_{VBB} = 24\text{ V}$ , all channels inactive, $V_{CC} = 0\text{ V}$
Voltage Level of VDDIO	$V_{VDDIO}$	–	3.3	–	V	$V_{VBB} = 24\text{ V}$
Voltage Level of VCORE	$V_{VCORE}$	–	1.5	–	V	$V_{VBB} = 24\text{ V}$
Startup Delay (time between $V_{BBon}/V_{CCon}$ and first active mode) <sup>1)</sup>	$t_{VXXon}$	–	0.3	–	ms	–
$V_{CC}$ UVLO startup threshold	$V_{VCCoff}$	–	–	2.75	V	–
$V_{CC}$ UVLO shutdown threshold <sup>2)</sup>	$V_{VCCon}$	2.5	–	–	V	–
$V_{CC}$ UVLO threshold hysteresis	$V_{VCChys}$	0.01	–	–	V	–
Quiescent Current $V_{CC}$	$I_{VCCq}$	–	1.2	–	mA	$V_{VCC} = 2.4\text{ V}$
Current $V_{CC}$ without SPI-Activity	$I_{VCC}$	–	5.8	8.5	mA	$V_{VCC} = 3.6\text{ V}$
Current $V_{CC}$ without SPI-Activity	$I_{VCC}$	–	–	8	mA	$V_{VCC} = 3.3\text{ V}$
Current $V_{CC}$ without SPI-Activity	$I_{VCC}$	–	–	7	mA	$V_{VCC} = 2.75\text{ V}$

1) Not subject to production test, specified by design.

2) Note that the specified operation of the IC requires  $V_{VCC}$  as given in [Table 12](#).

## 4 Electrical characteristics

### 4.3 Load switching capabilities and characteristics

**Table 15** Load switching capabilities and characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
On-state resistance	$R_{ON}$	–	210	250	mΩ	$I_L = 0.6\text{ A}$ $T_j = 125\text{ °C}$ $V_{BB} = 24\text{ V}$ , Each channel
Leakage output current (included in $I_{BB(off)}$ )	$I_{L(off)}$	–	–	35	μA	$V_{ADx} = \text{low}$ , each channel, $x = 0, \dots, 7$ , $V_{BB} = 24\text{ V}$
Turn-on time to 90% $V_{OUT}$ <sup>1)</sup>	$t_{on}$	–	–	30	μs	$R_L = 48\text{ Ω}$ , $V_{ADx} = 0$ to 3.3 V, $V_{BB} = 24\text{ V}$
Turn-off time to 10% $V_{OUT}$ <sup>1)</sup>	$t_{off}$	–	–	30	μs	$R_L = 48\text{ Ω}$ , $V_{ADx} = 3.3$ to 0 V, $V_{BB} = 24\text{ V}$
Slew rate $V_{OUT}$	$dV/dt_{on}$	–	2	–	V/μs	$R_L = 48\text{ Ω}$ , $V_{BB} = 24\text{ V}$
Slew rate $V_{OUT}$	$-dV/dt_{off}$	–	2	–	V/μs	$R_L = 48\text{ Ω}$ , $V_{BB} = 24\text{ V}$

1) The turn-on and turn-off time includes the switching time of the high-side switch and the transmission time via the coreless transformer in normal operating mode. During a transmission error on the coreless transformer transmission turn-on or turn-off time can increase by up to 20 μs.

### 4.4 Output protection functions

**Table 16** Output protection functions<sup>1)</sup>

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Overload current limit	$I_{OCL}$	0.73	1	1.3	A	$V_{BB} - V_{out} = 1\text{ V}$
Short circuit current	$I_{SCL}$	0.7	1	1.4	A	$V_{BB} - V_{out} = 28.8\text{ V}$ <sup>2)</sup>
Output clamp (inductive load switch off) <sup>3)</sup> at $V_{OUT} = V_{BB} - V_{ON(CL)}$	$V_{ON(CL)}$	45	52	60	V	$I_{ON(CL)} = 50\text{ mA}$
Thermal overload trip temperature <sup>4)</sup>	$T_{jt}$	135	150	–	°C	–
Thermal hysteresis <sup>4)</sup>	$\Delta T_{jt}$	–	15	–	K	–

1) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

## 4 Electrical characteristics

- 2) Thermal effects when  $T_{\text{switch}} \gg T_{\text{case}}$   
 3) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest  $V_{\text{ON(CL)}}$ .  
 4) Not subject to production test, specified by design.

### 4.5 Electrical characteristics $\mu$ Controller interface

For the Parallel Mode see Table 17, Table 19, Table 23 and Table 25

For the Serial Mode see Table 17, Table 19, Table 24 and Table 25

Timing characteristics refer to  $C_L < 50$  pF and  $R_L > 10$  k $\Omega$

**Table 17** Setting at the configuration pin (CLKADJ)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
CLKADJ Pin Regulated Voltage	$V_{\text{CLKADJreg}}$	–	0.5	–	V	–

**Table 18** Error pins ( $\overline{\text{ERR}}$ ,  $\overline{\text{CRCERR}}$ )

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Error Voltage ( $\overline{\text{ERR}}$ , $\overline{\text{CRCERR}} = 0$ )	$V_{\text{ERR\_CRCERR}}$	–	–	$0.25 V_{\text{CC}}$	V	$I_{\text{ERR\_CRCERR}} = 5$ mA <sup>1)</sup>
Error Pin Pull-Up Resistance ( $\overline{\text{ERR}}$ , $\overline{\text{CRCERR}} = 1$ )	$R_{\text{ERR\_CRCERR pu}}$	–	50	–	k $\Omega$	–
Maximum Switching Frequency ( $\overline{\text{ERR}}$ , $\overline{\text{CRCERR}}$ ) <sup>2)</sup>	$f_{\text{SW}}$	–	200	–	kHz	10 k $\Omega$ external Pull-Up Resistor

- 1) Spikes on  $\overline{\text{CRCERR}}$  due to e.g. cross coupling between SCLK and  $\overline{\text{CRCERR}}$  are not expected to violate this figure  $V_{\text{ERR\_CRCERR}}$ , because cross coupling pulses are very small (10 nsec),  $V_{\text{ERR\_CRCERR}}$  is evaluated after the rising edge of  $\overline{\text{CS}}$  (and not during any edges of SCLK) and with a lower  $I_{\text{ERR\_CRCERR}}$  (e.g. 1 mA)  $V_{\text{ERR\_CRCERR}}$  is also lowered (in the example by a factor of 5).  
 2) Not subject to production test, specified by design; worst case is the reading in serial mode 2 with a frequency of 500 kHz  $\overline{\text{CRCERR}}$  can toggle with 500 kHz

**Table 19** Logical pins ( $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ , ALE, MS0/1,  $\overline{\text{CS}}$ , AD7: AD0, SCLK, SDO, SDI, SEL, SYNC,  $\overline{\text{ODIS}}$ )

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input Voltage High Level	$V_{\text{IH}}$	$0.7 \cdot V_{\text{CC}}$	–	$V_{\text{CC}} + 0.3$	V	–
Input Voltage Low Level	$V_{\text{IL}}$	$-0.3$ <sup>1)</sup>	–	$0.3 \cdot V_{\text{CC}}$	V	–
Input Voltage Hysteresis	$V_{\text{Ihys}}$	–	100	–	mV	–
Output Voltage High Level	$V_{\text{OH}}$	$0.75 \cdot V_{\text{CC}}$	–	$1 \cdot V_{\text{CC}}$	V	$I_{\text{OH}} = 5$ mA <sup>2)</sup>
Output Voltage Low Level	$V_{\text{OL}}$	0	–	$0.25 \cdot V_{\text{CC}}$	V	$I_{\text{OL}} = 5$ mA
Output Voltage High Level	$V_{\text{OH}}$	–	2.65	–	V	$V_{\text{CC}} = 2.75$ V, $I_{\text{OH}} = 1$ mA <sup>3)</sup>
Output Voltage Low Level	$V_{\text{OL}}$	–	0.1	–	V	$V_{\text{CC}} = 2.75$ V - 3.6 V, $I_{\text{OL}} = 1$ mA

- 1) Not subject to production test, specified by design.

#### 4 Electrical characteristics

- 2) Maximum source / sink current:  $I_{OHmax} = I_{OLmin} = 5 \text{ mA}$ ; external load  $C_L < 50 \text{ pF}$ ,  $R_L > 10 \text{ k}\Omega$
- 3) Same argumentation as for Digital Input Isoface: typical values over temperature derived for  $I_{OH} = 5 \text{ mA}$  and  $I_{OL} = 5 \text{ mA}$ . Extrapolation to  $I_{OH} = 1 \text{ mA}$  and  $I_{OL} = 1 \text{ mA}$  to possible. Voltage drop scales with a factor of 1/5 with the change of 5 mA to 1 mA. Not subject to production test.

**Table 20 SYNC-Timing**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Minimum time interval for $\mu\text{C}$ -Read-Access after falling edge of SYNC-signal	$t_{\text{syncmin}}$	400	500		ns	1)
Minimum width of SYNC-signal	$t_{\text{syncw}}$	200			ns	1)
SYNC-period	$t_{\text{syncper}}$	500			ns	1)
Minimum time interval for Direct-Write-Access after falling edge of SYNC-signal (to ensure that the new data are not CT-transmitted during SYNC = low)	$t_h$	400	500		ns	1)

1) not subject of production test, specified by design

**Table 21 RESYNCH-Timing**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Minimum width of SYNC-low-phase during resynchronization	$t_{\text{resynch}}$	7.0	–	240	us	1)
Minimum time interval between two resynchronization processes (minimum width of SYNC-high-phase)	$t_{\text{resync\_gap}}$	1.0			us	1)
Timing jitter of transmission of drive-data over CT	$t_{\text{resynch\_jitter}}$	-0.75	–	0.75	us	1)

1) not subject of production test, specified by design

**Table 22 Interface timing parameters**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
$\overline{\text{CS}}$ Disable time ( $\overline{\text{CS}}$ high time between two read accesses on different registers)	$t_{\text{CSD}}$		400		ns	1)
Read-Period for two read accesses on the same register (especially for COLDIAG, GLERR, INTERR)	$t_{\text{RD\_PER}}$		2000		ns	1)
$\overline{\text{CS}}$ Disable time ( $\overline{\text{CS}}$ high time between a write access and a read access for reading back the written value)	$t_{\text{CSD\_WRRD}}$		400		ns	1)

1) not subject of production test, specified by design

#### 4 Electrical characteristics

**Table 23**      **Parallel interface**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance (RD, WR, CS)	$R_{PU}$	–	50	–	kΩ	–
Input Pull Down Resistance (ALE)	$R_{PD}$	–	50	–	kΩ	–
CS setup time related to ALE	$t_{CS\_ALE}$	14			ns	
ALE high duration (for addressing)	$t_{ALE\_high}$	200			ns	
WR Low duration (for Write Data)	$t_{WRlow}$	100			ns	
WR High duration (for Write Data)	$t_{WRhigh}$	100			ns	
Read Request Frequency	$f_{RD}$	0.033 <sup>1)</sup>	–	2.5	MHz	repeated read access during $\overline{CS} = 0$
Read Request Period (1/ $f_{RD}$ )	$t_{RD}$	400	–	30000 <sup>2)</sup>	ns	repeated read access during $\overline{CS} = 0$
RD Low duration (by Read)	$t_{RDlow}$	200			ns	
AD7:AD0 Output disable time	$t_{float}$	20		80	ns	
AD0-7 Output Valid (by Read)	$t_{ADout}$			180	ns	
RD setup time	$t_{RD\_su}$	50			ns	
WR setup time	$t_{WR\_su}$	50			ns	
RD hold time	$t_{RD\_hd}$	20			ns	
WR hold time	$t_{WR\_hd}$	20			ns	
WR latency time	$t_{lat}$ <sup>3)</sup>		300		ns	
RD Pad to COLDIAG, GLERR and INTERR Registers Update (Bits Clearing)	$t_{clrrdy}$ <sup>4)</sup>		300		ns	
AD0-7 Data bus setup time	$t_{AD\_su}$	20			ns	
AD0-7 Data bus hold time	$t_{AD\_hd}$	60			ns	
Time for $\overline{CS} = \overline{WR} = ALE = 0$ , $\overline{RD} = 1$ until direct mode is entered	$t_{direct}$		30		us	

1) Minimum value to guarantee that the direct control mode is not entered, see also  $t_{RD}$  and  $t_{direct}$

2) After 30 us the interface may enter the direct control mode, see also  $t_{direct}$

3) not subject to production test,  $t_{lat}$  determined by internal synchronization cycles (internal clock 10 MHz) and propagation over CT (5 us)

4) not subject to production test,  $t_{clrrdy}$  determined by internal synchronization cycles (internal clock 10 MHz)



#### 4 Electrical characteristics

**Table 24**      **Serial interface**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance ( $\overline{CS}$ )	$R_{PU}$	–	50	–	k $\Omega$	–
Input Pull Down Resistance (SCLK, SDI)	$R_{PD}$	–	50	–	k $\Omega$	–
Serial Clock Frequency	$f_{SCLK}$	0.06	–	6	MHz	–
Serial Clock Period (1/fSCLK)	$t_{SCLK}$	166	–	–	ns	–
Serial Clock High Period	$t_{SCLKH}$	83	–	–	ns	–
Serial Clock Low Period	$t_{SCLKL}$	83	–	–	ns	–
$\overline{CS}$ Hold time (rising edge of SCLK to rising edge of $\overline{CS}$ )	$t_{CSH}$	100			ns	
Data setup time (required time SDI to rising edge of SCLK)	$t_{SU}$	20			ns	
Data hold time (rising edge of SCLK to SDI)	$t_{HD}$	20			ns	
$\overline{CS}$ falling edge to SDO output valid time	$t_{CS\_valid}$			150	ns	
$\overline{CS}$ falling edge to first rising SCLK edge	$t_{SCLK\_su}$	200			ns	
SCLK falling edge to SDO output valid time	$t_{SCLK\_valid}$			80	ns	
Minimum SDO Output disable time	$t_{float}$			90	ns	
New serial mode activation time (MS0/MS1 change to earliest interface access)	$t_{MS\_rdy}$		400		ns	no $\mu$ Controller access allowed during the change <sup>1)</sup> ( $\overline{CS} = 1$ )

1) not subject to production test, specified by design

**Table 25**       **$\overline{ODIS}$ , ALE/RST Timing**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance ( $\overline{ODIS}$ )	$R_{PU}$	–	50	–	k $\Omega$	–
Minimum width of $\overline{ODIS}$ -signal	$t_{ODISW}$	5	–		$\mu$ s	–
Minimal Duration for triggering Reset	$t_{RSTW}$	100	–	–	$\mu$ s	ALE/RST = $V_{CC}$ and $\overline{CS} = GND$

## 4 Electrical characteristics

### 4.6 Diagnostics

**Table 26** Channel specific diagnostics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Overload threshold	$ITH_{OCL}$	0.73	1	1.3	A	$R_{IADJ} = 6.81 \text{ k}\Omega$
Active open load threshold	$ITH_{OLA1}$	0.1	0.35	0.55	mA	$R_{OLADJ} = 24,3 \text{ k}\Omega$
Active open load threshold	$ITH_{OLA2}$	1.8	2.4	3.3	mA	$R_{OLADJ} = 3.48 \text{ k}\Omega$
Active open load threshold	$ITH_{OLA3}$	0.9	1.4	2.1	mA	$I_{OLADJ} = 200 \mu\text{A}^{1)}$
Inactive bypass current	$I_{OLI}$	10.0	21	32	$\mu\text{A}$	Including switch leakage
Inactive open load voltage	$V_{OLI}$	5.75	6.7	7.8	V	–
Inactive open load detection, On-threshold	$VTH_{OLI}$	5	5.4	5.75	V	–
Inactive short to $V_{BB}$ detection, On-threshold	$VTH_{SCV}$	8.4	9.2	10	V	take care when $V_{VBB} = V_{VBBmin} = 11 \text{ V}$ for stability of VBB (good buffering)
Overload filtering normal mode <sup>2)</sup>	$t_{FILT\_OCL}$	–	0.5	–	ms	for the thermal shutdown other value 50 $\mu\text{s}$
Overload filtering cold lamp mode <sup>2)</sup>	$t_{FILT\_COL}$	–	200	–	ms	–
Active open load blanking <sup>2)</sup>	$t_{blank\_OLA}$	–	6	–	ms	blanking time = filter length, other values 100 $\mu\text{s}$ , 0.5 ms, 1.0 ms <sup>3)</sup>
Inactive open load blanking <sup>2)</sup>	$t_{blank\_OLI}$	–	6	–	ms	blanking time = filter length, values 100 $\mu\text{s}$ , 0.5 ms, 1.0 ms
Inactive short to $V_{BB}$ blanking <sup>2)</sup>	$t_{blank\_SCV}$	–	6	–	ms	the blanking time for SCV is 6 ms but the internal filterlength is 2 ms , other values 100 $\mu\text{s}$ , 0.5 ms, 1.0 ms
LEDy matrix driver ON-resistance	$R_{ON\_LEDy}$	–	–	70	$\Omega$	Load current 10 mA, $V_{BB} = 24 \text{ V}$
LEDx matrix driver ON-resistance	$R_{ON\_LEDx}$	–	–	30	$\Omega$	Load current 30 mA, $V_{BB} = 24 \text{ V}$

- 1) A current of 200  $\mu\text{A}$  is forced out of the OLADJ Pin, this is equivalent to an nominal  $R_{OLADJ}$  of 6 k $\Omega$ .  $R_{OLADJ} = V_{OLADJ} / I_{OLADJ} = 1.2 \text{ V} / 200 \mu\text{A}$
- 2) all timing values defined and checked by design; test in production: structural test by SCAN-pattern plus test of internal oscillator frequency (24 MHz + 17,5 %)
- 3) other values 100  $\mu\text{s}$ , 0.5 ms, 1.0 ms are dynamically adapted to the switching frequency of the user

## 4 Electrical characteristics

### 4.7 Isolation and safety-related specification

Measured from input terminals to output terminals, unless otherwise specified

**Table 27 Isolation and Safety-Related Specification**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Rated dielectric isolation voltage <sup>1)</sup>	$V_{ISO}$	2500	–	–	VAC	1 - minute duration <sup>2)</sup>
Short term temporary overvoltage	$V_{IOTM}$	4250	–	–	Vpk	1s
Minimum external air gap (clearance)		–	3.5	–	mm	Shortest distance through air
Minimum external tracking (creepage)		–	3.5	–	mm	Shortest distance path along body
Minimum Internal Gap		–	0.01	–	mm	Isolation distance through insulation

1) The dielectric withstand voltage class (Nennisolationsklasse) is: 500 V.

2) The parameter is not subject to production test, verified by characterization.

### Approvals

UL508, CSA C22.2 NO. 14

Certificate Number: 20090514-E329661

### 4.8 Reliability

For Qualification Report please contact your local Infineon Technologies office!

## 4 Electrical characteristics

### 4.9 Typical performance characteristics

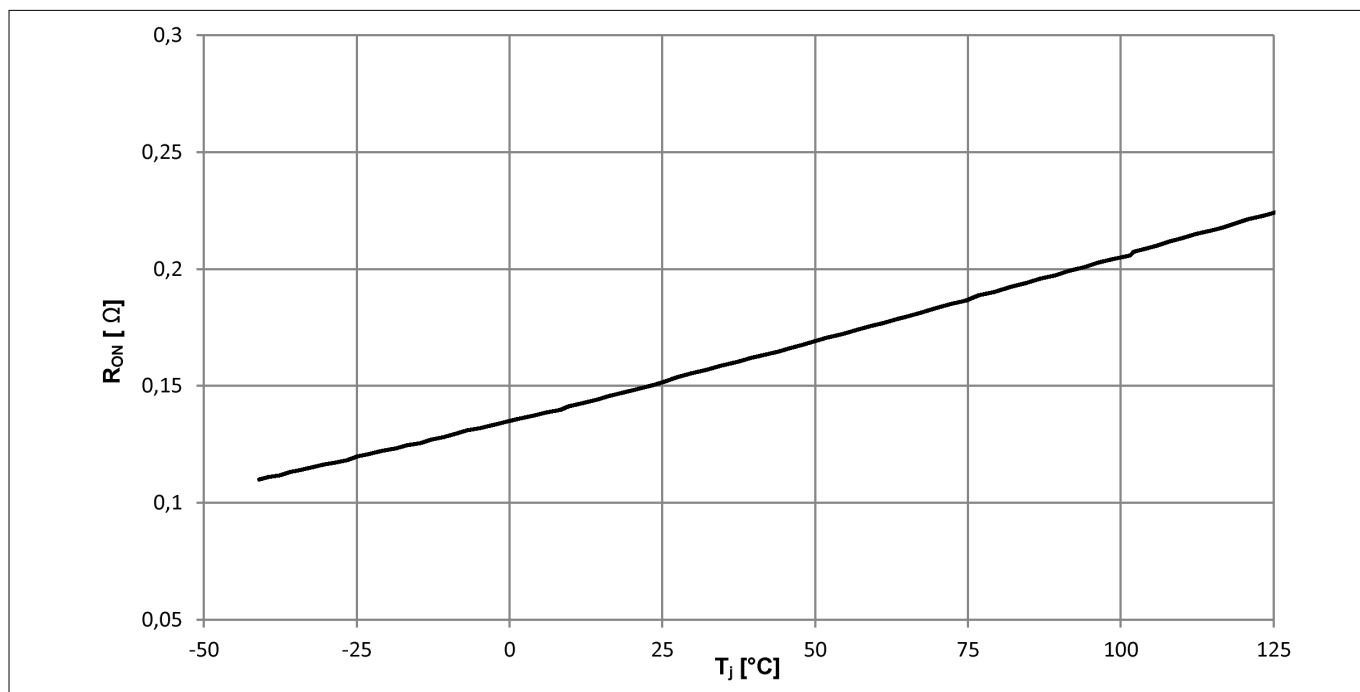


Figure 28 Typ. On-State Resistance ( $R_{ON} = f(T_j)$ ,  $I_L = 0.6$  A,  $V_{BB} = 24$  V,  $V_{in} = \text{high}$ )

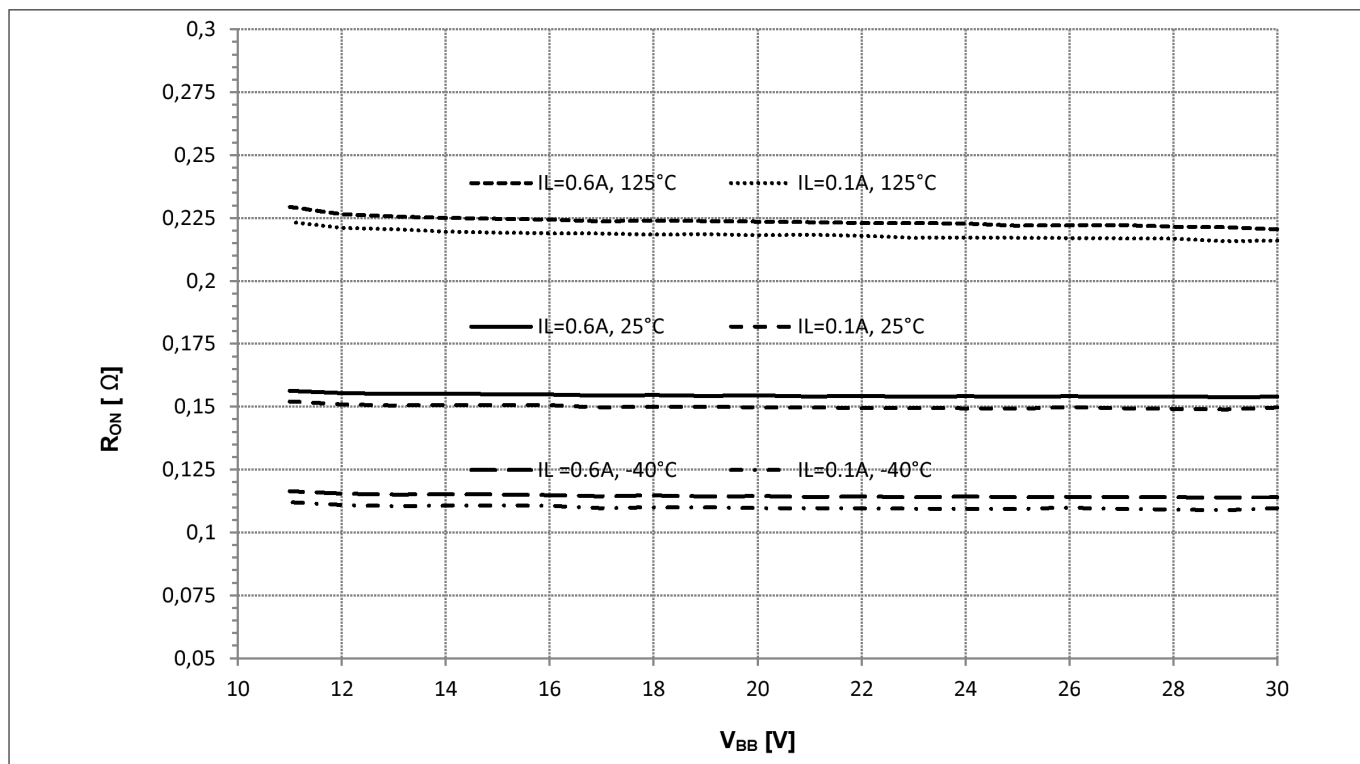
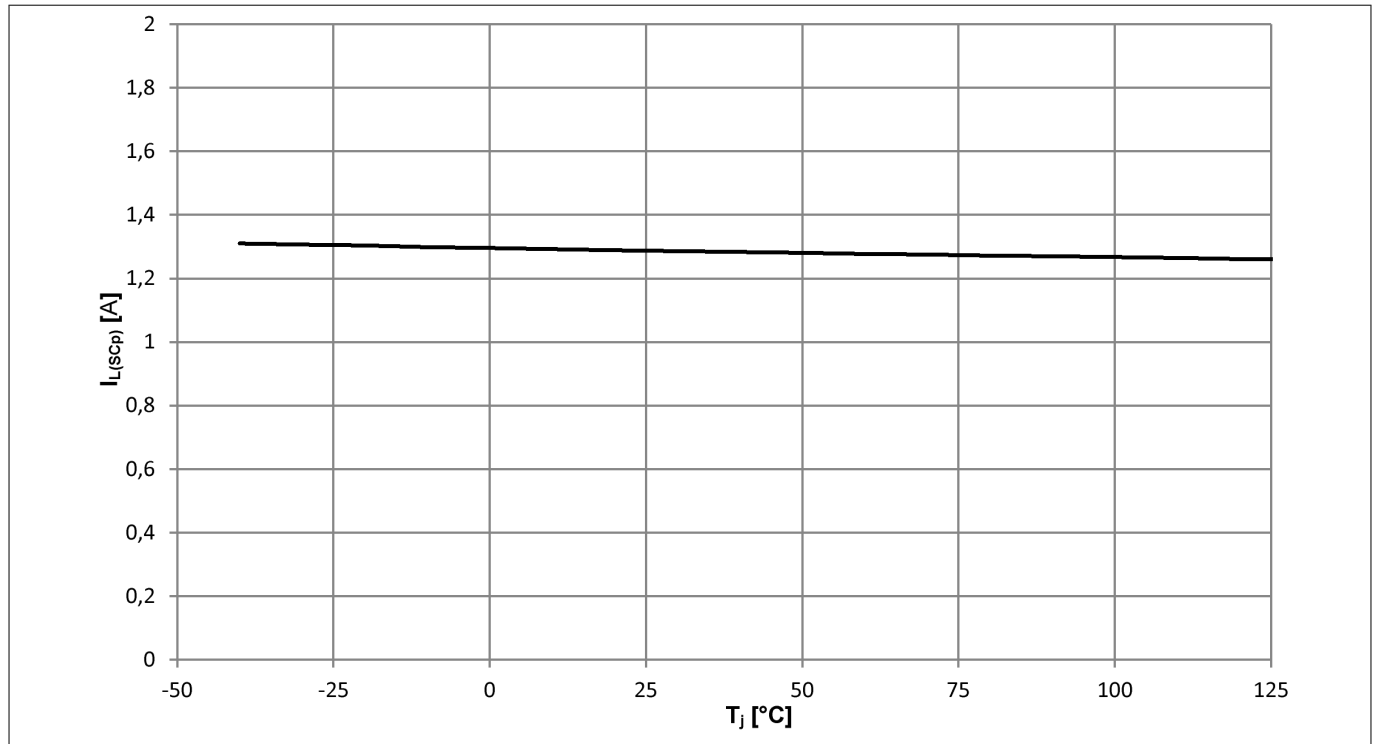
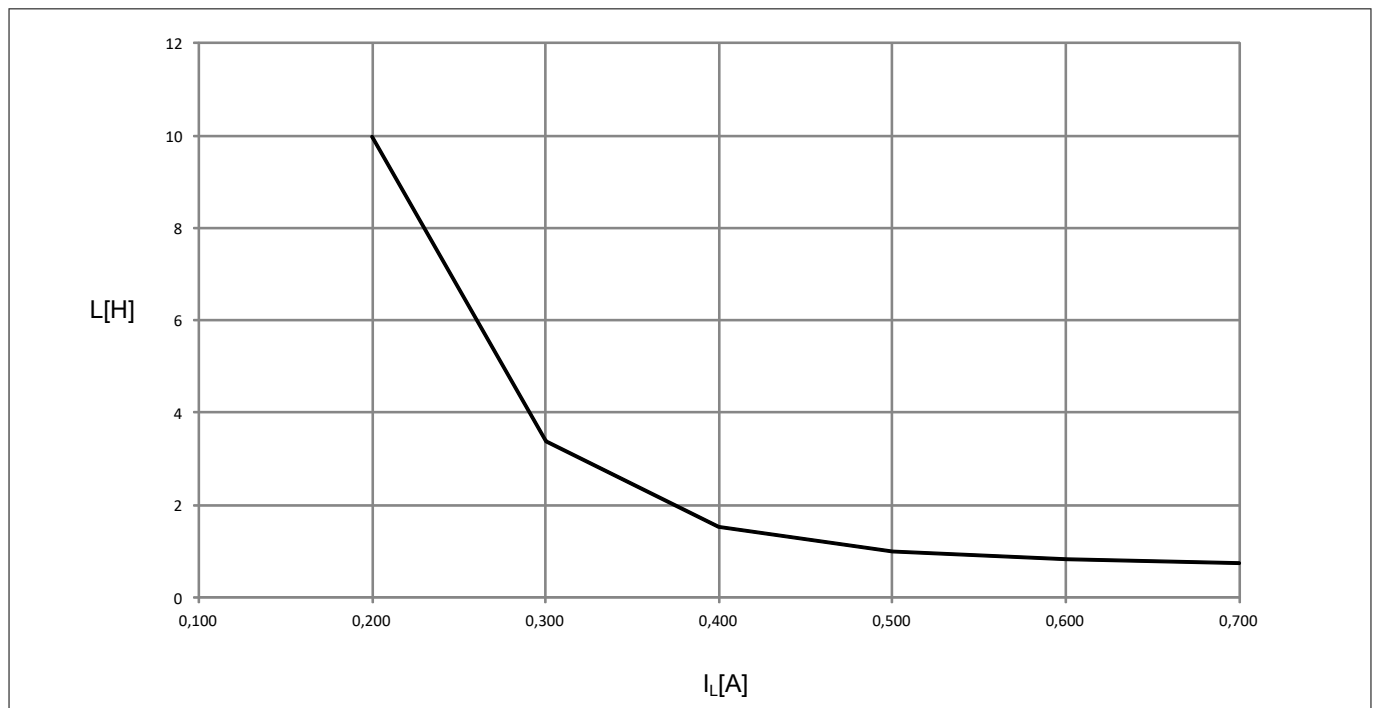


Figure 29 Typ. On-State Resistance ( $R_{ON} = f(V_{BB})$ ,  $I_L = 0.6$  A,  $I_L = 0.1$  A,  $V_{in} = \text{high}$ )

#### 4 Electrical characteristics

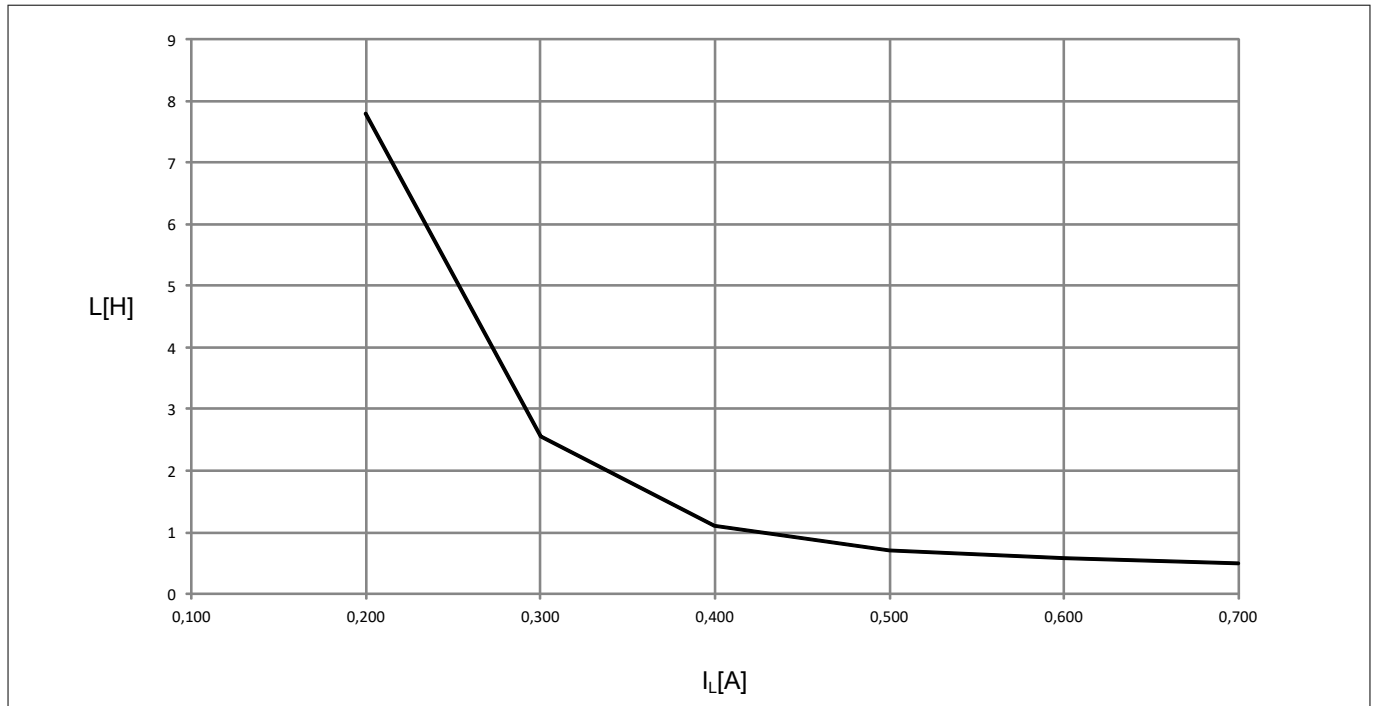


**Figure 30** Typical Initial Peak Short Circuit Current Limit vs  $T_j$  ( $I_{L(SCP)} = f(T_j)$ ,  $V_{BB} = 24$  V, output switched on with a short circuit present at the output)

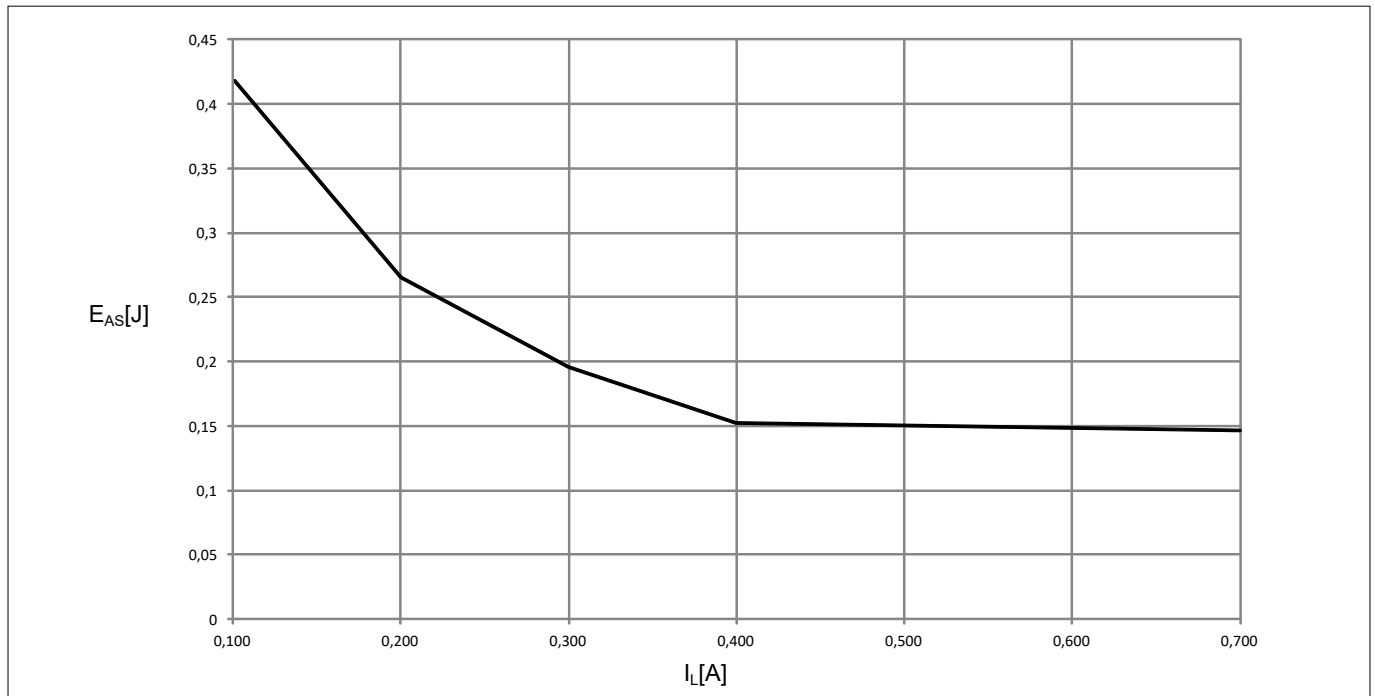


**Figure 31** Maximum allowable load inductance for a Single Switch-OFF of each channel; calculated ( $L = f(I_L)$ ,  $T_{jstart} = 125^\circ\text{C}$ ,  $V_{BB} = 24$  V,  $R_L = 48 \Omega$ , all channels are switching simultaneously)

#### 4 Electrical characteristics



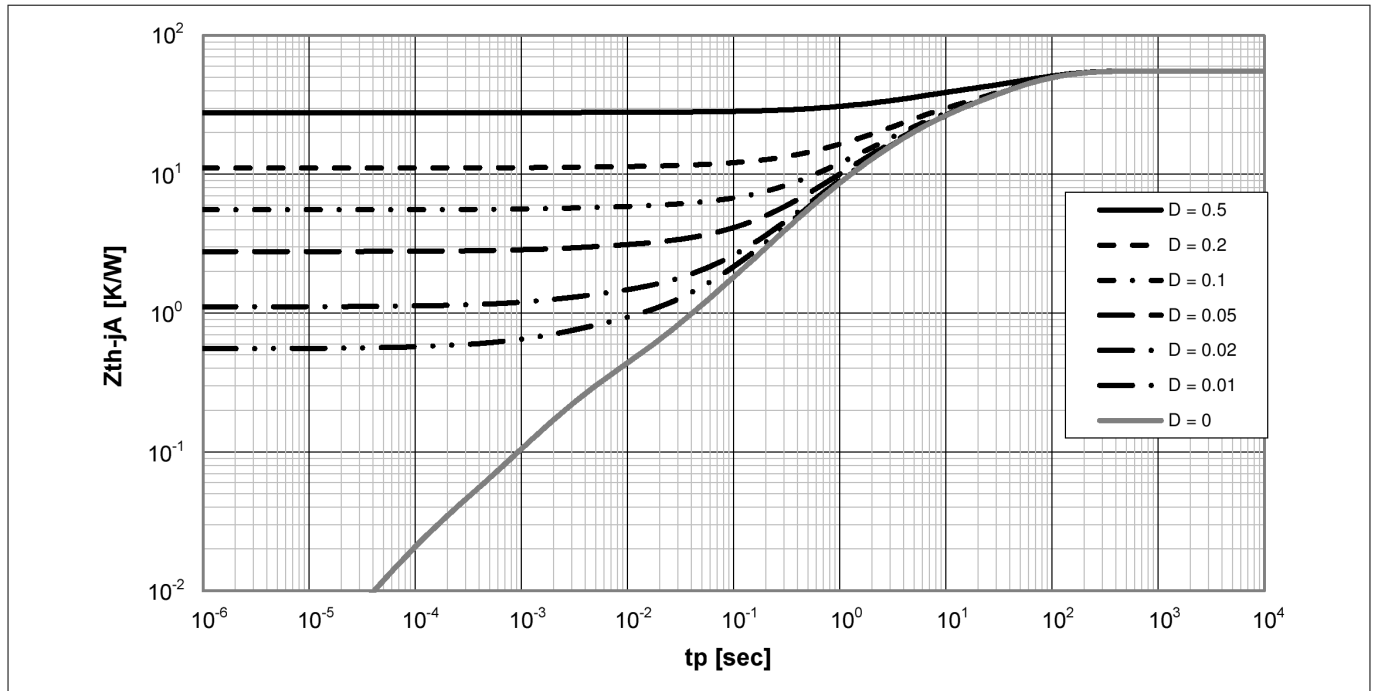
**Figure 32** Maximum allowable load inductance for a Single Switch-OFF of each channel; calculated ( $L = f(I_L)$ ,  $T_{jstart} = 125\text{ °C}$ ,  $V_{BB} = 24\text{ V}$ ,  $R_L = 0\text{ }\Omega$ , all channels are switching simultaneously)



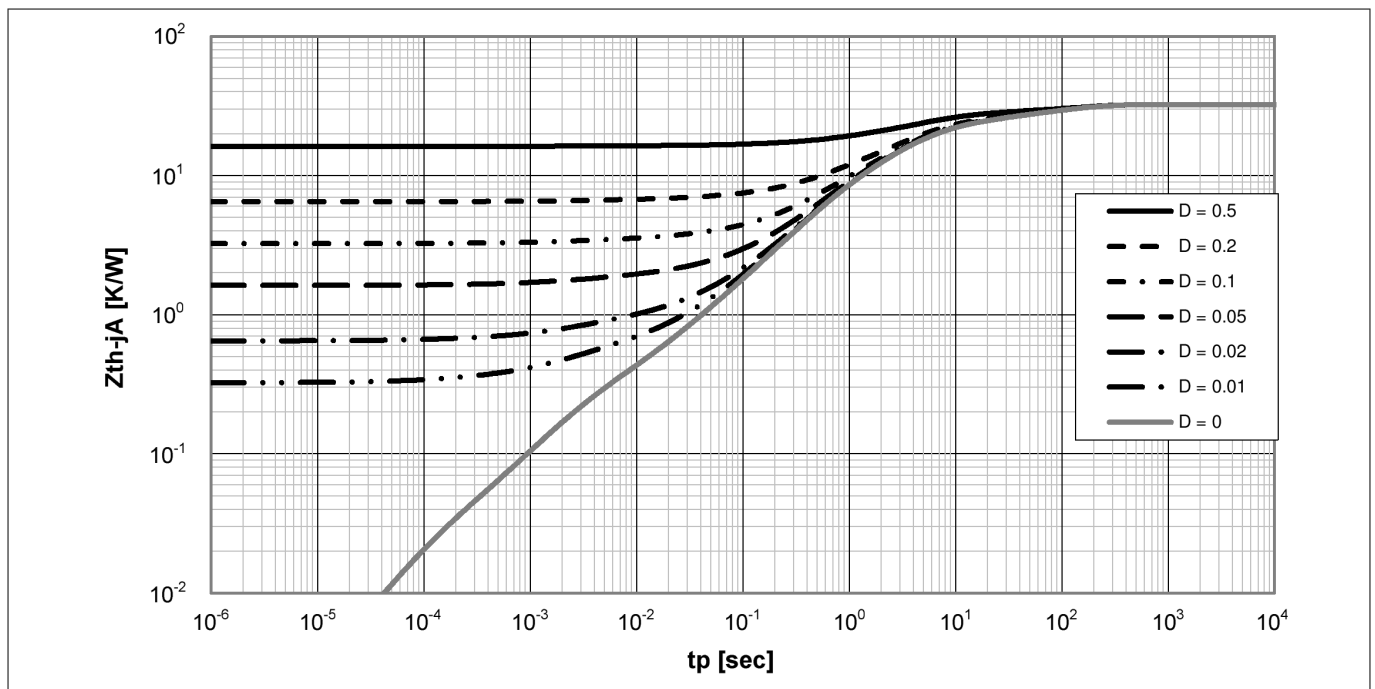
**Figure 33** Maximum Allowable Inductive Switch Off Energy, Single Pulse for Each Channel ( $E_{AS} = f(I_L)$ ,  $T_{jstart} = 125\text{ °C}$ ,  $V_{BB} = 24\text{ V}$ , all channels are switching simultaneously)<sup>2)</sup>

<sup>2)</sup> Single pulse means that the thermal recovery time is sufficient so that an increase of the chip temperature is avoided or at least limited (depends on the thermal connection of chip with PCB-board, [Figure 34](#) - [Figure 36](#)) .

#### 4 Electrical characteristics



**Figure 34** Typ. Transient Thermal Impedance 1s0p ( $Z_{thJA} = f(t_p)$ ; Parameter:  $D = t_p/T$ ; Product simulated on a 76.2 x 114.3 x 1.5 mm 1s0p board according JEDEC JESD 51-3



**Figure 35** Typ. Transient Thermal Impedance 2s2p no vias ( $Z_{thJA} = f(t_p)$ ; Parameter:  $D = t_p/T$ ; Product simulated on a 76.2 x 114.3 x 1.5 mm 2s2p board without thermal vias used in the exposed pad area according JEDEC JESD 51-5,7

#### 4 Electrical characteristics

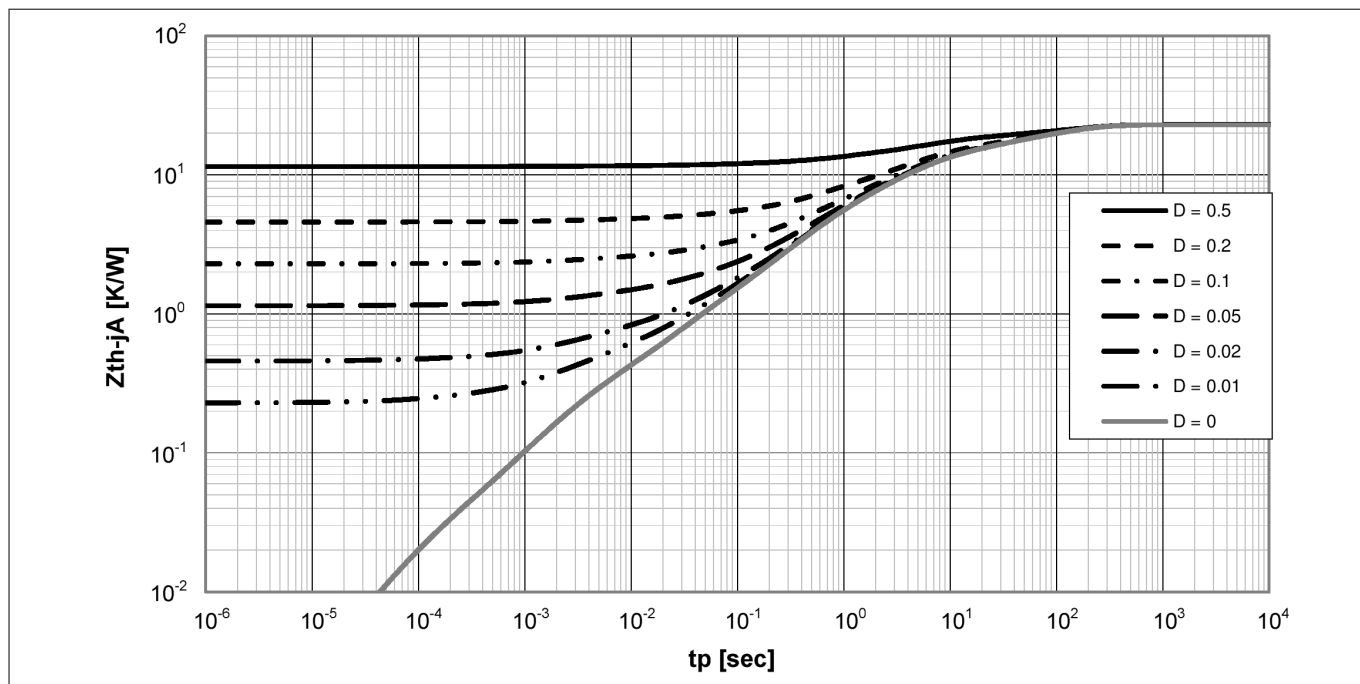


Figure 36

Typ. Transient Thermal Impedance 2s2p ( $Z_{thJA} = f(t_p)$ ; Parameter:  $D = t_p/T$ ; Product simulated on a 76.2 x 114.3 x 1.5 mm 2s2p board with thermal vias connected to the first inner copper layer in the exposed pad area according JEDEC JESD 51-5,7



## 5 µController interface registers

This section presents the user registers.

### Access conventions

**Table 28** Register access definition

Type	Symbol	Description
Read	r	The bit can be read
Read only, updated by hardware	h	The bit is updated by the device itself (for instance: sticky bit)
Write	w	The bit can be written

### Presentation

The User Registers are 8-bit wide and can be accessed over either the serial or the parallel interface. The [Table 29](#) lists the registers of the chip. The address is 8-bit whereby the MSB is used to indicate whether it is a write access (MSB=1) or Read access (MSB=0). The address is even i.e. the LSB is ignored (for addressing). The default selected register is the [DRIVE](#) register for write access.

**Table 29** Register overview

Register short name	Register long name	Offset address	Page number
<a href="#">µController interface registers, User registers</a>			
<a href="#">DRIVE</a>	Output Driver Register (rw)	00 <sub>H</sub>	<a href="#">58</a>
<a href="#">DRIVE_RESYNCH</a>	Output Driver Register for Resynchronization (rw)	1C <sub>H</sub>	<a href="#">59</a>
<a href="#">COLDIAG</a>	Collective Diagnostics Register (rh)	02 <sub>H</sub>	<a href="#">60</a>
<a href="#">GLERR</a>	Global Error Register (rh)	04 <sub>H</sub>	<a href="#">62</a>
<a href="#">DIAGCFG</a>	Channel Diagnostics Configuration Register (rw)	06 <sub>H</sub>	<a href="#">62</a>
<a href="#">DIAG0</a>	Diagnostics Register for Channel-0 (rh)	08 <sub>H</sub>	<a href="#">64</a>
<a href="#">DIAG1</a>	Diagnostics Register for Channel-1 (rh)	0A <sub>H</sub>	<a href="#">65</a>
<a href="#">DIAG2</a>	Diagnostics Register for Channel-2 (rh)	0C <sub>H</sub>	<a href="#">65</a>
<a href="#">DIAG3</a>	Diagnostics Register for Channel-3 (rh)	0E <sub>H</sub>	<a href="#">65</a>
<a href="#">DIAG4</a>	Diagnostics Register for Channel-4 (rh)	10 <sub>H</sub>	<a href="#">65</a>
<a href="#">DIAG5</a>	Diagnostics Register for Channel-5 (rh)	12 <sub>H</sub>	<a href="#">65</a>
<a href="#">DIAG6</a>	Diagnostics Register for Channel-6 (rh)	14 <sub>H</sub>	<a href="#">65</a>
<a href="#">DIAG7</a>	Diagnostics Register for Channel-7 (rh)	16 <sub>H</sub>	<a href="#">65</a>
<a href="#">INTERR</a>	Internal Error Register (rh)	18 <sub>H</sub>	<a href="#">65</a>
<a href="#">GLCFG</a>	Global Configuration Register (rwh)	1A <sub>H</sub>	<a href="#">67</a>

The registers are addressed wordwise.

## 5 µController interface registers

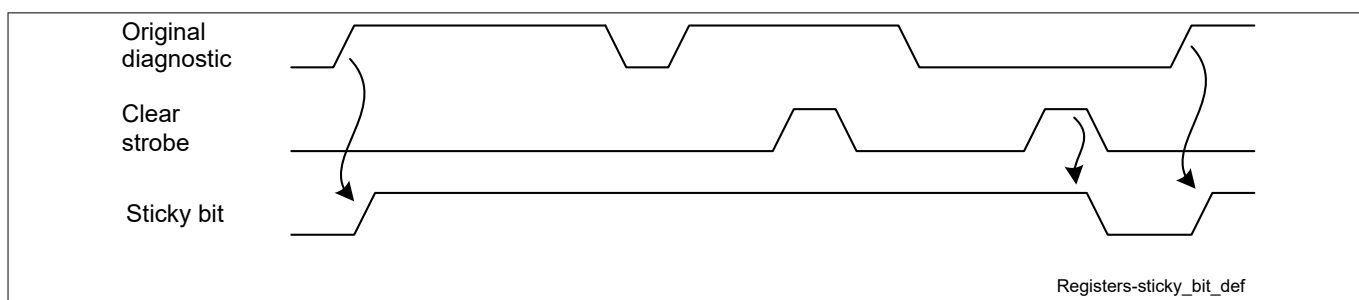
### 5.1 User registers

These registers can be accessed via the serial or parallel interface. The default selected register is the **DRIVE** register for write access.

#### Update of the diagnostics registers

The different faults monitored at each output channel are filtered with blanking time units. They are then stored in registers and sent over the Coreless Transformer to the µController-Interface chip with an update rate of 35 µs.

On the µController-Interface side, the diagnostics are stored in an intermediate register bank to be processed as sticky bits: once a fault is detected (and received) the corresponding bit is set and remains set even if the fault disappears. The bit can only be cleared once the fault is not detected anymore and the clearing was requested by a serial or parallel access (see [Figure 37](#)).



**Figure 37** Sticky Bit Operation

#### 5.1.1 Output Driver register

This register contains the command for the 8 output channels. When the pin  $\overline{\text{ODIS}}$  is High, the output channels are controlled as set by this register. When the  $\overline{\text{ODIS}}$  is Low, the output channels are immediately turned off and the contents of the **DRIVE** register is cleared.

DRIVE Offset: 00<sub>H</sub> Address: 00<sub>H</sub>  
Output Driver Register (rw) Reset value: 00<sub>H</sub>

7	6	5	4	3	2	1	0
SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SW7	7	rw	<b>Output Driver Control for Channel 7</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
SW6	6	rw	<b>Output Driver Control for Channel 6</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.

(table continues...)

## 5 µController interface registers

(continued)

Field	Bits	Type	Description
SW5	5	rw	<b>Output Driver Control for Channel 5</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
SW4	4	rw	<b>Output Driver Control for Channel 4</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
SW3	3	rw	<b>Output Driver Control for Channel 3</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
SW2	2	rw	<b>Output Driver Control for Channel 2</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
SW1	1	rw	<b>Output Driver Control for Channel 1</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
SW0	0	rw	<b>Output Driver Control for Channel 0</b> This bit field controls the state of the output driver. 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.

### 5.1.2 Output Driver register for resynchronization

This register contains the command for the 8 output channels for resynchronization. It has to be written in case a resynchronization of the CT-transmission is desired. Then the contents of [DRIVE\\_RESYNCH](#) is used for the CT-transmission instead of the contents of [DRIVE](#).

DRIVE\_RESYNCH                      Offset: 1C<sub>H</sub>                      **Address:**                      00<sub>H</sub>  
Output Driver                      **Reset value:**                      00<sub>H</sub>  
Register (rw)

7	6	5	4	3	2	1	0
<b>RW7</b>	<b>RW6</b>	<b>RW5</b>	<b>RW4</b>	<b>RW3</b>	<b>RW2</b>	<b>RW1</b>	<b>RW0</b>
rw	rw	rw	rw	rw	rw	rw	rw

## 5 µController interface registers

Field	Bits	Type	Description
RW7	7	rw	<b>Output Driver Resynchronization Control for Channel 7</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
RW6	6	rw	<b>Output Driver Resynchronization Control for Channel 6</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
RW5	5	rw	<b>Output Driver Resynchronization Control for Channel 5</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
RW4	4	rw	<b>Output Driver Resynchronization Control for Channel 4</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
RW3	3	rw	<b>Output Driver Resynchronization Control for Channel 3</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
RW2	2	rw	<b>Output Driver Resynchronization Control for Channel 2</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
RW1	1	rw	<b>Output Driver Resynchronization Control for Channel 1</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.
RW0	0	rw	<b>Output Driver Resynchronization Control for Channel 0</b> This bit field controls the state of the output driver 0 <sub>B</sub> The channel output is inactive. 1 <sub>B</sub> The channel output is driven.

### 5.1.3 Collective Diagnostics register

This register contains the overall diagnostics for each of the 8 output channels. Each channel-bit corresponds to the OR-combination of the [SCVx](#), [OCLx](#), [OLIx](#), [OLAx](#) and [OTx](#)-bits of the enabled diagnostic functions. This register contains the state of the channel diagnostics. On read access the internal diagnostic data is cleared and the [DIAG0](#),..., [DIAG7](#) registers are updated (see [Update of the Diagnostics Registers](#)). In serial mode 0 and 1 the update of the [DIAG0](#),..., [DIAG7](#) is generated automatically after every access whereas in serial modes 2 and 3 as well as in parallel mode the [DIAG0](#),..., [DIAG7](#) registers are updated after each direct access to the [COLDIAG](#) register.

5 µController interface registers

COLDIAG

Offset: 02<sub>H</sub>

Address:

00<sub>H</sub>

Collective  
Diagnostics Register  
(rh)

Reset value:

00<sub>H</sub>

7	6	5	4	3	2	1	0
<b>CH7</b>	<b>CH6</b>	<b>CH5</b>	<b>CH4</b>	<b>CH3</b>	<b>CH2</b>	<b>CH1</b>	<b>CH0</b>
rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CH7	7	rh	<b>Overall Diagnostics for Channel 7</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.
CH6	6	rh	<b>Overall Diagnostics for Channel 6</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.
CH5	5	rh	<b>Overall Diagnostics for Channel 5</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.
CH4	4	rh	<b>Overall Diagnostics for Channel 4</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.
CH3	3	rh	<b>Overall Diagnostics for Channel 3</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.
CH2	2	rh	<b>Overall Diagnostics for Channel 2</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.
CH1	1	rh	<b>Overall Diagnostics for Channel 1</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.
CH0	0	rh	<b>Overall Diagnostics for Channel 0</b> This bit field indicates the overall diagnostics. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.

## 5 µController interface registers

### 5.1.4 Global Error register

This register contains the overall status of the IC parameters monitored during system operation. The bits are routed to the  $\overline{\text{ERR}}$  pin as well (see Table 3). The UV and MV bits are reset to High during UVLO. In some operation modes, the register needs to be read to clear these bits and release the  $\overline{\text{ERR}}$  pin (see “Update of GLERR, INTERR-Reg”). The CF-bit is the OR-combination of COLDIAG bits.

GLERR Offset: 04<sub>H</sub> Address: 00<sub>H</sub>  
Global Error Register Reset value: 46<sub>H</sub>  
(rh)

7	6	5	4	3	2	1	0
<b>Vers_3</b>	<b>Vers_2</b>	<b>Vers_1</b>	<b>Vers_0</b>	<b>RES</b>	<b>UV</b>	<b>MV</b>	<b>CF</b>
r	r	r	r	r	rh	rh	rh

Field	Bits	Type	Description
Vers_3	7	r	<b>Actual : "0"</b>
Vers_2	6	r	<b>Actual : "1"</b>
Vers_1	5	r	<b>Actual : "0"</b>
Vers_0	4	r	<b>Actual : "0"</b>
RES	3	r	<b>Reserved</b> Returns 0 when read.
UV	2	rh	<b>VBB Undervoltage</b> This bit field indicates if an undervoltage condition has been detected at VBB. 0 <sub>B</sub> No undervoltage detected. 1 <sub>B</sub> Undervoltage detected.
MV	1	rh	<b>VBB Missing Voltage</b> This bit field indicates if a missing voltage condition has been detected at VBB. 1 <sub>B</sub> No Missing Voltage detected. 0 <sub>B</sub> Missing Voltage detected.
CF	0	rh	<b>Common Diagnostics Fault</b> This bit field is the OR-combination of all bits of the COLDIAG register. 0 <sub>B</sub> No fault is detected. 1 <sub>B</sub> At least one failure is detected.

### 5.1.5 Channel Diagnostics Configuration register

This register enables the diagnostics for each channel and selects whether the channel collective diagnostic bit is updated in the COLDIAG register (and as a consequence reflected in the CF-bit field of the GLERR register and at the  $\overline{\text{ERR}}$  pin).

DIAGCFG Offset: 06<sub>H</sub> Address: 00<sub>H</sub>  
Channel Diagnostics Configuration Register (rw) Reset value: FF<sub>H</sub>

5 µController interface registers

7	6	5	4	3	2	1	0
<b>DIAGEN7</b>	<b>DIAGEN6</b>	<b>DIAGEN5</b>	<b>DIAGEN4</b>	<b>DIAGEN3</b>	<b>DIAGEN2</b>	<b>DIAGEN1</b>	<b>DIAGEN0</b>
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DIAGEN7	7	rw	<b>Enables Diagnostics for Channel 7</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.
DIAGEN6	6	rw	<b>Enables Diagnostics for Channel 6</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.
DIAGEN5	5	rw	<b>Enables Diagnostics for Channel 5</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.
DIAGEN4	4	rw	<b>Enables Diagnostics for Channel 4</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.
DIAGEN3	3	rw	<b>Enables Diagnostics for Channel 3</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.
DIAGEN2	2	rw	<b>Enables Diagnostics for Channel 2</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.
DIAGEN1	1	rw	<b>Enables Diagnostics for Channel 1</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.

(table continues...)

5 µController interface registers

(continued)

Field	Bits	Type	Description
DIAGEN0	0	rw	<b>Enables Diagnostics for Channel 0</b> This bit field enables all the channel diagnostics. 0 <sub>B</sub> All the channel diagnostics are disabled. 1 <sub>B</sub> The channel diagnostics are enabled and updated in the <a href="#">COLDIAG</a> register.

### 5.1.6 Diagnostics registers for channel-x

These registers contain the individual diagnostics bits for a given channel. The bit field [LEDGx](#) is not used in the [COLDIAG](#) register (and as a consequence it is not reflected in the [CF](#)-bit and at the ERR pin). All bits are sticky (see [Update of the Diagnostics Registers](#)). The diagnostics are enabled with the [DIAGCFG](#) register.

DIAGO	Offset: 08 <sub>H</sub>	Address:	00 <sub>H</sub>
Diagnostics Register for Channel-0 (rh)		Reset value:	00 <sub>H</sub>

7	6	5	4	3	2	1	0
<b>RES</b>	<b>RES</b>	<b>LEDGx</b>	<b>SCVx</b>	<b>OCLx</b>	<b>OLAx</b>	<b>OLIx</b>	<b>OTx</b>
r	r	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
RES	7	r	<b>Reserved</b> returns 0 if read.
RES	6	r	<b>Reserved</b> returns 0 if read.
LEDGx	5	rh	<b>Gated LED Drive Information of Channel x (Active Mode only)</b> This bit field indicates that the led of this channel is gated due to overcurrent or over-temperature conditions. 0 <sub>B</sub> LED not gated 1 <sub>B</sub> LED gated
SCVx	4	rh	<b>Short Circuit to VBB at Channel x (Inactive Mode only)</b> This bit field indicates that a short circuit to VBB has been detected. 0 <sub>B</sub> No short circuit to VBB detected. 1 <sub>B</sub> A short circuit to VBB has been detected.
OCLx	3	rh	<b>Overcurrent at Channel x (Active Mode only)</b> This bit field indicates that an overload condition has been detected and that the current is being limited. 0 <sub>B</sub> No overcurrent detected 1 <sub>B</sub> An overcurrent has been detected and limited.

(table continues...)



5  $\mu$ Controller interface registers

(continued)

Field	Bits	Type	Description
OLAx	2	rh	<b>Open Load / Wire Break at Channel x (Active Mode)</b> This bit field indicates that an open load condition has been detected. 0 <sub>B</sub> No open load detected. 1 <sub>B</sub> An open load condition has been detected.
OLIx	1	rh	<b>Open Load / Wire Break at Channel x (Inactive Mode)</b> This bit field indicates that an open load condition has been detected. 0 <sub>B</sub> No open load detected. 1 <sub>B</sub> An open load condition has been detected.
OTx	0	rh	<b>Over-temperature at Channel x (Active Mode Only)</b> This bit field indicates that an over-temperature condition has been detected. 0 <sub>B</sub> No over-temperature detected. 1 <sub>B</sub> An over-temperature has been detected.

## 5.1.7 Other channel diagnostics registers

The other channel diagnostics registers in the table below have the same layout as [DIAGO](#). Their names and offset addresses are listed below:

Table 30 Diagnostics registers for channel 1-7

Register Short Name	Register Long Name	Offset Address	Reset Value
DIAG1	Diagnostics Register for Channel-1 (rh)	0A <sub>H</sub>	00 <sub>H</sub>
DIAG2	Diagnostics Register for Channel-2 (rh)	0C <sub>H</sub>	00 <sub>H</sub>
DIAG3	Diagnostics Register for Channel-3 (rh)	0E <sub>H</sub>	00 <sub>H</sub>
DIAG4	Diagnostics Register for Channel-4 (rh)	10 <sub>H</sub>	00 <sub>H</sub>
DIAG5	Diagnostics Register for Channel-5 (rh)	12 <sub>H</sub>	00 <sub>H</sub>
DIAG6	Diagnostics Register for Channel-6 (rh)	14 <sub>H</sub>	00 <sub>H</sub>
DIAG7	Diagnostics Register for Channel-7 (rh)	16 <sub>H</sub>	00 <sub>H</sub>

## 5.1.8 Internal Error register

This register contains the status of internal errors monitored for safe IC operation. The [TE](#), [W4P](#), [ALLOFF](#) bits are sticky and routed out to the ERR pin (according to the [Table 3](#)). The bits [OTP](#) and [LAMP](#) are volatile i.e. are updated every 35  $\mu$ s. Sticky bits are cleared every time the [INTERR](#) register is accessed or by every serial access in mode 0 and 1.

INTERR Offset: 18<sub>H</sub> Address: 00<sub>H</sub>  
Internal Error Register (rh) Reset value: 07<sub>H</sub>

7	6	5	4	3	2	1	0
RES	OTC	RES	OTP	LAMP	ALLOFF	W4P	TE
r	rh	r	rh	rh	rh	rh	rh

5 µController interface registers

Field	Bits	Type	Description
RES	7	r	<b>Reserved</b> returns 0 if read.
OTC	6	rh	<b>Overtemperature Common (Volatile)</b> This bit field indicates that an overtemperature or overcurrent condition of at least one of the channels has been detected. OR-ed LEDGx-values. 0 <sub>B</sub> No overtemperature or overcurrent has been detected. 1 <sub>B</sub> An overtemperature or overcurrent condition has been detected.
RES	5	r	<b>Reserved</b> returns 0 if read.
OTP	4	rh	<b>Overtemperature Package (Volatile)</b> This bit field indicates that an overtemperature of the package has been detected. 0 <sub>B</sub> No package overtemperature detected. 1 <sub>B</sub> An overtemperature in the package has been detected.
LAMP	3	rh	<b>Cold Lamp Detected (Volatile)</b> This bit field indicates that at least a cold lamp behaviour has been detected at one output channel. 0 <sub>B</sub> No cold lamp behaviour detected. 1 <sub>B</sub> At least one load at the output channels behaves as a cold lamp.
ALLOFF	2	rh	<b>All Outputs Channels are Switched Off (Sticky)</b> This bit field indicates that all the output channels have been switched off either due to an internal error (e.g. overtemperature), the ODIS pin or according to the data in the DRIVE register. 0 <sub>B</sub> The output channels are enabled and controlled by the DRIVE register. 1 <sub>B</sub> The output channels are switched off.
W4P	1	rh	<b>Wait for Power Chip (Sticky)</b> This bit field indicates that the Power Chip is correctly supplied and ready for operation. 0 <sub>B</sub> Power Chip is ready. 1 <sub>B</sub> Power Chip is not ready because of insufficient voltage or longer persisting transmission error.
TE	0	rh	<b>Transmission Error (Sticky)</b> This bit field indicates a transmission error over the galvanic isolation detected either from the Process Side or from the µController-Interface. 0 <sub>B</sub> No transmission error is detected. 1 <sub>B</sub> Transmission error has occurred.

## 5 µController interface registers

### 5.1.9 Global Configuration register

This register configures some extended functionalities of the chip.

GLCFG Offset: 1A<sub>H</sub> Address: 00<sub>H</sub>  
Global Configuration Register (rwh) Reset value: 00<sub>H</sub>

7	6	5	4	3	2	1	0
<b>FRZSC</b>	<b>RESYN</b>	<b>RSTOFF</b>	<b>LEDON</b>	<b>RES</b>	<b>LEDGOFF</b>	<b>OLOFF</b>	<b>SWRST</b>
rw	rw	rw	rw	rw	rw	rw	rwh

Field	Bits	Type	Description
FRZSC	7	rw	<b>Selection of Isochronous Mode for Diagnostics</b> This bit field enables the isochronous mode for diagnostics. The entry of this mode is ignored when RESYN = 1. 0 <sub>B</sub> Diagnostics are treated independently of SYNC-level 1 <sub>B</sub> Diagnostics are frozen with falling edge of SYNC and released with rising edge. During SYNC = 0 <b>DIAG0</b> ,,, <b>DIAG7</b> and <b>COLDIAG</b> are not updated. But read bits in <b>COLDIAG</b> can be reset.
RESYN	6	rw	<b>Resynchronization of CT-Transmission</b> This bit field enables the resynchronization of CT-transmission. 0 <sub>B</sub> functionality of SYNC is as defined by bit FRZSC. 1 <sub>B</sub> SYNC-pin is used for resynchronization of CT-transmission.  <b>Note:</b> <i>It is not possible to select RESYN = 1 and to use isochronous mode for drive signals or/and diagnostics at the same time. That means resynchronization and isochronous mode of driver information and diagnostics at the same time is not possible. Edges on SYNC are used solely for resynchronization. In the following the driver information can be only transferred when SYNC = 1 when RESYN is set to "1". A negative pulse on SYNC initializes the resynchronization.</i>
RSTOFF	5	rw	<b>HW Reset of ALE Pin Disabled</b> This bit field disables the external reset functionality. 0 <sub>B</sub> The HW reset at the ALE pin is enabled (default). 1 <sub>B</sub> The HW reset is disabled.
LEDON	4	rw	<b>LED Matrix Enabled</b> This bit field enables the LED Matrix in serial mode. In this case the HW reset cannot be used (activation of HW Reset is ignored). 0 <sub>B</sub> The LED matrix is disabled (default). 1 <sub>B</sub> The LED matrix is enabled in serial mode.
RES	3	rw	<b>Reserved</b> <b>Must be set to "0"</b>

(table continues...)

## 5 µController interface registers

(continued)

Field	Bits	Type	Description
LEDGOFF	2	rw	<b>LEDG Report Disabled</b> This bit field disables the report of the LEDGx-information. 0 <sub>B</sub> The LEDGx diagnostic is enabled (default). 1 <sub>B</sub> The LEDGx diagnostic is disabled and not reported in the DIAGO ..., DIAG7 registers.
OLOFF	1	rw	<b>Open-Load Diagnostic Disabled</b> This bit field disables the monitoring of the Open-Load diagnostic OLAX and OLIX. 0 <sub>B</sub> The Open-Load diagnostic is enabled and updated in the DIAGO ..., DIAG7 registers (default). 1 <sub>B</sub> The Open-Load diagnostic is disabled and does not appear in the DIAGO ..., DIAG7 registers.
SWRST	0	rwh	<b>Soft Reset</b> This bit field triggers the clearing of the user registers and restarts the CT transmission. After setting the soft reset, this bit field will clear itself. 0 <sub>B</sub> No reset is generated. 1 <sub>B</sub> A clearing of the user registers is generated.

6 Package : Outlines and marking pattern

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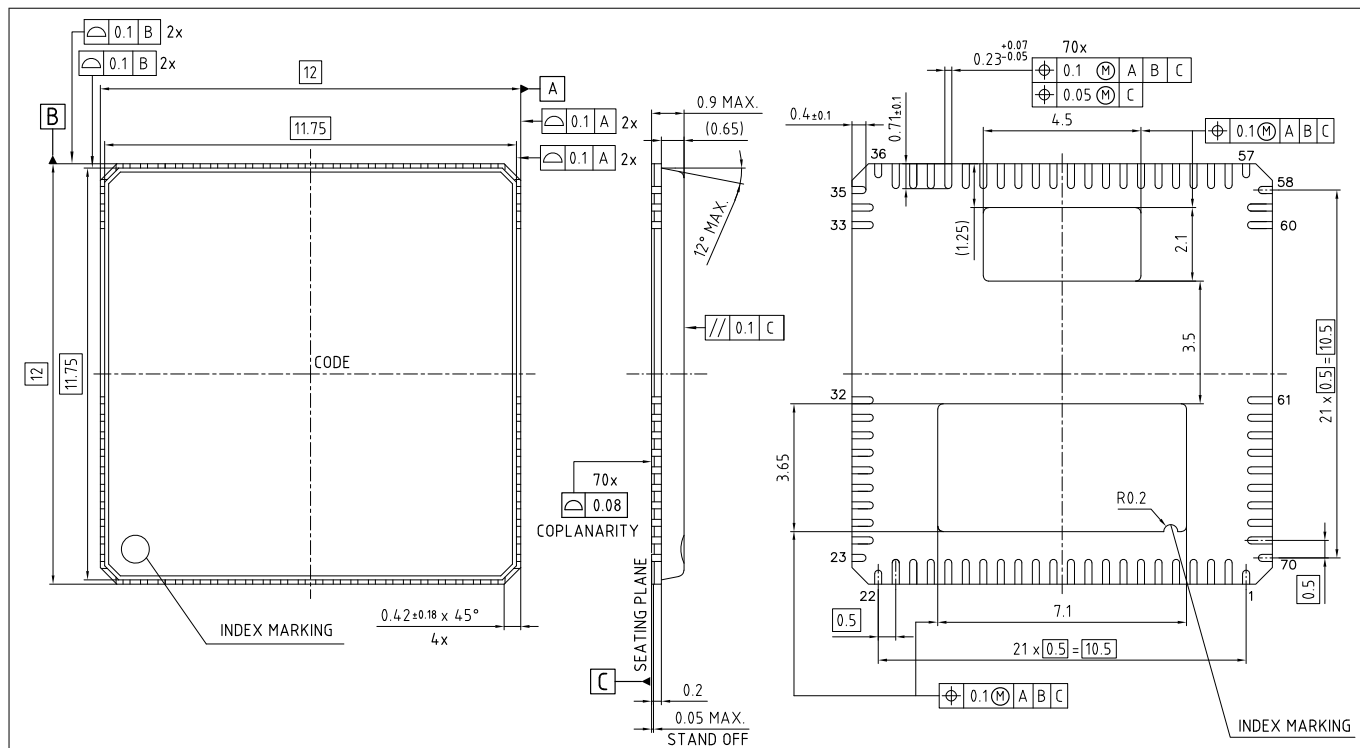


Figure 38 PG-VQFN-70 (Plastic (Green) Very Thin Profile Quad Flat Non Leaded Package)

## Information of Marking Pattern:

Infineon  
ISOFACE™  
ISO2H823V2.5

Lotnumber  
Datecode

Figure 39 Marking Pattern

## Revision history

### Revision history

Document version	Date of release	Subject (major changes since previous revision)
2.1	2024-11-01	<ul style="list-style-type: none"> <li>Figure 11 corrected (missing arrow added at most right topology)</li> <li>Table 4 and Table 5 revised to improve readability</li> <li>Maximum limit increased for parameters <math>ITH_{OLA2}</math> and <math>ITH_{OLA3}</math> (Table 26) (<math>ITH_{OLA2}</math> : 2.9 mA to now 3.3 mA/<math>ITH_{OLA3}</math> : 1.9 mA to now 2.1 mA)</li> <li>Global Error Register (GLERR): typo corrected in description of reset value (Chapter 5.1.4) (corrected from 16<sub>H</sub> to now 46<sub>H</sub>)</li> <li>Editorial changes including new template</li> </ul>
2.0	2015-02-12	

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