

MOSFET

OptiMOS™ 6 Power-Transistor, 100 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Optimized for high frequency switching and synchronous rectification
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

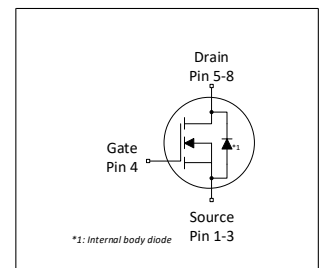
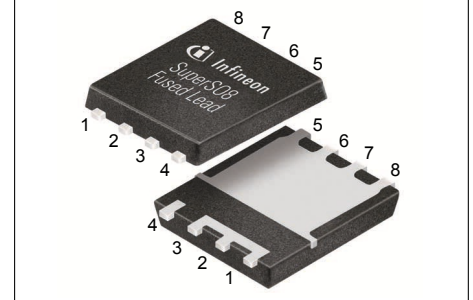
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	23	mΩ
I_D	31	A
Q_{oss}	14	nC
$Q_G(0V \dots 10V)$	7.4	nC
$Q_{rr}(100A/\mu s)$	23	nC

TDSON-8 FL (enlarged source interconnection)



RoHS

Type / Ordering Code	Package	Marking	Related Links
ISC230N10NM6	PG-TDSON-8 FL	230N10N6	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	31 22 19 7.7	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=8\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	124	A	$T_A=25\text{ °C}$
Avalanche current, single pulse ⁴⁾	I_{AS}	-	-	10	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	40	mJ	$I_D=6.6\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	48 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.6	3.1	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area	R_{thJA}	-	-	50	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.3	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=13\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}^{1)}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	19.3 23.5	23 30	m Ω	$V_{GS}=10\text{ V}$, $I_D=10\text{ A}$ $V_{GS}=8\text{ V}$, $I_D=5\text{ A}$
Gate resistance	R_G	0.55	1.0	1.65	Ω	-
Transconductance	g_{fs}	6.4	13	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=10\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	530	690	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	120	150	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	6.5	9.8	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	4.5	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	1	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	6.5	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	9	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge ¹⁾	Q_{gs}	-	2.5	3.3	nC	$V_{DD}=50\text{ V}$, $I_D=5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold ¹⁾	$Q_{g(th)}$	-	1.5	1.8	nC	$V_{DD}=50\text{ V}$, $I_D=5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	1.5	2.3	nC	$V_{DD}=50\text{ V}$, $I_D=5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	2.5	-	nC	$V_{DD}=50\text{ V}$, $I_D=5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	7.4	9.3	nC	$V_{DD}=50\text{ V}$, $I_D=5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DD}=50\text{ V}$, $I_D=5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	6.5	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	14	17	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

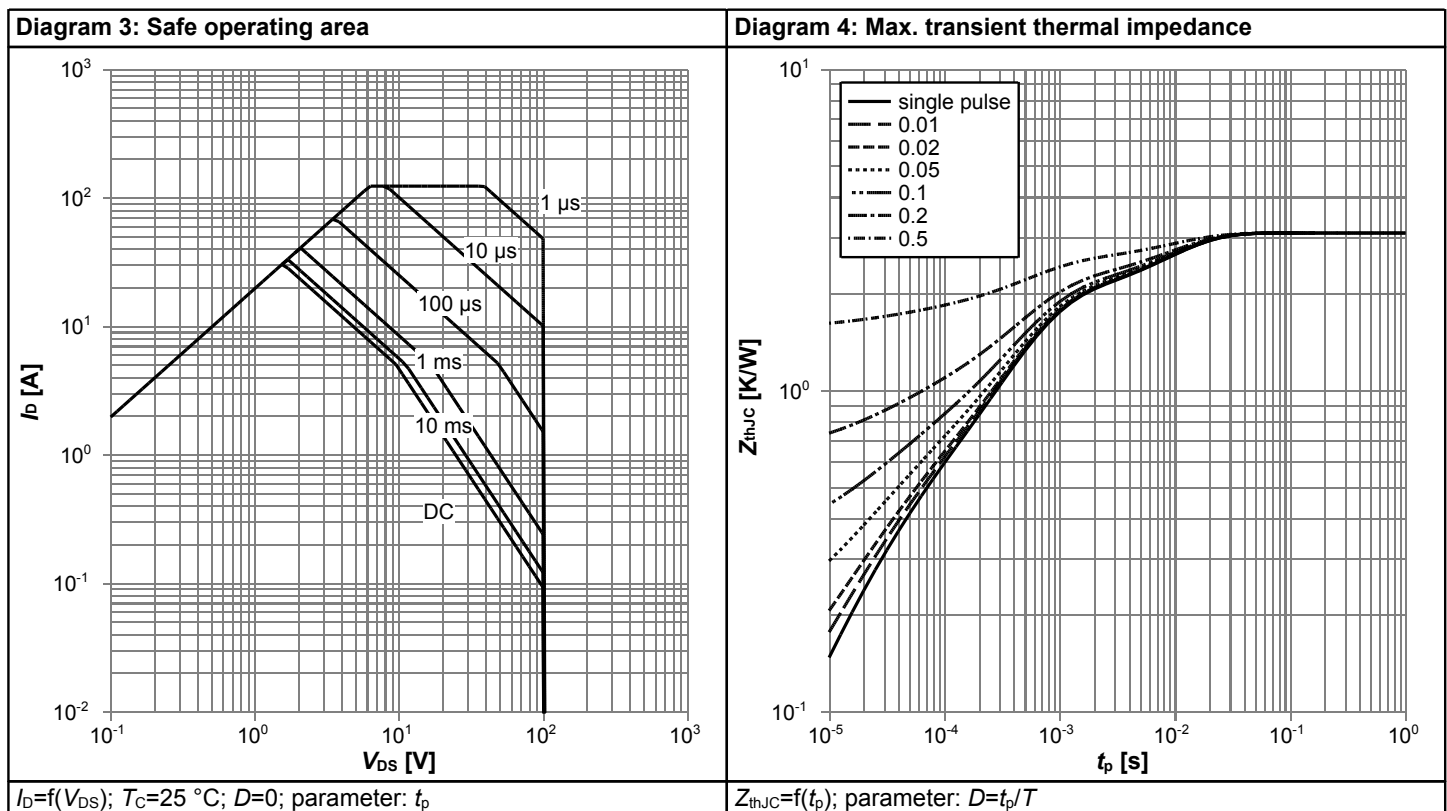
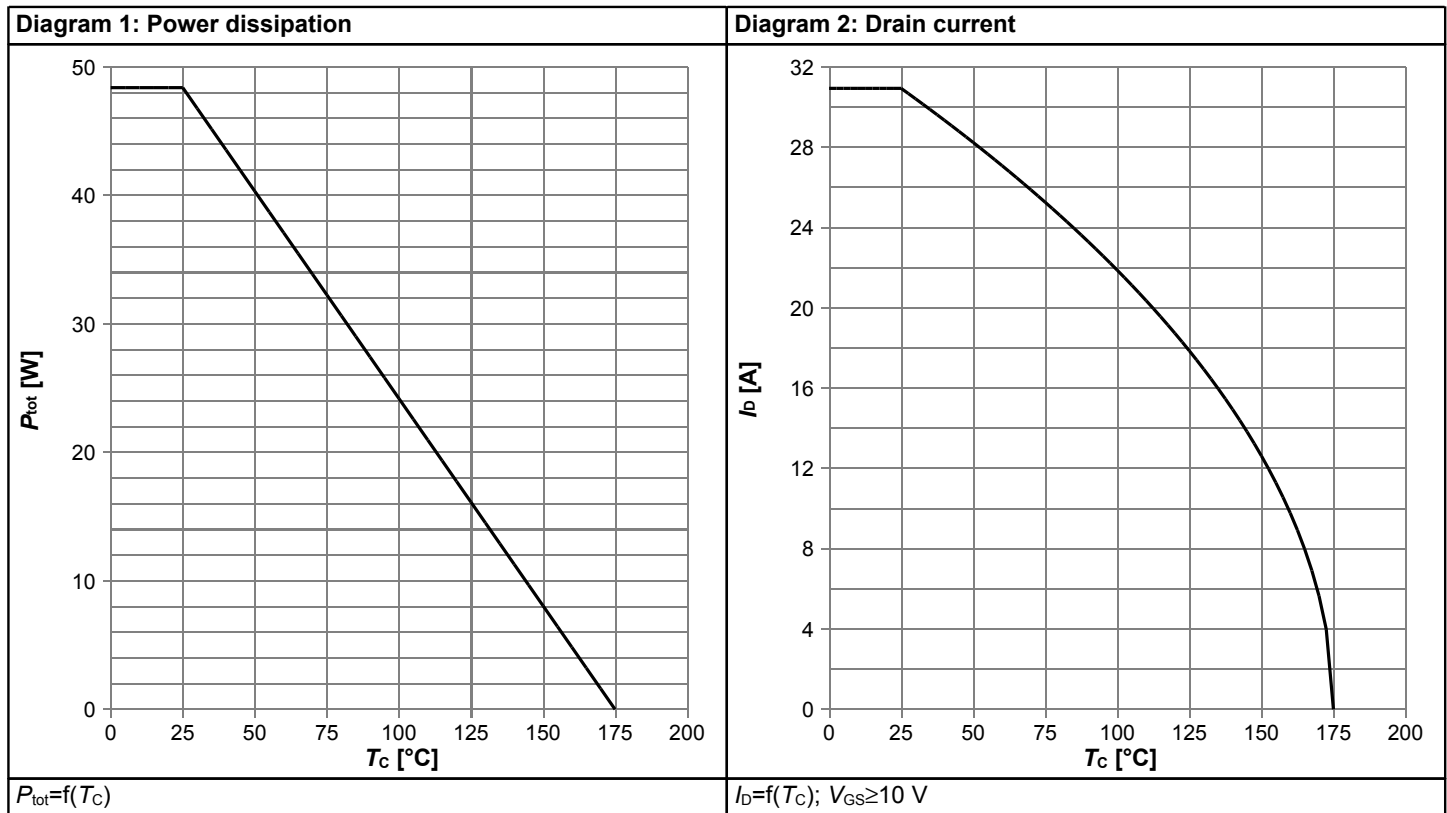
²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	31	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	124	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.84	1.0	V	$V_{GS}=0\text{ V}$, $I_F=10\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	30	45	ns	$V_R=50\text{ V}$, $I_F=5\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	23	35	nC	$V_R=50\text{ V}$, $I_F=5\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time ¹⁾	t_{rr}	-	14	21	ns	$V_R=50\text{ V}$, $I_F=5\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	86.5	130	nC	$V_R=50\text{ V}$, $I_F=5\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

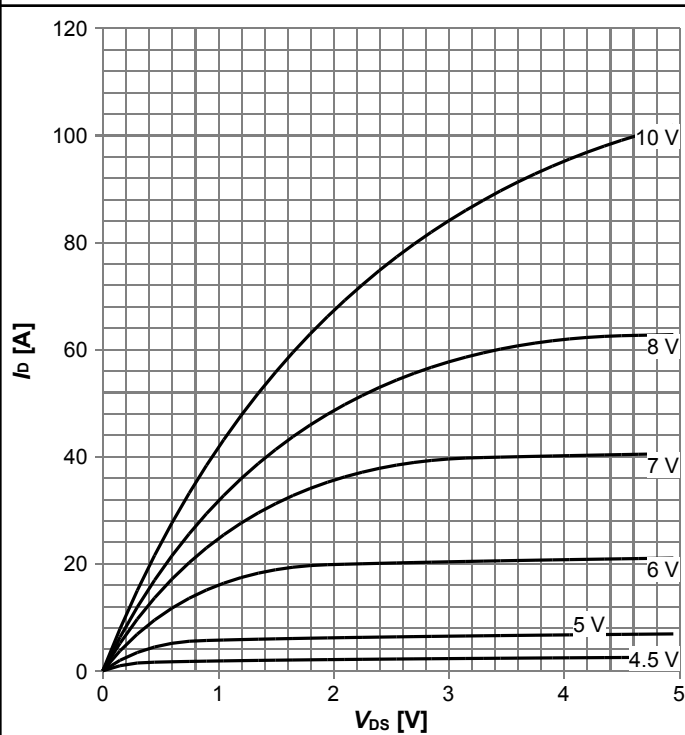
4 Electrical characteristics diagrams



OptiMOS™ 6 Power-Transistor, 100 V

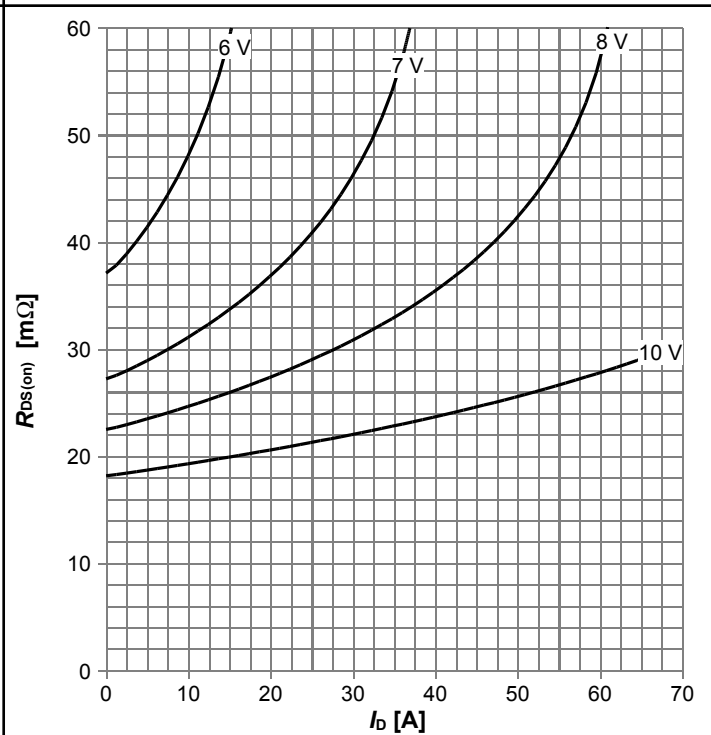
ISC230N10NM6

Diagram 5: Typ. output characteristics



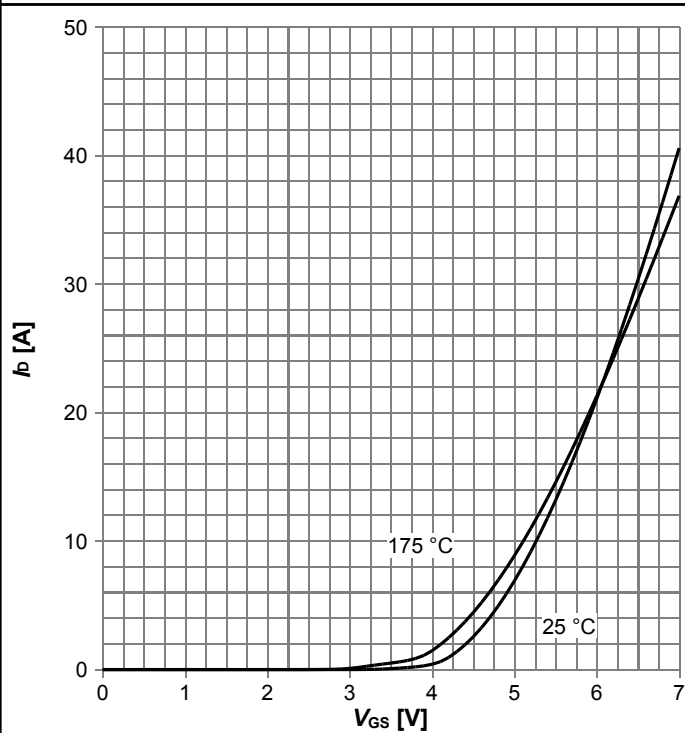
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



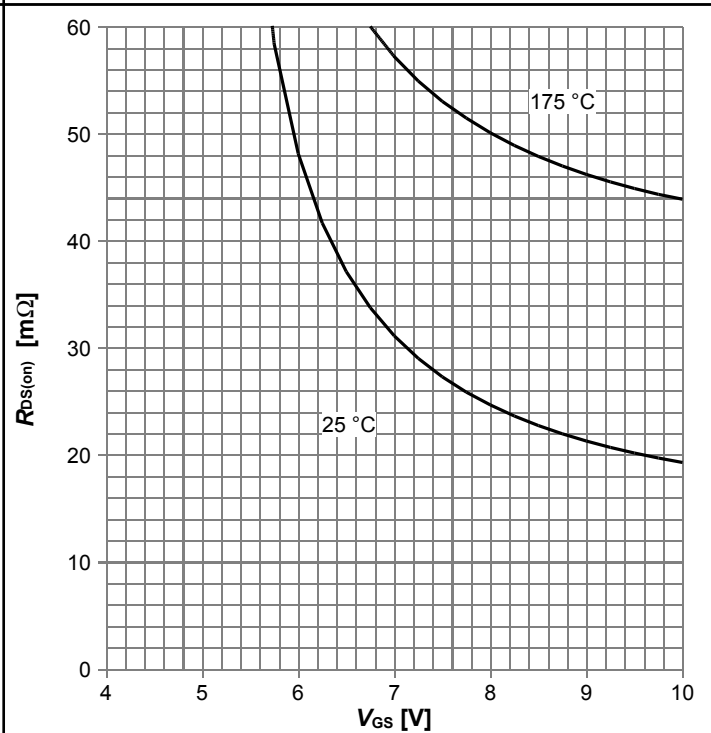
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



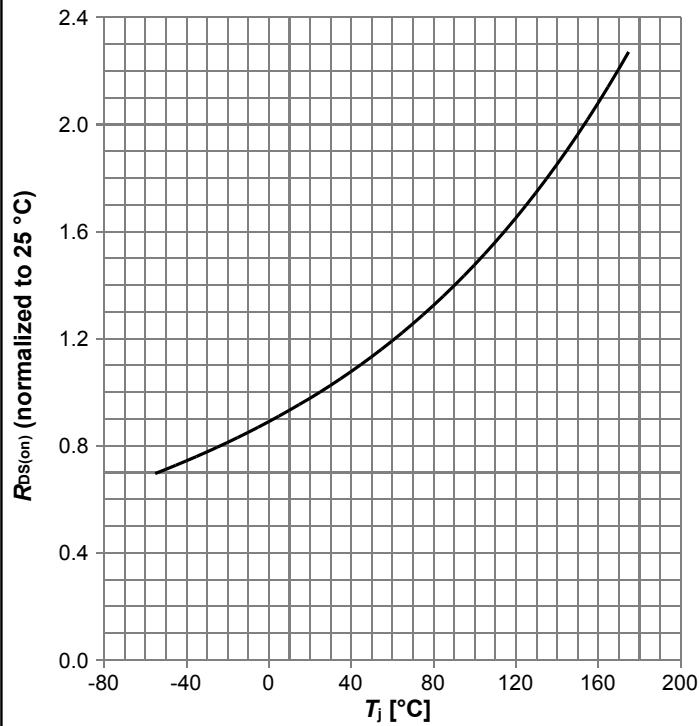
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



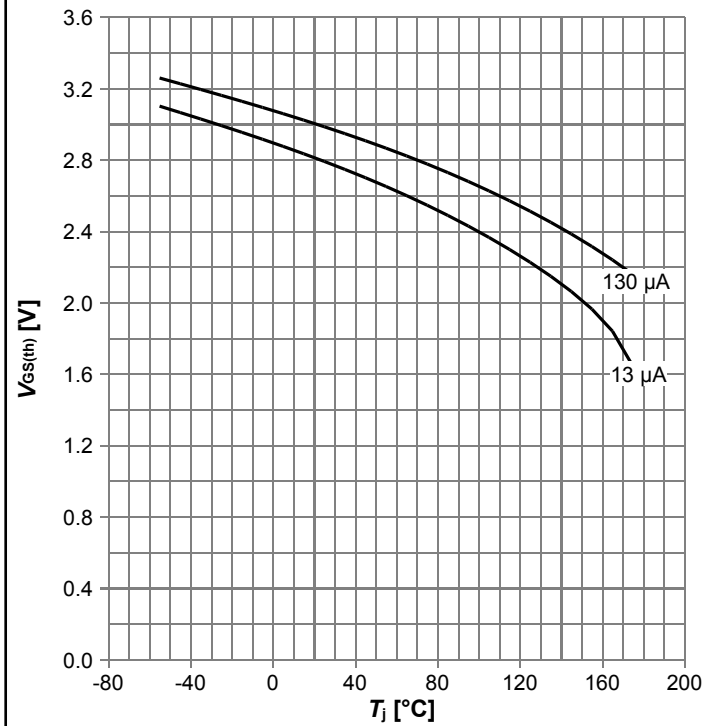
$R_{DS(on)} = f(V_{GS})$, $I_D = 10\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



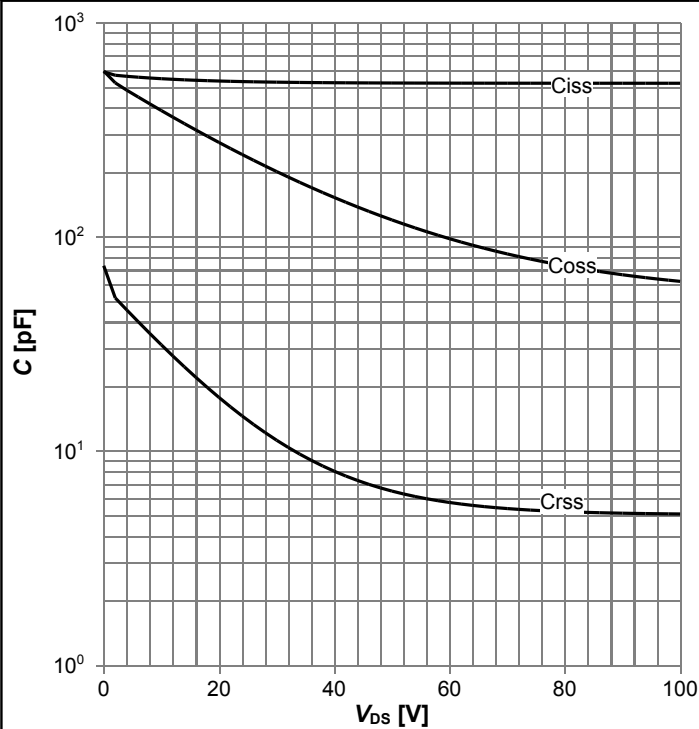
$R_{DS(on)} = f(T_j)$, $I_D = 10$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



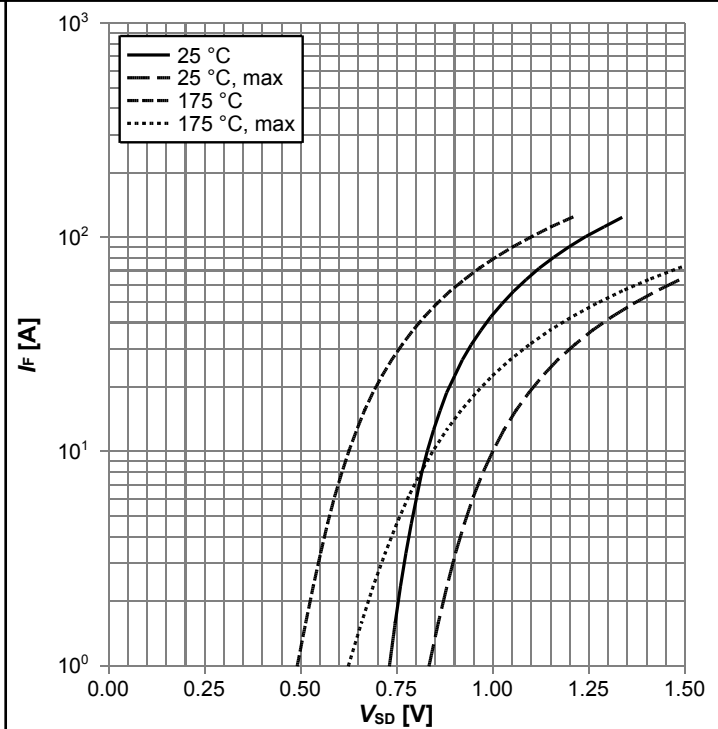
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics

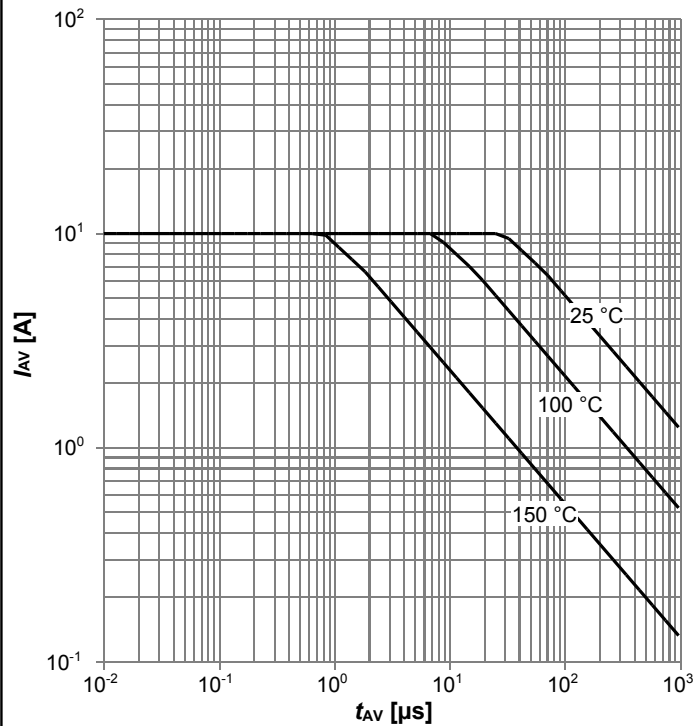


Diagram 14: Typ. gate charge

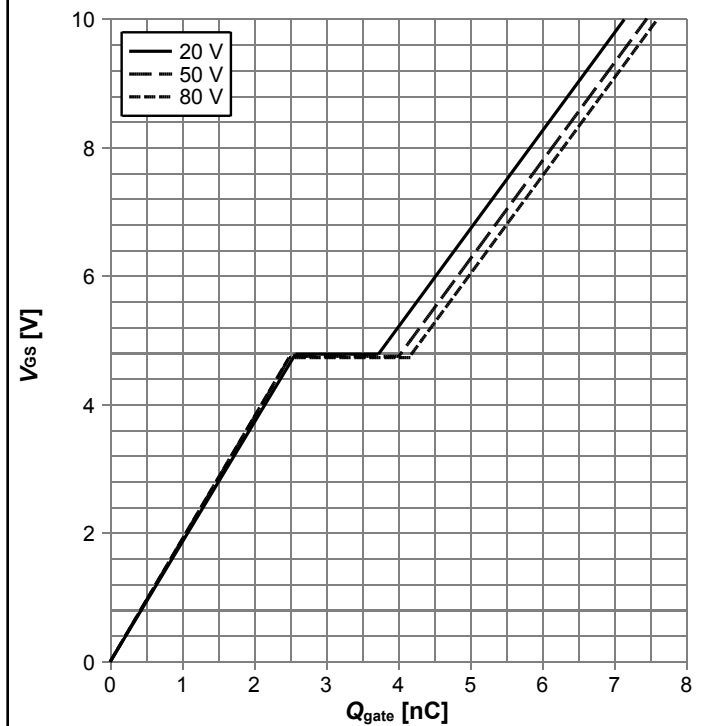


Diagram 15: Drain-source breakdown voltage

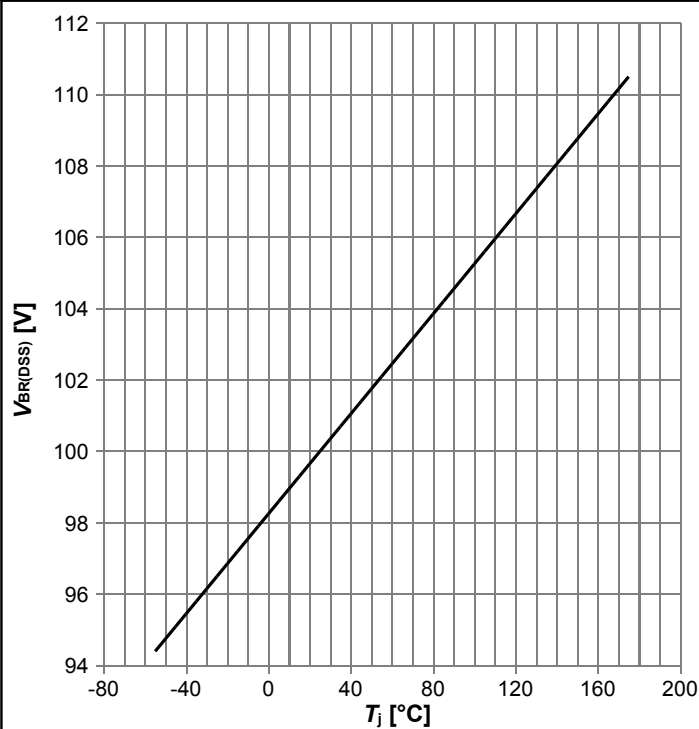
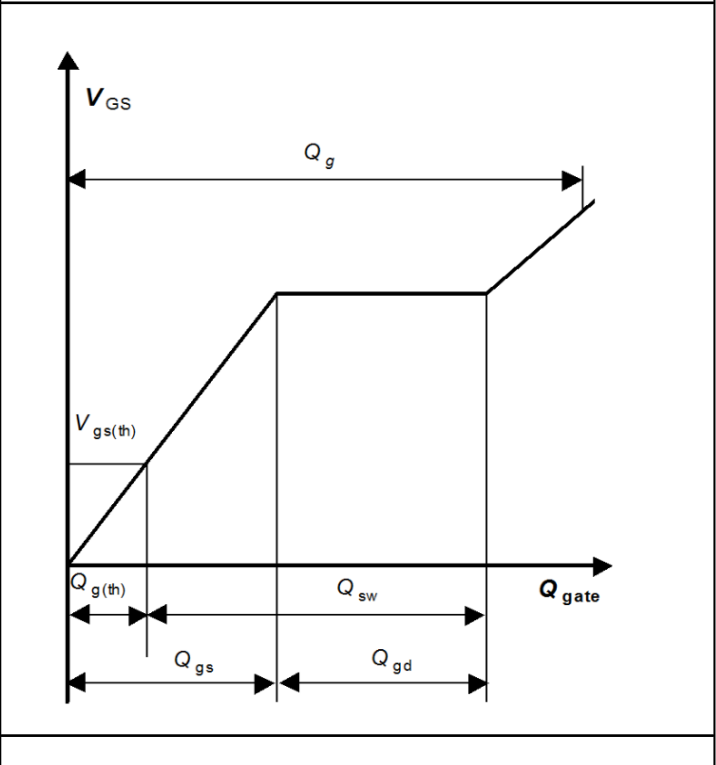
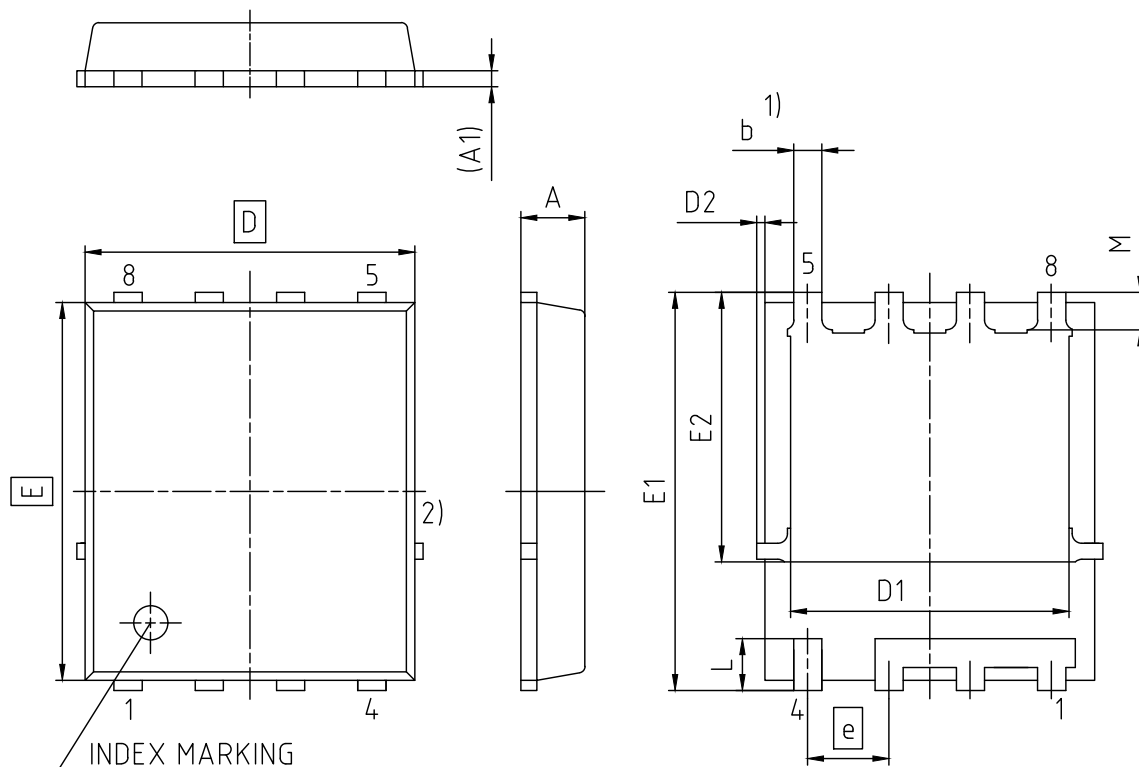


Diagram Gate charge waveforms



5 Package Outlines



1) EXCLUDING MOLD FLASH

2) REMOVAL ON MOLD GATE

INTRUSION 0.1 mm

PROTRUSION 0.1 mm

LEAD LENGTH UP TO ANTI FLASH LINE

ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.26	0.54
D	4.80	5.35
D1	3.70	4.40
D2	0.00	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.42
e	1.27	
L	0.69	0.90
M	0.45	0.69

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Figure 1 Outline PG-TDSON-8 FL, dimensions in mm

PG-TDSON-8-FL: Recommended Boardpads & Apertures

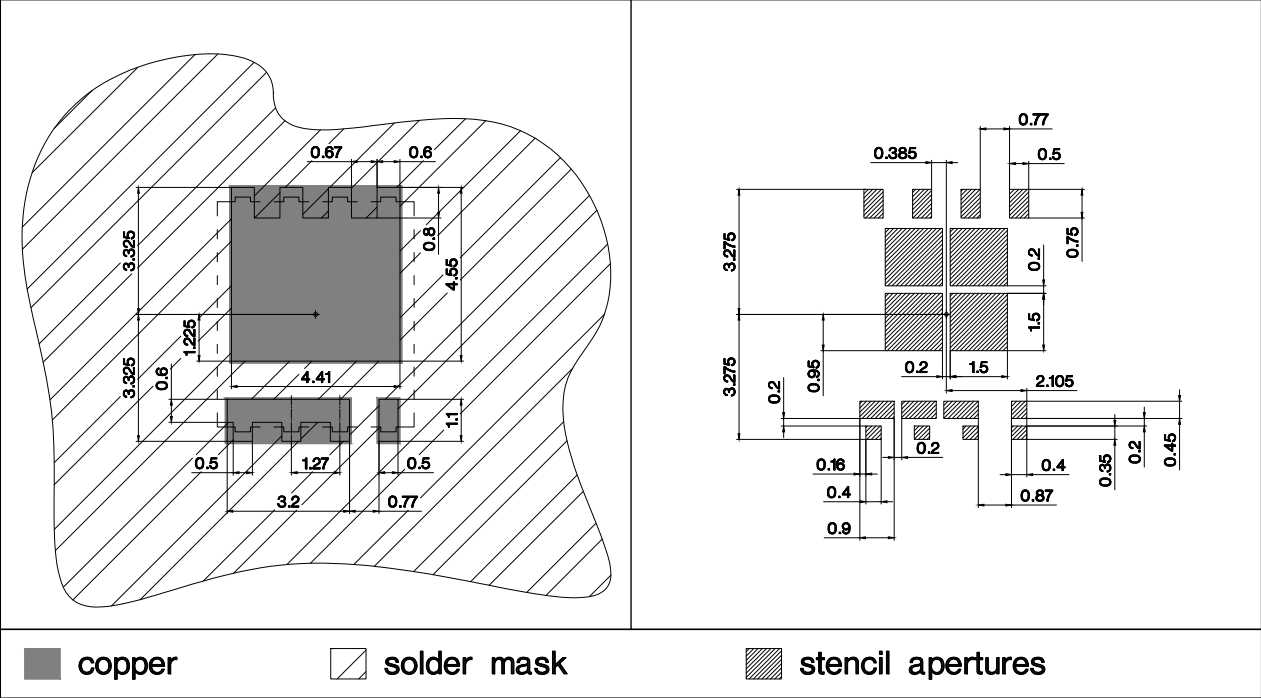


Figure 2 Outline Boardpads (TDSON-8 FL)

Revision History

ISC230N10NM6

Revision: 2023-02-10, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-07-05	Release of final version
2.1	2021-07-20	Update IAS
2.2	2023-02-10	Update SOA Diagram

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