

MOSFET
OptiMOS™ 3 Power-Transistors, 40 V

PG-DSO-8

Features

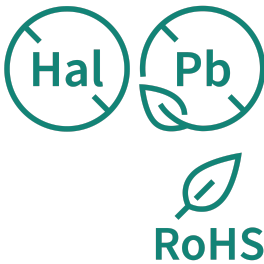
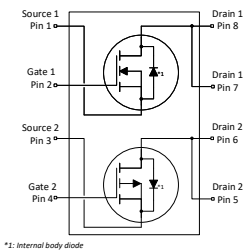
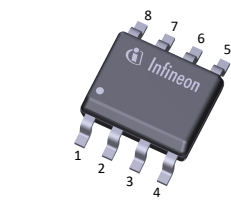
- Complementary N- and P-channel
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} (n-channel)	40	V
$R_{DS(on),max}$ (n-channel)	25	mΩ
I_D (n-channel)	7.9	A
V_{DS} (p-channel)	-40	V
$R_{DS(on),max}$ (p-channel)	30	mΩ
I_D (p-channel)	-7.8	A



Type/Ordering Code	Package	Marking	Related Links
ISA250300C04LMDS	PG-DSO-8	2530C04L	-



Table of Contents

Description 1

Maximum ratings 3

Thermal characteristics 5

Electrical characteristics 6

Electrical characteristics diagrams 9

Package Outlines 17

Revision History 18

Trademarks 18

Disclaimer 18

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	7.9 5.0 4.4 5.9	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=90\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	32	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	17.2	mJ	$I_D=7.9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	2.5 1.4	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=90\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2 for n-channel and the Diagram 17 for the p-channel. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

³⁾ See Diagrams 3 and 18 for more detailed information

⁴⁾ See Diagrams 13 and 28 for more detailed information

Table 3 Maximum ratings (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ⁵⁾	I_D	-	-	-7.8 -4.9 -4.1 -5.8	A	$V_{GS}=-10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=90\text{ °C/W}$ ⁶⁾
Pulsed drain current ⁷⁾	$I_{D,pulse}$	-	-	-31	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁸⁾	E_{AS}	-	-	17.2	mJ	$I_D=-7.8\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	2.5 1.4	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=90\text{ °C/W}$ ⁶⁾
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	-

⁵⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2 for n-channel and the Diagram 17 for the p-channel. De-rating will be required based on the actual environmental conditions.

⁶⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

- 7) See Diagrams 3 and 18 for more detailed information
- 8) See Diagrams 13 and 28 for more detailed information

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJC}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, minimal footprint, steady state	R_{thJA}	-	-	150	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area, steady state ⁹⁾	R_{thJA}	-	-	90	°C/W	-

⁹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	-	2.7	V	$V_{DS}=V_{GS}$, $I_D=1000\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	18 26	25 32	m Ω	$V_{GS}=10\text{ V}$, $I_D=7.9\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=7.1\text{ A}$
Gate resistance	R_G	-	1.5	-	Ω	-
Transconductance ¹⁰⁾	g_{fs}	9.0	18	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=7.9\text{ A}$

¹⁰⁾ Defined by design. Not subject to production test.

Table 6 Static characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	-1.1	-	-2.7	V	$V_{DS}=V_{GS}$, $I_D=-1000\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1 -100	μA	$V_{DS}=-40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=-40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	25 35	30 44	m Ω	$V_{GS}=-10\text{ V}$, $I_D=-7.8\text{ A}$ $V_{GS}=-4.5\text{ V}$, $I_D=-7\text{ A}$
Gate resistance	R_G	-	8.5	-	Ω	-
Transconductance ¹¹⁾	g_{fs}	9	18	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=-7.8\text{ A}$

¹¹⁾ Defined by design. Not subject to production test.

Table 7 Dynamic characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹²⁾	C_{iss}	-	550	720	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹²⁾	C_{oss}	-	150	200	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹²⁾	C_{rss}	-	10	18	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	5.8	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=7.9\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 7 Dynamic characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Rise time	t_r	-	5.3	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=7.9\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	2.9	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=7.9\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Fall time	t_f	-	4.0	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=7.9\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Gate to source charge	Q_{gs}	-	1.8	-	nC	$V_{DD}=20\text{ V}$, $I_D=7.9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	0.9	-	nC	$V_{DD}=20\text{ V}$, $I_D=7.9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	1.0	-	nC	$V_{DD}=20\text{ V}$, $I_D=7.9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	1.9	-	nC	$V_{DD}=20\text{ V}$, $I_D=7.9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹²⁾	Q_g	-	3.8	5.7	nC	$V_{DD}=20\text{ V}$, $I_D=7.9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	$V_{DD}=20\text{ V}$, $I_D=7.9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹²⁾	Q_g	-	7.9	11.9	nC	$V_{DD}=20\text{ V}$, $I_D=7.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	5.3	-	nC	$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$

¹²⁾ Defined by design. Not subject to production test.**Table 8 Dynamic characteristics (p-channel)**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹³⁾	C_{iss}	-	1200	1600	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹³⁾	C_{oss}	-	460	600	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹³⁾	C_{rss}	-	26	46	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=-20\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-7.8\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Rise time	t_r	-	11	-	ns	$V_{DD}=-20\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-7.8\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	16	-	ns	$V_{DD}=-20\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-7.8\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Fall time	t_f	-	9.8	-	ns	$V_{DD}=-20\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-7.8\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Gate to source charge	Q_{gs}	-	-3.8	-	nC	$V_{DD}=-20\text{ V}$, $I_D=-7.8\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	-2.0	-	nC	$V_{DD}=-20\text{ V}$, $I_D=-7.8\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	-2.4	-	nC	$V_{DD}=-20\text{ V}$, $I_D=-7.8\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Switching charge	Q_{sw}	-	-4.2	-	nC	$V_{DD}=-20\text{ V}$, $I_D=-7.8\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total ¹³⁾	Q_g	-	-8.1	-12	nC	$V_{DD}=-20\text{ V}$, $I_D=-7.8\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$

Table 8 Dynamic characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	V_{plateau}	-	-3.2	-	V	$V_{\text{DD}} = -20 \text{ V}$, $I_{\text{D}} = -7.8 \text{ A}$, $V_{\text{GS}} = 0 \text{ to } -4.5 \text{ V}$
Gate charge total	Q_{g}	-	-16.1	-24	nC	$V_{\text{DD}} = -20 \text{ V}$, $I_{\text{D}} = -7.8 \text{ A}$, $V_{\text{GS}} = 0 \text{ to } -10 \text{ V}$
Output charge	Q_{oss}	-	-14	-	nC	$V_{\text{DS}} = -20 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$

¹³⁾ Defined by design. Not subject to production test.

Table 9 Reverse diode (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_{S}	-	-	3.1	A	$T_{\text{C}} = 25 \text{ °C}$
Diode pulse current	$I_{\text{S,pulse}}$	-	-	32	A	$T_{\text{A}} = 25 \text{ °C}$
Diode forward voltage	V_{SD}	-	0.87	1.0	V	$V_{\text{GS}} = 0 \text{ V}$, $I_{\text{F}} = 7.9 \text{ A}$, $T_{\text{j}} = 25 \text{ °C}$
Reverse recovery time	t_{rr}	-	12	-	ns	$V_{\text{R}} = 20 \text{ V}$, $I_{\text{F}} = 7.9 \text{ A}$, $di_{\text{F}}/dt = 100 \text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	3.6	-	nC	$V_{\text{R}} = 20 \text{ V}$, $I_{\text{F}} = 7.9 \text{ A}$, $di_{\text{F}}/dt = 100 \text{ A}/\mu\text{s}$

Table 10 Reverse diode (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_{S}	-	-	-3.5	A	$T_{\text{C}} = 25 \text{ °C}$
Diode pulse current	$I_{\text{S,pulse}}$	-	-	-31	A	$T_{\text{A}} = 25 \text{ °C}$
Diode forward voltage	V_{SD}	-	-0.88	-1.0	V	$V_{\text{GS}} = 0 \text{ V}$, $I_{\text{F}} = -7.8 \text{ A}$, $T_{\text{j}} = 25 \text{ °C}$
Reverse recovery time	t_{rr}	-	18	-	ns	$V_{\text{R}} = -20 \text{ V}$, $I_{\text{F}} = -7.8 \text{ A}$, $di_{\text{F}}/dt = -100 \text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	6.9	-	nC	$V_{\text{R}} = -20 \text{ V}$, $I_{\text{F}} = -7.8 \text{ A}$, $di_{\text{F}}/dt = -100 \text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

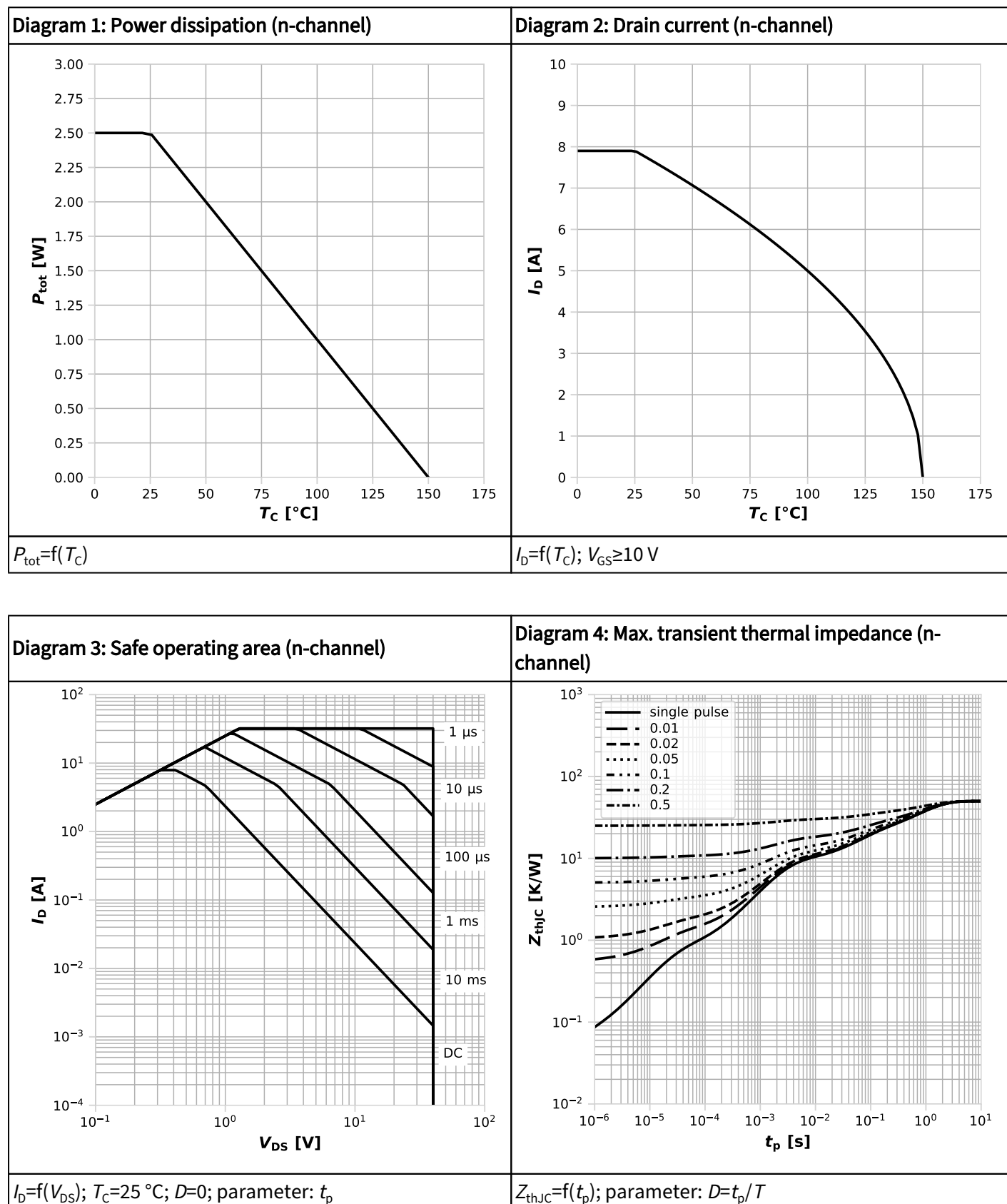
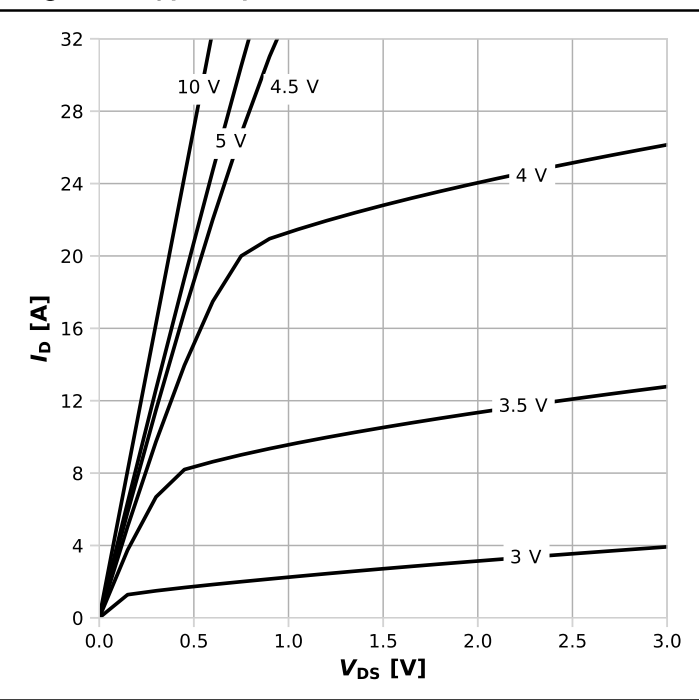
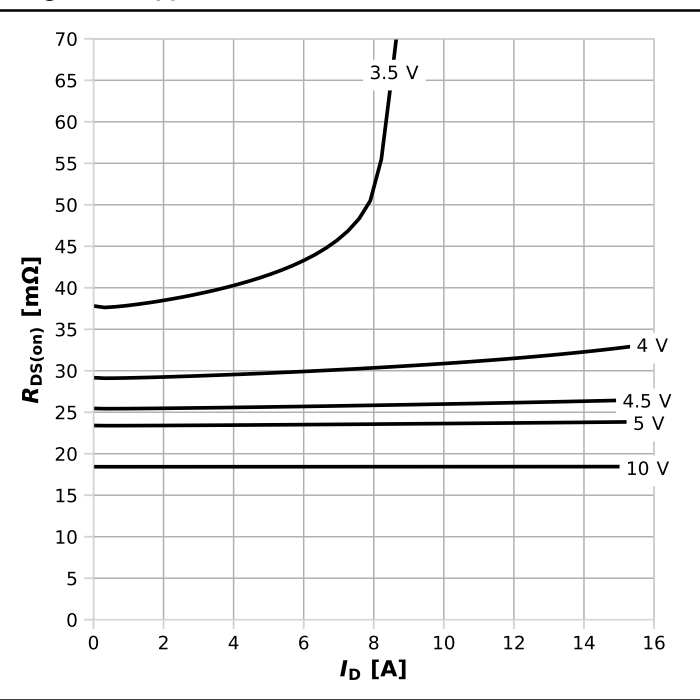


Diagram 5: Typ. output characteristics (n-channel)



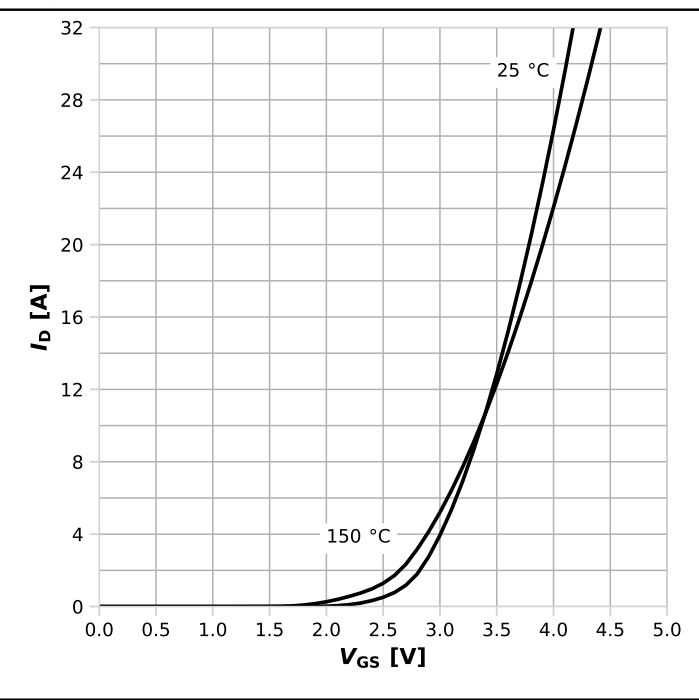
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance (n-channel)



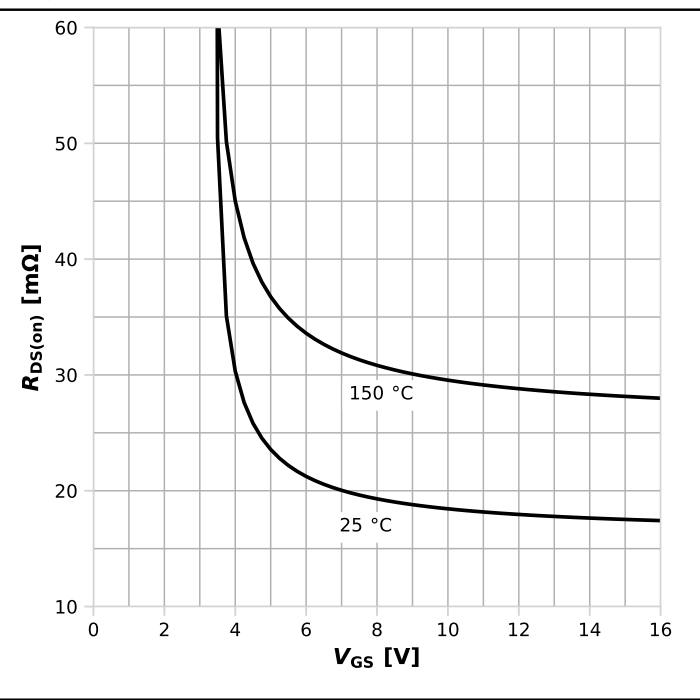
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics (n-channel)



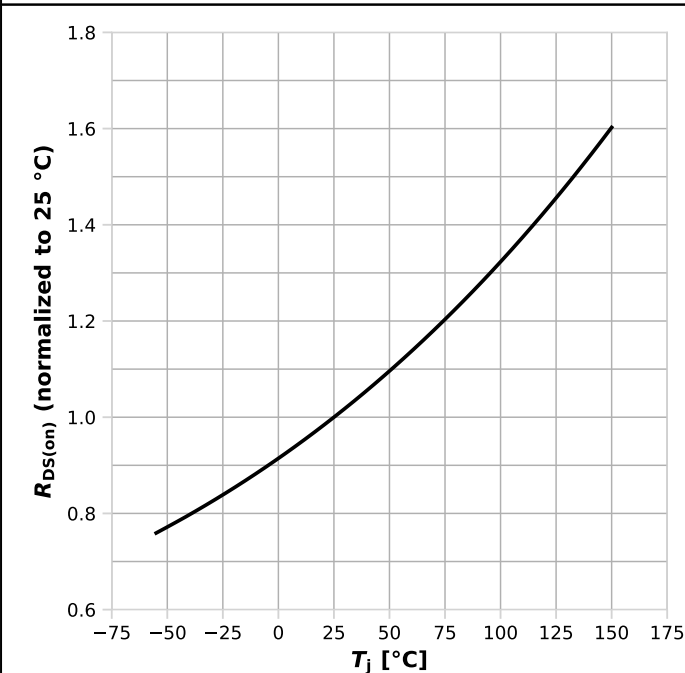
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance (n-channel)



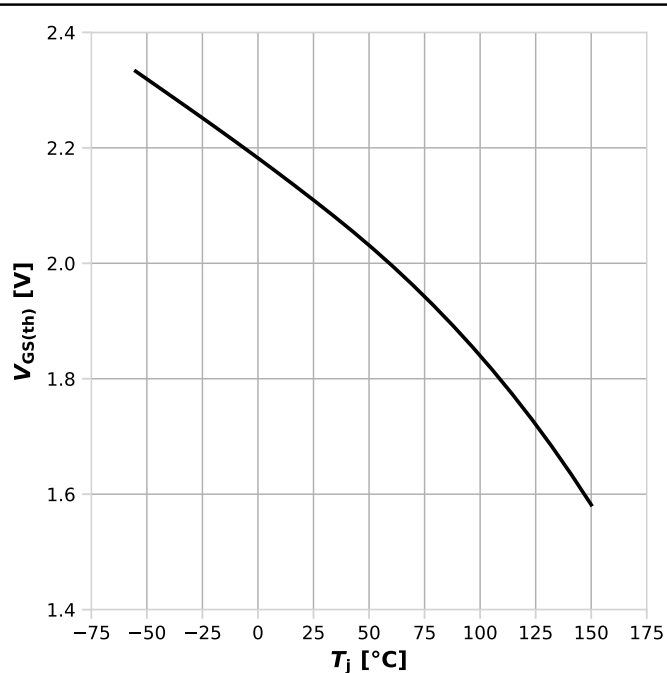
$R_{DS(on)} = f(V_{GS})$, $I_D = 7.9\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance (n-channel)



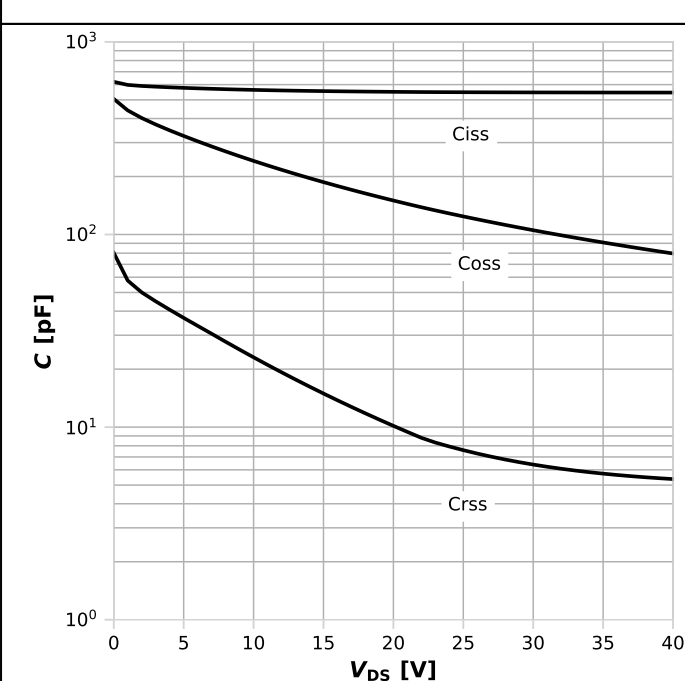
$$R_{DS(on)} = f(T_j), I_D = 7.9 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage (n-channel)



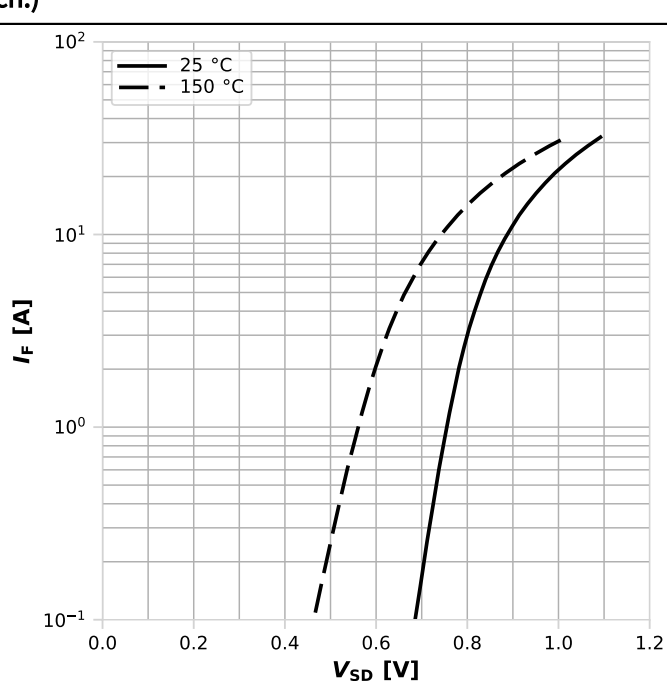
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D = 1000 \mu\text{A}$$

Diagram 11: Typ. capacitances (n-channel)



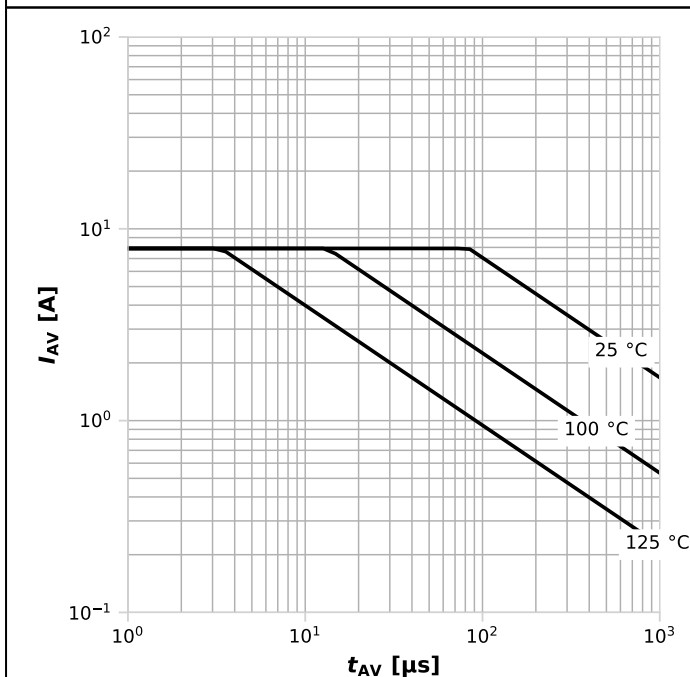
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode (n-ch.)



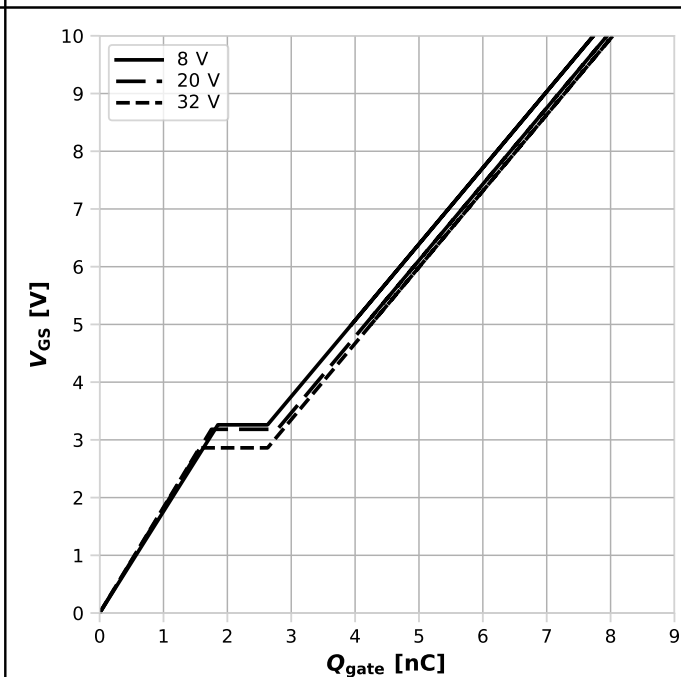
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics (n-channel)



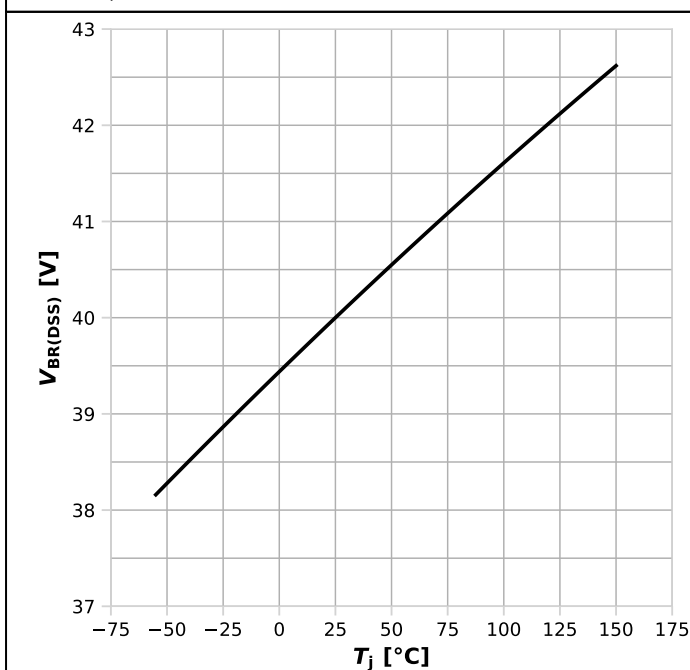
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge (n-channel)



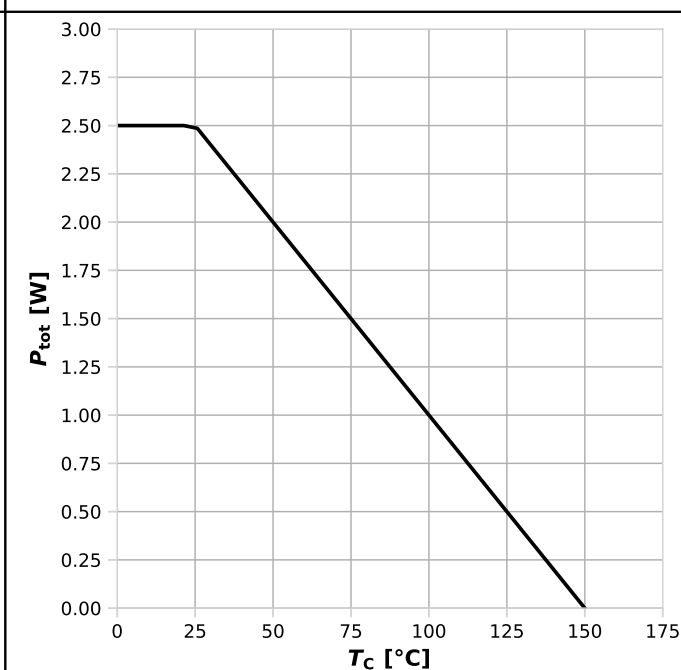
$V_{GS}=f(Q_{gate})$, $I_D=7.9\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage (n-channel)

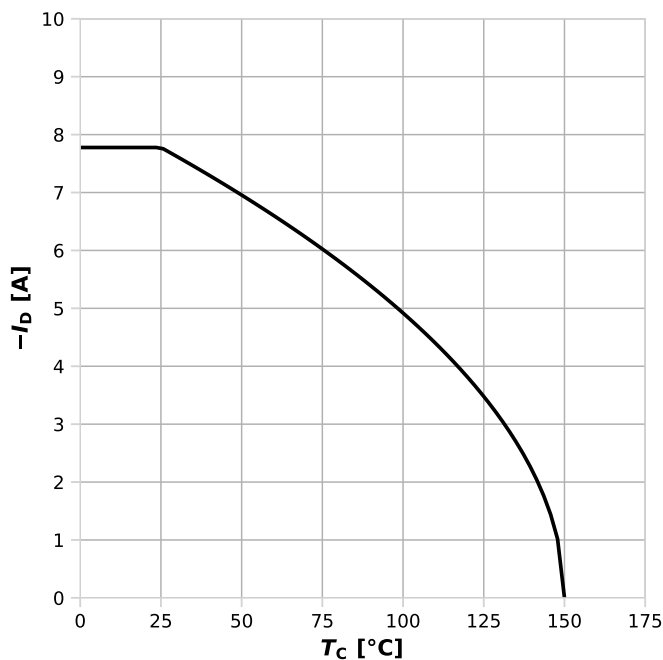


$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

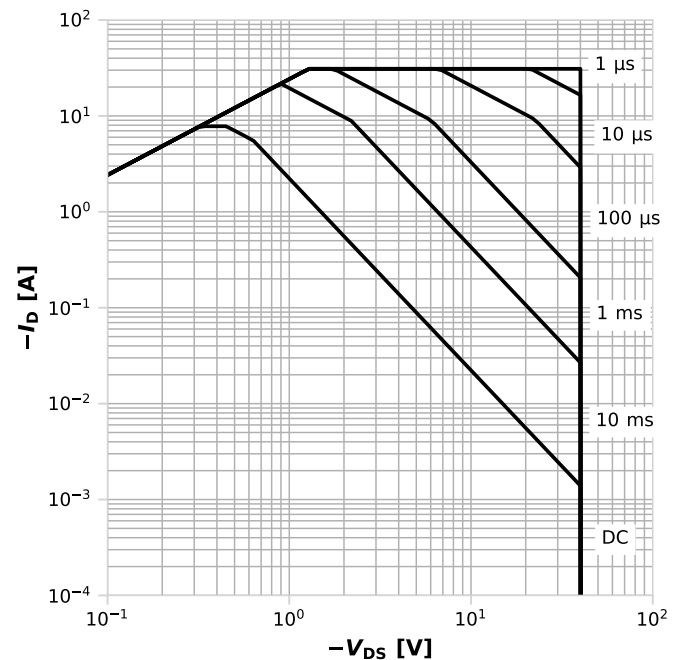
Diagram 16: Power dissipation (p-channel)



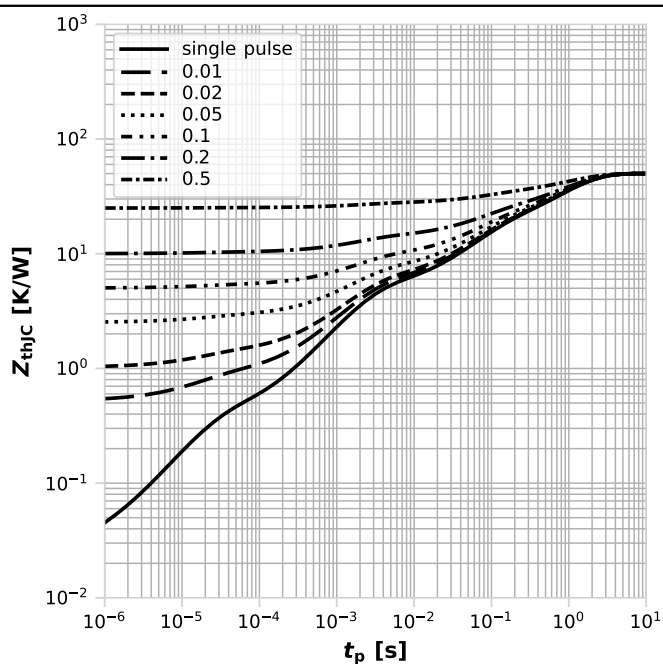
$P_{tot}=f(T_c)$

Diagram 17: Drain current (p-channel)


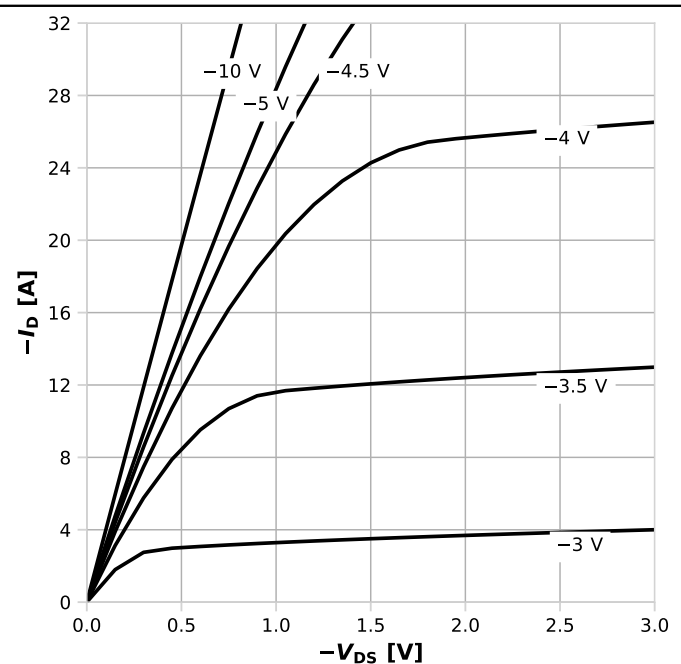
$$I_D = f(T_C); |V_{GS}| \geq 10 \text{ V}$$

Diagram 18: Safe operating area (p-channel)


$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0; \text{parameter: } t_p$$

Diagram 19: Max. transient thermal impedance (p-channel)


$$Z_{thJC} = f(t_p); \text{parameter: } D = t_p / T$$

Diagram 20: Typ. output characteristics (p-channel)


$$I_D = f(V_{DS}), T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$$

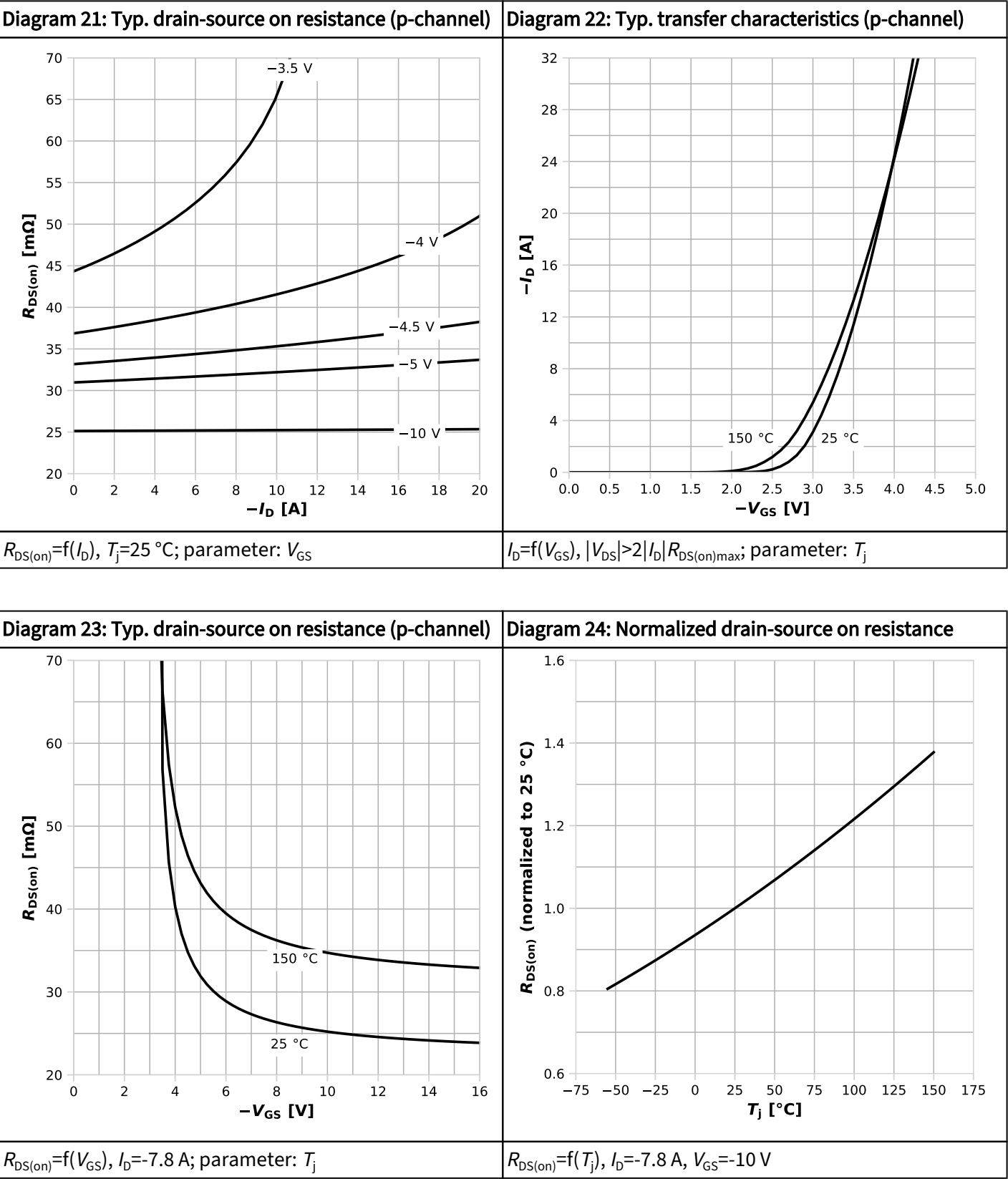


Diagram 25: Typ. gate threshold voltage (p-channel)

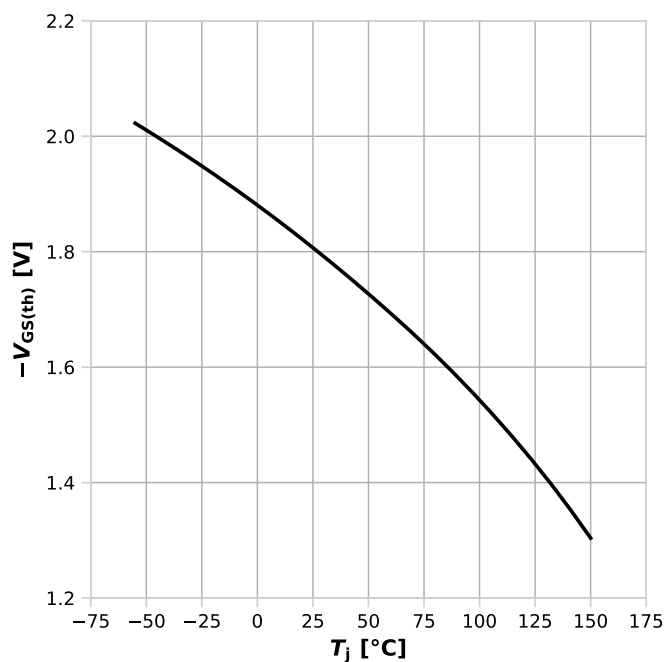

 $V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: $I_D = 1000 \mu A$

Diagram 26: Typ. capacitances (p-channel)

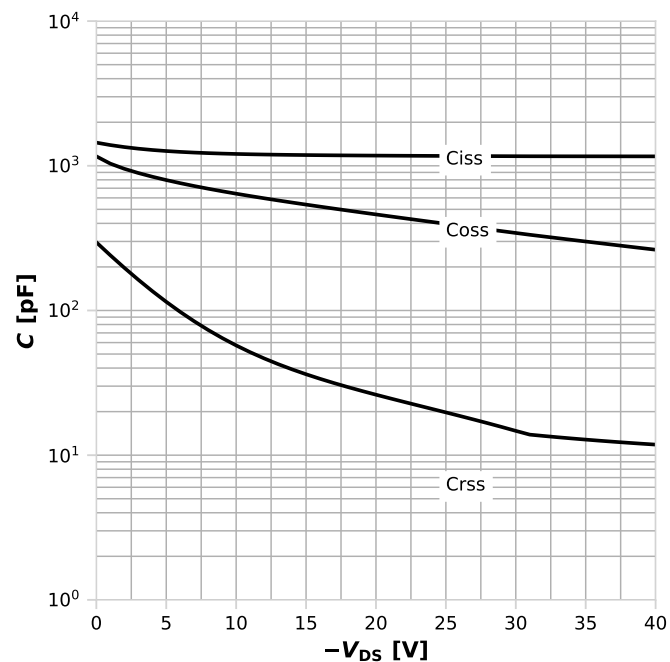

 $C = f(V_{DS})$; $V_{GS} = 0 V$; $f = 1 MHz$

Diagram 27: Forward characteristics of reverse diode (p-ch.)

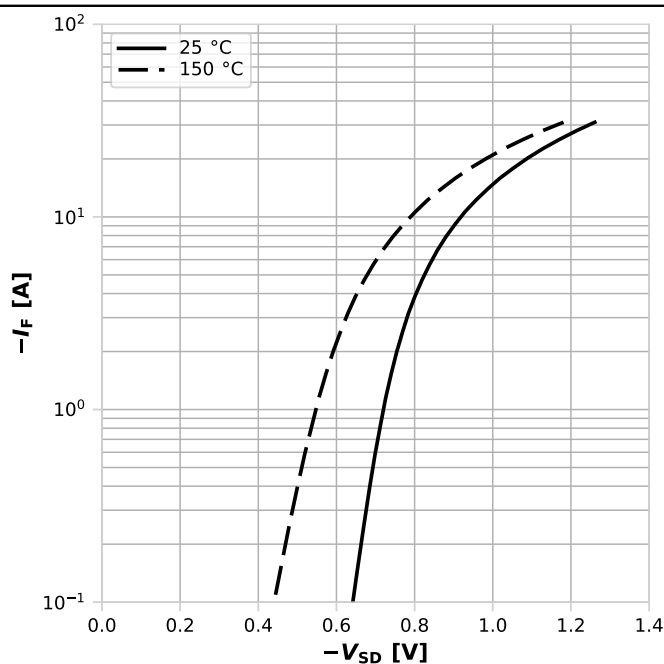
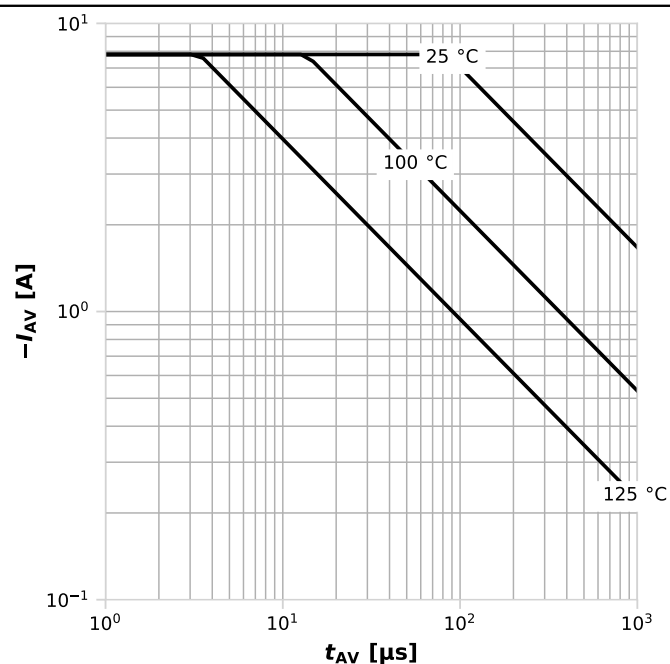
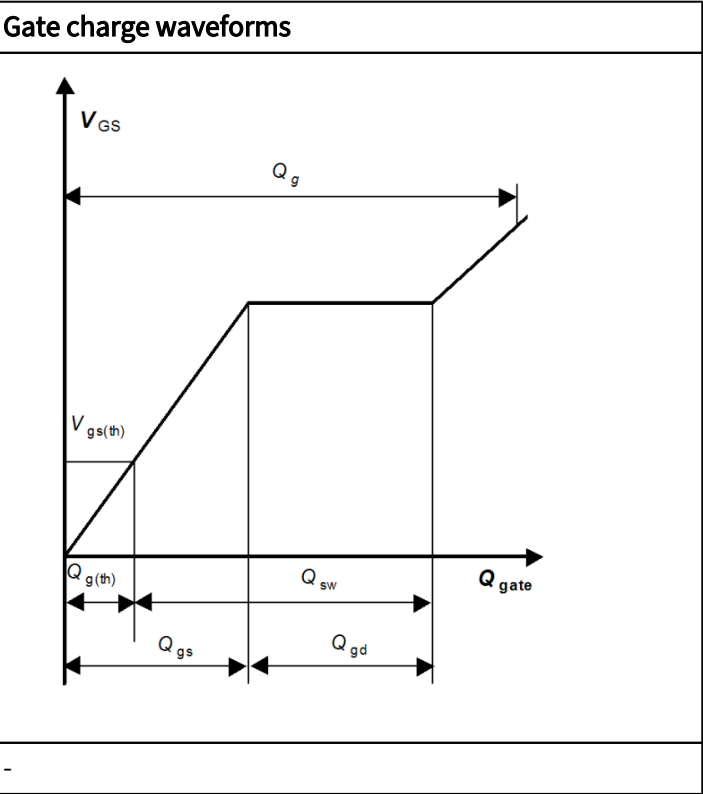
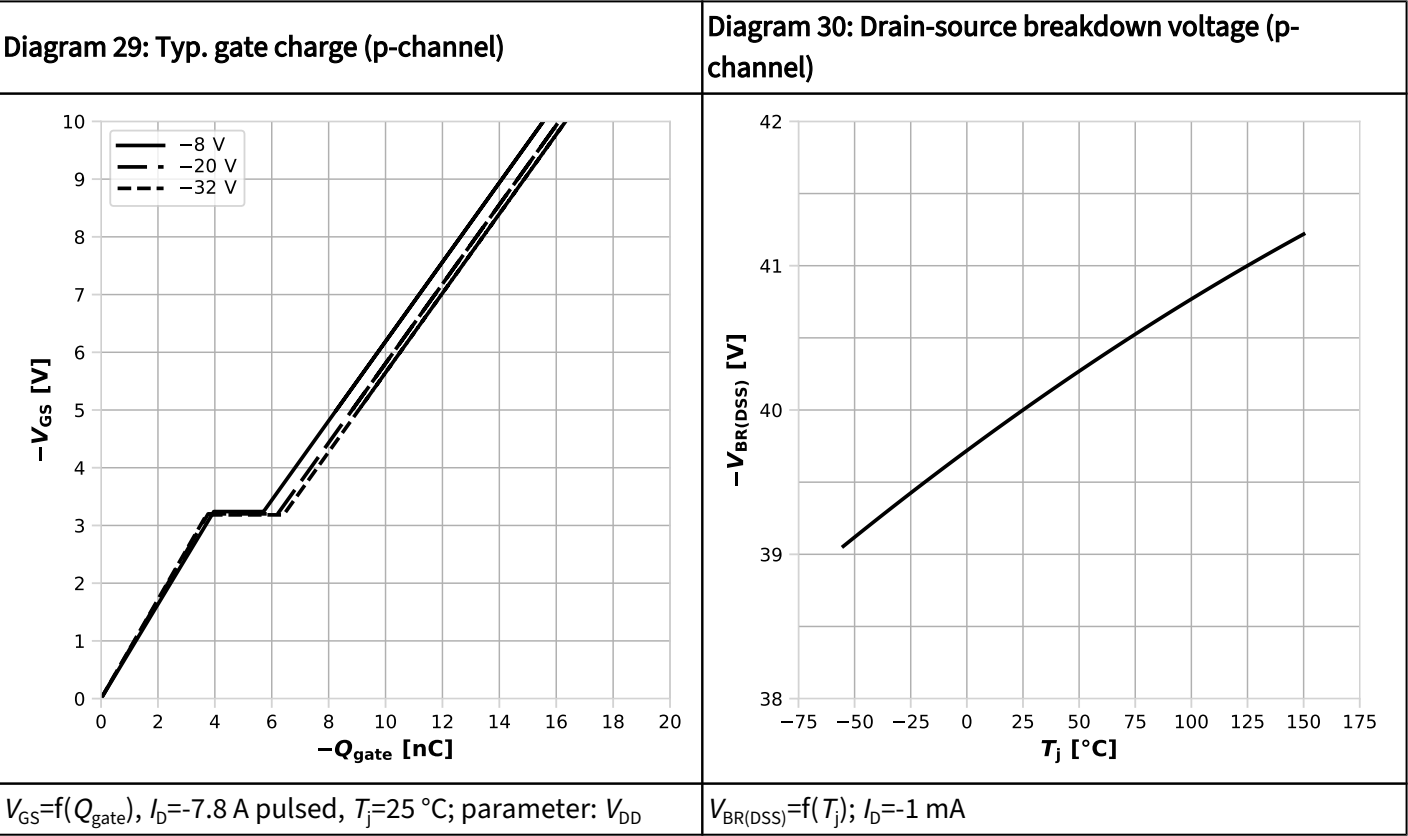
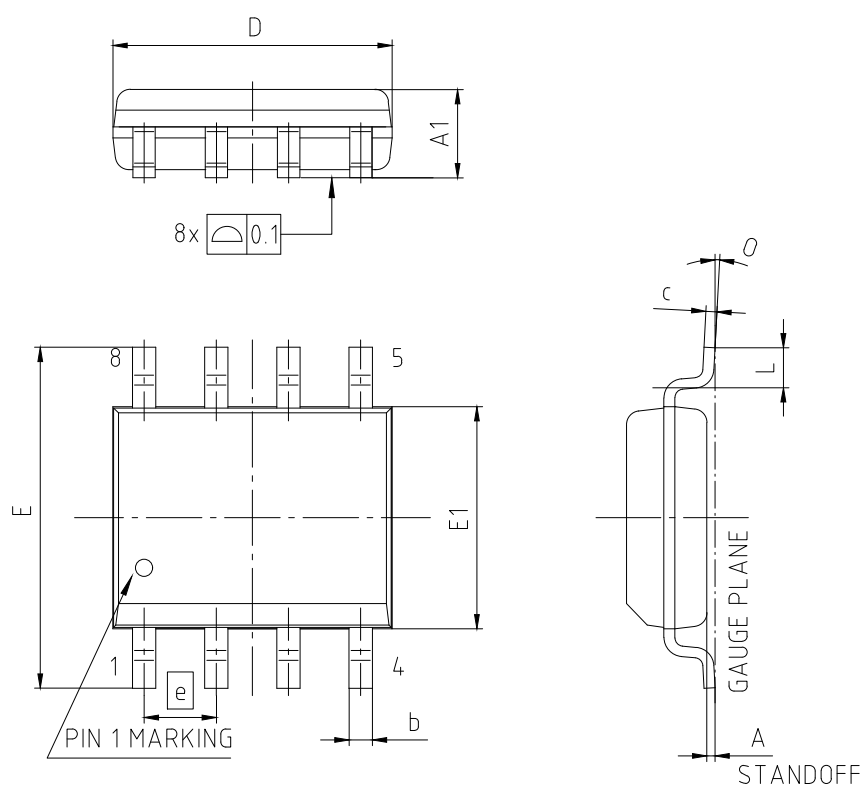

 $I_F = f(V_{SD})$; parameter: T_j

Diagram 28: Avalanche characteristics (p-channel)


 $I_{AS} = f(t_{AV})$; $R_{GS} = 25 \Omega$; parameter: $T_{j,start}$



5 Package Outlines



PACKAGE - GROUP NUMBER: PG-DSO-8-U02		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.18	0.25
A1	1.35	1.75
b	0.38	0.51
c	0.254	
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27	
L	0.48	0.91
O	4°	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-DSO-8, dimensions in mm

Revision History

ISA250300C04LMDS

Revision 2024-10-02, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-10-02	Release of final datasheet

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

Published by

Infineon Technologies AG
81726 München, Germany
© 2024 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[ISA250300C04LMDSXTMA1](#)