

IRS2153(1)D(S)PbF

SELF-OSCILLATING HALF-BRIDGE DRIVER IC

Features

- Integrated 600 V half-bridge gate driver
- C_T , R_T programmable oscillator
- 15.4 V Zener clamp on V_{CC}
- Micropower startup
- Non-latched shutdown on C_T pin ($1/6$ th V_{CC})
- Internal bootstrap FET
- Excellent latch immunity on all inputs and outputs
- +/- 50 V/ns dV/dt immunity
- ESD protection on all pins
- 8-lead SOIC or PDIP package
- Internal deadtime

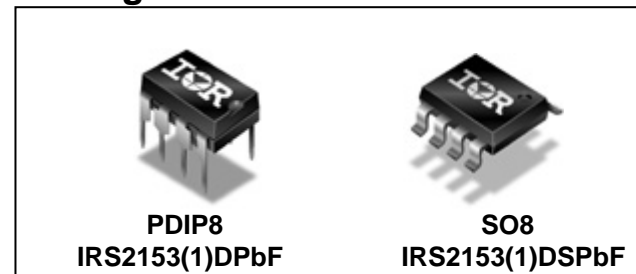
Product Summary

V_{OFFSET}	600 V Max
Duty cycle	50%
Driver source/sink current	180 mA/260 mA typ.
V_{clamp}	15.4 V typ.
Deadtime	1.1 μ s typ. (IRS2153D) 0.6 μ s typ. (IRS21531D)

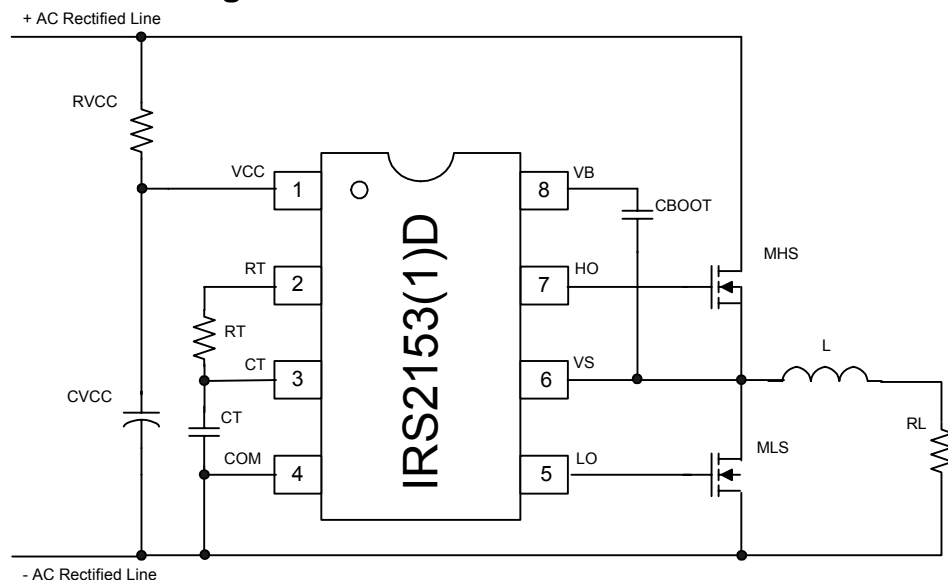
Description

The IRS2153(1)D is based on the popular IR2153 self-oscillating half-bridge gate driver IC using a more advanced silicon platform, and incorporates a high voltage half-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. HVIC and latch immune CMOS technologies enable rugged monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers.

Package



Typical Connection Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameter		Min.	Max.	Units
Symbol	Definition			
V_B	High side floating supply voltage	-0.3	625	V
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
I_{RT}	R_T pin current	-5	5	mA
V_{RT}	R_T pin voltage	-0.3	$V_{CC} + 0.3$	V
V_{CT}	C_T pin voltage	-0.3	$V_{CC} + 0.3$	
I_{CC}	Supply current (Note 1)	---	20	mA
I_{OMAX}	Maximum allowable current at LO and HO due to external power transistor Miller effect.	-500	500	
dV_S/dt	Allowable offset voltage slew rate	-50	50	V/ns
P_D	Maximum power dissipation @ $T_A \leq +25^\circ\text{C}$, 8-Pin DIP	---	1.0	W
P_D	Maximum power dissipation @ $T_A \leq +25^\circ\text{C}$, 8-Pin SOIC	---	0.625	
R_{thJA}	Thermal resistance, junction to ambient, 8-Pin DIP	---	85	$^\circ\text{C/W}$
R_{thJA}	Thermal resistance, junction to ambient, 8-Pin SOIC	---	128	
T_J	Junction temperature	-55	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.4 V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Parameter		Min.	Max.	Units
Symbol	Definition			
V_{BS}	High side floating supply voltage	$V_{CC} - 0.7$	V_{CLAMP}	V
V_S	Steady state side floating supply offset voltage	-3.0 (Note 2)	600	
V_{CC}	Supply voltage	$V_{CCUV+} + 0.1$ V	$V_{CC CLAMP}$	
I_{CC}	Supply current	(Note 3)	5	mA
T_J	Junction temperature	-40	125	°C

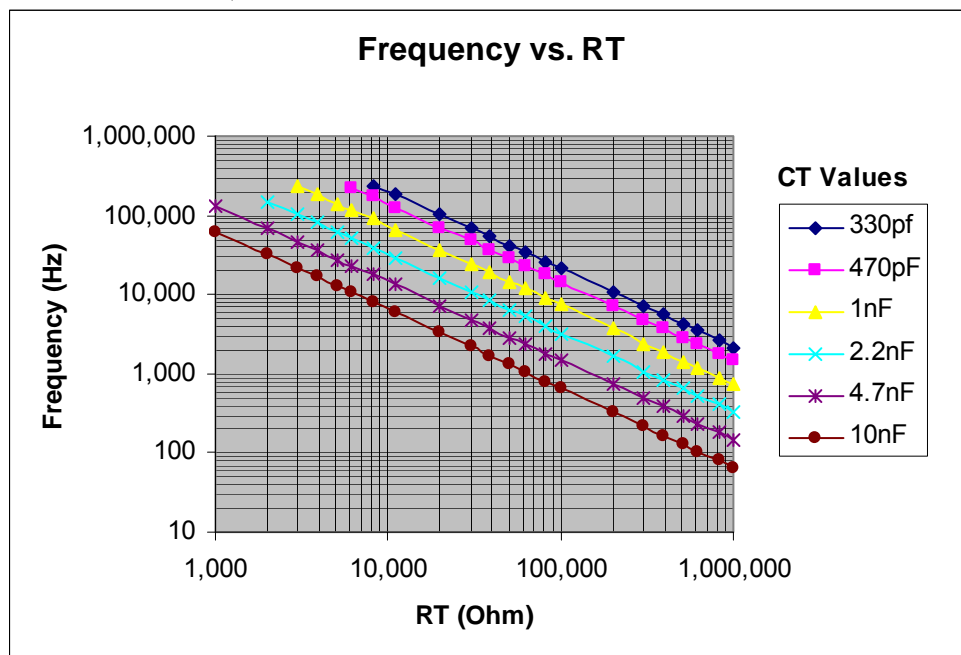
Note 2: It is recommended to avoid output switching conditions where the negative-going spikes at the V_S node would decrease V_S below ground by more than -5 V.

Note 3: Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6 V zener diode clamping the voltage at this pin.

Recommended Component Values

Parameter		Min.	Max.	Units
Symbol	Component			
R_T	Timing resistor value	1	---	k Ω
C_T	C_T pin capacitor value	330	---	pF

$V_{BIAS} (V_{CC}, V_{BS}) = 14$ V, $V_S = 0$ V and $T_A = 25$ °C, $C_{LO} = C_{HO} = 1$ nF.



For further information, see Fig. 12.

Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 14 V, C_T = 1 nF, V_S = 0 V and T_A = 25 °C unless otherwise specified. The output voltage and current (V_o and I_o) parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO = CHO = 1 nF.

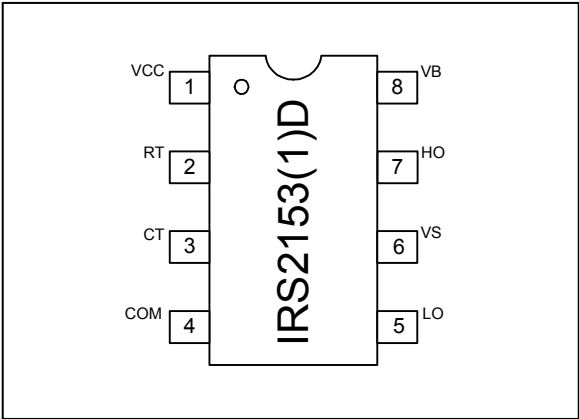
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V _{CCUV+}	Rising V _{CC} undervoltage lockout threshold	10.0	11.0	12.0	V	
V _{CCUV-}	Falling V _{CC} undervoltage lockout threshold	8.0	9.0	10.0		
V _{CCUVHYS}	V _{CC} undervoltage lockout hysteresis	1.6	2.0	2.4		
I _{QCCUV}	Micropower startup V _{CC} supply current	---	130	170	μA	V _{CC} ≤ V _{CCUV-}
I _{QCC}	Quiescent V _{CC} supply current	---	800	1000		
I _{CC}	V _{CC} supply current	---	1.8	---	mA	R _T = 36.9 kΩ
V _{CC CLAMP}	V _{CC} zener clamp voltage	14.4	15.4	16.8	V	I _{CC} = 5 mA
Floating Supply Characteristics						
I _{QBS}	Quiescent V _{BS} supply current	---	60	80	μA	
V _{BSUV+}	V _{BS} supply undervoltage positive going threshold	8.0	9.0	9.5	V	
V _{BSUV-}	V _{BS} supply undervoltage negative going threshold	7.0	8.0	9.0		
I _{LK}	Offset supply leakage current	---	---	50	μA	V _B = V _S = 600 V
Oscillator I/O Characteristics						
f _{OSC}	Oscillator frequency	18.4	19.0	19.6	kHz	R _T = 36.5 kΩ
		88	93	100		R _T = 7.15 kΩ
d	R _T pin duty cycle	---	50	---	%	f _o < 100 kHz
I _{CT}	C _T pin current	---	0.02	1.0	μA	
I _{CTUV}	UV-mode C _T pin pulldown current	0.20	0.30	0.6	mA	V _{CC} = 7 V
V _{CT+}	Upper C _T ramp voltage threshold	---	9.32	---	V	
V _{CT-}	Lower C _T ramp voltage threshold	---	4.66	---		
V _{CTSD}	C _T voltage shutdown threshold	2.2	2.3	2.4		
V _{RT+}	High-level R _T output voltage, V _{CC} - V _{RT}	---	10	50	mV	I _{RT} = -100 μA
		---	100	300		I _{RT} = -1 mA
V _{RT-}	Low-level R _T output voltage	---	10	50		I _{RT} = 100 μA
		---	100	300		I _{RT} = 1 mA
V _{RTUV}	UV-mode R _T output voltage	---	0	100		V _{CC} ≤ V _{CCUV-}
V _{RTSD}	SD-mode R _T output voltage, V _{CC} - V _{RT}	---	10	50		I _{RT} = -100 μA, V _{CT} = 0 V
		---	100	300		I _{RT} = -1 mA, V _{CT} = 0 V

Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 14 V, C_T = 1 nF, V_S =0 V and T_A = 25 °C unless otherwise specified. The output voltage and current (V_o and I_o) parameters are referenced to COM and are applicable to the respective output leads: HO or LO. C_{LO} = C_{HO} = 1 nF.

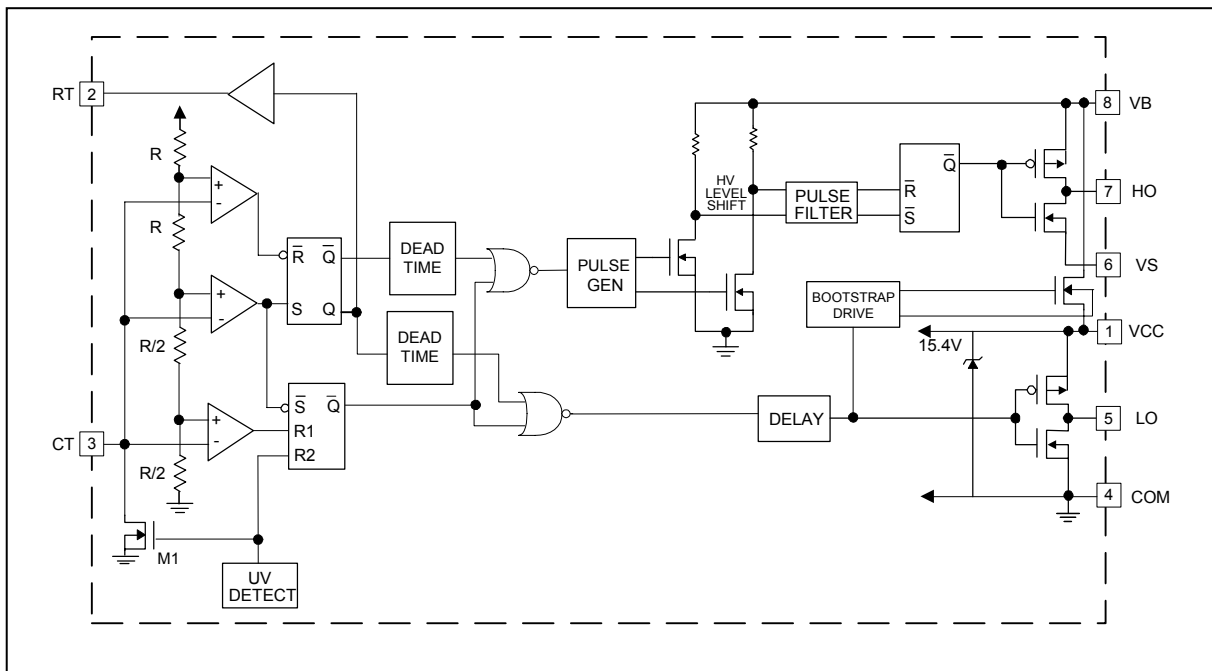
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver Output Characteristics						
V _{OH}	High-level output voltage	---	V _{CC}	---	V	I _O = 0 A
V _{OL}	Low-level output voltage	---	COM	---		I _O = 0 A, V _{CC} ≤ V _{CCUV-}
V _{OL_UV}	UV-mode output voltage	---	COM	---		
t _r	Output rise time	---	120	220	ns	
t _f	Output fall time	---	50	80		
t _{sd}	Shutdown propagation delay	---	350	---		
t _d	Output deadtime (HO or LO) (IRS2153D)	0.65	1.1	1.75	μs	
t _d	Output deadtime (HO or LO) (IRS21531D)	0.35	0.6	0.85	μs	
I _{O+}	Output source current	---	180	---	mA	
I _{O-}	Output sink current	---	260	---		
Bootstrap FET Characteristics						
V _{B_ON}	V _B when the bootstrap FET is on	---	13.7	---	V	
I _{B_CAP}	V _B source current when FET is on	40	55	---	mA	C _{BS} =0.1 uF
I _{B_10V}	V _B source current when FET is on	10	12	---		V _B =10 V

Lead Definitions



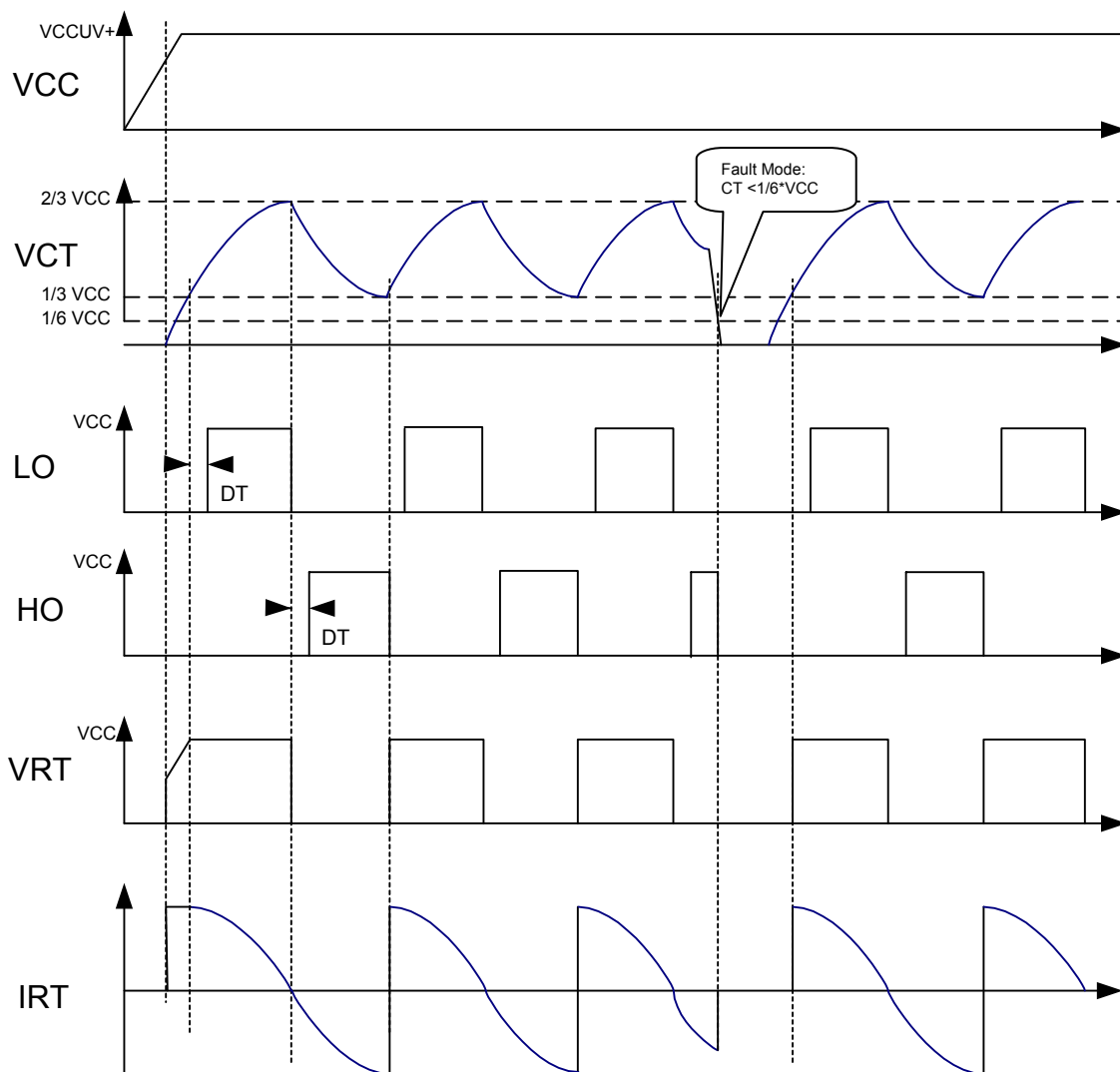
Lead	
Symbol	Description
V _{CC}	Logic and internal gate drive supply voltage
R _T	Oscillator timing resistor input
C _T	Oscillator timing capacitor input
COM	IC power and signal ground
LO	Low-side gate driver output
V _S	High voltage floating supply return
HO	High-side gate driver output
V _B	High side gate driver floating supply

Functional Block Diagram

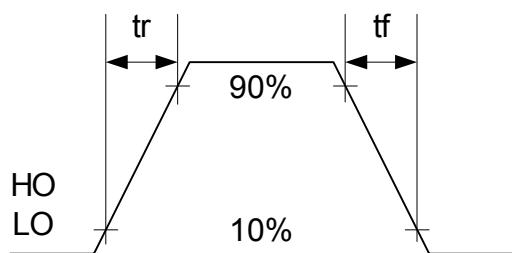


Timing Diagram

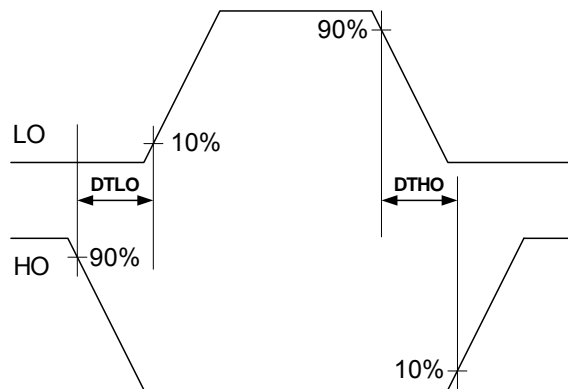
Operating Mode



Switching Time Waveform



Deadtime Waveform



Functional Description

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lockout mode (UVLO) is defined as the state the IC is in when V_{CC} is below the turn-on threshold of the IC. The IRS2153(1)D under voltage lock-out is designed to maintain an ultra low supply current of less than 170 μA , and to guarantee the IC is fully functional before the high and low side output drivers are activated. During under voltage lock-out mode, the high and low-side driver outputs HO and LO are both low.

Supply voltage

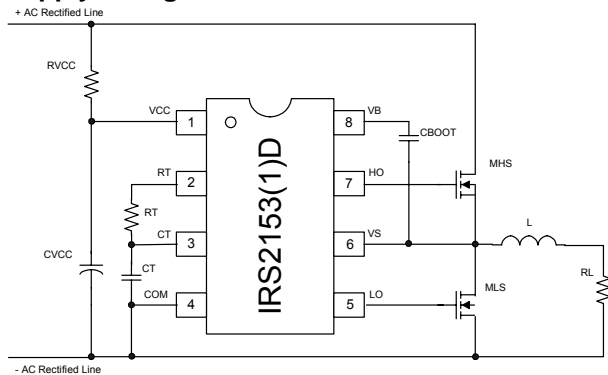


Fig. 1 Typical Connection Diagram

Fig. 1 shows an example of supply voltage. The start-up capacitor (C_{VCC}) is charged by current through supply resistor (R_{VCC}) minus the start-up current drawn by the IC. This resistor is chosen to provide sufficient current to supply the IRS2153(1)D from the DC bus. C_{VCC} should be large enough to hold the voltage at V_{CC} above the UVLO threshold for one half cycle of the line voltage as it will only be charged at the peak, typically 0.1 μF . It will be necessary for R_{VCC} to dissipate around 1 W.

The use of a two diode charge pump made of DC1, DC2 and CVS (Fig. 2) from the half bridge (V_s) is also possible however the above approach is simplest and the dissipation in R_{VCC} should not be unacceptably high.

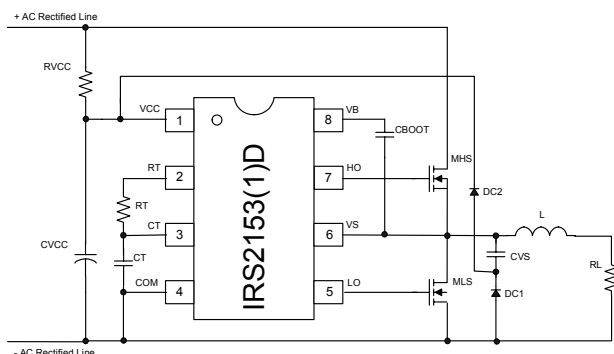


Fig. 2 Charge pump circuit

The supply resistor (R_{VCC}) must be selected such that enough supply current is available over all operating conditions.

Once the capacitor voltage on V_{CC} reaches the start-up threshold V_{CCUV+} , the IC turns on and HO and LO begin to oscillate.

Bootstrap MOSFET

The internal bootstrap FET and supply capacitor (C_{BOOT}) comprise the supply voltage for the high side driver circuitry. The internal bootstrap FET only turns on when LO is high. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin.

Normal operating mode

Once the V_{CCUV+} threshold is passed, the MOSFET M1 opens, RT increases to approximately V_{CC} ($V_{CC}-V_{RT+}$) and the external CT capacitor starts charging. Once the CT voltage reaches V_{CT-} (about 1/3 of V_{CC}), established by an internal resistor ladder, LO turns on with a delay equivalent to the deadtime (t_d). Once the CT voltage reaches V_{CT+} (approximately 2/3 of V_{CC}), LO goes low, RT goes down to approximately ground (V_{RT-}), the CT capacitor discharges and the deadtime circuit is activated. At the end of the deadtime, HO goes high. Once the CT voltage reaches V_{CT-} , HO goes low, RT goes high again, the deadtime is activated. At the end of the deadtime, LO goes high and the cycle starts over again.

The following equation provides the oscillator frequency:

$$f \sim \frac{1}{1.453 \times RT \times CT}$$

This equation can vary slightly from actual measurements due to internal comparator over- and under-shoot delays. For a more accurate determination of the output frequency, the frequency characteristic curves should be used (RT vs. Frequency, page 3).

Shut-down

If CT is pulled down below V_{CTSD} (approximately $1/6$ of V_{CC}) by an external circuit, CT doesn't charge up and oscillation stops. LO is held low and the bootstrap FET is off. Oscillation will resume once CT is able to charge up again to V_{CT-} .

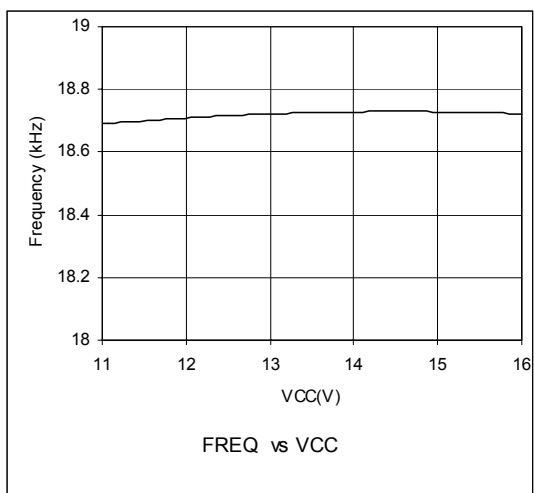


Fig. 3

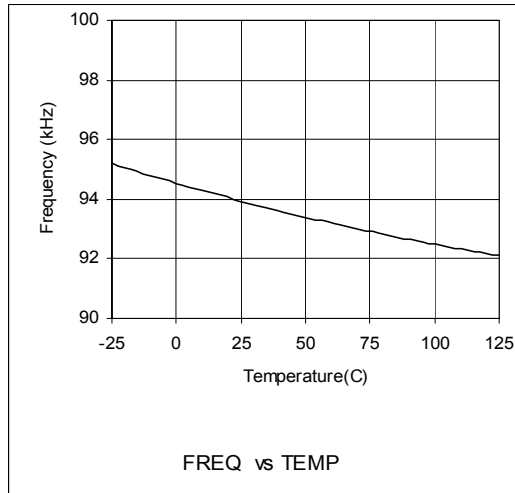


Fig. 4

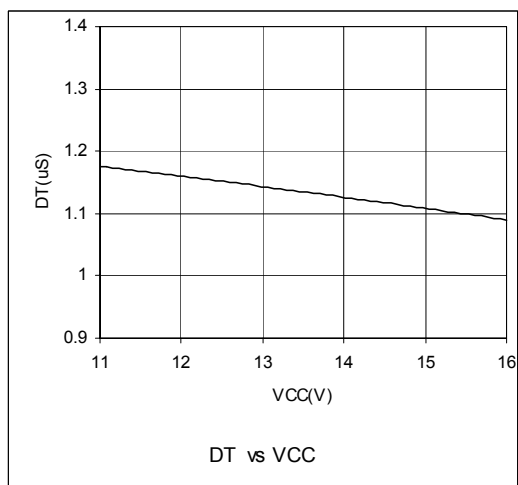


Fig. 5 (IRS2153D)

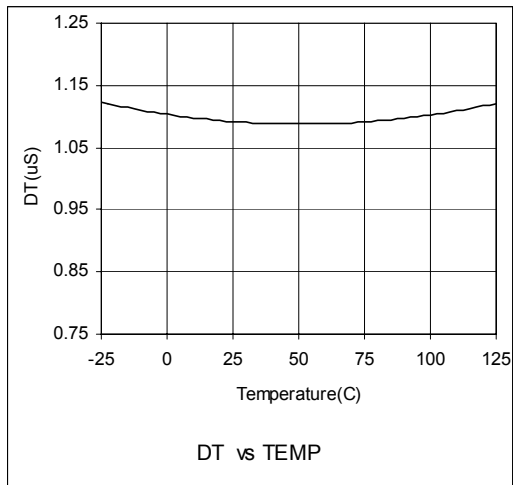


Fig. 6 (IRS2153D)

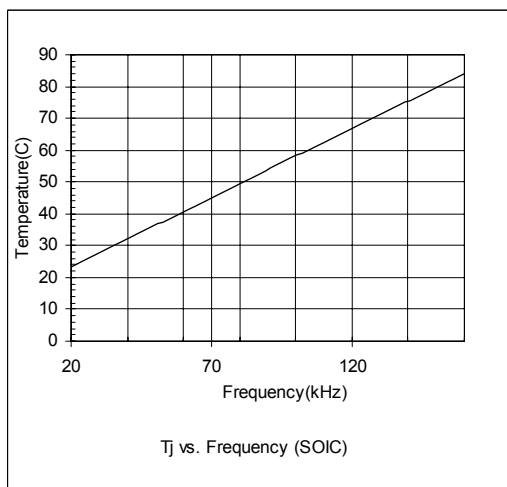


Fig. 7

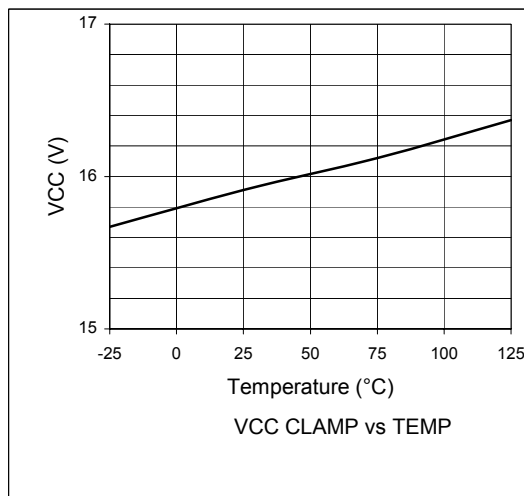


Fig. 8

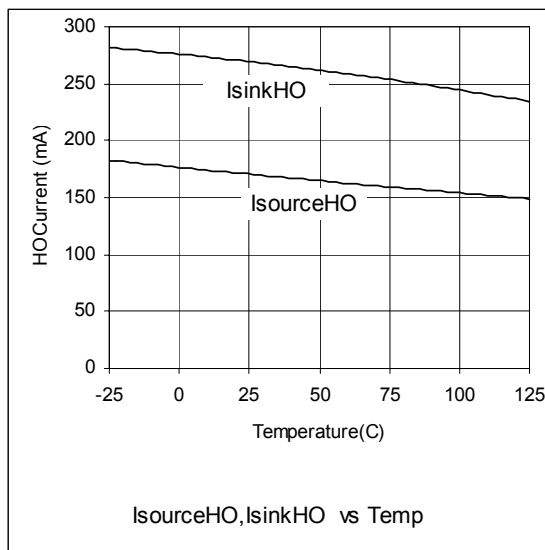


Fig. 9

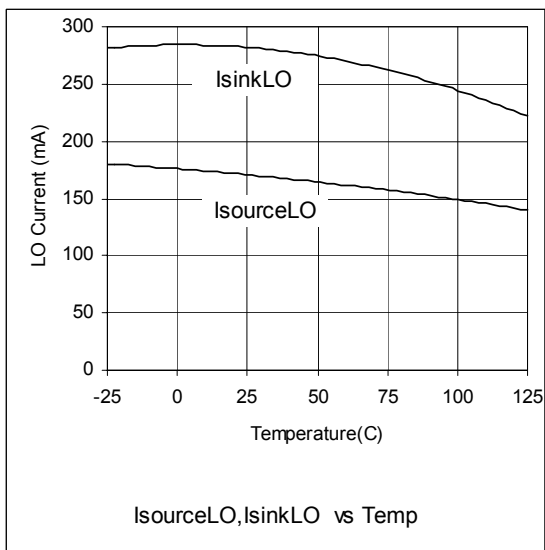


Fig. 10

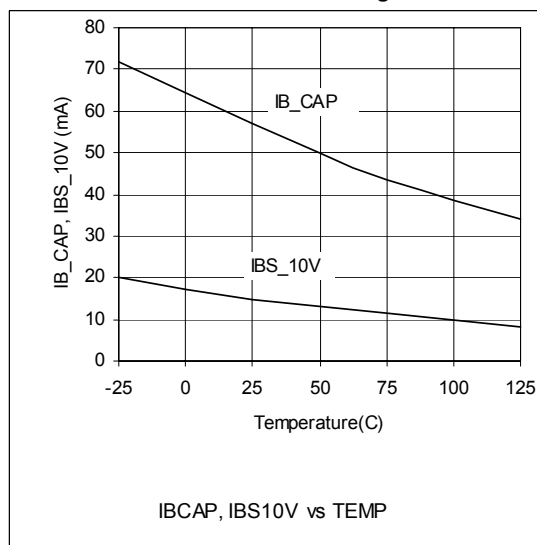


Fig. 11

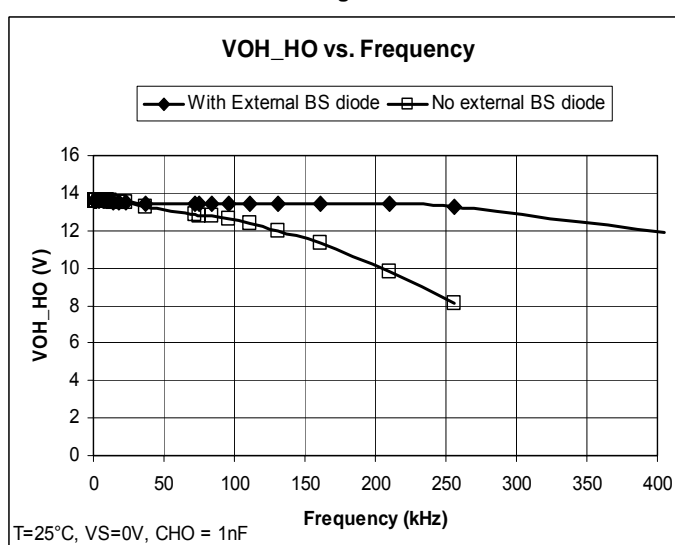


Fig. 12

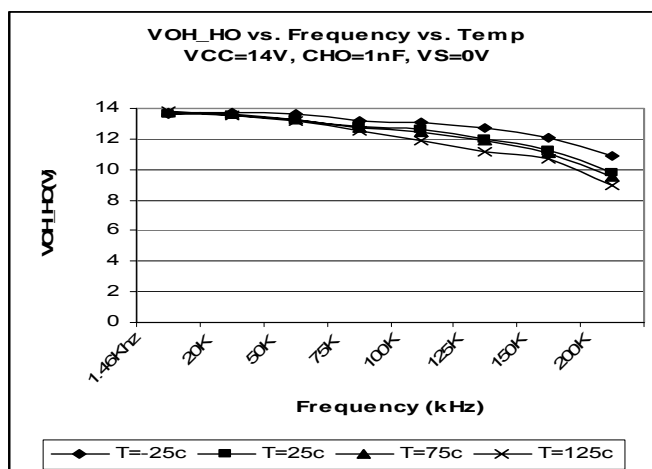
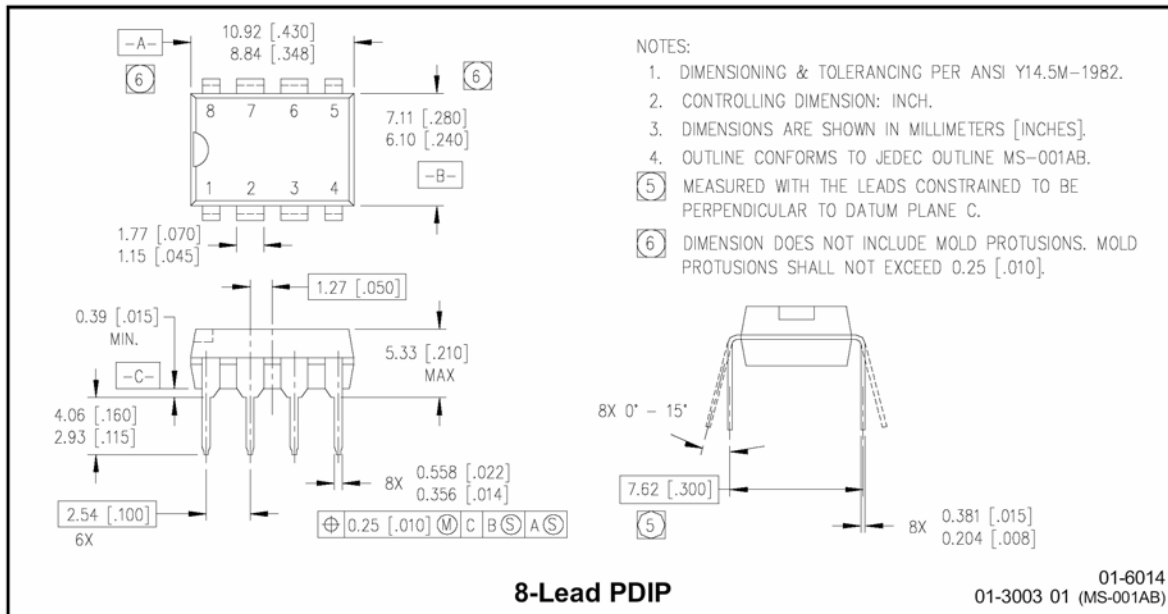
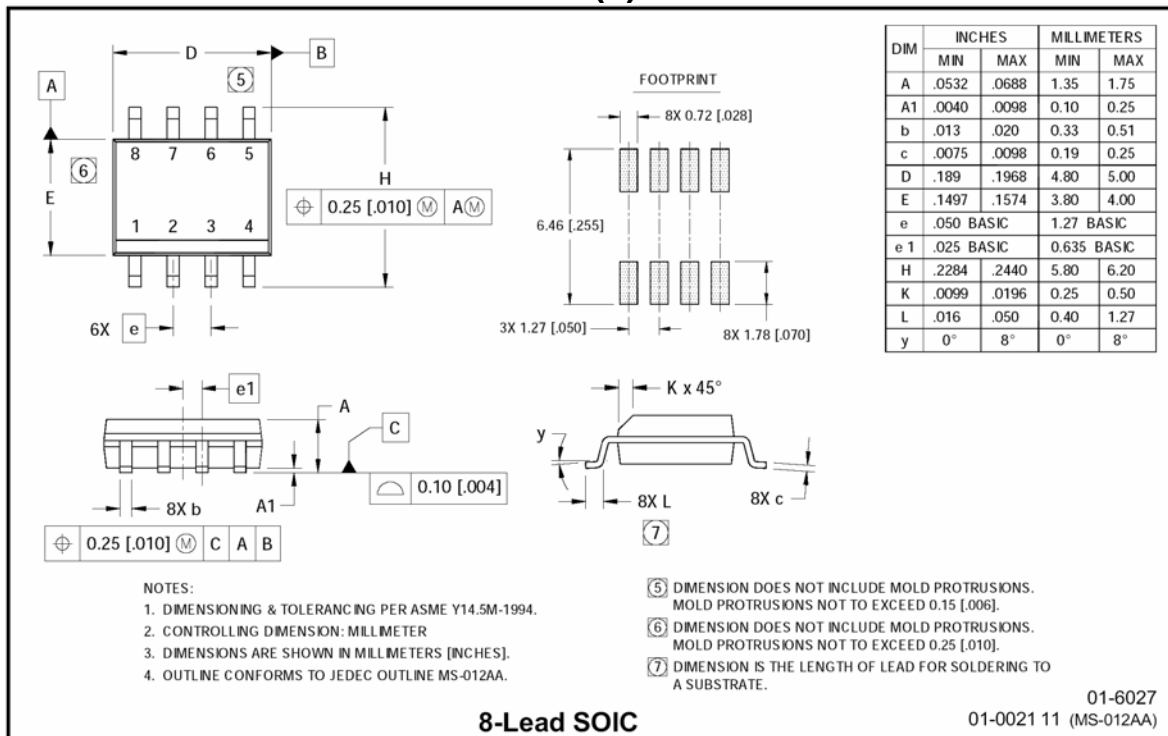


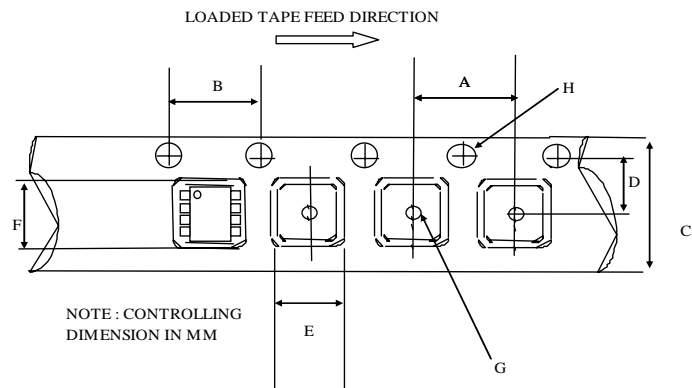
Fig. 13



IRS2153(1)DPbF

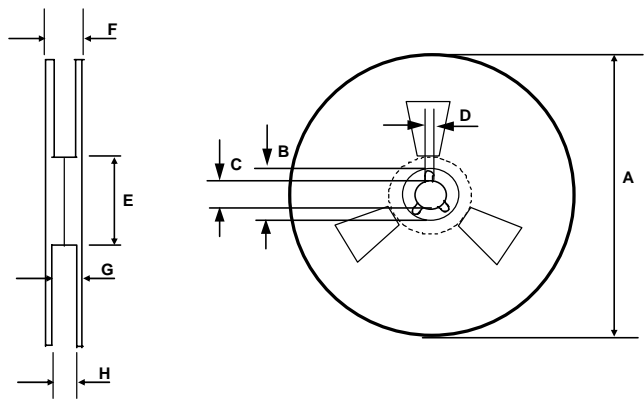


IRS2153(1)DSPbF



CARRIER TAPE DIMENSION FOR 8SOICN

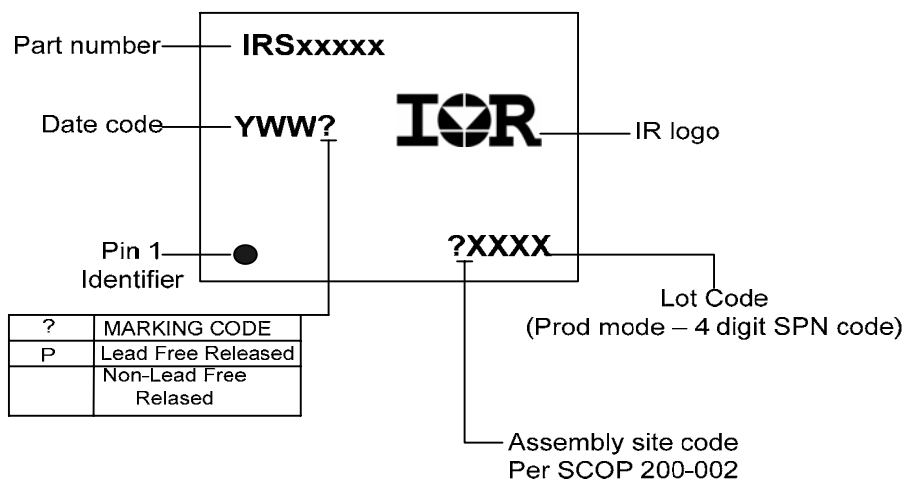
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

PART MARKING INFORMATION



ORDER INFORMATION

8-Lead PDIP IRS2153DPbF

8-Lead PDIP IRS21531DPbF

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