

## HIGH AND LOW SIDE DRIVER

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +500 V or +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground  $\pm 5V$  offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant

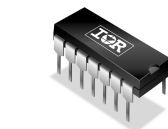
### Description

The IRS2110/IRS2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 500 V or 600 V.

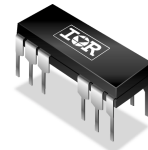
### Product Summary

V <sub>OFFSET</sub> (IRS2110)	500 V max.
(IRS2113)	600 V max.
I <sub>O+/-</sub>	2 A/2 A
V <sub>OUT</sub>	10 V - 20 V
t <sub>on/off</sub> (typ.)	130 ns & 120 ns
Delay Matching (IRS2110)	10 ns max.
(IRS2113)	20 ns max.

### Packages



14-Lead PDIP  
IRS2110 and IRS2113



16-Lead PDIP  
(w/o leads 4 & 5)  
IRS2110-2 and IRS2113-2

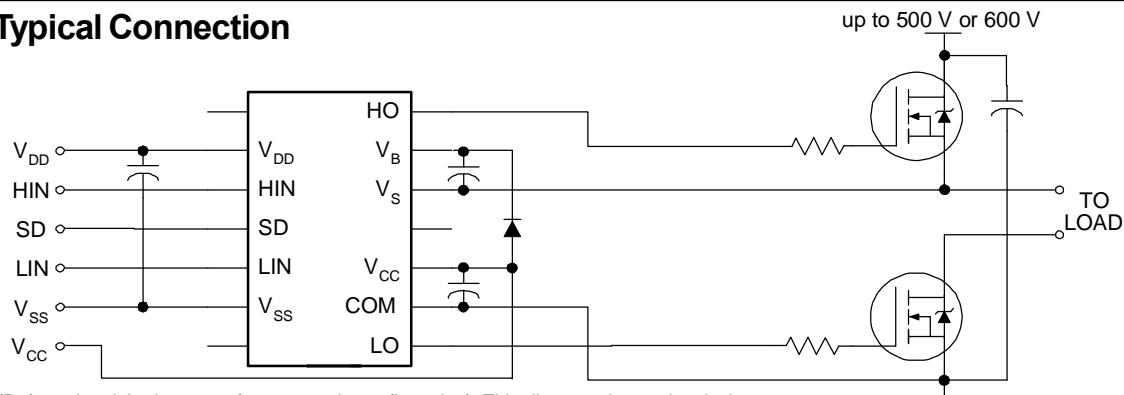


14-Lead PDIP  
(w/o lead 4)  
IRS2110-1 and IRS2113-1



16-Lead SOIC  
IRS2110S and  
IRS2113S

### Typical Connection



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figs. 28 through 35.

Symbol	Definition		Min.	Max.	Units
V <sub>B</sub>	High-side floating supply voltage	(IRS2110)	-0.3	520 (Note 1)	V
		(IRS2113)	-0.3	620 (Note 1)	
V <sub>S</sub>	High-side floating supply offset voltage		V <sub>B</sub> - 20	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High-side floating output voltage		V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low-side fixed supply voltage		-0.3	20 (Note 1)	
V <sub>LO</sub>	Low-side output voltage		-0.3	V <sub>CC</sub> + 0.3	
V <sub>DD</sub>	Logic supply voltage		-0.3	V <sub>SS</sub> +20 (Note 1)	
V <sub>SS</sub>	Logic supply offset voltage		V <sub>CC</sub> - 20	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic input voltage (HIN, LIN, & SD)		V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable offset supply voltage transient (Fig. 2)		—	50	
PD	Package power dissipation @ T <sub>A</sub> ≤ +25 °C	(14 lead DIP)	—	1.6	W
		(16 lead SOIC)	—	1.25	
R <sub>THJA</sub>	Thermal resistance, junction to ambient	(14 lead DIP)	—	75	°C/W
		(16 lead SOIC)	—	100	
T <sub>J</sub>	Junction temperature		—	150	°C
T <sub>S</sub>	Storage temperature		-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: All supplies are fully tested at 25 V, and an internal 20 V clamp exists for each supply.

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation, the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset ratings are tested with all supplies biased at a 15 V differential. Typical ratings at other bias conditions are shown in Figs. 36 and 37.

Symbol	Definition		Min.	Max.	Units
V <sub>B</sub>	High-side floating supply absolute voltage		V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage	(IRS2110)	Note 2	500	
		(IRS2113)	Note 2	600	
V <sub>HO</sub>	High-side floating output voltage		V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side fixed supply voltage		10	20	
V <sub>LO</sub>	Low-side output voltage		0	V <sub>CC</sub>	
V <sub>DD</sub>	Logic supply voltage		V <sub>SS</sub> + 3	V <sub>SS</sub> + 20	
V <sub>SS</sub>	Logic supply offset voltage		-5 (Note 3)	5	
V <sub>IN</sub>	Logic input voltage (HIN, LIN & SD)		V <sub>SS</sub>	V <sub>DD</sub>	
T <sub>A</sub>	Ambient temperature		-40	125	°C

Note 2: Logic operational for V<sub>S</sub> of -4 V to +500 V. Logic state held for V<sub>S</sub> of -4 V to -V<sub>BS</sub>. (Refer to the Design Tip DT97-3)

Note 3: When V<sub>DD</sub> < 5 V, the minimum V<sub>SS</sub> offset is limited to -V<sub>DD</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15 V,  $C_L$  = 1000 pF,  $T_A$  = 25 °C and  $V_{SS}$  = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

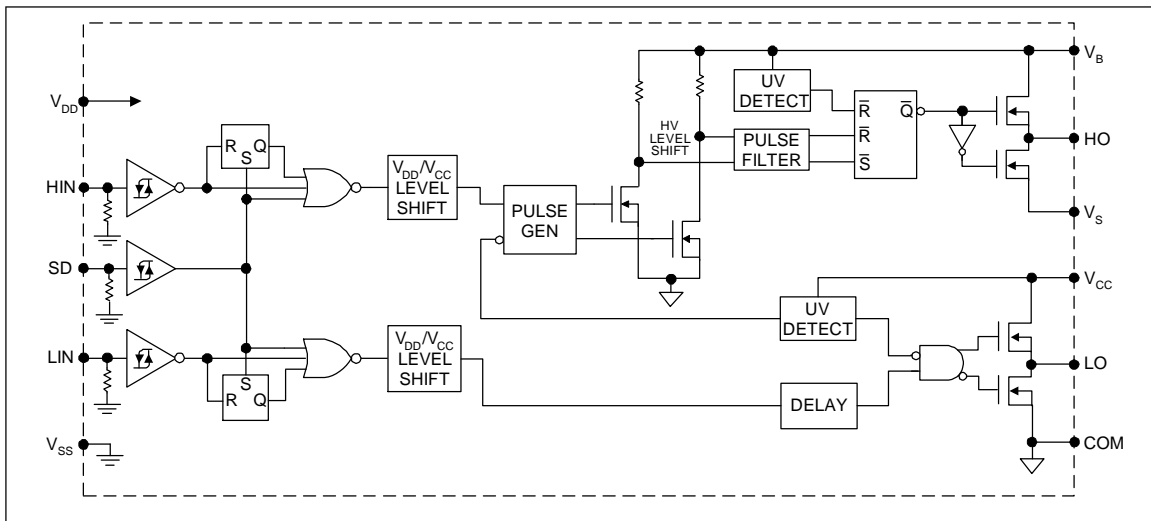
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	130	160	ns	$V_S = 0$ V
$t_{off}$	Turn-off propagation delay	—	120	150		$V_S = 500$ V/600 V
$t_{sd}$	Shutdown propagation delay	—	130	160		
$t_r$	Turn-on rise time	—	25	35		
$t_f$	Turn-off fall time	—	17	25		
MT	Delay matching, HS & LS turn-on/off	(IRS2110)	—	—		10
		(IRS2113)	—	—	20	

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15 V,  $T_A$  = 25 °C and  $V_{SS}$  = COM unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input leads: HIN, LIN, and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage	9.5	—	—	V	
$V_{IL}$	Logic "0" input voltage	—	—	6.0		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4		$I_O = 0$ A
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.15		$I_O = 20$ mA
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu$ A	$V_B = V_S = 500$ V/600 V
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	125	230		$V_{IN} = 0$ V or $V_{DD}$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	180	340		
$I_{QDD}$	Quiescent $V_{DD}$ supply current	—	15	30		
$I_{IN+}$	Logic "1" input bias current	—	20	40		$V_{IN} = V_{DD}$
$I_{IN-}$	Logic "0" input bias current	—	—	5.0	$V_{IN} = 0$ V	
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold	7.5	8.6	9.7	V	
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold	7.0	8.2	9.4		
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	7.4	8.5	9.6		
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.0	8.2	9.4		
$I_{O+}$	Output high short circuit pulsed current	2.0	2.5	—	A	$V_O = 0$ V, $V_{IN} = V_{DD}$ $PW \leq 10$ $\mu$ s
$I_{O-}$	Output low short circuit pulsed current	2.0	2.5	—		$V_O = 15$ V, $V_{IN} = 0$ V $PW \leq 10$ $\mu$ s

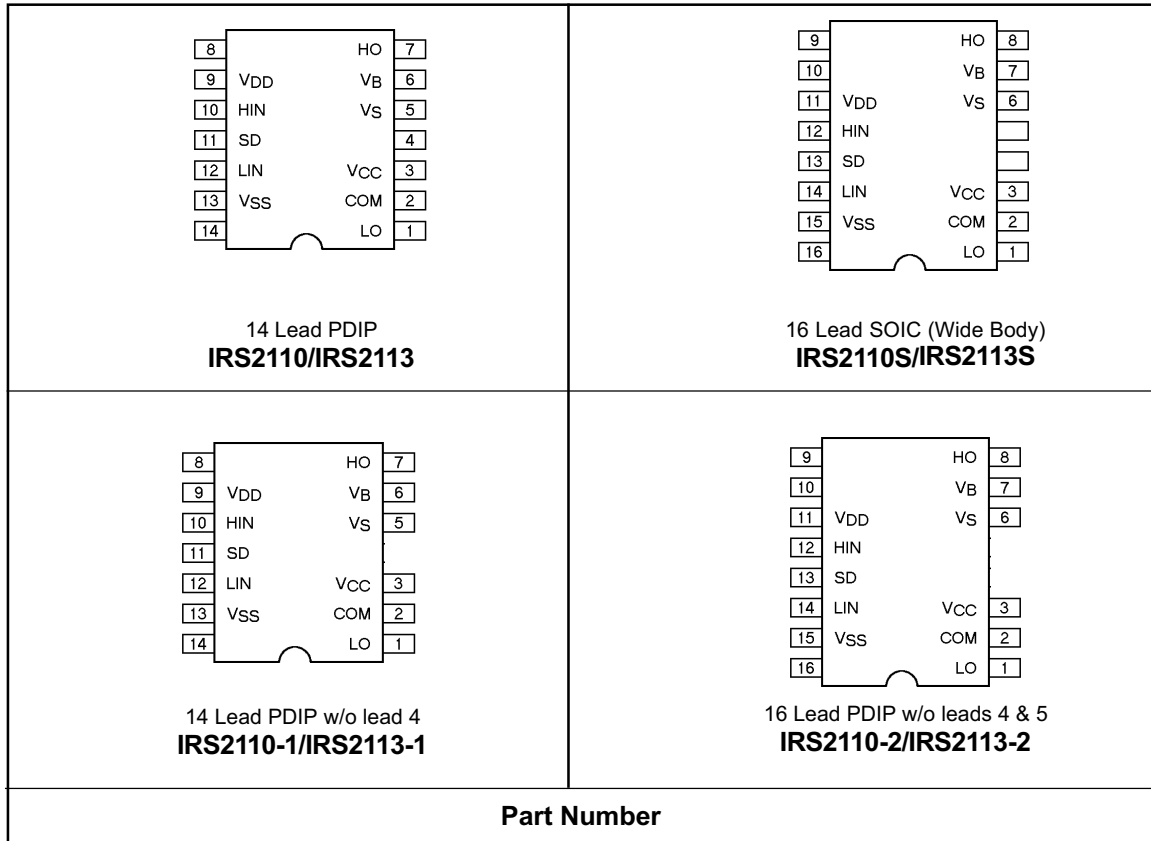
### Functional Block Diagram



### Lead Definitions

Symbol	Description
V <sub>DD</sub>	Logic supply
HIN	Logic input for high-side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low-side gate driver output (LO), in phase
V <sub>SS</sub>	Logic ground
V <sub>B</sub>	High-side floating supply
HO	High-side gate drive output
V <sub>S</sub>	High-side floating supply return
V <sub>CC</sub>	Low-side supply
LO	Low-side gate drive output
COM	Low-side return

**Lead Assignments**



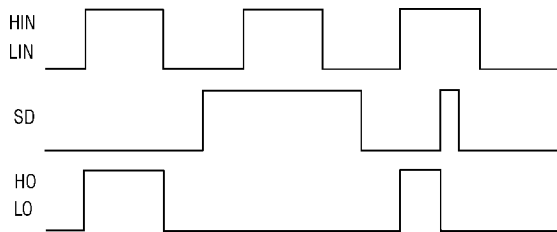


Figure 1. Input/Output Timing Diagram

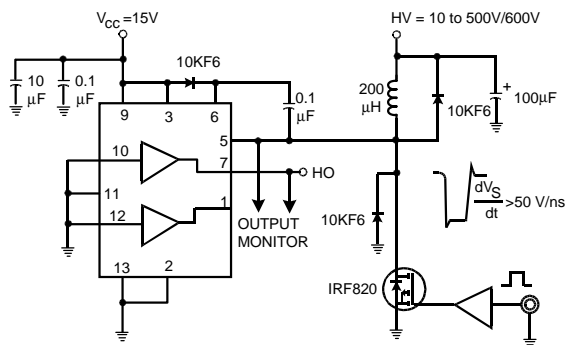


Figure 2. Floating Supply Voltage Transient Test Circuit

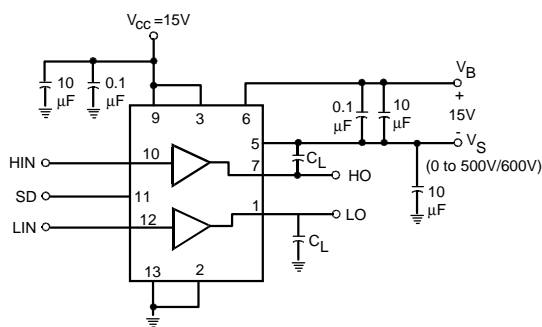


Figure 3. Switching Time Test Circuit

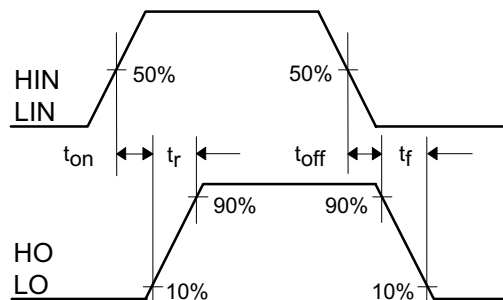


Figure 4. Switching Time Waveform Definition

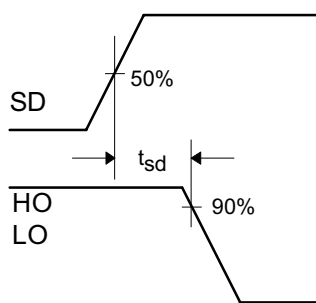


Figure 5. Shutdown Waveform Definitions

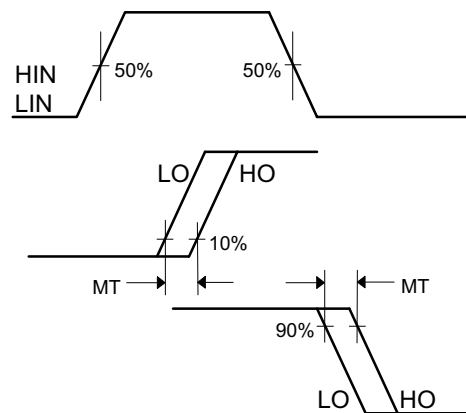


Figure 6. Delay Matching Waveform Definitions

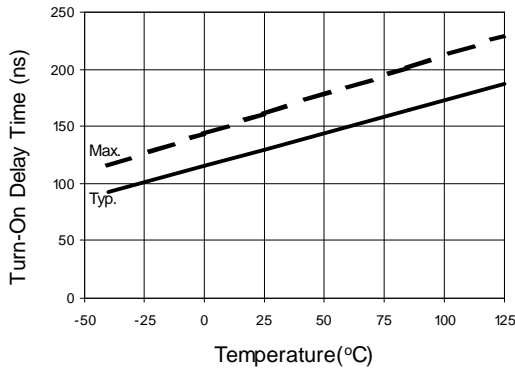


Figure 7A. Turn-On Time vs. Temperature

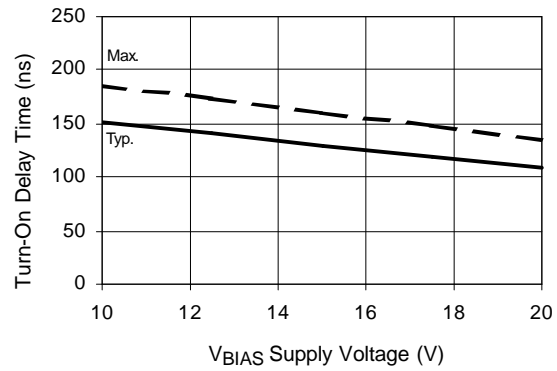


Figure 7B. Turn-On Time vs. Supply Voltage

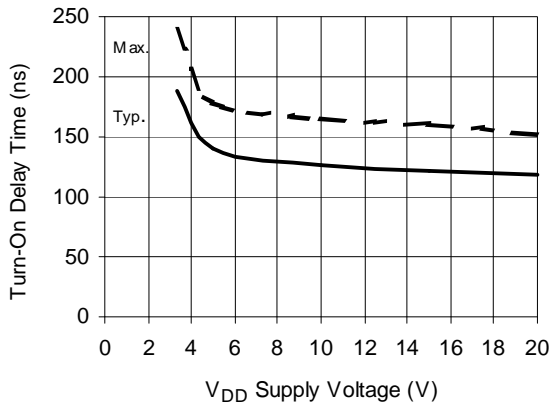


Figure 7C. Turn-On Time vs.  $V_{DD}$  Supply Voltage

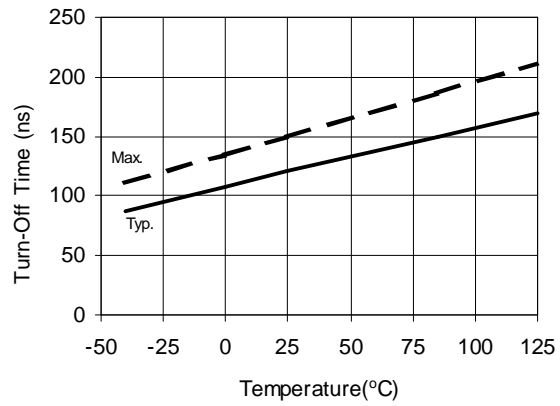


Figure 8A. Turn-Off Time vs. Temperature

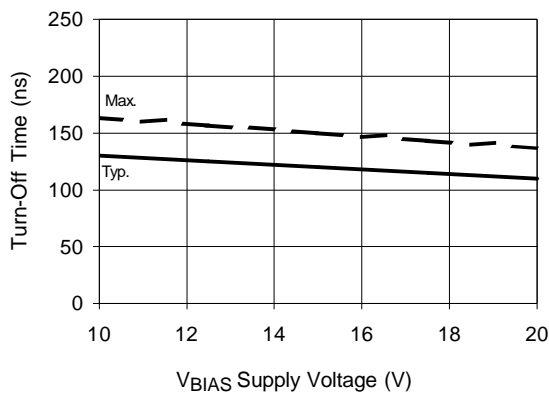


Figure 8B. Turn-Off Time vs. Supply Voltage

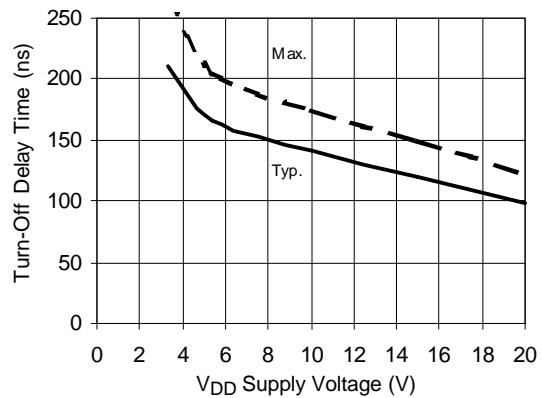


Figure 8C. Turn-Off Time vs.  $V_{DD}$  Supply Voltage

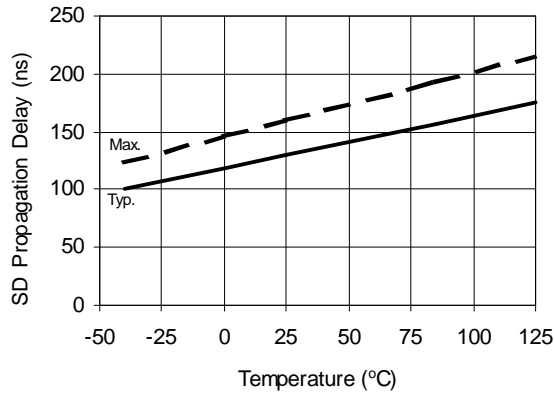


Figure 9A. Shutdown Time vs. Temperature

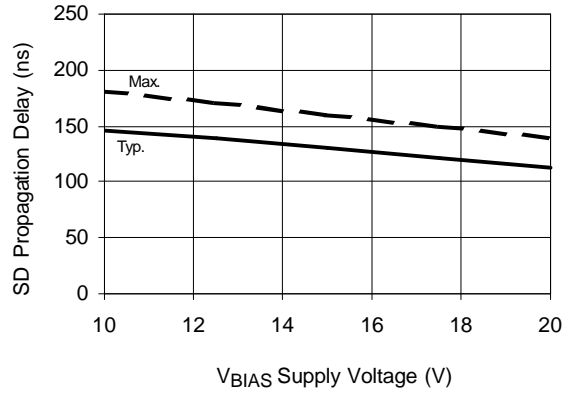


Figure 9B. Shutdown Time vs. Supply Voltage

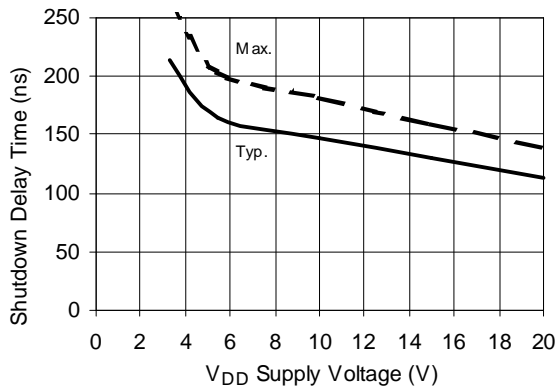


Figure 9C. Shutdown Time vs. VDD Supply Voltage

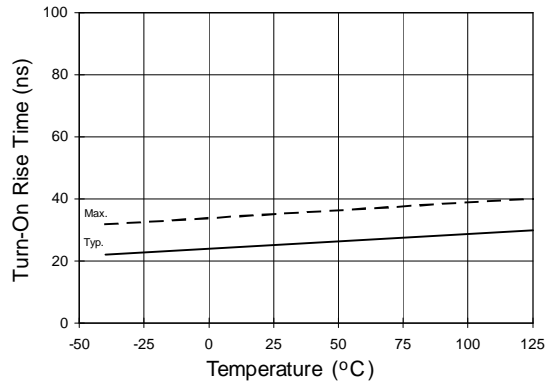


Figure 10A. Turn-On Rise Time vs. Temperature

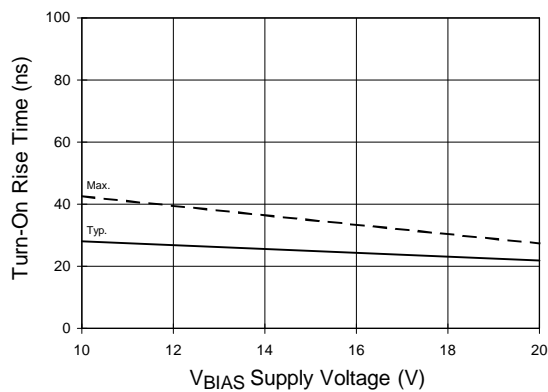


Figure 10B. Turn-On Rise Time vs. Voltage

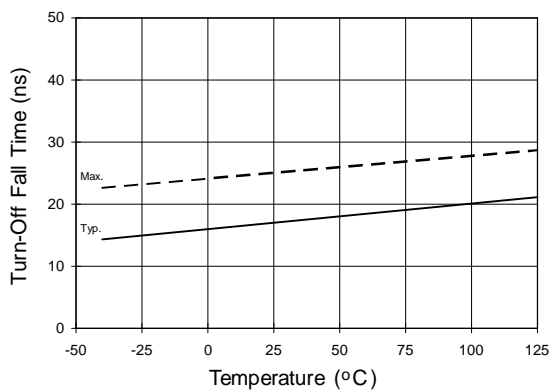


Figure 11A. Turn-Off Fall Time vs. Temperature



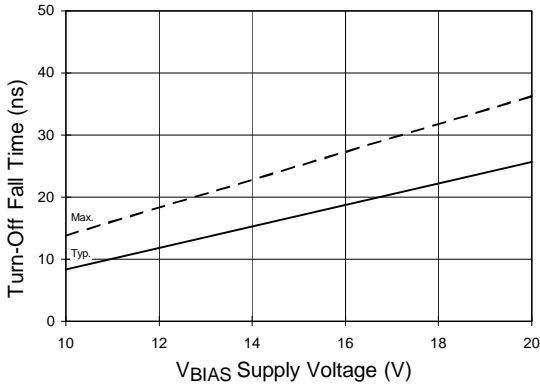


Figure 11B. Turn-Off Fall Time vs. Voltage

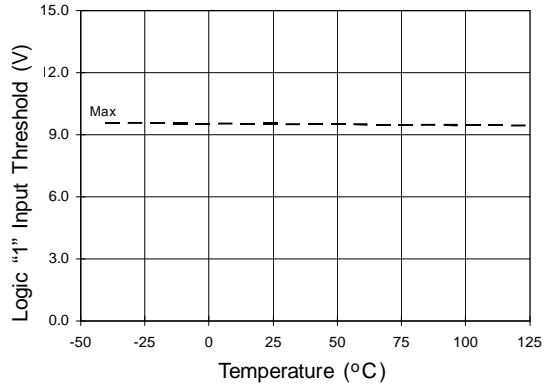


Figure 12A. Logic "1" Input Threshold vs. Temperature

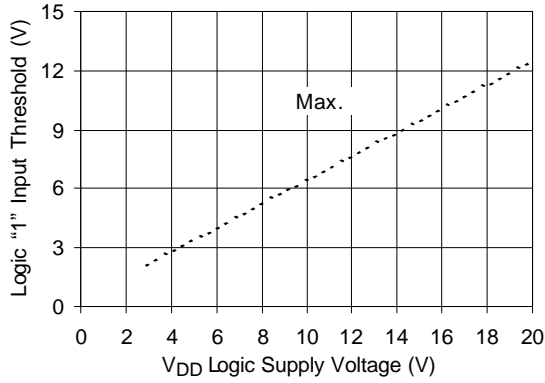


Figure 12B. Logic "1" Input Threshold vs. Voltage

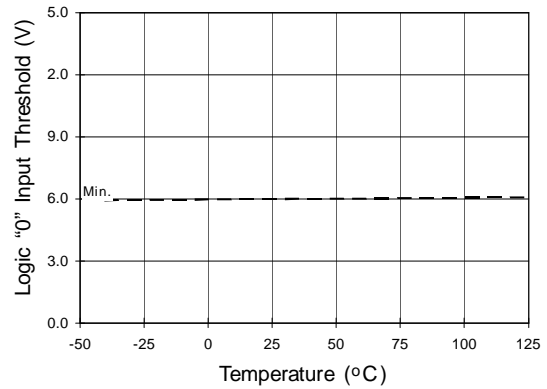


Figure 13A. Logic "0" Input Threshold vs. Temperature

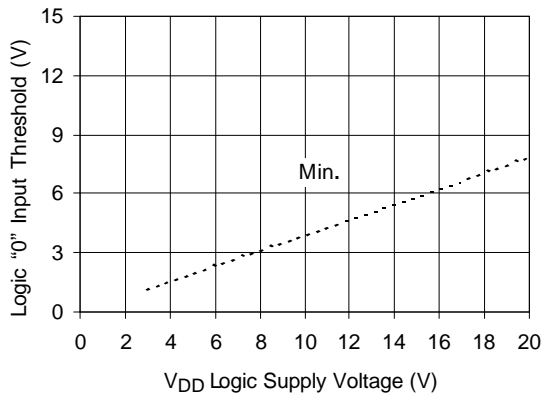


Figure 13B. Logic "0" Input Threshold vs. Voltage

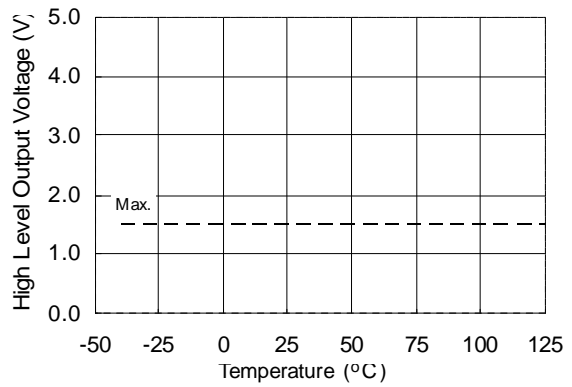


Figure 14A. High Level Output Voltage vs. Temperature ( $I_O = 0$  mA)

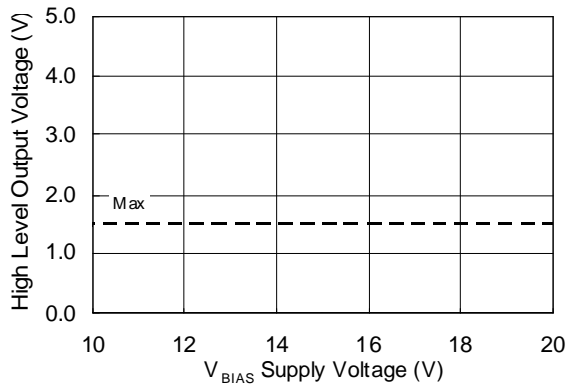


Figure 14B. High Level Output Voltage vs. Supply Voltage ( $I_o = 0 \text{ mA}$ )

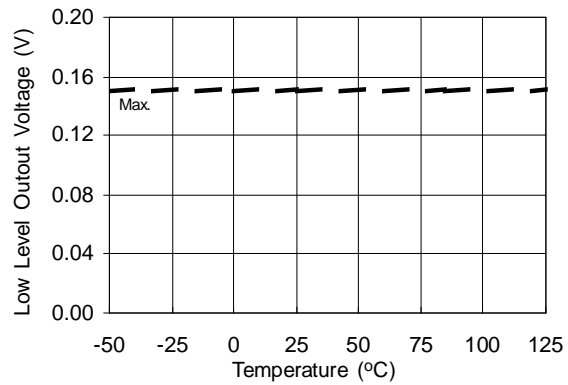


Figure 15A. Low Level Output vs. Temperature

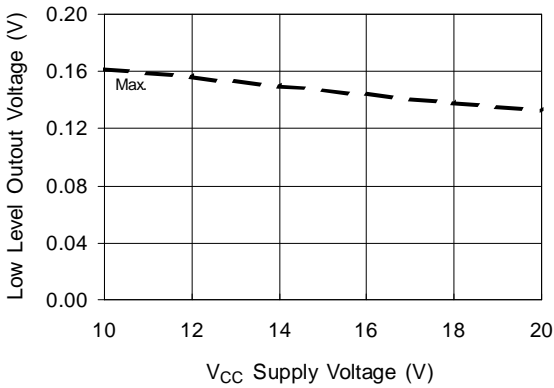


Figure 15B. Low Level Output vs. Supply Voltage

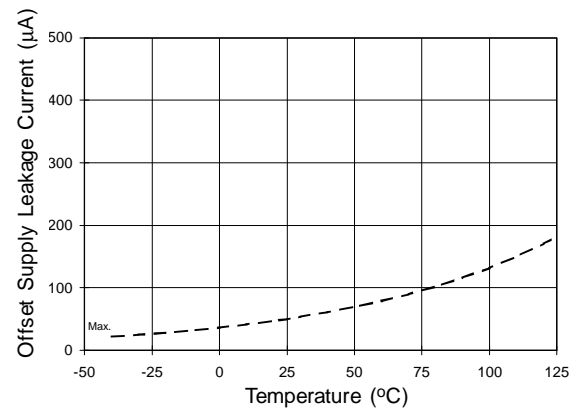


Figure 16A. Offset Supply Current vs. Temperature

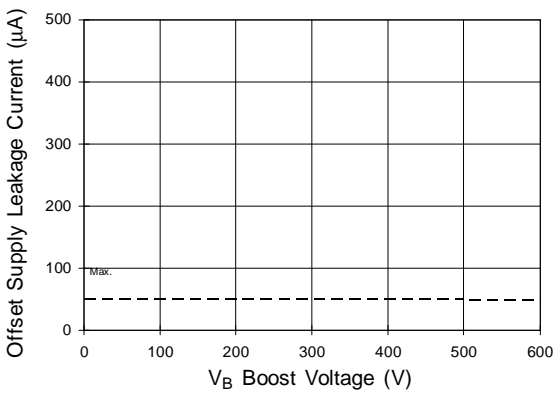


Figure 16B. Offset Supply Current vs. Voltage

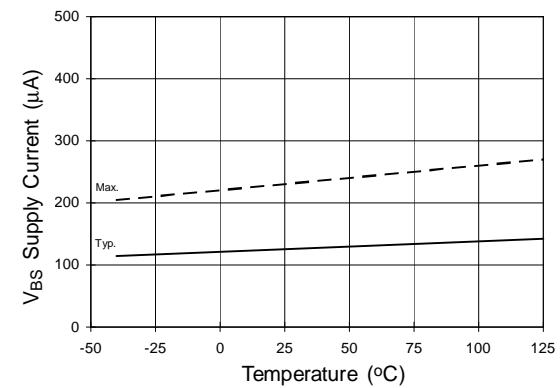


Figure 17A. V<sub>BS</sub> Supply Current vs. Temperature

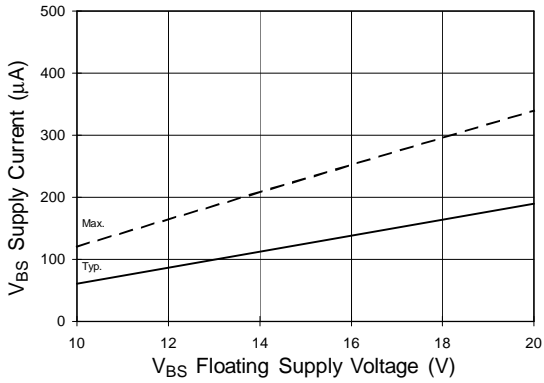


Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage

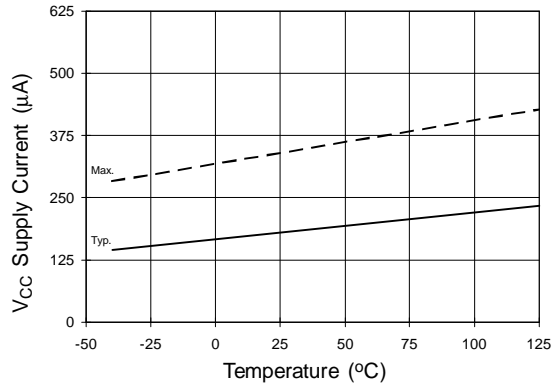


Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature

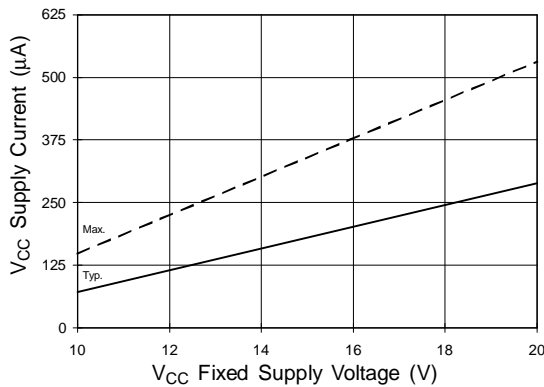


Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage

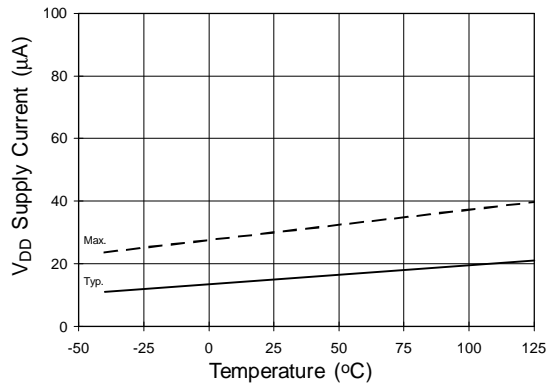


Figure 19A. V<sub>DD</sub> Supply Current vs. Temperature

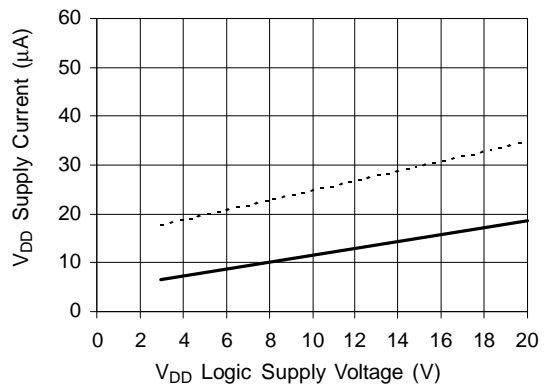


Figure 19B. V<sub>DD</sub> Supply Current vs. V<sub>DD</sub> Voltage

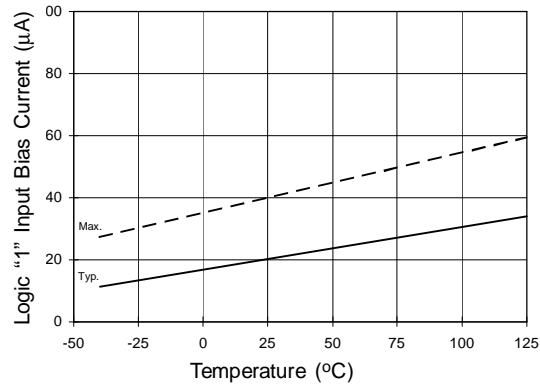


Figure 20A. Logic "1" Input Current vs. Temperature

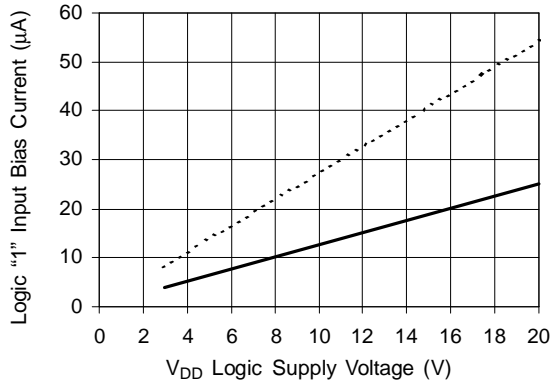


Figure 20B. Logic "1" Input Current vs. V<sub>DD</sub> Voltage

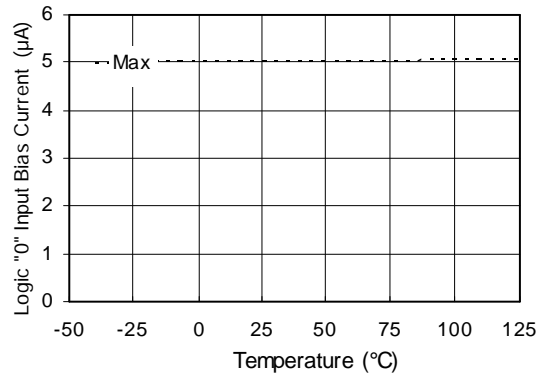


Figure 21A. Logic "0" Input Bias Current vs. Temperature

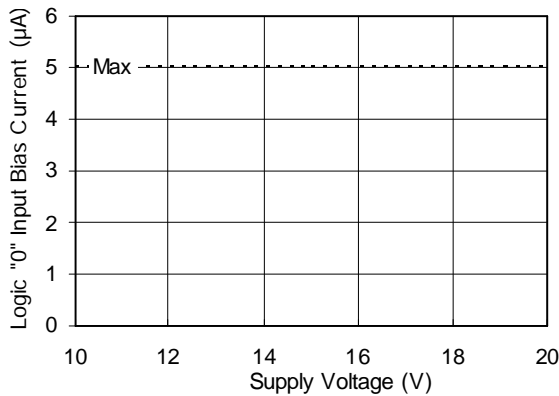


Figure 21B. Logic "0" Input Bias Current vs. Voltage

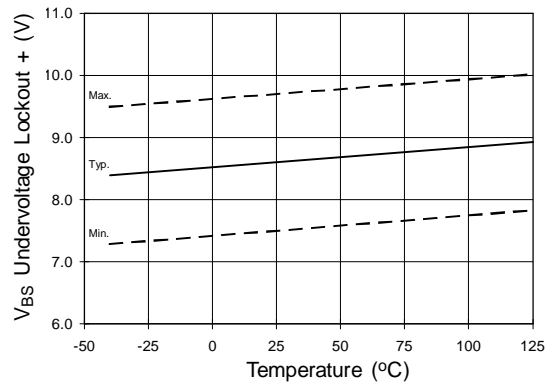


Figure 22. V<sub>BS</sub> Undervoltage (+) vs. Temperature

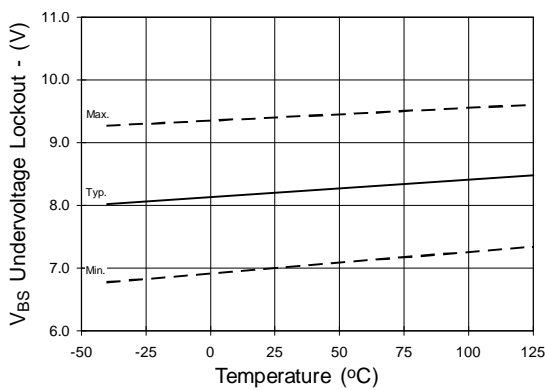


Figure 23. V<sub>BS</sub> Undervoltage (-) vs. Temperature

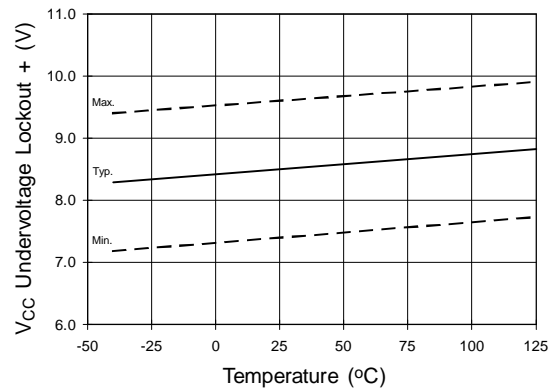


Figure 24. V<sub>CC</sub> Undervoltage (+) vs. Temperature

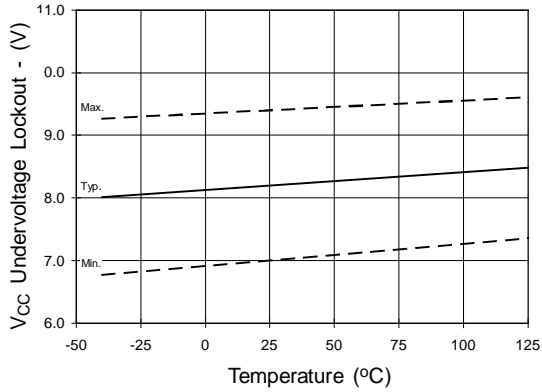


Figure 25.  $V_{CC}$  Undervoltage Lockout (-) vs. Temperature

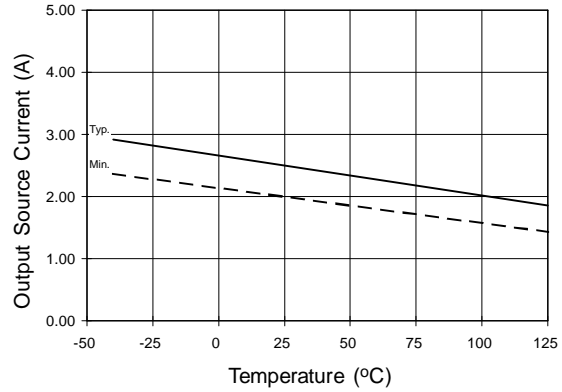


Figure 26A. Output Source Current vs. Temperature

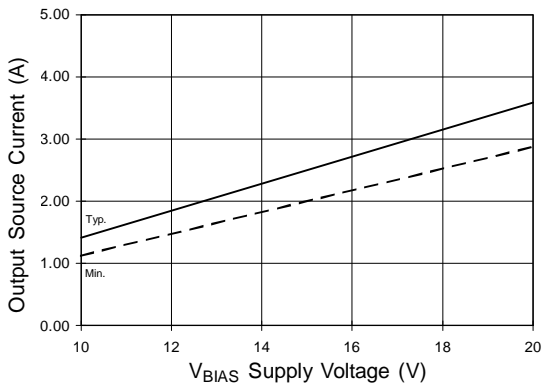


Figure 26B. Output Source Current vs. Voltage

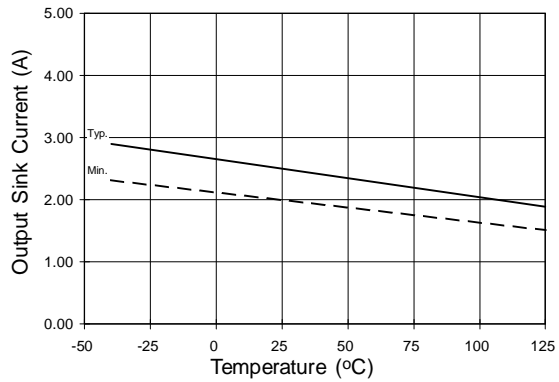


Figure 27A. Output Sink Current vs. Temperature

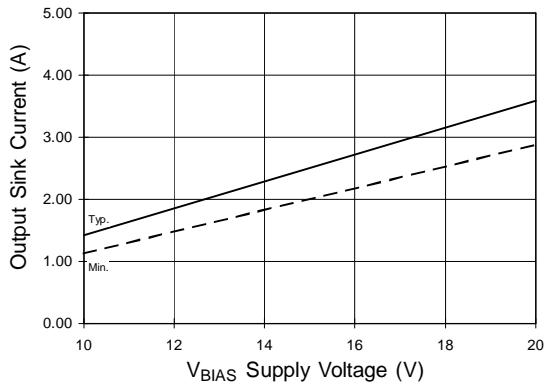


Figure 27B. Output Sink Current vs. Voltage

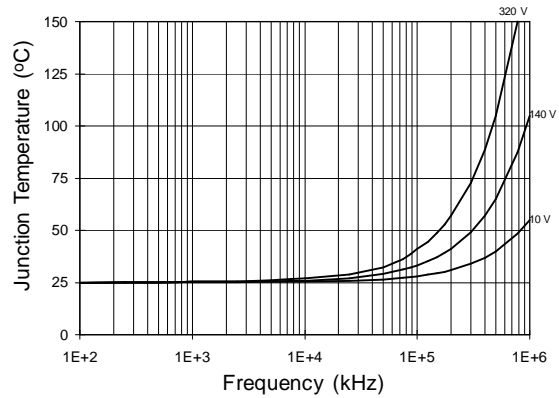


Figure 28. IRS2110/IRS2113  $T_J$  vs. Frequency (IRFBC20)  $R_{GATE} = 33 \text{ } \Omega$ ,  $V_{CC} = 15 \text{ V}$

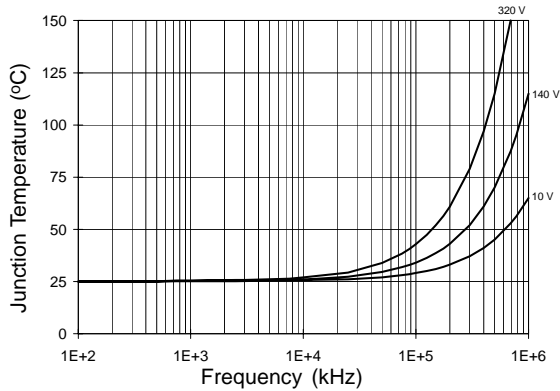


Figure 29. IRS2110/IRS2113 T<sub>J</sub> vs. Frequency (IRFBC30) R<sub>GATE</sub> = 22 Ω, V<sub>CC</sub> = 15 V

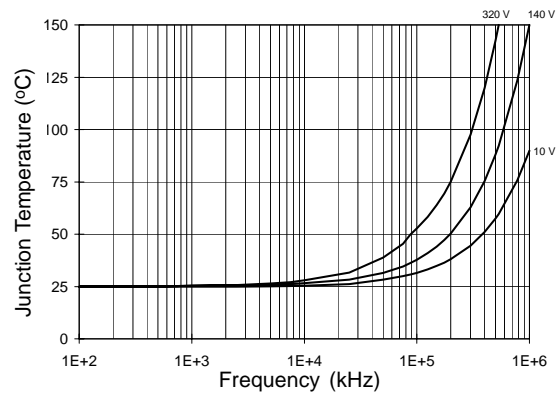


Figure 30. IRS2110/IRS2113 T<sub>J</sub> vs. Frequency (IRFBC40) R<sub>GATE</sub> = 15 Ω, V<sub>CC</sub> = 15 V

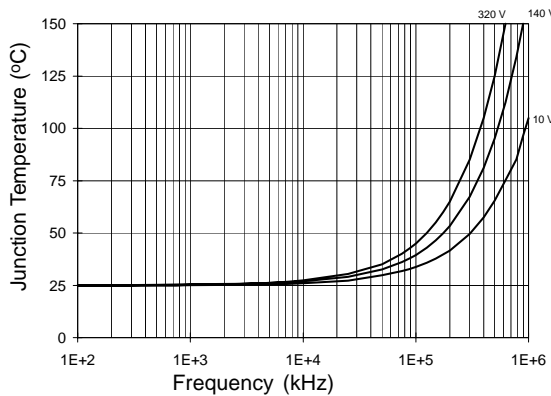


Figure 31. IRS2110/IRS2113 T<sub>J</sub> vs. Frequency (IRFPE50) R<sub>GATE</sub> = 10 Ω, V<sub>CC</sub> = 15 V

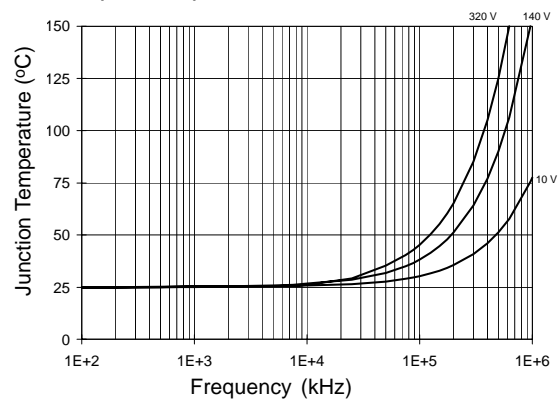


Figure 32. IRS2110S/IRS2113S T<sub>J</sub> vs. Frequency (IRFBC20) R<sub>GATE</sub> = 33 Ω, V<sub>CC</sub> = 15 V

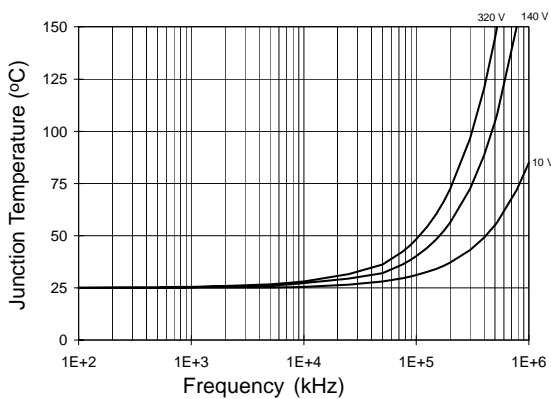


Figure 33. IRS2110S/IRS2113S T<sub>J</sub> vs. Frequency (IRFBC30) R<sub>GATE</sub> = 22 Ω, V<sub>CC</sub> = 15 V

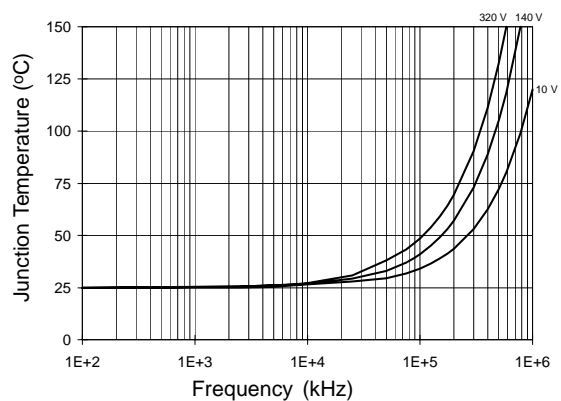


Figure 34. IRS2110S/IRS2113S T<sub>J</sub> vs. Frequency (IRFBC40) R<sub>GATE</sub> = 15 Ω, V<sub>CC</sub> = 15 V

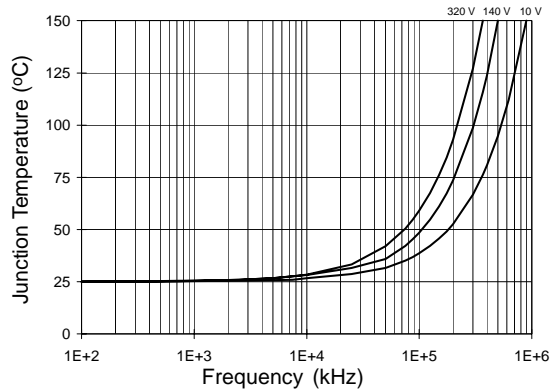


Figure 35. IRS2110S/IRS2113S T<sub>J</sub> vs. Frequency (IRFPE50) R<sub>GATE</sub> = 10 Ω, V<sub>CC</sub> = 15 V

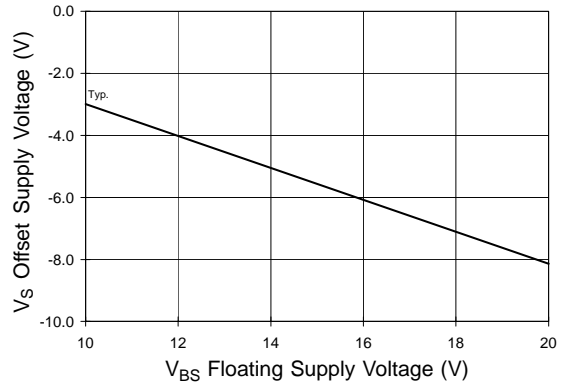


Figure 36. Maximum V<sub>S</sub> Negative Offset vs. V<sub>BS</sub> Supply Voltage

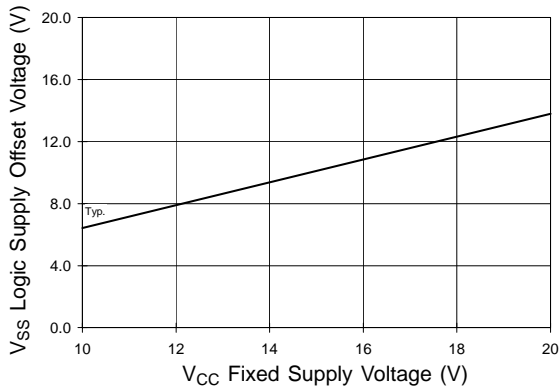
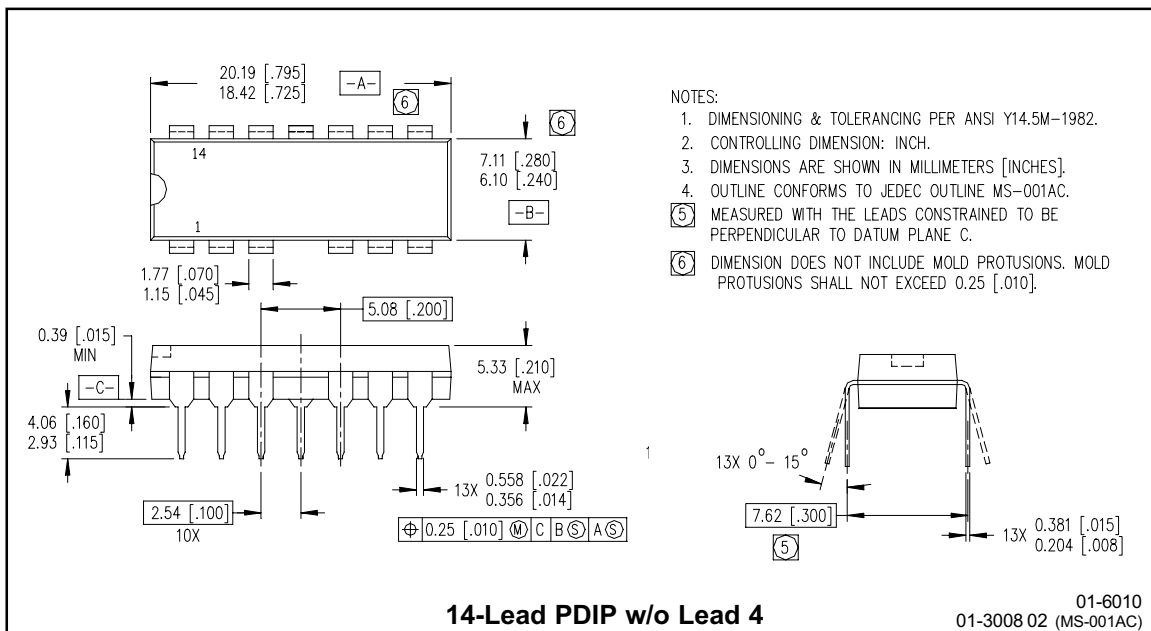
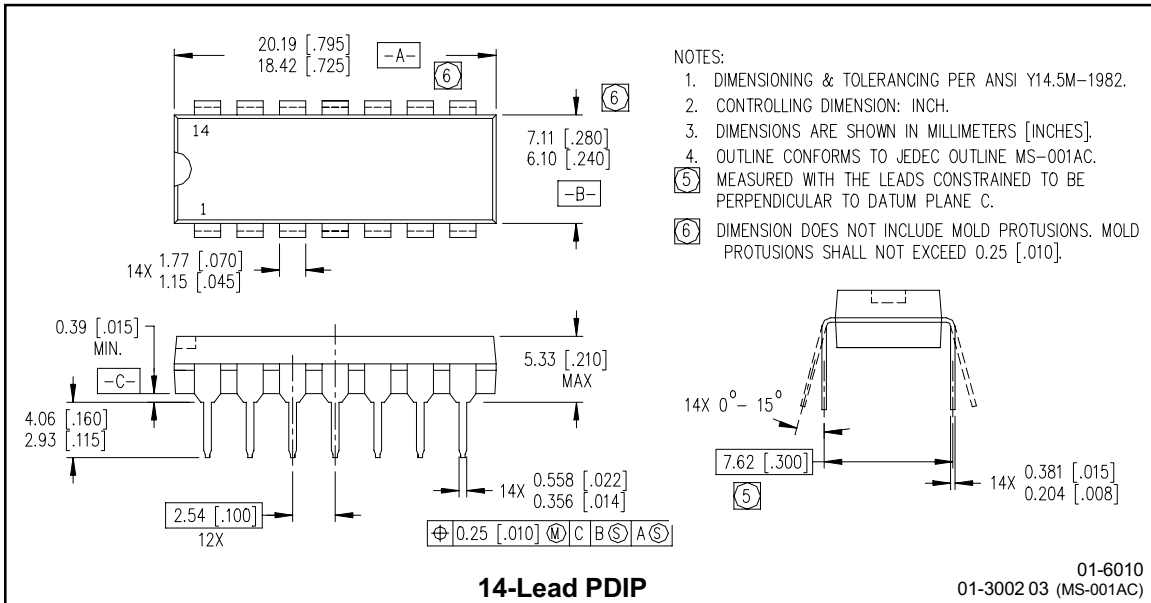
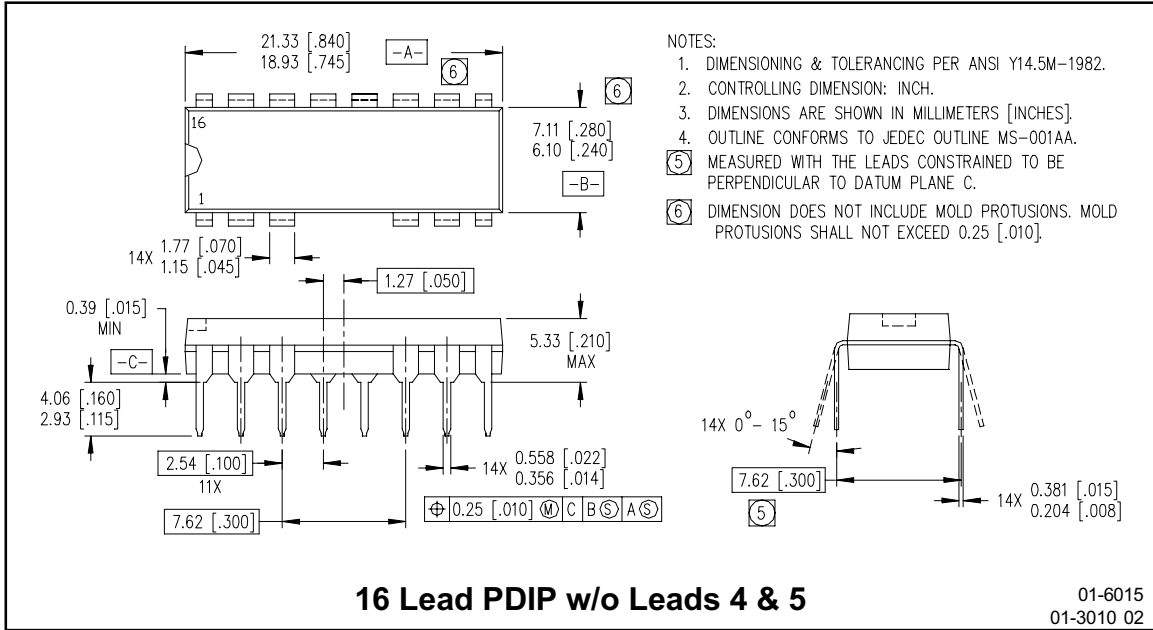


Figure 37. Maximum V<sub>SS</sub> Positive Offset vs. V<sub>CC</sub> Supply Voltage

Case Outlines

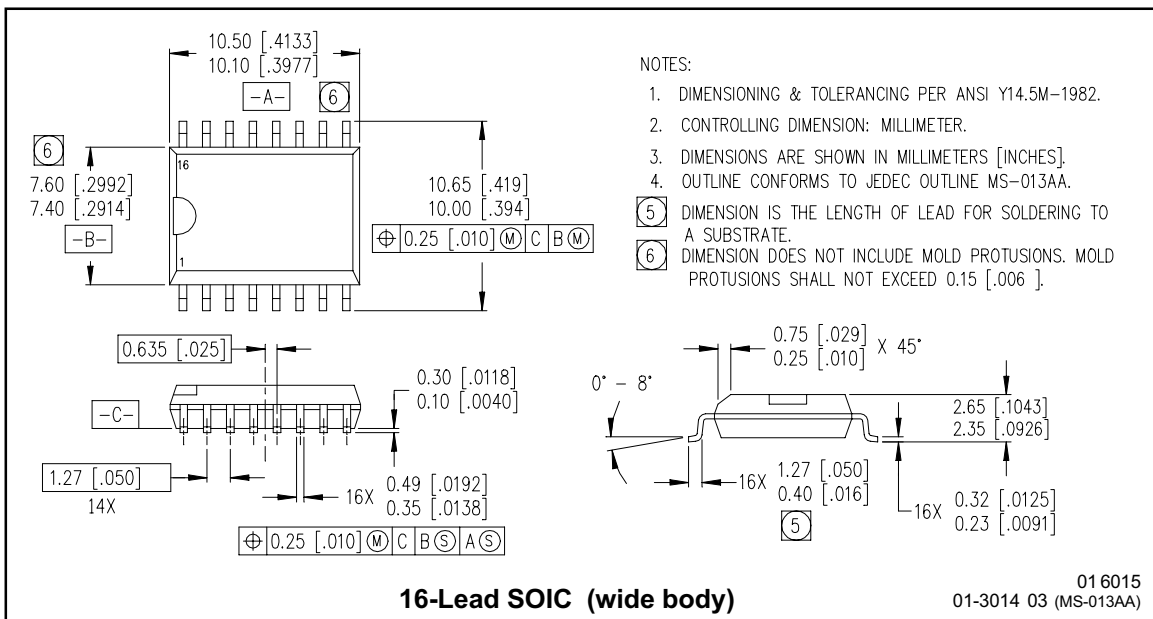






NOTES:

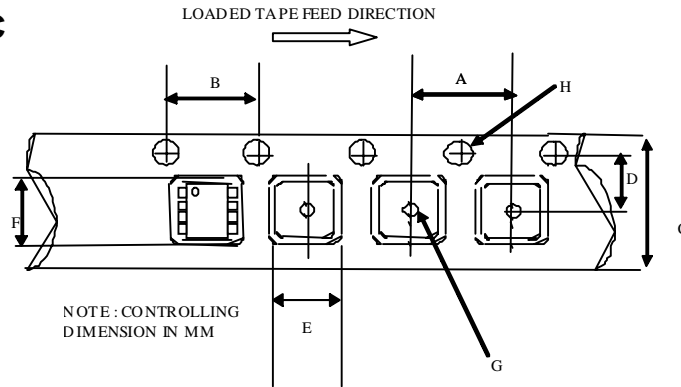
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



NOTES:

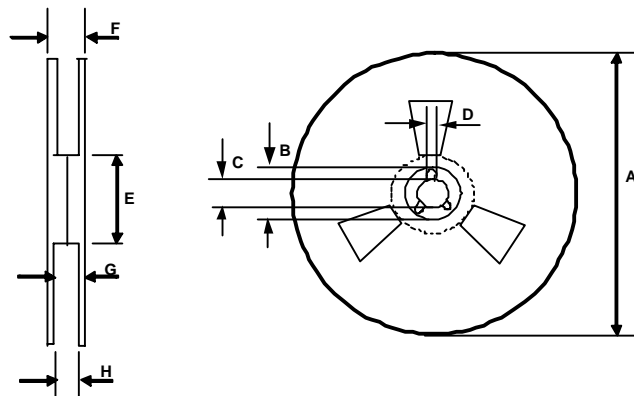
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

Tape & Reel  
16-Lead SOIC



CARRIER TAPE DIMENSION FOR 16SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	10.80	11.00	0.425	0.433
F	10.60	10.80	0.417	0.425
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

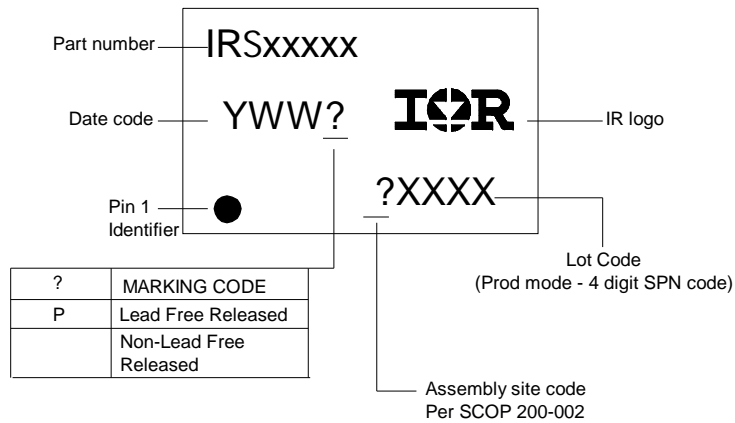


REEL DIMENSIONS FOR 16SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

# IRS2110(-1,-2,S)PbF/IRS2113(-1,-2,S)PbF

## LEADFREE PART MARKING INFORMATION



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- 14-Lead PDIP IRS2110PbF
- 14-Lead PDIP IRS2110-1PbF
- 14-Lead PDIP IRS2113PbF
- 14-Lead PDIP IRS2113-1PbF
- 16-Lead PDIP IRS2110-2PbF
- 16-Lead PDIP IRS2113-2PbF
- 16-Lead SOIC IRS2110SPbF
- 16-Lead SOIC IRS2113SPbF
- 16-Lead SOIC Tape & Reel IRS2110STRPbF
- 16-Lead SOIC Tape & Reel IRS2113STRPbF

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