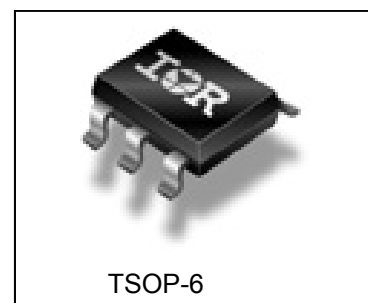
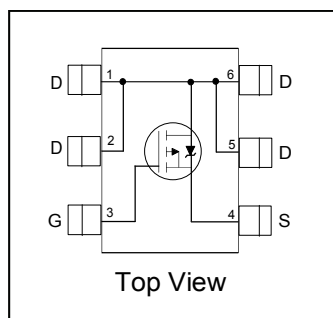


HEXFET® Power MOSFET

V_{DS}	-20	V
V_{GS}	± 12	V
$R_{DS(on)}$ max (@ $V_{GS} = -4.5V$)	32	mΩ
$R_{DS(on)}$ max (@ $V_{GS} = -2.5V$)	55	mΩ
Q_g (typical)	12	nC
I_D (@ $T_A = 25^\circ C$)	-6.9	A



Applications

- Battery operated DC motor inverter MOSFET
- System/Load Switch

Features

Industry-Standard TSOP-6 Package
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Consumer Qualification

results in

⇒

Benefits

Multi-Vendor Compatibility
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLTS2242TRPbF	TSOP-6	Tape and Reel	3000	IRLTS2242TRPbF

Absolute Maximum Ratings

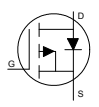
	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	- 20	V
V_{GS}	Gate-to-Source Voltage	± 12	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V	-6.9	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V	-5.5	
I_{DM}	Pulsed Drain Current ①	-55	
P_D @ $T_A = 25^\circ C$	Power Dissipation	2.0	W
P_D @ $T_A = 70^\circ C$	Power Dissipation	1.3	
	Linear Derating Factor	0.02	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ③ are on page 2

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	9.4	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	26	32	m Ω	$V_{GS} = -4.5V, I_D = -6.9A$ ②
		—	45	55		$V_{GS} = -2.5V, I_D = -5.5A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.4	—	-1.1	V	$V_{DS} = V_{GS}, I_D = -10\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-3.8	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-150		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
g_{fs}	Forward Transconductance	8.5	—	—	S	$V_{DS} = -10V, I_D = -5.5A$
Q_g	Total Gate Charge	—	12	—	nC	$V_{DS} = -10V$
Q_{gs}	Pre-V _{th} Gate-to-Source Charge	—	1.5	—		$V_{GS} = -4.5V$
Q_{gd}	Gate-to-Drain Charge	—	4.3	—		$I_D = -5.5A$
R_G	Gate Resistance	—	17	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	5.8	—	ns	$V_{DD} = -10V, V_{GS} = -4.5V$ $I_D = -5.5A$ $R_G = 6.8\Omega$
t_r	Rise Time	—	18	—		
$t_{d(off)}$	Turn-Off Delay Time	—	81	—		
t_f	Fall Time	—	68	—		
C_{iss}	Input Capacitance	—	905	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	280	—		$V_{DS} = -10V$
C_{rss}	Reverse Transfer Capacitance	—	200	—		$f = 1.0KHz$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-55		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -5.5A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	41	62	ns	$T_J = 25^\circ\text{C}, I_F = -5.5A, V_{DD} = -16V$ $di/dt = 100A/\mu s$ ②
Q_{rr}	Reverse Recovery Charge	—	16	24	nC	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	62.5	$^\circ\text{C}/W$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ③ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>

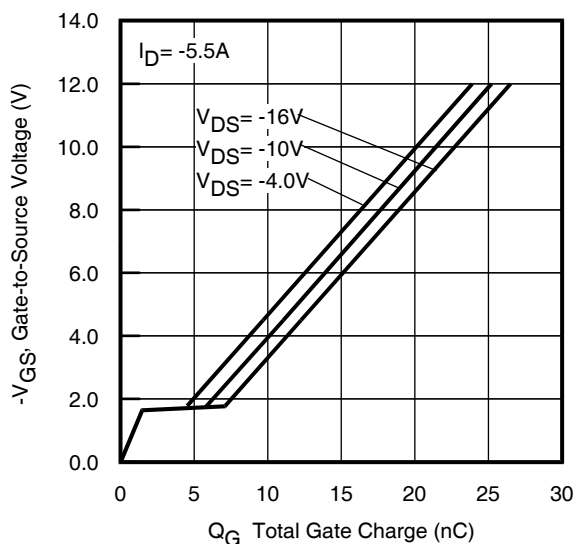
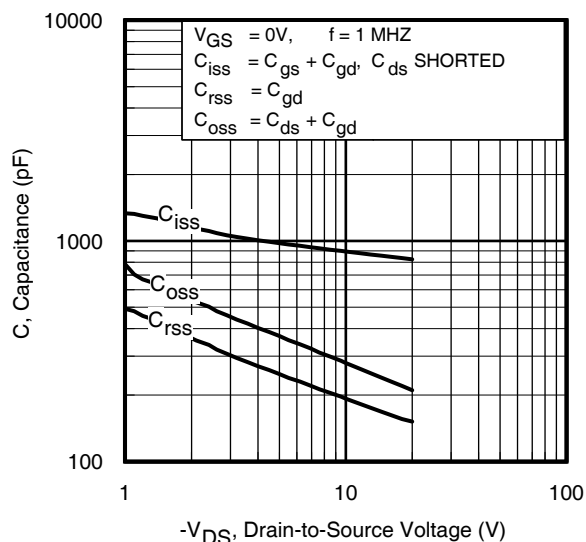
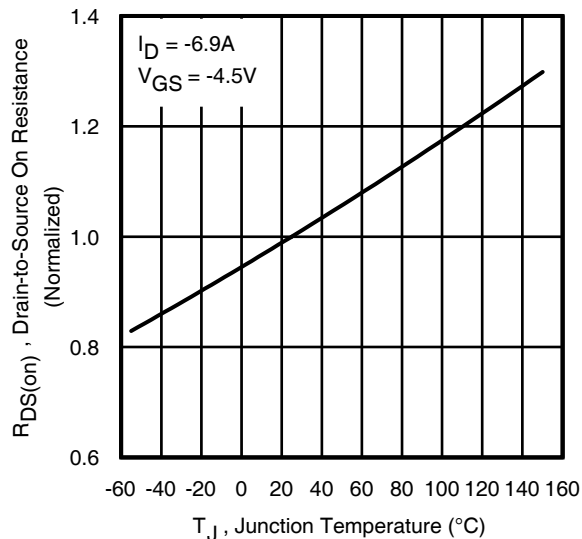
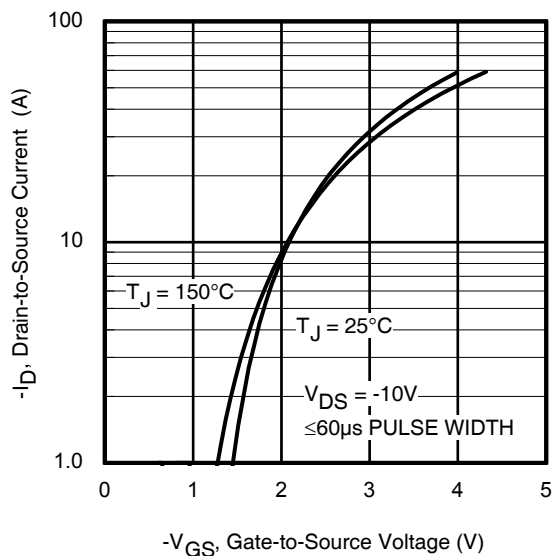
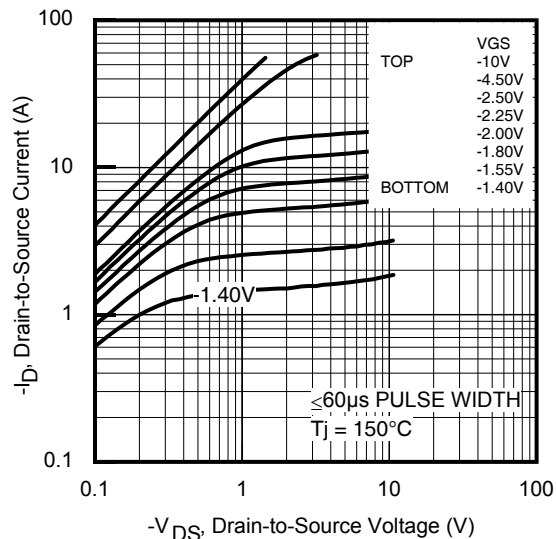
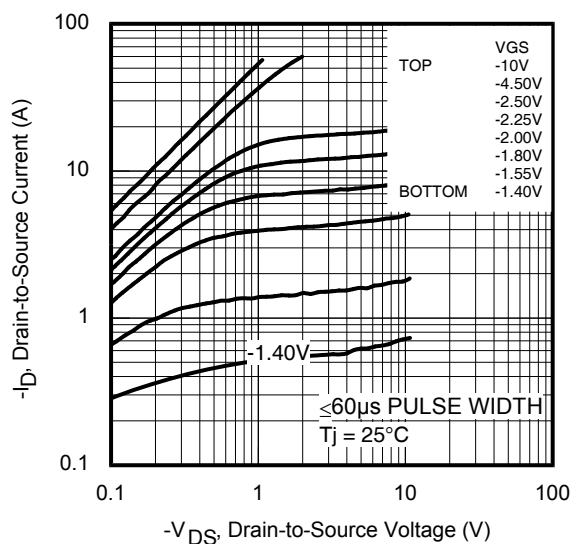
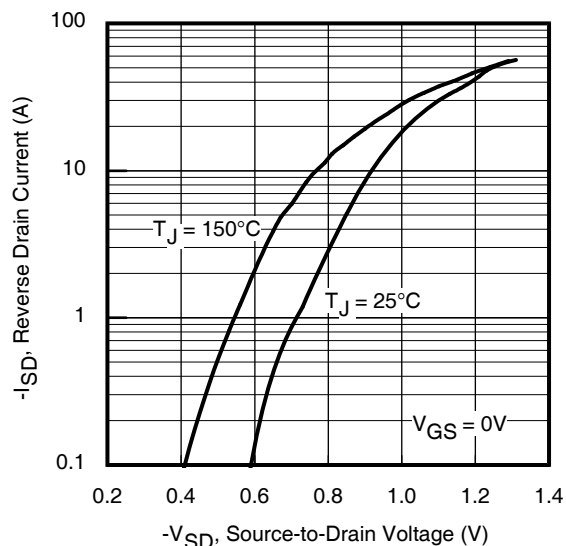
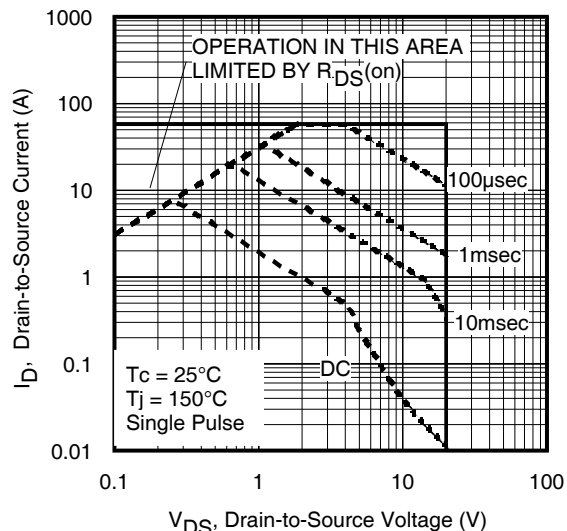
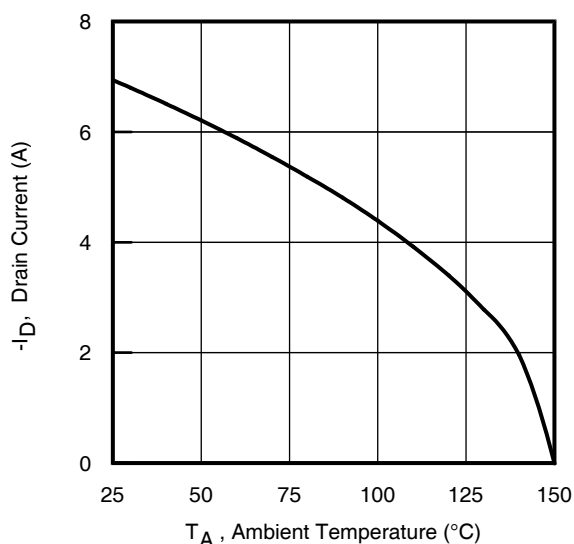
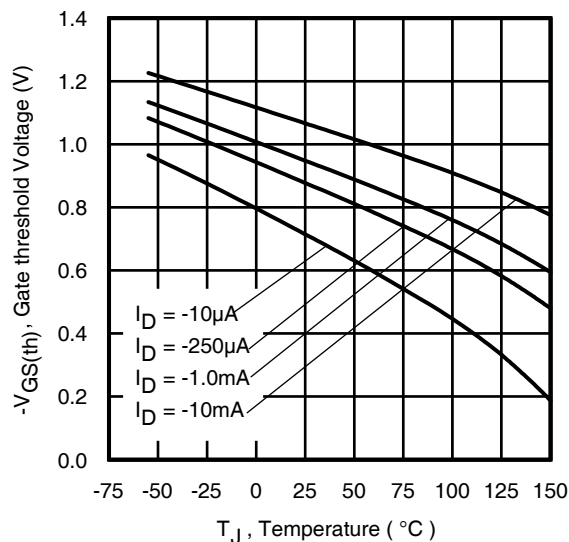
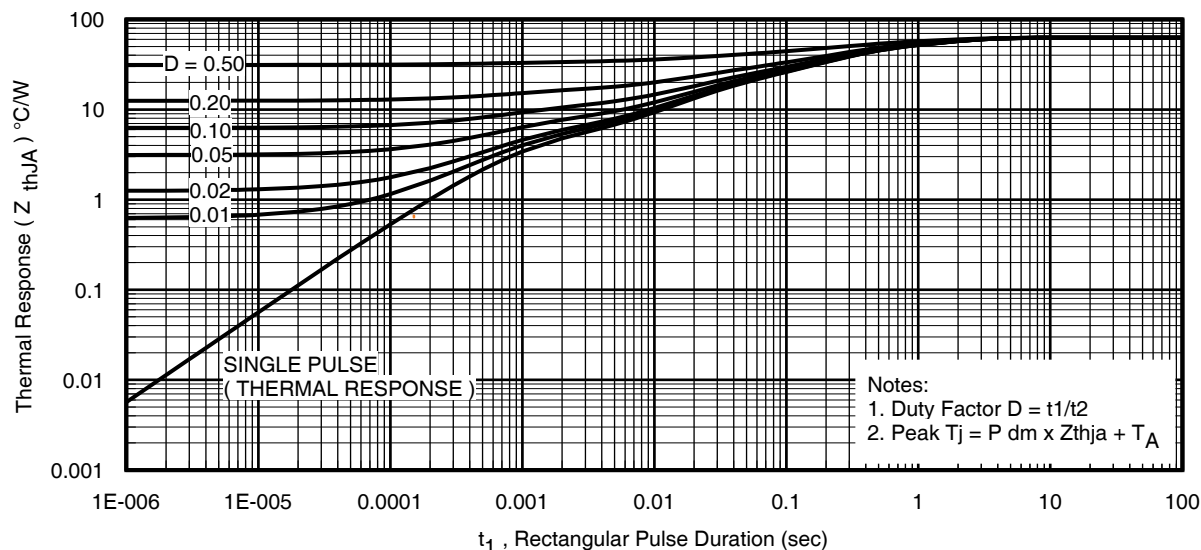
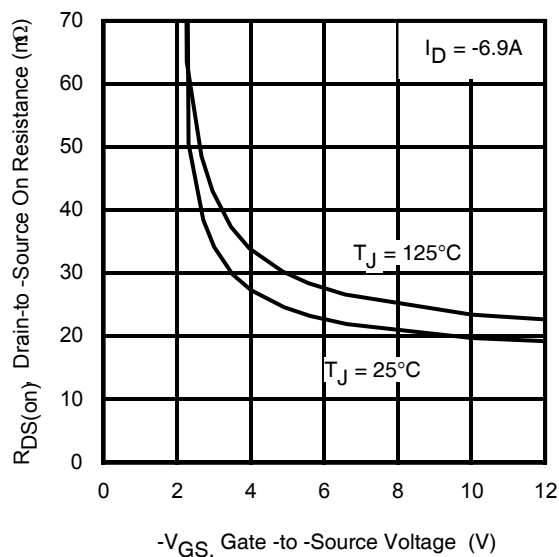
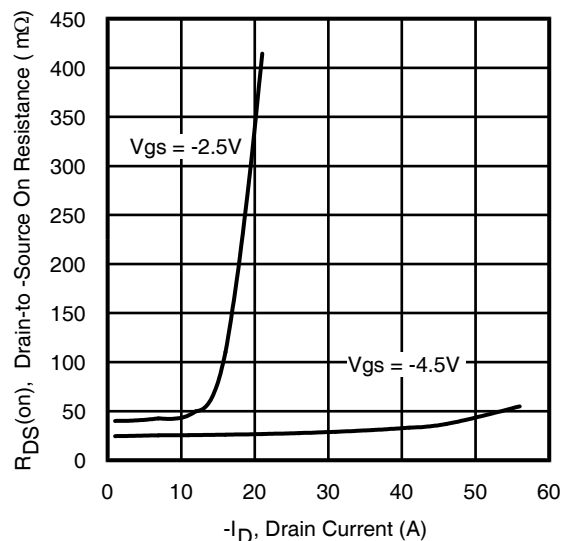
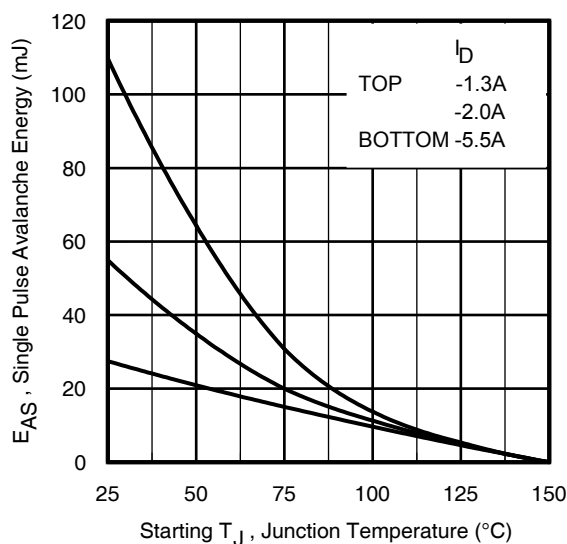
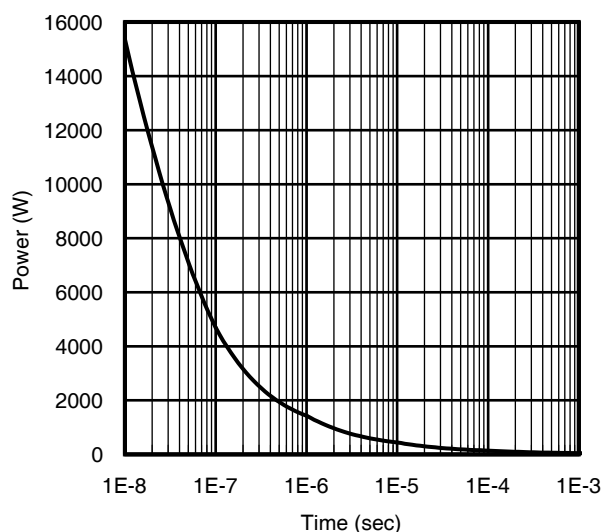
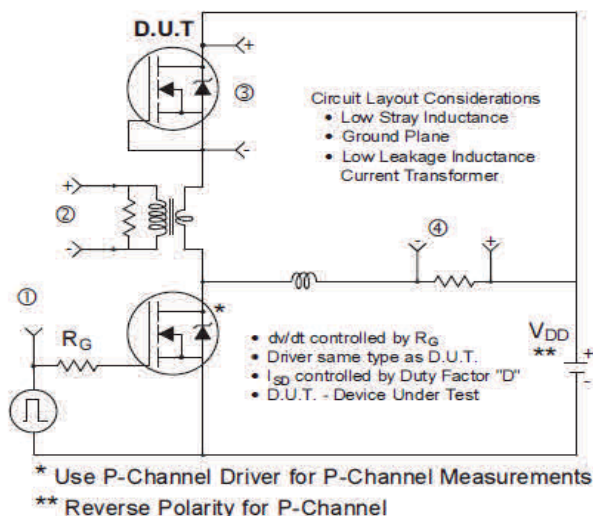
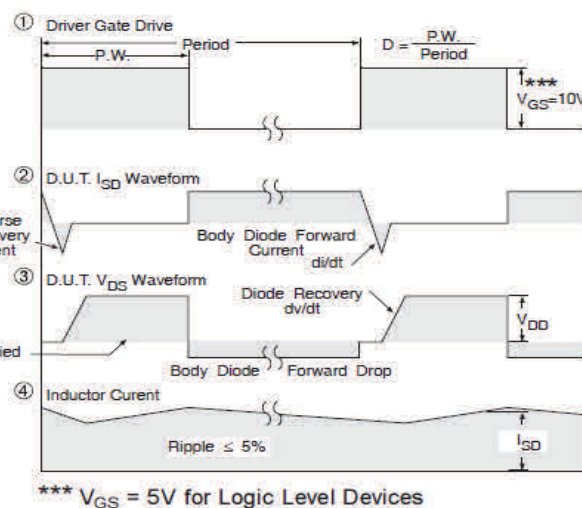
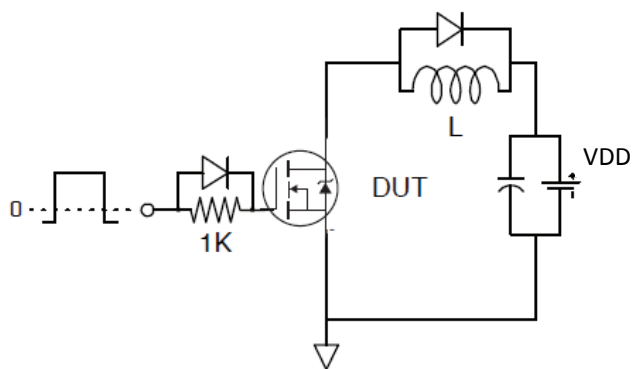
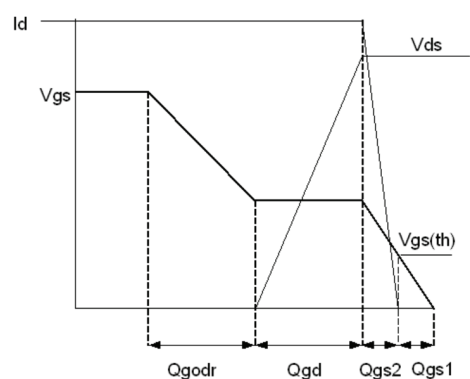
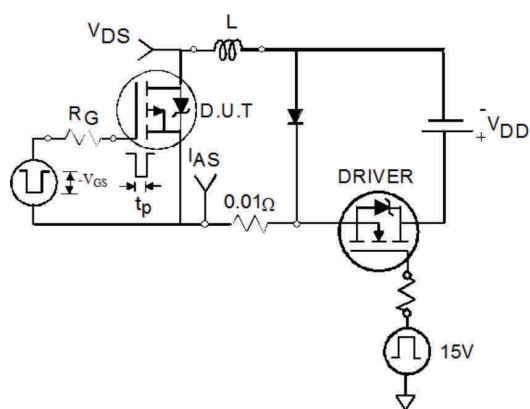
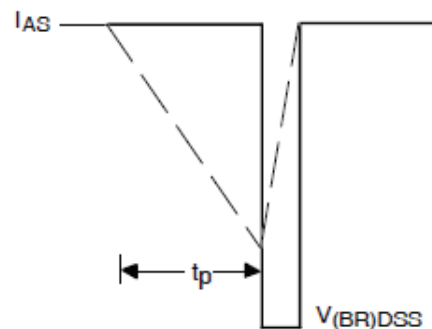
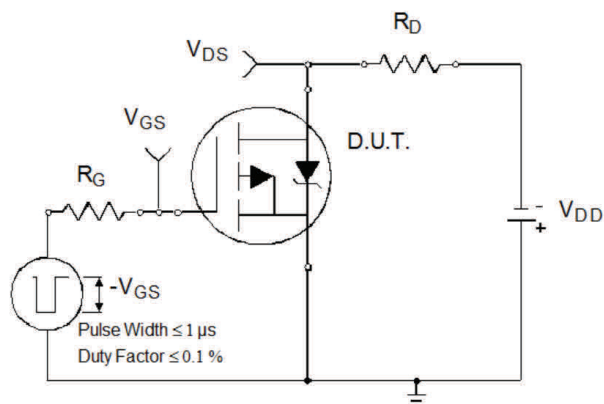
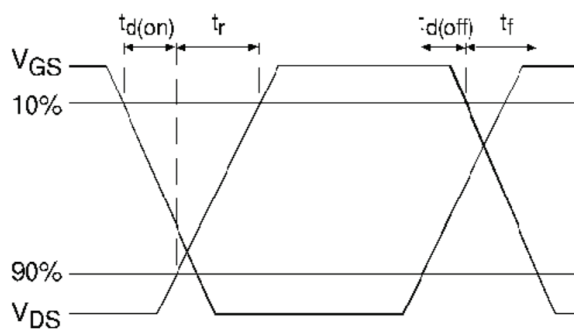


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

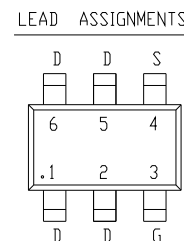
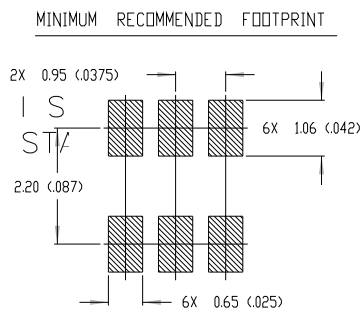
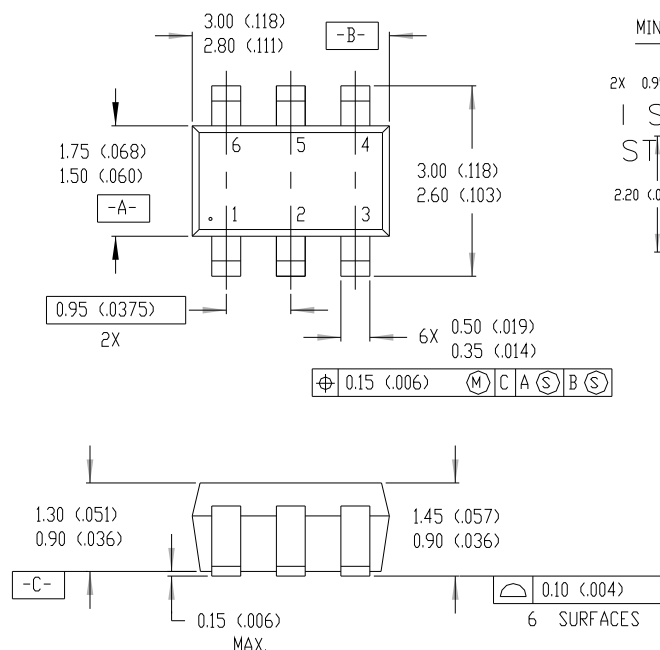
Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Typical On-Resistance vs. Drain Current

Fig 14. Maximum Avalanche Energy vs. Drain Current

Fig 15. Typical Power vs. Time

Fig 16. Diode Reverse Recovery Test Circuit for P-Channel HEXFET® Power MOSFETs


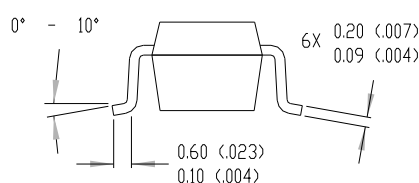

Fig 17a. Gate Charge Test Circuit

Fig 17b. Gate Charge Waveform

Fig 18a. Unclamped Inductive Test Circuit

Fig 18b. Unclamped Inductive Waveforms

Fig 19a. Switching Time Test Circuit

Fig 19b. Switching Time Waveforms

TSOP-6 Package Outline

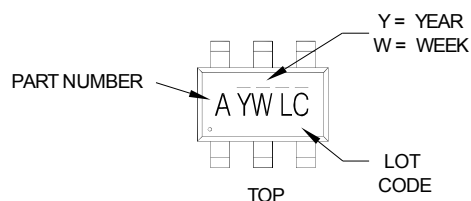


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).



TSOP-6 Part Marking Information



PART NUMBER CODE REFERENCE:

A = SI3443DV	O = IRLTS6342TRPBF
B = IRF5800	P = IRF5800
C = IRF5850	R = IRF5850
D = IRF5851	S = Not applicable
E = IRF5852	T = IRLTS2242TRPBF
F = IRF5801	
G = IRF5803	
H = IRF5804	
I = IRF5805	
J = IRF5806	
K = IRF5810	
N = IRF5802	

Note: A line above the work week
(as shown here) indicates Lead-Free.

DATE CODE MARKING INSTRUCTIONS

WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

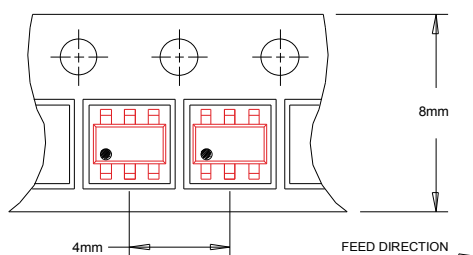
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2012	2002	2	02	B
2013	2003	3	03	C
2014	2004	4	04	D
2015	2005	5		
2016	2006	6		
2017	2007	7		
2018	2008	8		
2019	2009	9		
2020	2010	0	24	X
			25	Y
			26	Z

WW = (27-52) IF PRECEDED BY A LETTER

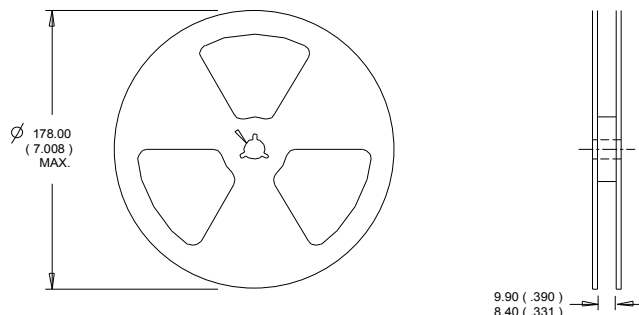
YEAR		Y	WORK WEEK	W
2011	2001	A	27	A
2012	2002	B	28	B
2013	2003	C	29	C
2014	2004	D	30	D
2015	2005	E		
2016	2006	F		
2017	2007	G		
2018	2008	H		
2019	2009	J		
2020	2010	K	50	X
			51	Y
			52	Z

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TSOP-6 Tape and Reel Information



NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Consumer ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	TSOP-6	MSL1 (per IPC/JEDEC J-STD-020D ^{††})
RoHS Compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

^{††} Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
11/18/2014	- Updated data sheet with IR corporate template. - Updated figure 12 on page 5 for V_{GS} from "20V" to "12V" due to error.

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

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