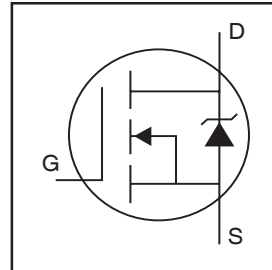


- Logic-Level Gate Drive
- Surface Mount (IRLR024N)
- Straight Lead (IRLU024N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



$$V_{DS} = 55V$$

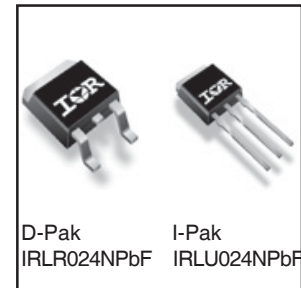
$$R_{DS(on)} = 0.065\Omega$$

$$I_D = 17A$$

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



D-Pak IRLR024NPbF I-Pak IRLU024NPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	17	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	
I_{DM}	Pulsed Drain Current ①	72	
$P_D @ T_C = 25^\circ C$	Power Dissipation	45	W
	Linear Derating Factor	0.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy ②	68	mJ
I_{AR}	Avalanche Current ③	11	A
E_{AR}	Repetitive Avalanche Energy ④	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.3	°C/W
$R_{\theta JA}$	Case-to-Ambient (PCB mount)**	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

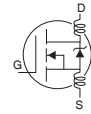
** When mounted on 1" square PCB (FR-4 or G-10 Material) .

For recommended footprint and soldering techniques refer to application note #AN-994

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.061	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.065	Ω	$V_{GS} = 10V, I_D = 10A$ ④
		—	—	0.080		$V_{GS} = 5.0V, I_D = 10A$ ④
		—	—	0.110		$V_{GS} = 4.0V, I_D = 9.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	8.3	—	—	S	$V_{DS} = 25V, I_D = 11A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	15	nC	$I_D = 11A$
Q_{gs}	Gate-to-Source Charge	—	—	3.7		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.5		$V_{GS} = 5.0V$, See Fig. 6 and 13 ④ ⑥
$t_{d(on)}$	Turn-On Delay Time	—	7.1	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	74	—		$I_D = 11A$
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		$R_G = 12\Omega, V_{GS} = 5.0V$
t_f	Fall Time	—	29	—		$R_D = 2.4\Omega$, See Fig. 10 ④ ⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	480	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	130	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	61	—		$f = 1.0MHz$, See Fig. 5 ⑥



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	72		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 11A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	60	90	ns	$T_J = 25^\circ\text{C}, I_F = 11A$
Q_{rr}	Reverse Recovery Charge	—	130	200	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 790\mu H$
 $R_G = 25\Omega$, $I_{AS} = 11A$. (See Figure 12)
- ③ $I_{SD} \leq 11A$, $di/dt \leq 290A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

- ⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

- ⑥ Uses IRLZ24N data and test conditions.

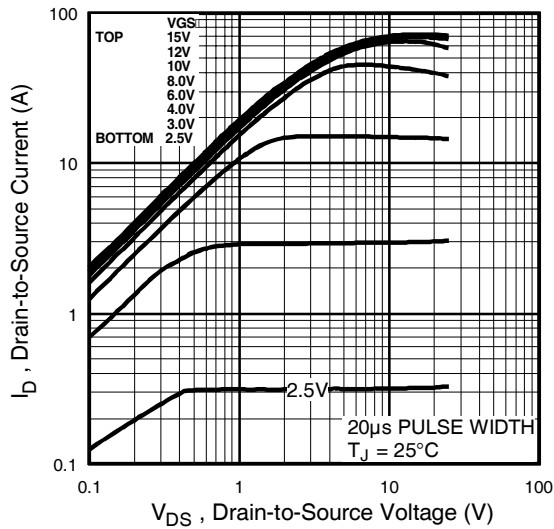


Fig 1. Typical Output Characteristics

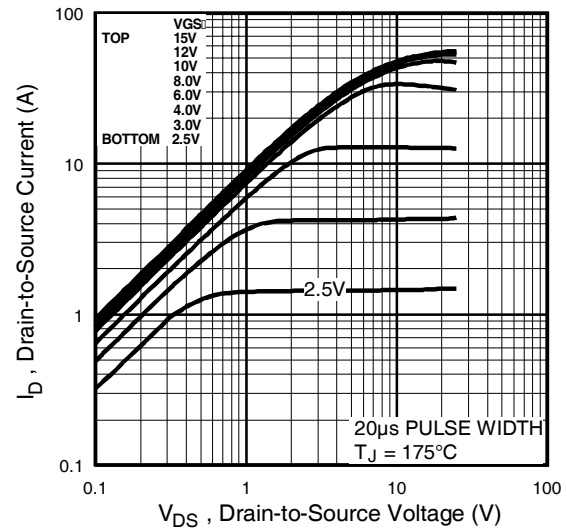


Fig 2. Typical Output Characteristics

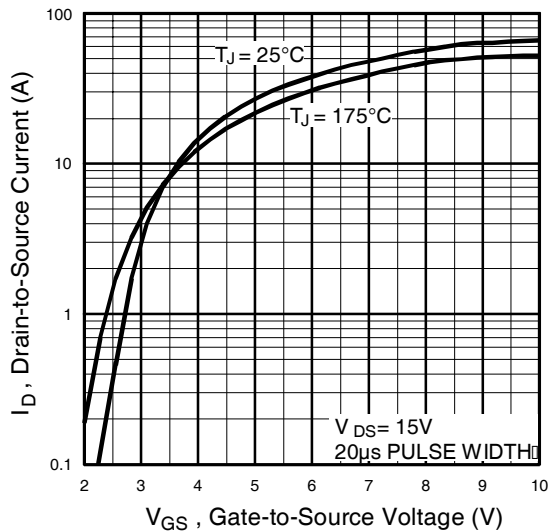


Fig 3. Typical Transfer Characteristics

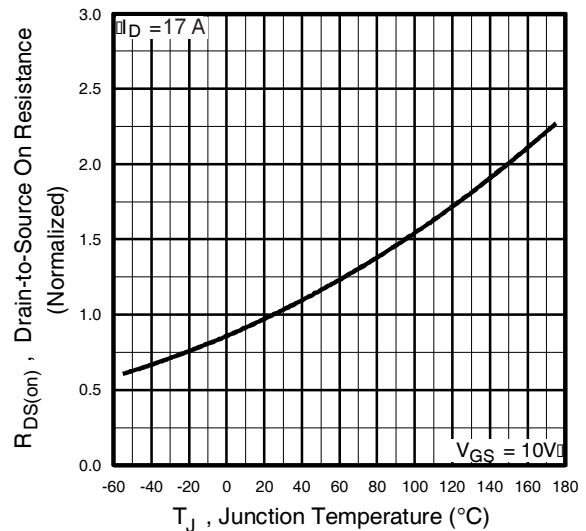


Fig 4. Normalized On-Resistance Vs. Temperature

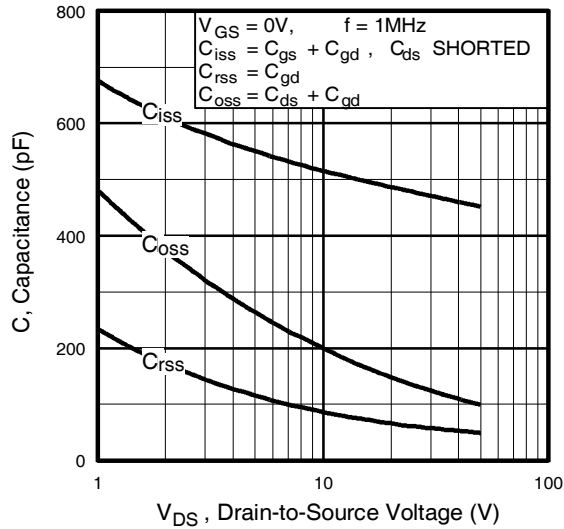


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

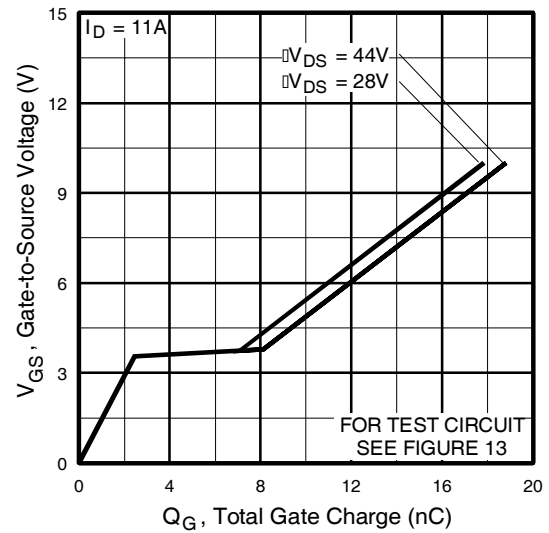


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

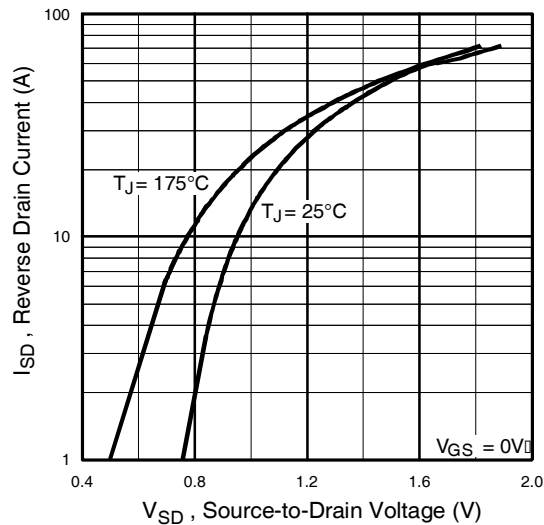


Fig 7. Typical Source-Drain Diode Forward Voltage

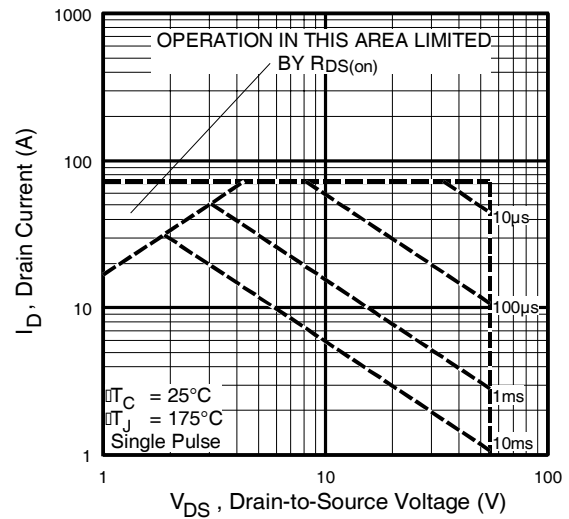


Fig 8. Maximum Safe Operating Area

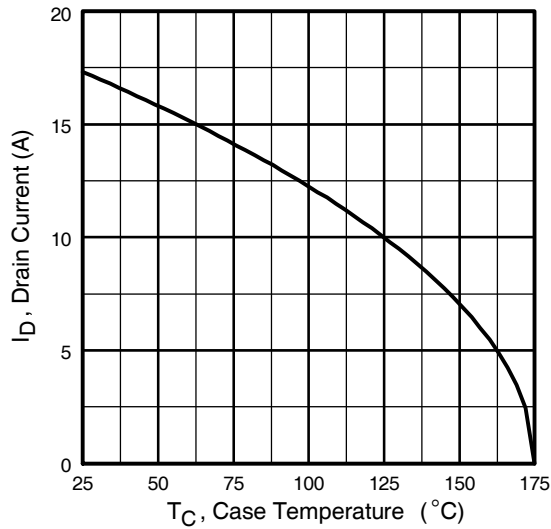


Fig 9. Maximum Drain Current Vs. Case Temperature

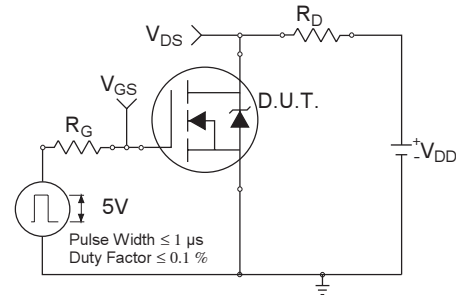


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

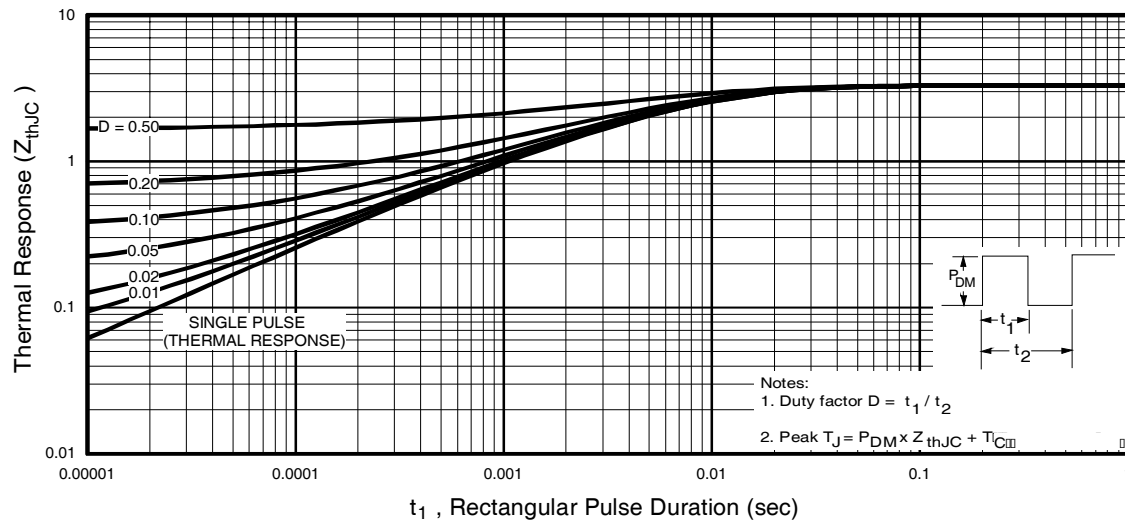


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

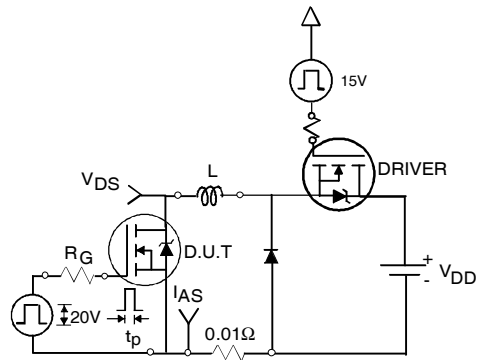


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms

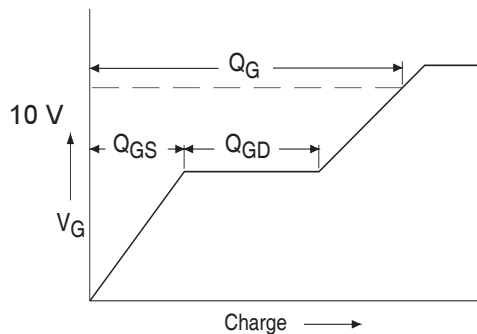


Fig 13a. Basic Gate Charge Waveform

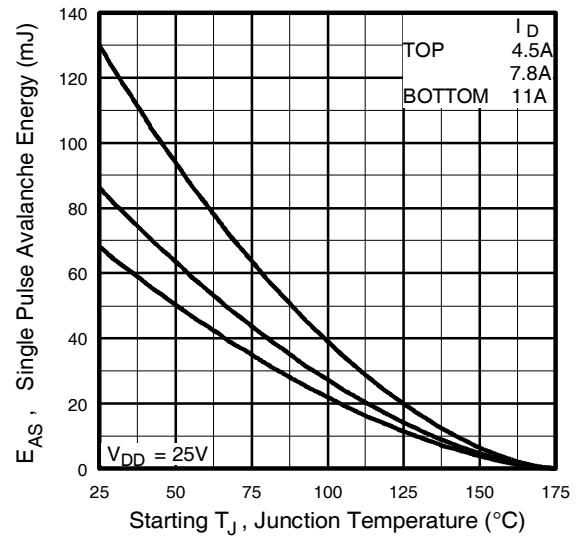


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

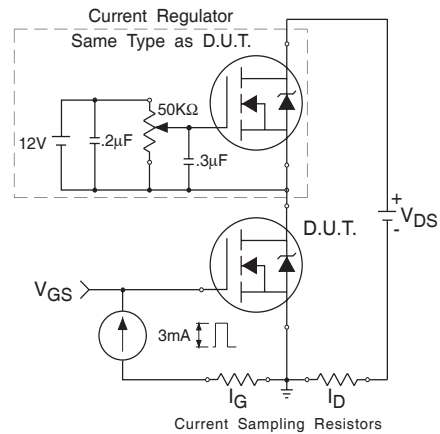


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

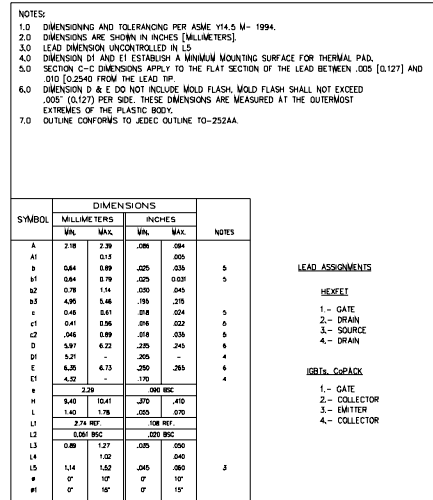


* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® MOSFETs

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Dimensions are shown in millimeters (inches)



PART NUMBER

✓ DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)

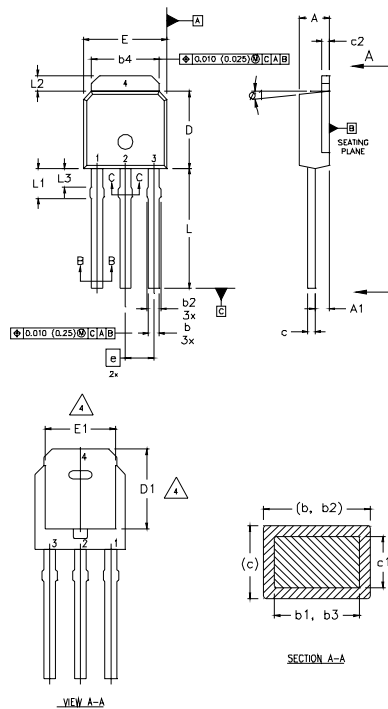
YEAR 9 = 1999

WEEK 16

A = ASSEMBLY SITE CODE

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

HEXFET

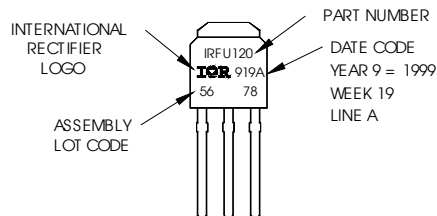
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.36	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	19°	Ø	19°	

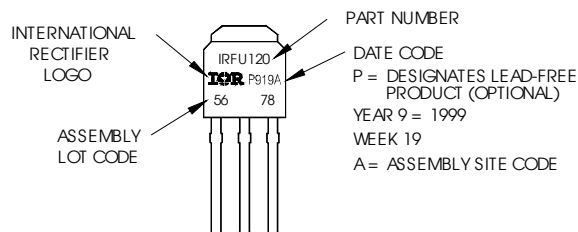
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line
position indicates "Lead-Free"

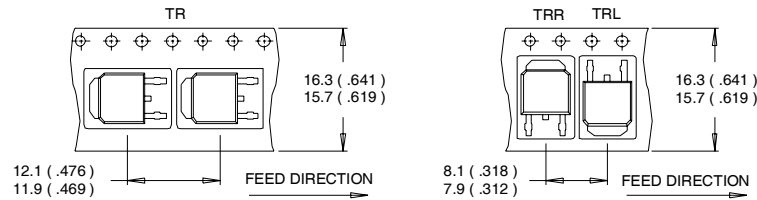


OR



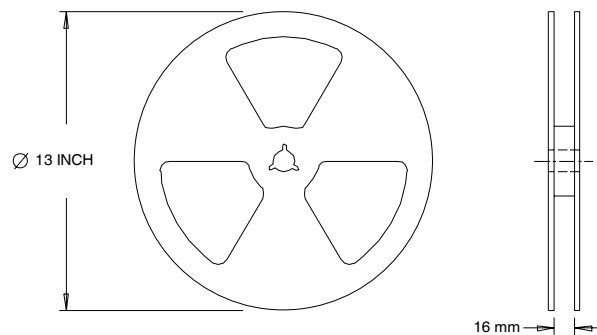
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International
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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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