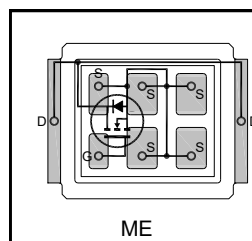**Application**
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits
- Optimized for Logic Level Drive
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Lead-Free, RoHS Compliant

V_{DSS}	**40V**
$R_{DS(on)}$ typ.	**1.0mΩ**
max @ V_{GS} = 10V	**1.25mΩ**
$R_{DS(on)}$ typ.	**1.5mΩ**
max @ V_{GS} = 4.5V	**2.0mΩ**
I_D (Silicon Limited)	**209A**

ME

DirectFET® ISOMETRIC

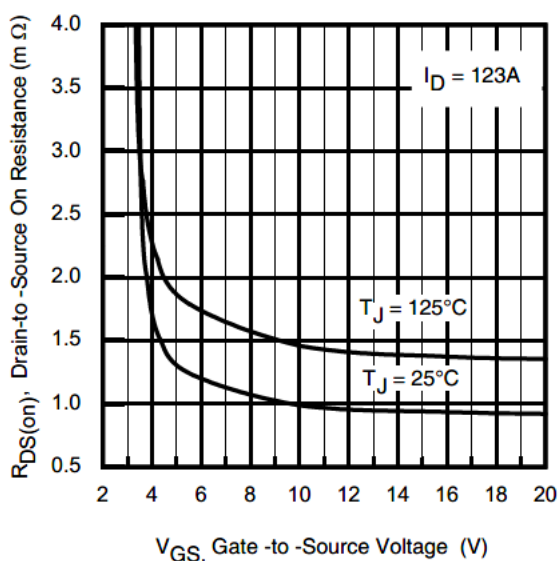| Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	**Quantity**	
IRL7486MPbF	DirectFET® ME	Tape and Reel	4800	IRL7486MTRPbF

Fig 1. Typical On-Resistance vs. Gate Voltage
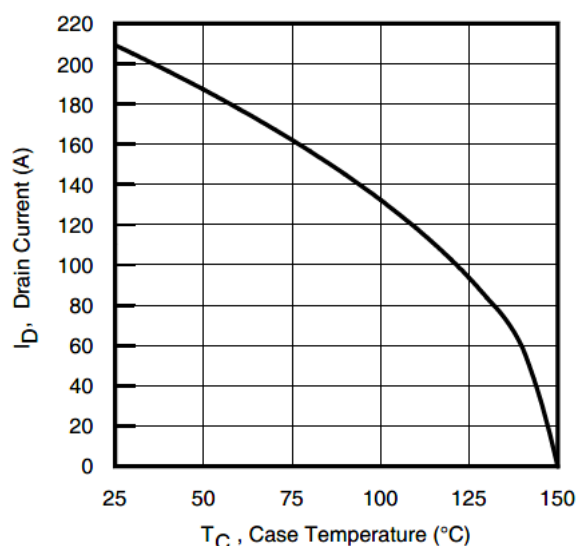
Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	209	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	132	
I_{DM}	Pulsed Drain Current ①	836	
P_D @T_C = 25°C	Maximum Power Dissipation	104	W
	Linear Derating Factor	0.83	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	80	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑨	190	
$E_{AS\ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑧	111	
I_{AR}	Avalanche Current ①	See Fig.15,16, 23a, 23b	A
E_{AR}	Repetitive Aval`anche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ❶	——	60	°C/W
$R_{\theta JA}$	Junction-to-Ambient ❸	12.5	——	
$R_{\theta JA}$	Junction-to-Ambient ❷	20	——	
$R_{\theta JC}$	Junction-to-Case ❹⑦	——	1.2	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	0.75	——	

Static @ T_J = 25°C (unless otherwise specified)

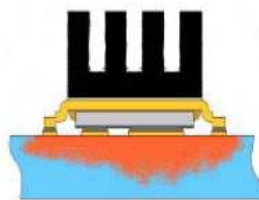| Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	35	——	mV/°C	Reference to 25°C, I_D = 1.0mA①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	1.0	1.25	mΩ	V_{GS} = 10V, I_D = 123A ④
		——	1.5	2.0		V_{GS} = 4.5V, I_D = 62A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.8	2.5	V	V_{DS} = V_{GS}, I_D = 150µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	µA	V_{DS} = 40V, V_{GS} = 0V
		——	——	150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Internal Gate Resistance	——	0.97	——	Ω	

Notes:

❷ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

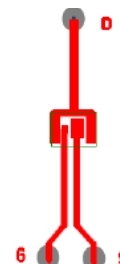❸ Used double sided cooling , mounting pad with large heatsink.

❹ TC measured with thermocouple mounted to top (Drain) of part.
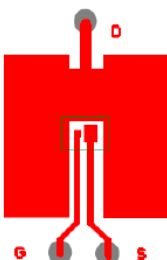
❶ Surface mounted on 1 in. square Cu board (still air).

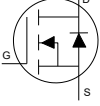
❷ Mounted to a PCB with small clip heatsink (still air)

❷ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

Dynamic @ T_J = 25°C (unless otherwise specified)

| Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	427	——	——	S	V_{DS} = 10V, I_D = 123A
Q_g	Total Gate Charge	——	76	111	nC	I_D = 123A
Q_{gs}	Gate-to-Source Charge	——	27	——		V_{DS} = 20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	33	——		V_{GS} = 4.5V ④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	41	——		I_D = 123A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	——	35	——	ns	V_{DD} = 20V
t_r	Rise Time	——	110	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	54	——		R_G = 2.7Ω
t_f	Fall Time	——	47	——		V_{GS} = 4.5V ④
C_{iss}	Input Capacitance	——	6904	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	939	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	607	——		f = 1.0MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	1150	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	——	1376	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	104	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	836		
V_{SD}	Diode Forward Voltage	——	——	1.2	V	T_J= 25°C, I_S =123A, V_{GS} = 0V④
dv/dt	Peak Diode Recovery ③	——	3.6	——	V/ns	T_J =150°C, I_S =123A, V_{DS} = 40V
t_{rr}	Reverse Recovery Time	——	43	——	ns	T_J = 25° C V_R = 34V,
		——	44	——		T_J = 125°C I_F = 123A
Q_{rr}	Reverse Recovery Charge	——	55	——	nC	T_J = 25°C di/dt = 100A/µs ④
		——	56	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	2.1	——	A	T_J = 25°C

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by $T_J$max, starting T_J = 25°C, L = 0.011mH R_G = 50Ω, I_{AS} = 123A, V_{GS} =10V.

③ I_{SD} ≤ 123A, di/dt ≤ 1056A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ $R_θ$ is measured at T_J approximately 90°C.

⑧ This value determined from sample failure population, starting T_J = 25°C, L= 0.011mH, R_G = 50Ω, V_{GS} =10V.

⑨ Limited by $T_J$max, starting T_J = 25°C, L = 1.0mH R_G = 50Ω, I_{AS} = 19.5A, V_{GS} =10V.
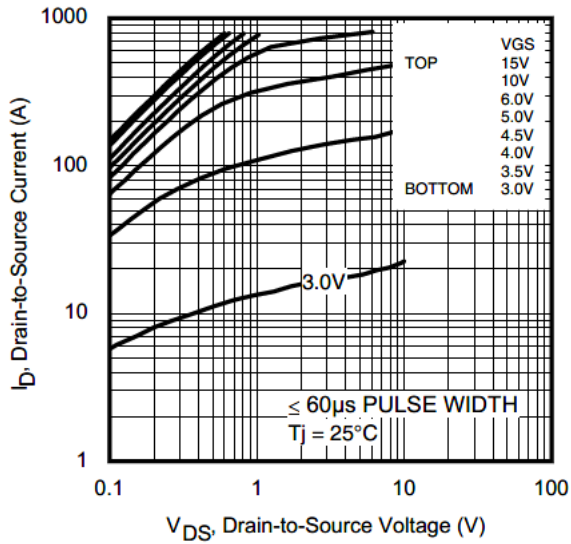
Fig 3. Typical Output Characteristics
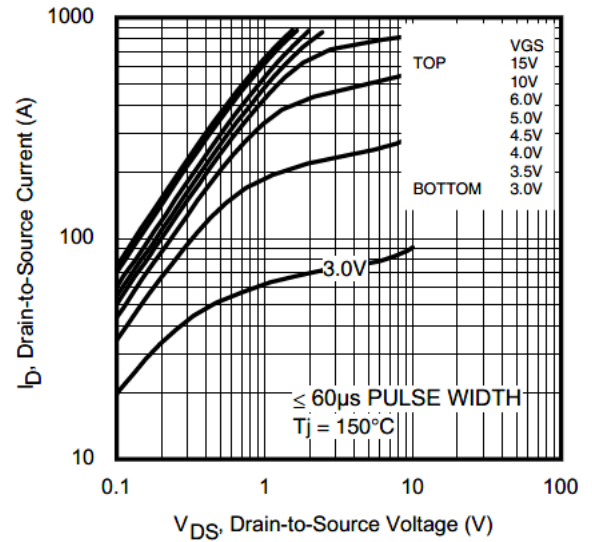
**Fig 4.** Typical Output Characteristics
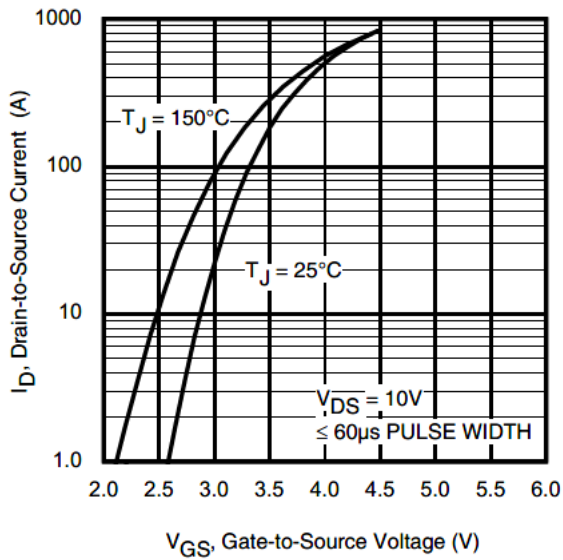
Fig 5. Typical Transfer Characteristics
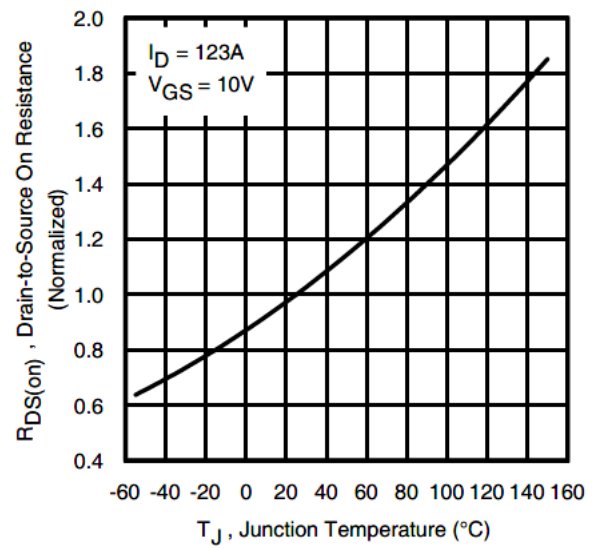
Fig 6. Normalized On-Resistance vs. Temperature
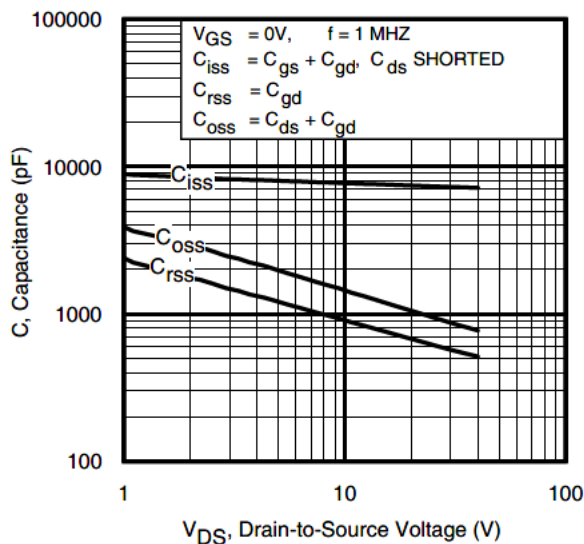
Fig 7. Typical Capacitance vs. Drain-to-Source Voltage
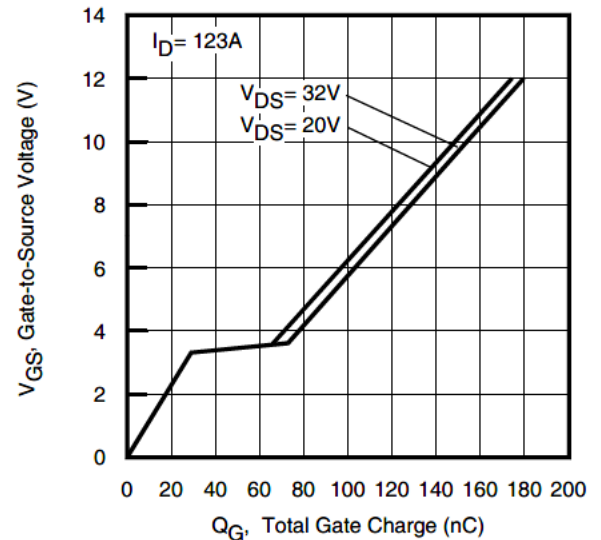
Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage
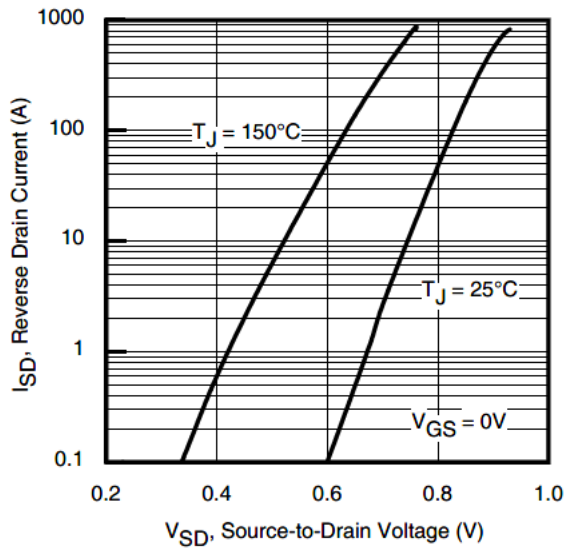
Fig 9. Typical Source-Drain Diode Forward Voltage
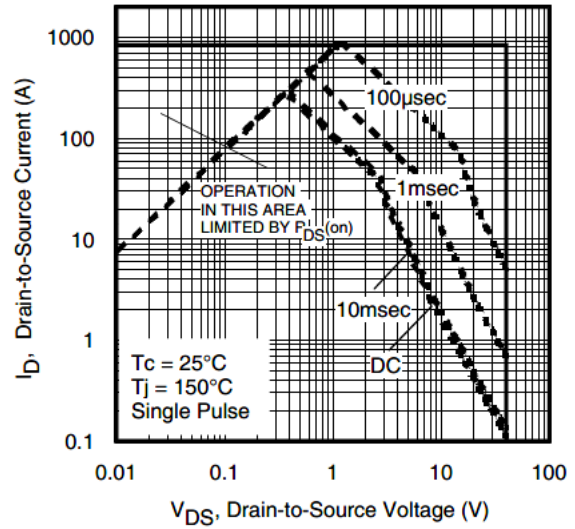
Fig 10. Maximum Safe Operating Area
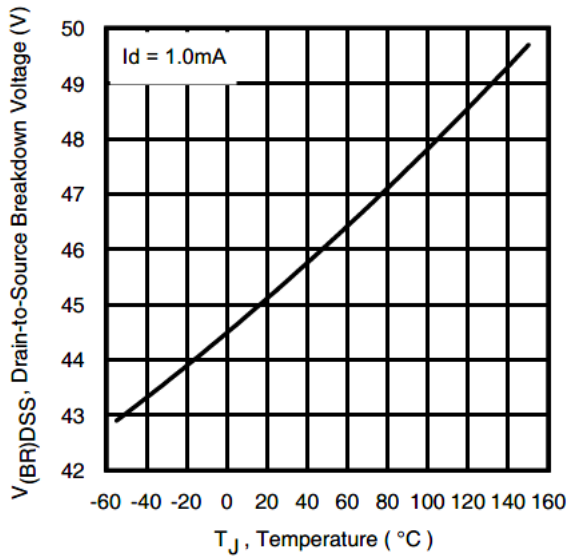
Fig 11. Drain-to-Source Breakdown Voltage
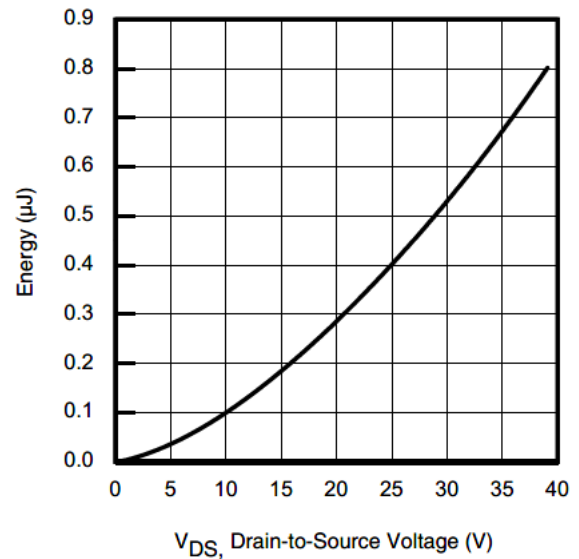
Fig 12. Typical C_{oss} Stored Energy
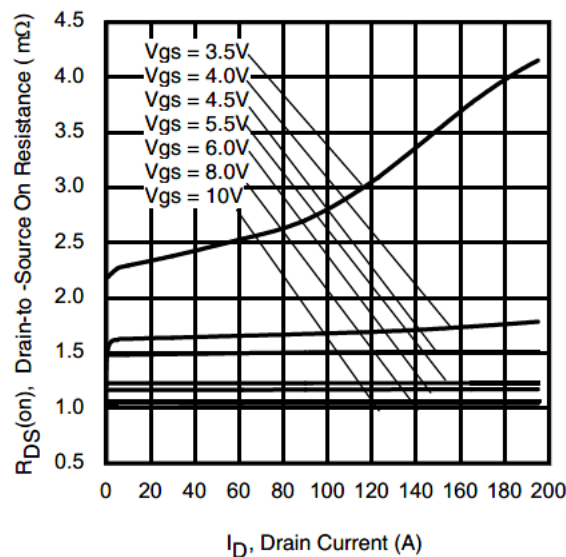
Fig 13. Typical On-Resistance vs. Drain Current

Rev. 2.1, 2021-07-01
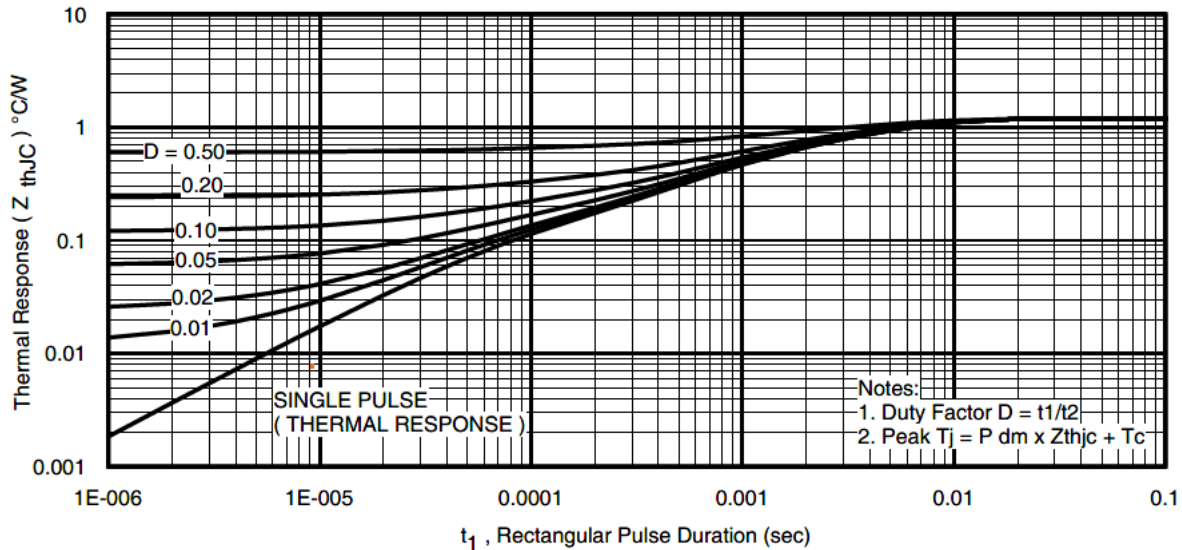
Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-
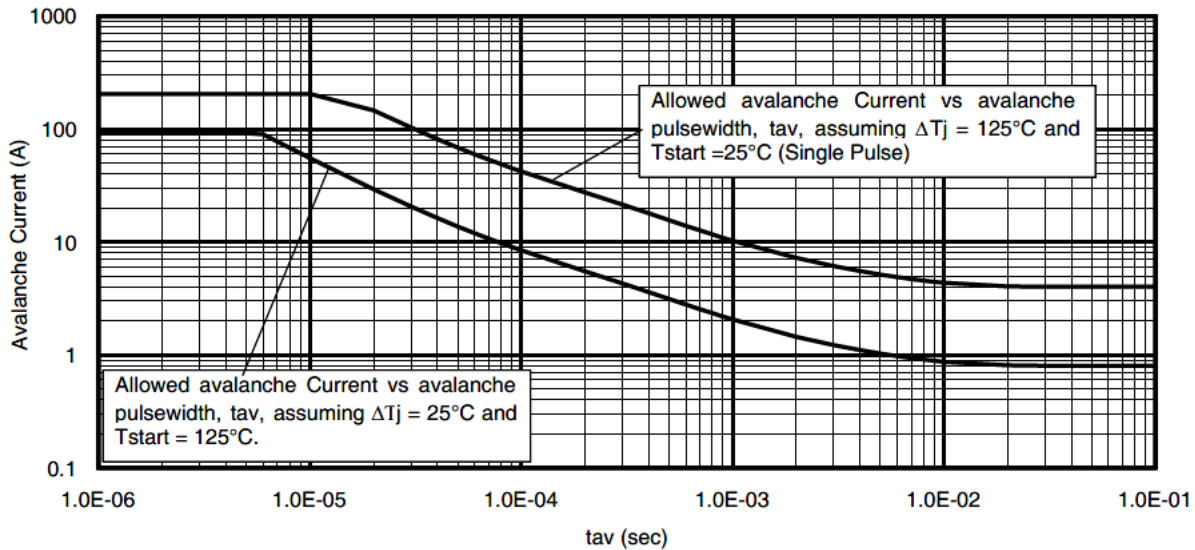
Fig 15. Avalanche Current vs. Pulse Width
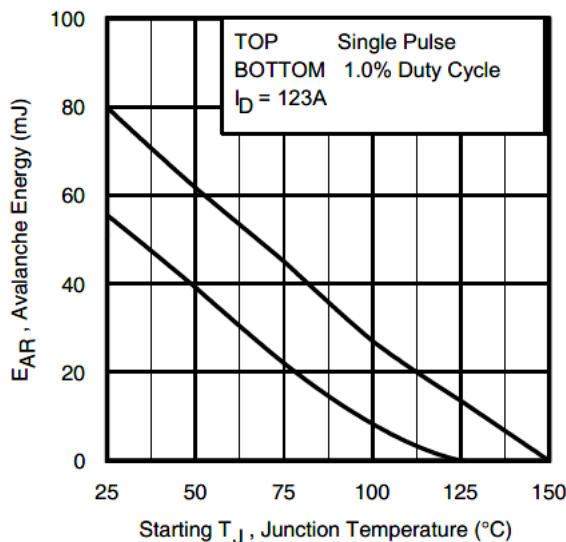
Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:

Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$PD (ave) = 1/2 \, (\, 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$
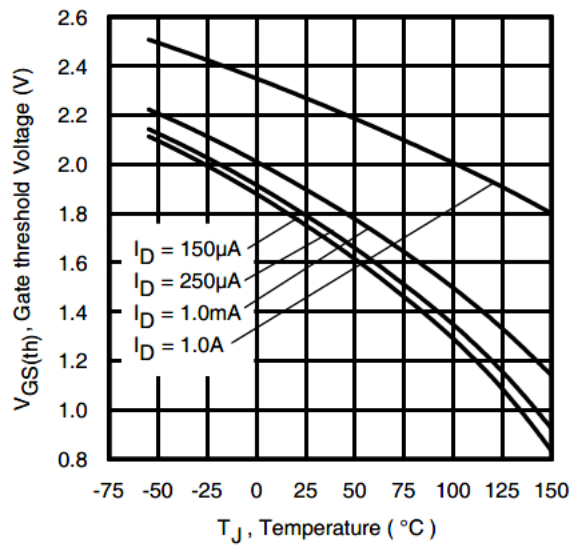
Fig 17. Threshold Voltage vs. Temperature
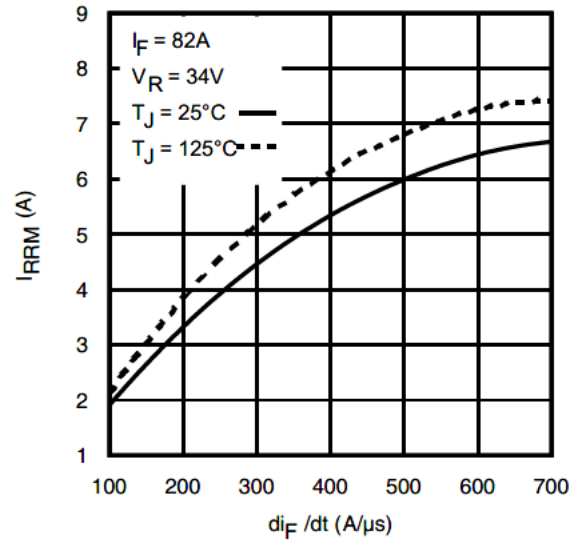
Fig 18. Typical Recovery Current vs. dif/dt
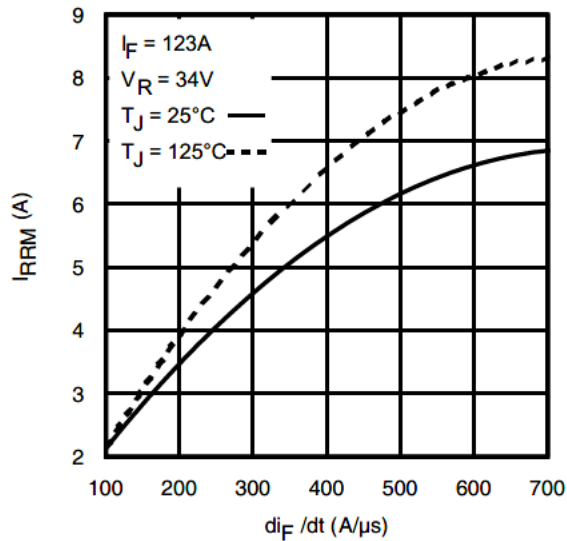
Fig 19. Typical Recovery Current vs. dif/dt
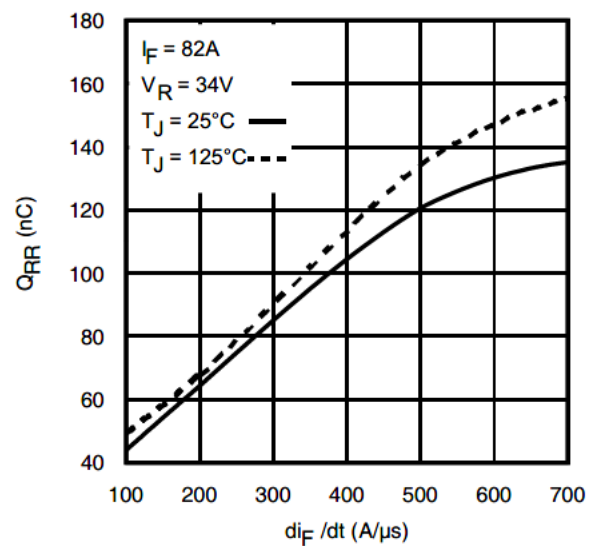
Fig 20. Typical Stored Charge vs. dif/dt
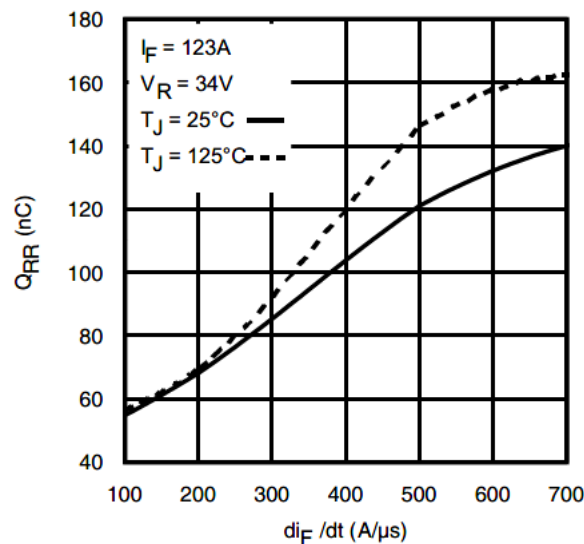
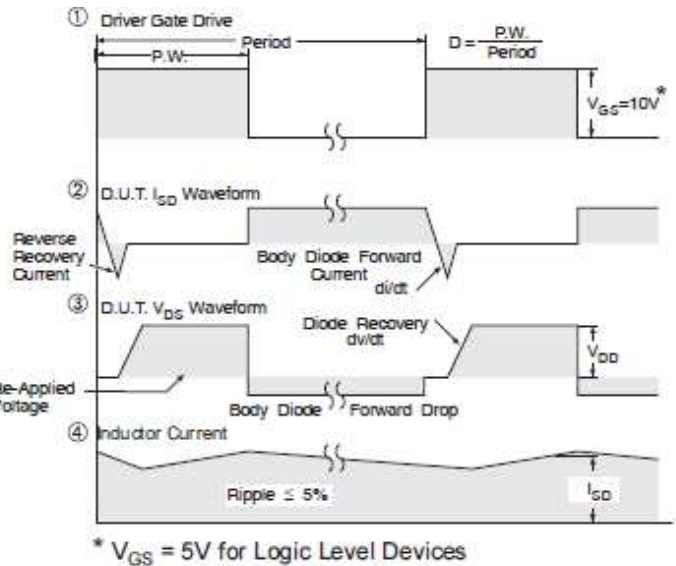**Fig 21.** Typical Stored Charge vs. dif/dt
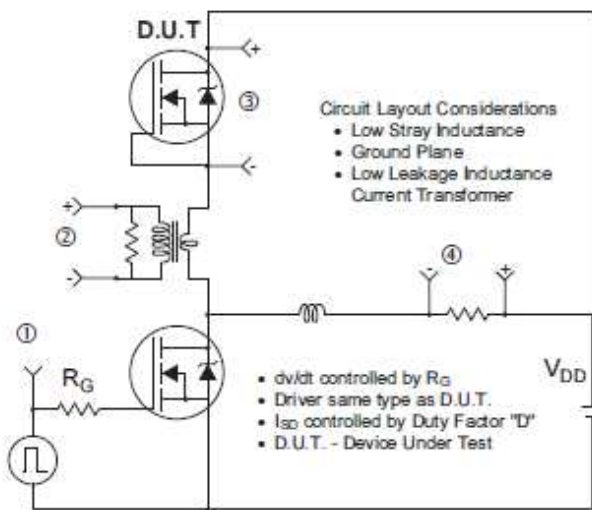
Rev. 2.1, 2021-07-01

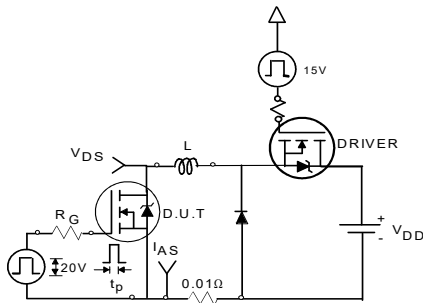**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs
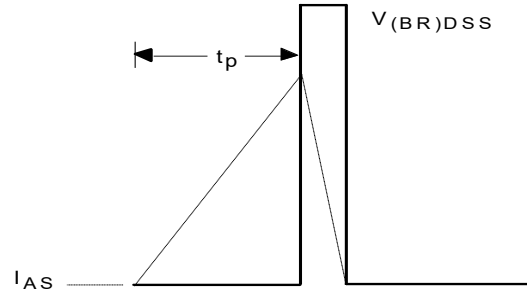

Fig 23a. Unclamped Inductive Test Circuit
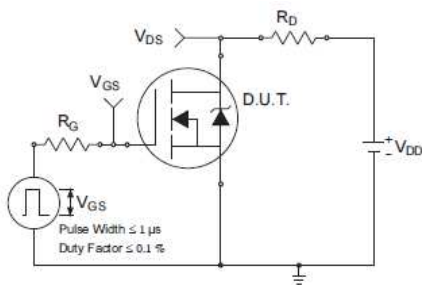

Fig 23b. Unclamped Inductive Waveforms

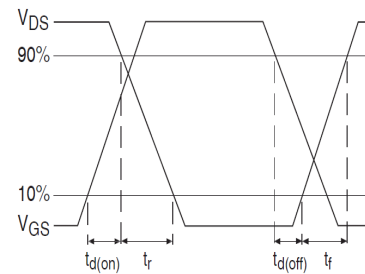**Fig 24a.** Switching Time Test Circuit
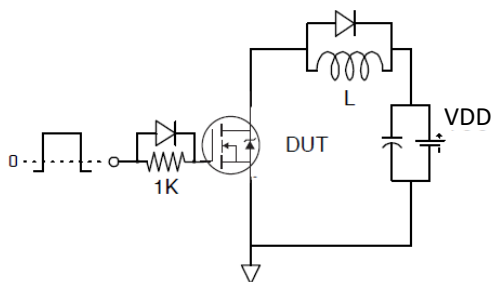

Fig 24b. Switching Time Waveforms

Fig 25a. Gate Charge Test Circuit
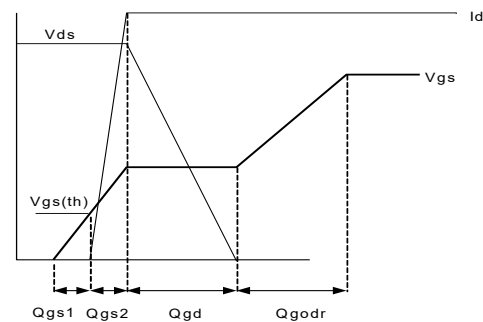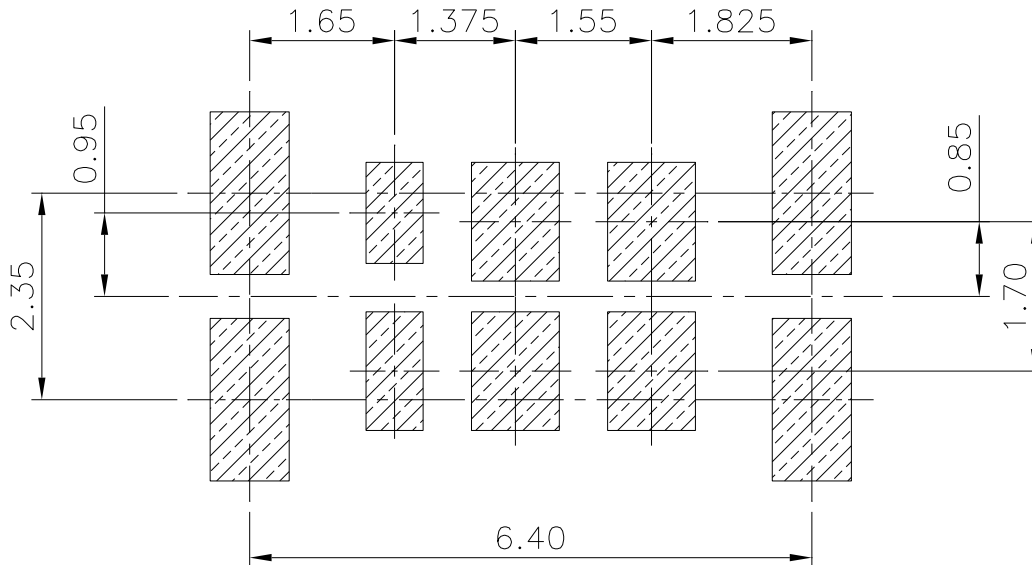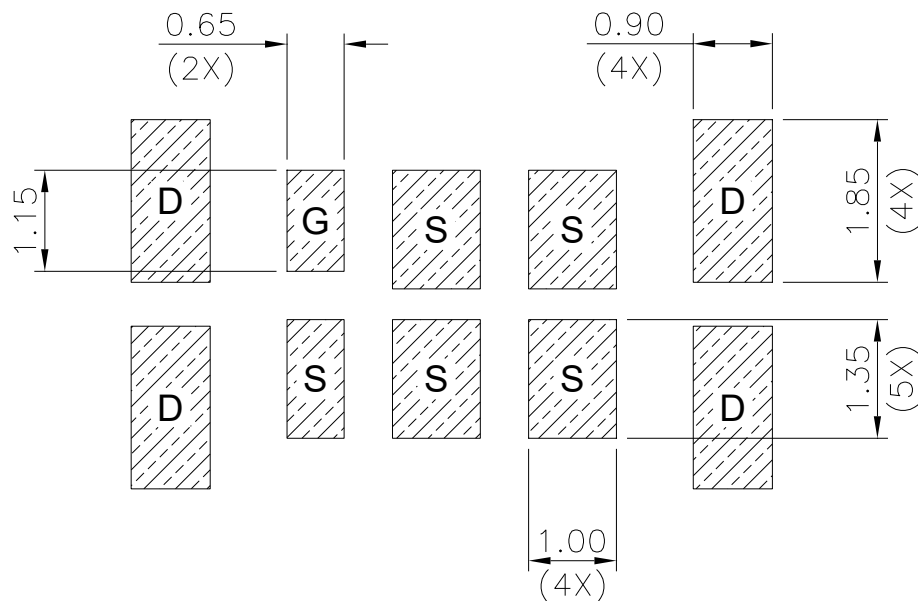

Fig 25b. Gate Charge Waveform

DirectFET® Board Footprint, ME Outline

(Medium Size Can, E-Designation)

Please see DirectFET® application note AN-1035 for all details regarding the assembly of DirectFET®.
This includes all recommendations for stencil and substrate designs.


G = GATE
D = DRAIN
S = SOURCE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Rev. 2.1, 2021-07-01
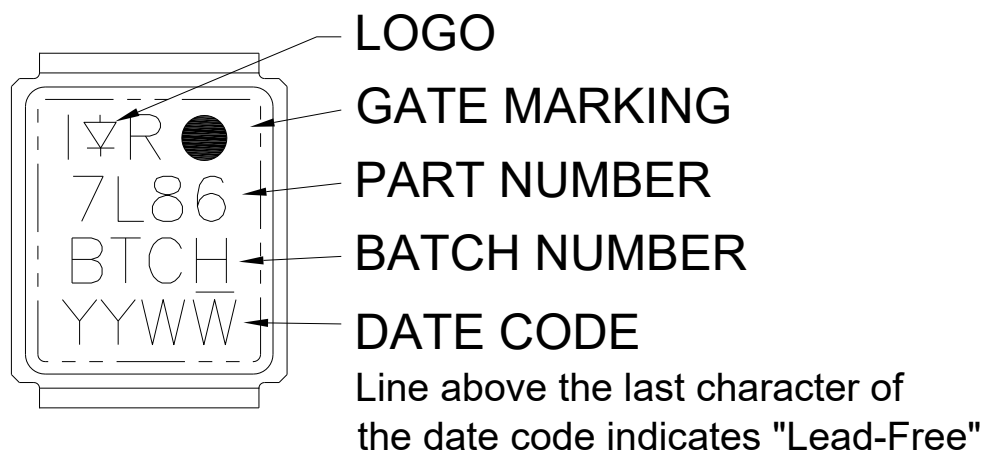
DirectFET® Outline Dimension, ME Outline

(Medium Size Can, E-Designation)

Please see DirectFET® application note AN-1035 for all details regarding the assembly of DirectFET®. This includes all recommendations for stencil and substrate designs.
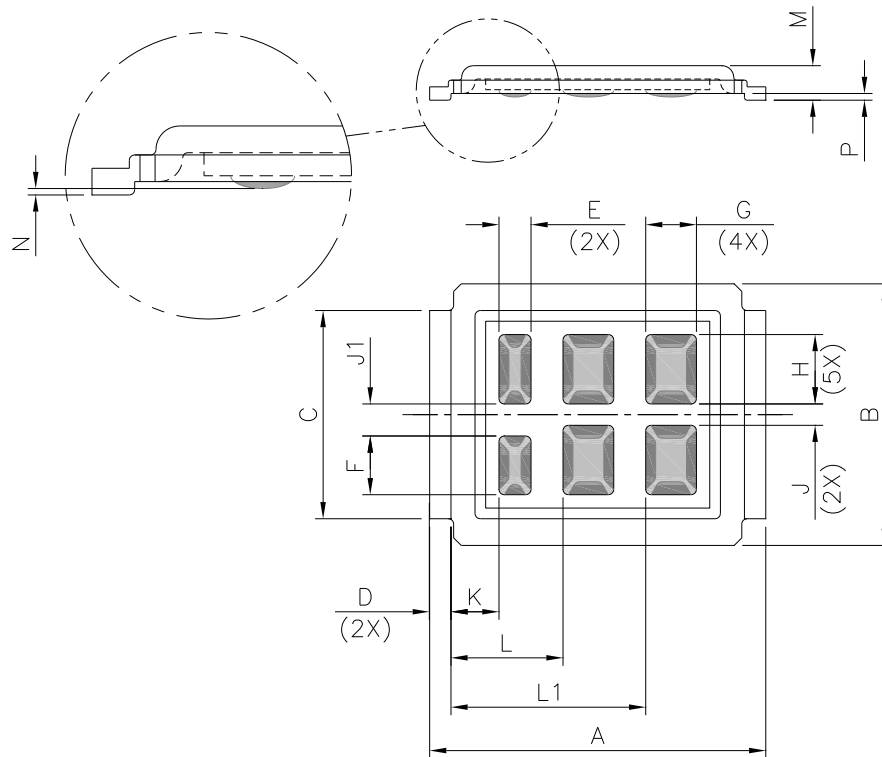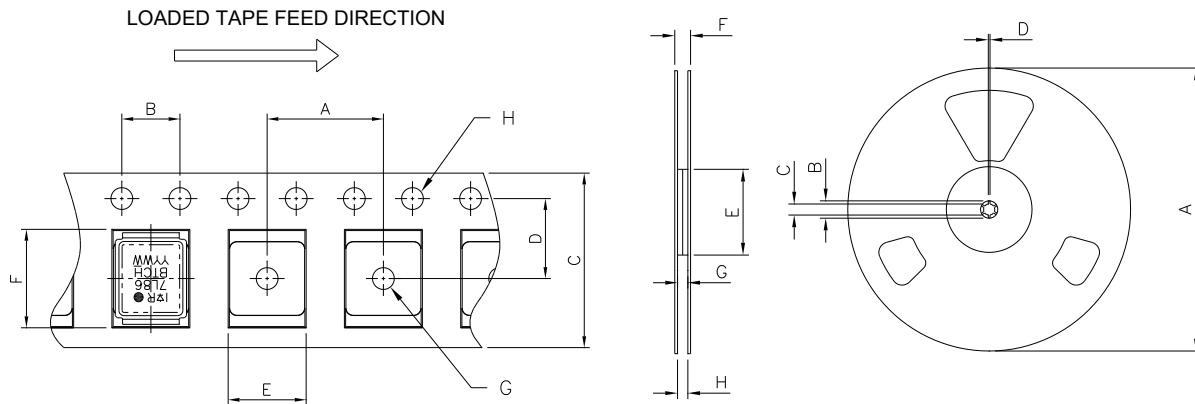
DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	1.08	1.12	0.043	0.044
G	0.93	0.97	0.037	0.038
H	1.28	1.32	0.050	0.052
J	0.38	0.42	0.015	0.017
J1	0.58	0.62	0.023	0.024
K	0.88	0.92	0.035	0.036
L	2.08	2.12	0.082	0.083
L1	3.63	3.67	0.143	0.144
M	0.59	0.70	0.023	0.028
N	0.02	0.08	0.0008	0.003
P	0.08	0.17	0.003	0.007

DirectFET® Part Marking

LOGO
GATE MARKING
PART NUMBER
BATCH NUMBER
DATE CODE
Line above the last character of the date code indicates "Lead-Free"

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

DirectFET® Tape & Reel Dimension (Showing component orientation).

LOADED TAPE FEED DIRECTION

NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. Ordered as IRL7486MTRPBF.

REEL DIMENSIONS				
STANDARD OPTION (QTY 4800)				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606

Note: For the most current drawing please refer to IR webite at http://www.irf.com/package/

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F† guidelines)	
Moisture Sensitivity Level	DFET 1.5	MSL1 (per JEDEC J-STD-020D†)
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
05/14/2015	2.1	• Updated registered trademark from DirectFET™ to DirectFET® on page 1,9 and 10.
07/01/2021	2.2	• Updated Eas notes

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µHVIC™, µIPM™, µPFC™, AU-ConvertIR™, AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolDP™, CoolGaN™, COOLiR™, CoolMOS™, CoolSET™, CoolSiC™, DAVE™, DI-POL™, DirectFET™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, GaNpowIR™, HEXFET™, HITFET™, HybridPACK™, iMOTION™, IRAM™, ISOFACE™, IsoPACK™, LEDrivIR™, LITIX™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OPTIGA™, OptiMOS™, ORIGA™, PowIRaudio™, PowIRStage™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, SmartLEWIS™, SOLID FLASH™, SPOC™, StrongIRFET™, SupIRBuck™, TEMPFET™, TRENCHSTOP™, TriCore™, UHVIC™, XHP™, XMC™

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  [IRL7486MTRPBF](#)