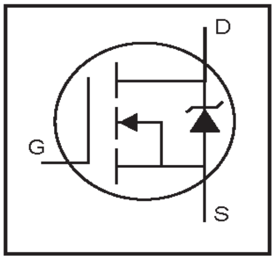
International
IOR Rectifier

PD - 95451

# IRL530NPbF

## HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



$V_{DSS}$ = 100V

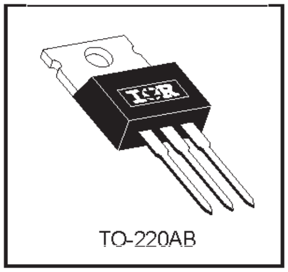
$R_{DS(on)}$ = 0.10Ω

$I_D$ = 17A

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

## Absolute Maximum Ratings

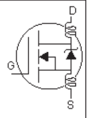
| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 17 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 12 | |
| $I_{DM}$ | Pulsed Drain Current ① | 60 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 79 | W |
| | Linear Derating Factor | 0.53 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 16 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy② | 150 | mJ |
| $I_{AR}$ | Avalanche Current① | 9.0 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | 7.9 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |
| | Mounting torque, 6-32 or M3 srew | 10 lbf•in (1.1N•m) | |

## Thermal Resistance

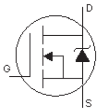
| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | 1.9 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | 0.50 | —— | |
| $R_{\theta JA}$ | Junction-to-Ambient | —— | 62 | |

6/23/04

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 100 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.122 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | —— | 0.100 | Ω | $V_{GS}$ = 10V, $I_D$ = 9.0A ④ |
| | | —— | —— | 0.120 | | $V_{GS}$ = 5.0V, $I_D$ = 9.0A ④ |
| | | —— | —— | 0.150 | | $V_{GS}$ = 4.0V, $I_D$ = 8.0A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | —— | 2.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $g_{fs}$ | Forward Transconductance | 7.7 | —— | —— | S | $V_{DS}$ = 25V, $I_D$ = 9.0A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 25 | μA | $V_{DS}$ = 100V, $V_{GS}$ = 0V |
| | | —— | —— | 250 | | $V_{DS}$ = 80V, $V_{GS}$ = 0V, $T_J$ = 150°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 16V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = -16V |
| $Q_g$ | Total Gate Charge | —— | —— | 34 | nC | $I_D$ = 9.0A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | —— | 4.8 | | $V_{DS}$ = 80V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | —— | 20 | | $V_{GS}$ = 5.0V, See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 7.2 | —— | ns | $V_{DD}$ = 50V |
| $t_r$ | Rise Time | —— | 53 | —— | | $I_D$ = 9.0A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 30 | —— | | $R_G$ = 6.0Ω, $V_{GS}$ = 5.0V |
| $t_f$ | Fall Time | | 26 | | | $R_D$ = 5.5Ω, See Fig. 10 ④ |
| $L_D$ | Internal Drain Inductance | —— | 4.5 | —— | nH | Between lead,<br>6mm (0.25in.)<br>from package<br>and center of die contact  |
| $L_S$ | Internal Source Inductance | —— | 7.5 | —— | | |
| $C_{iss}$ | Input Capacitance | —— | 800 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 160 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 90 | —— | | ƒ = 1.0MHz, See Fig. 5 |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current<br>(Body Diode) | —— | —— | 17 | A | MOSFET symbol<br>showing the<br>integral reverse<br>p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current<br>(Body Diode) ①⑥ | —— | —— | 60 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.3 | V | $T_J$ = 25°C, $I_S$ = 9.0A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | —— | 140 | 210 | ns | $T_J$ = 25°C, $I_F$ = 9.0A |
| $Q_{rr}$ | Reverse RecoveryCharge | —— | 740 | 1100 | nC | di/dt = 100A/μs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

② Starting $T_J$ = 25°C, L = 3.7mH $R_G$ = 25Ω, $I_{AS}$ = 9.0A. (See Figure 12)

③ $I_{SD} \leq 9.0A$, di/dt ≤ 540A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 300μs; duty cycle ≤ 2%

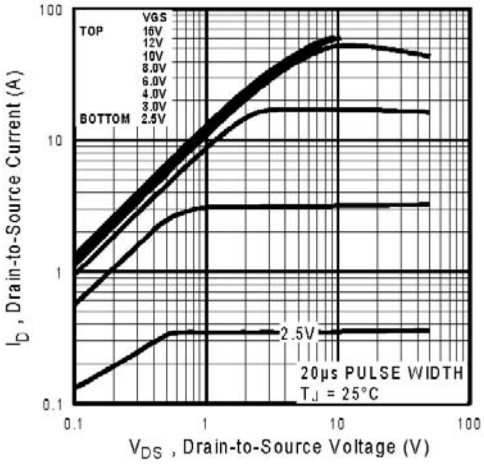


**Fig 1.** Typical Output Characteristics

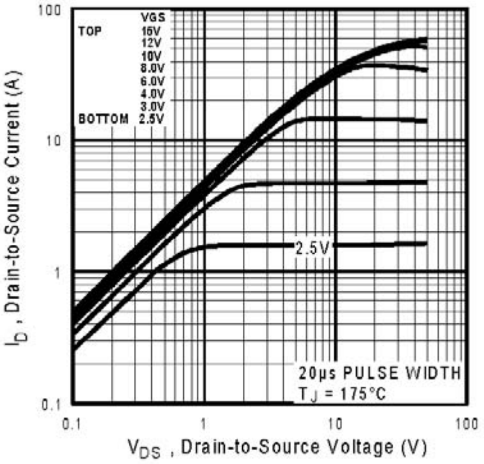


**Fig 2.** Typical Output Characteristics

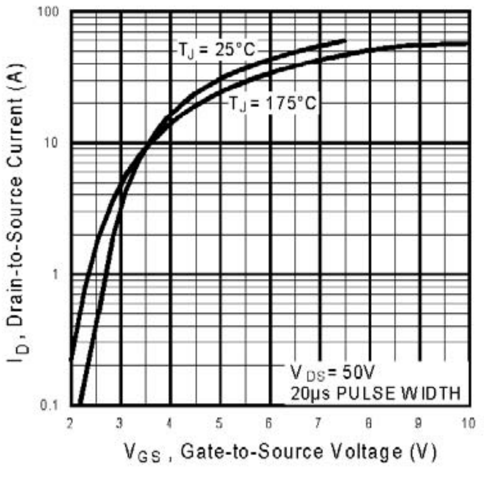


**Fig 3.** Typical Transfer Characteristics

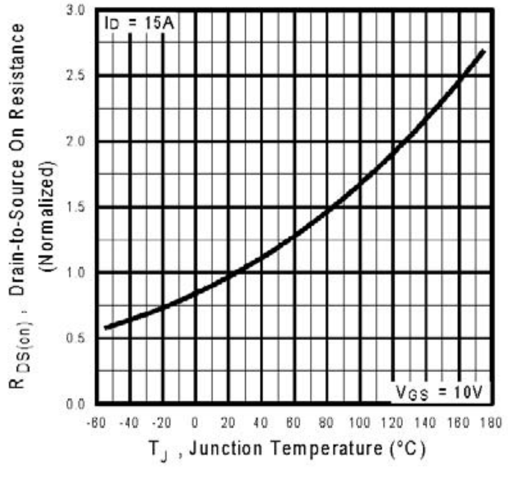


**Fig 4.** Normalized On-Resistance
Vs. Temperature

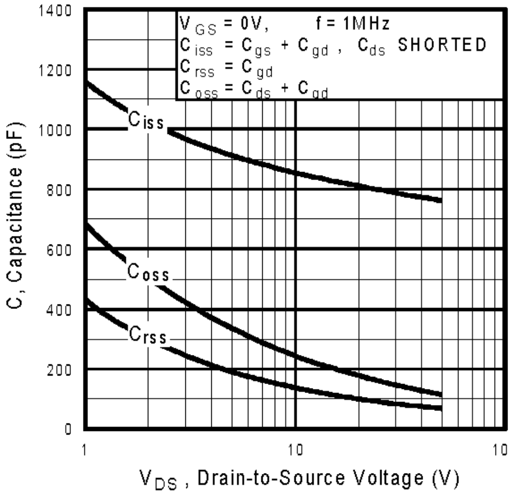


**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

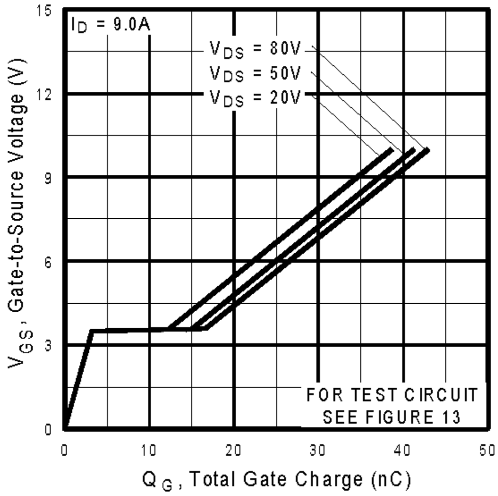


**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

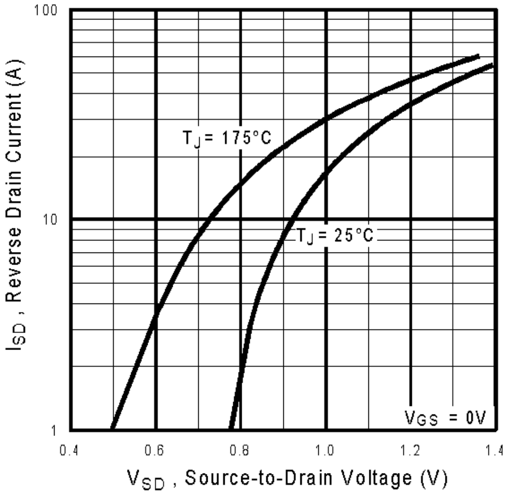


**Fig 7.** Typical Source-Drain Diode Forward Voltage

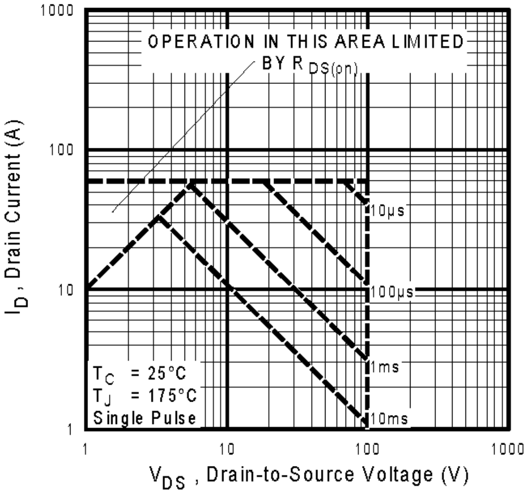


**Fig 8.** Maximum Safe Operating Area

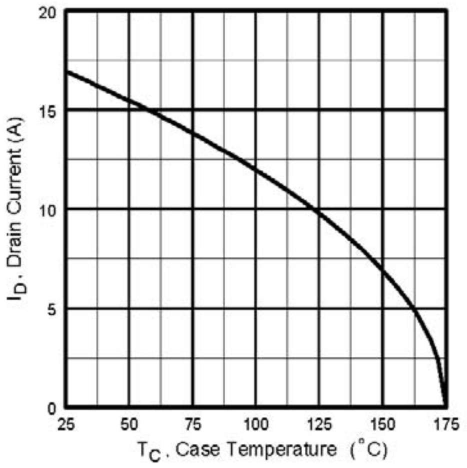


**Fig 9.** Maximum Drain Current Vs. Case Temperature

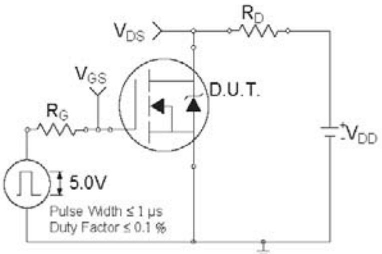


**Fig 10a.** Switching Time Test Circuit

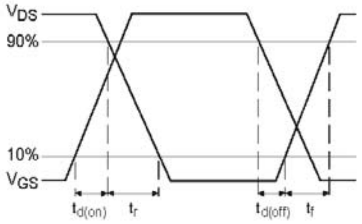


**Fig 10b.** Switching Time Waveforms

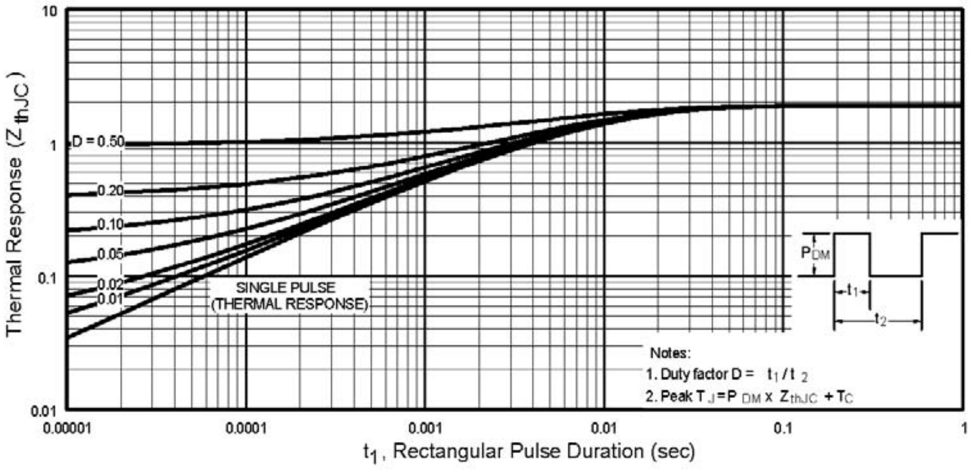


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

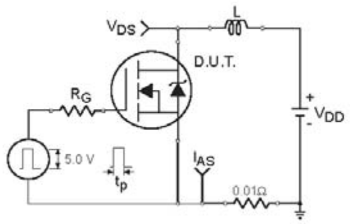


**Fig 12a.** Unclamped Inductive Test Circuit

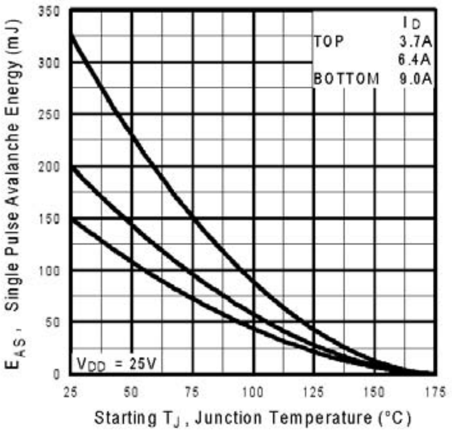


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

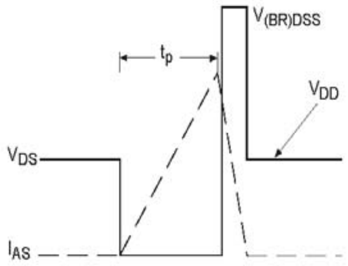


**Fig 12b.** Unclamped Inductive Waveforms

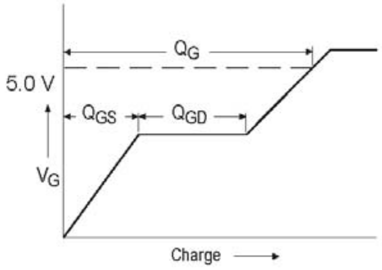


**Fig 13a.** Basic Gate Charge Waveform

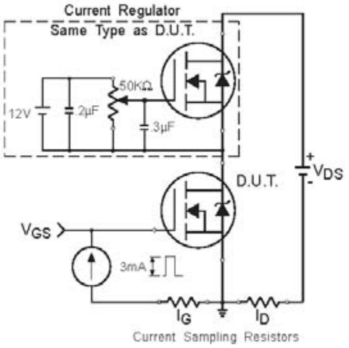
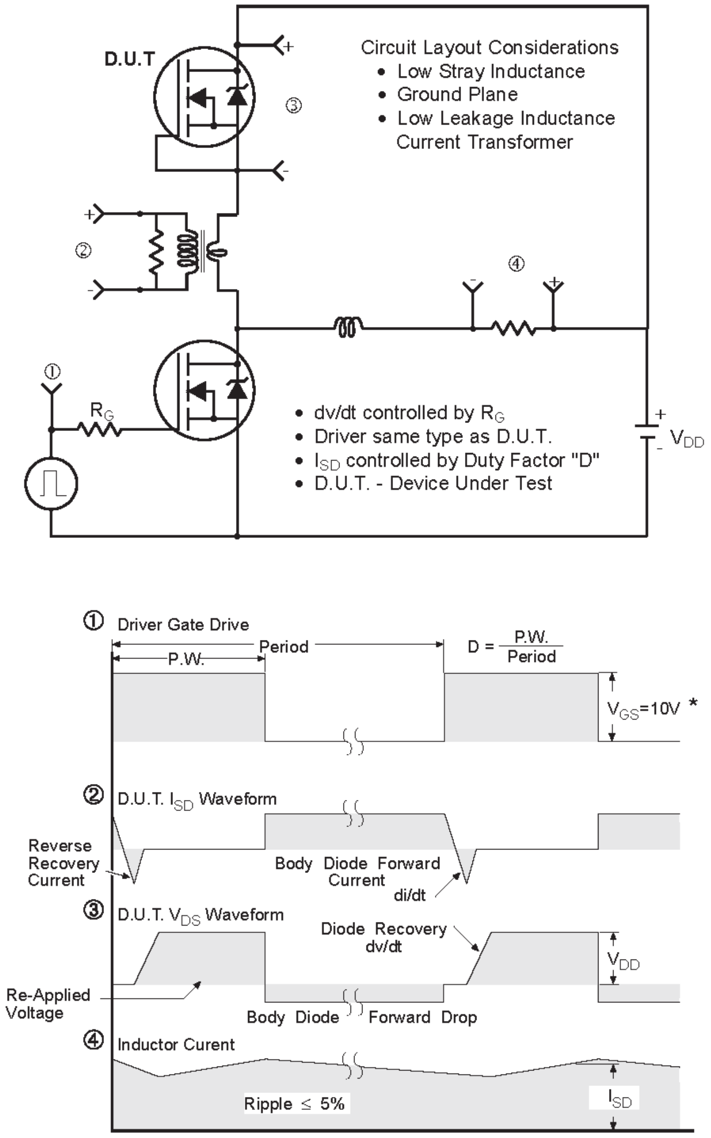


**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit

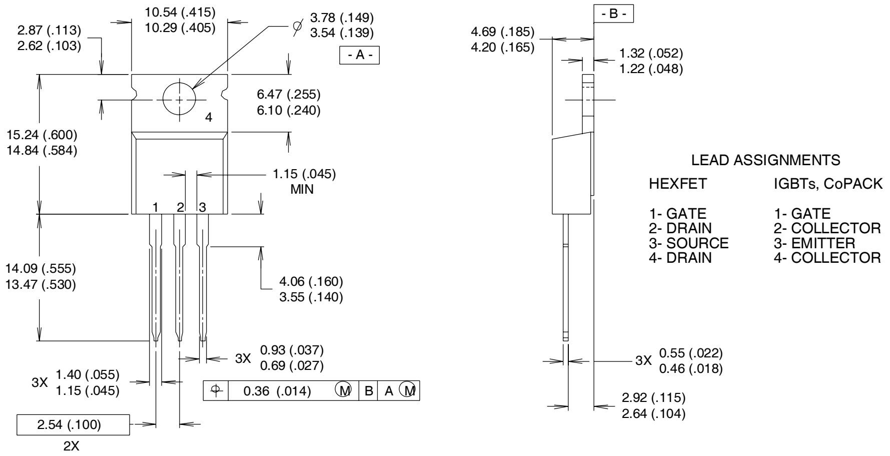


* $V_{GS}$ = 5V for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

| HEXFET | IGBTs, CoPACK |
|---|---|
| 1- GATE | 1- GATE |
| 2- DRAIN | 2- COLLECTOR |
| 3- SOURCE | 3- EMITTER |
| 4- DRAIN | 4- COLLECTOR |

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

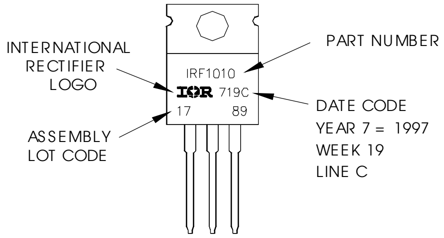
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

**Note:** "P" in assembly line position indicates "Lead-Free"



**TO-220AB package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

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