

MOSFET

OptiMOS™ 5, 40 V

Features

Application

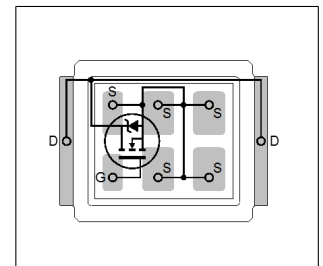
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{ds(on), max}$	0.82	mΩ
I_D	211	A
Q_{oss}	104	nC
$Q_g(0V..4.5V)$	61	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IRL40DM247	MG-WDSN-8-904 (ME)	M247	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	211 132 44	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$ (silicon limited), $R_{THJA}=45\text{ °C/W}^{(1)}$
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	844	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁽³⁾	E_{AS}	-	-	85	mJ	$I_D=50\text{ A}$, $R_{GS}=50\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	63 2.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=45\text{ °C/W}^{(1)}$
Operating and storage temperature	T_j , T_{stg}	-40	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2	°C/W	-
Thermal resistance, junction - Ambient, double sided cooling	$R_{thJA}^{(4)}$	-	12.5	-	°C/W	-
Thermal resistance, junction - Ambient, mounted on minimum foot print	$R_{thJA}^{(5)}$	-	20	-	°C/W	-
Thermal resistance, junction - Ambient	$R_{thJA}^{(1)}$	-	-	45	°C/W	-
Device on PCB, junction-to-pcb mounted	$R_{thJ-PCB}$	-	0.75	-	°C/W	-
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	reflow MSL3

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

⁴⁾ Used double sided cooling, mounting pad with large heat sink

⁵⁾ Mounted on minimum footprint full size board with metalized back with small clip heat sink

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	31	-	mV/°C	$I_D=1\text{ mA}$, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.62 0.79	0.82 1.3	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$
Gate resistance ¹⁾	R_G	-	1.2	-	Ω	-
Transconductance	g_{fs}	-	310	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	8400	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	2400	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	190	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Rise time	t_r	-	71	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	49	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Fall time	t_f	-	50	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$

¹⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	20	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	13	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge ²⁾	Q_{gd}	-	19	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	25	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ²⁾	Q_g	-	61	85	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.3	-	V	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	Q_g	-	118	165	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	99	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	104	-	nC	$V_{DD}=20\text{ V}$, $V_{GS}=0\text{ V}$

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	63	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	844	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	-	1	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ²⁾	t_{rr}	-	53	-	ns	$V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ²⁾	Q_{rr}	-	56	-	nC	$V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ See "Gate charge waveforms" for parameter definition

²⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

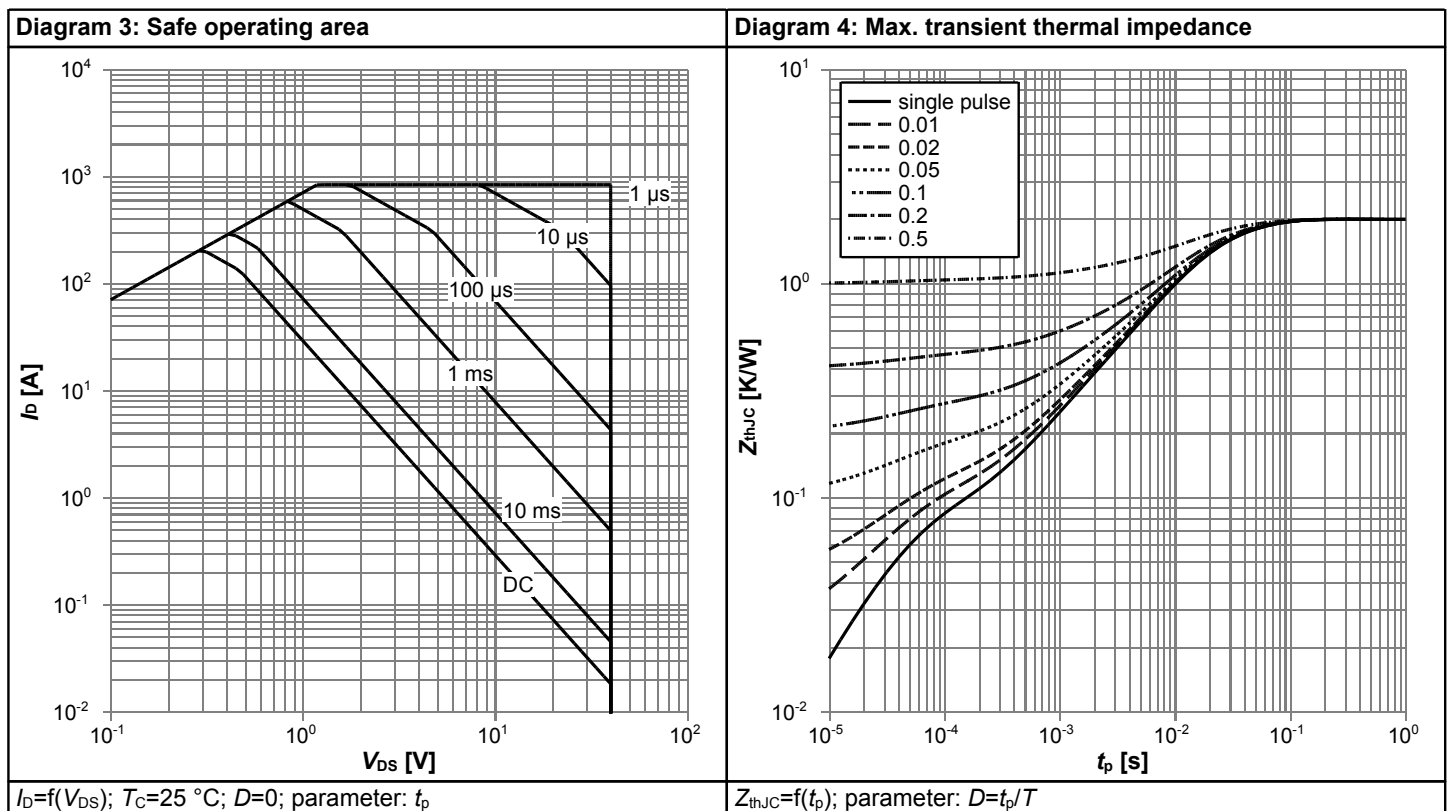
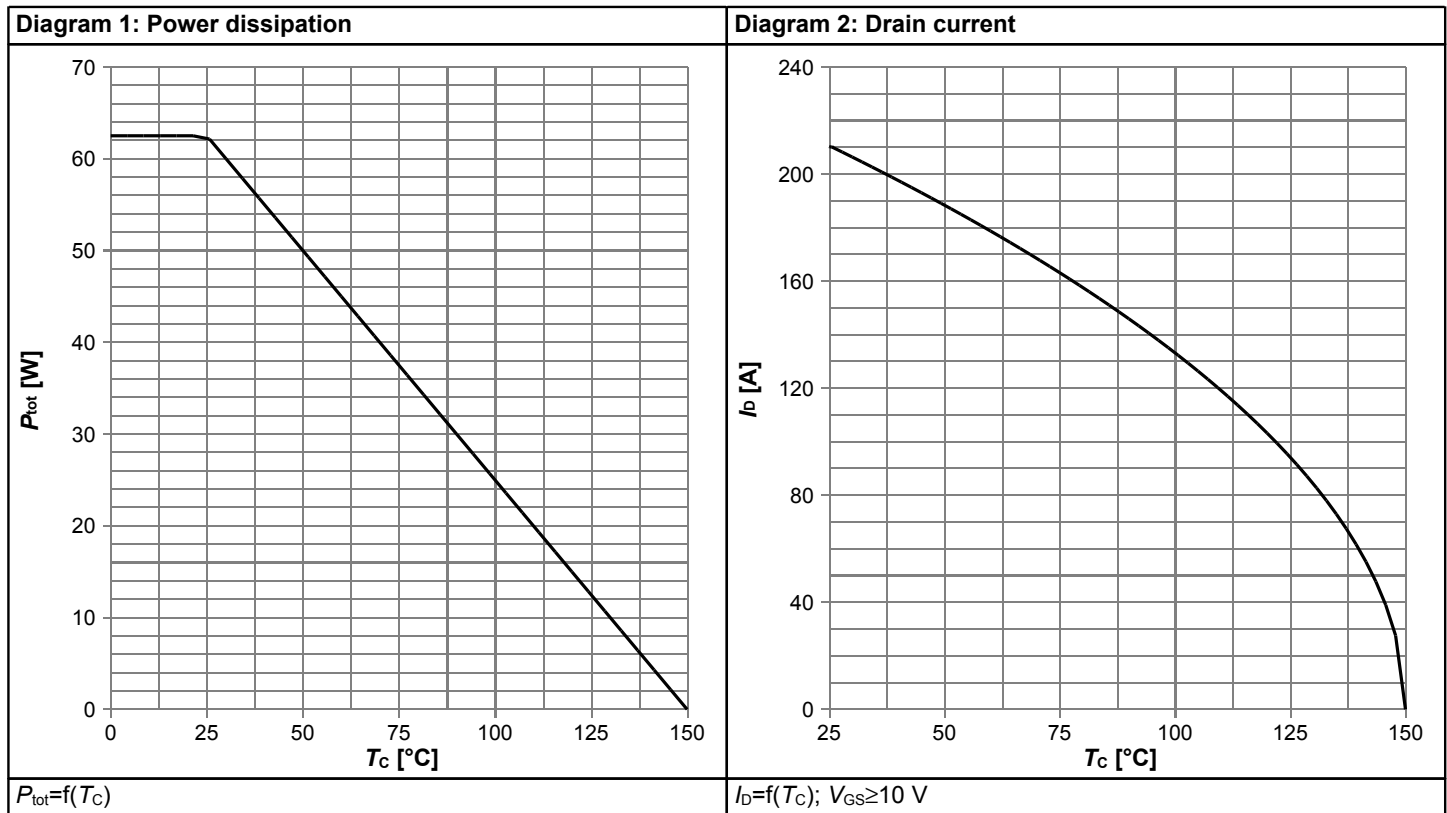
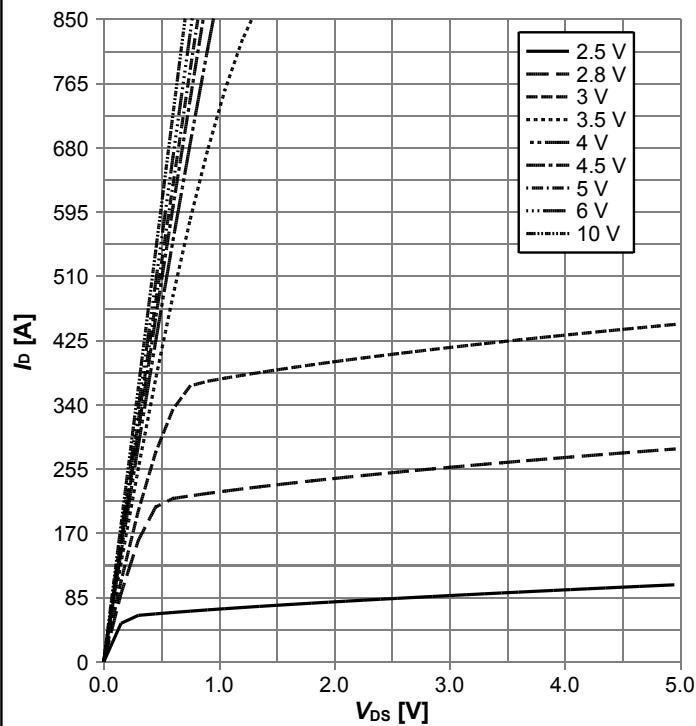
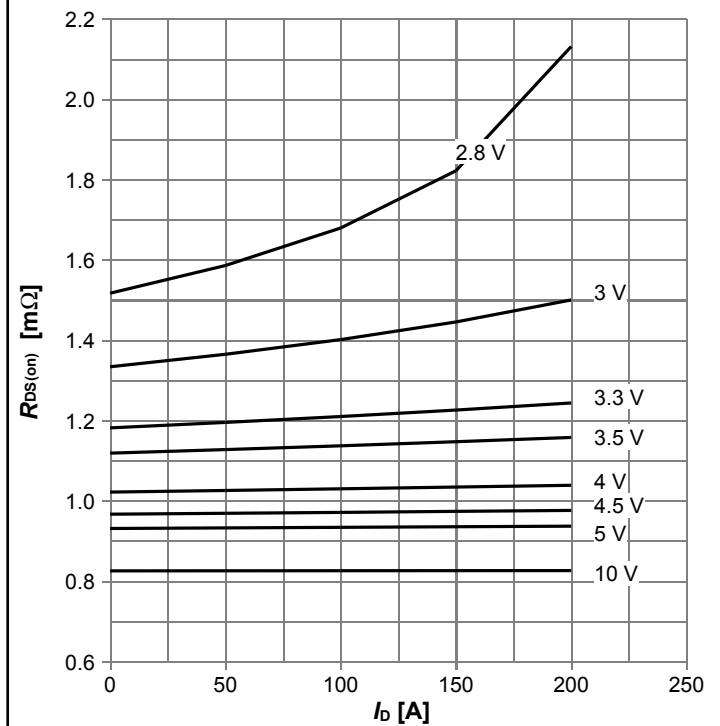


Diagram 5: Typ. output characteristics



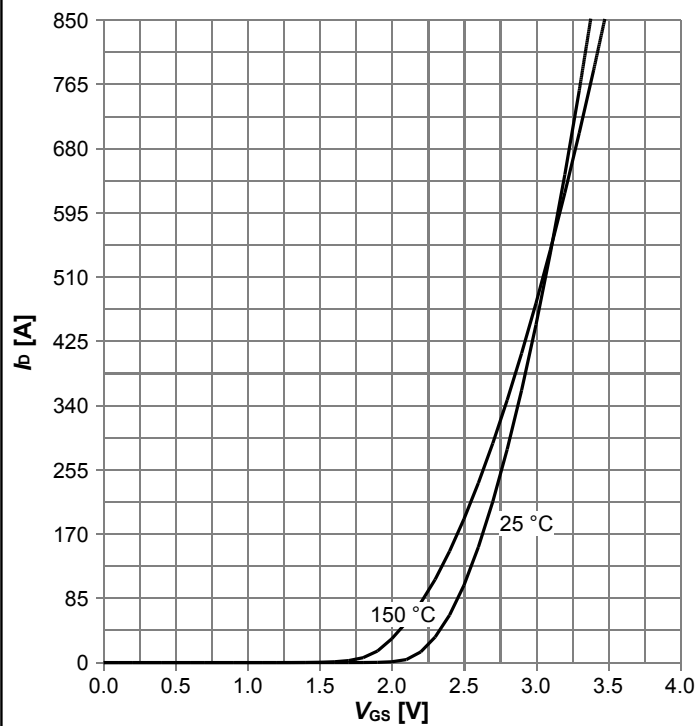
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



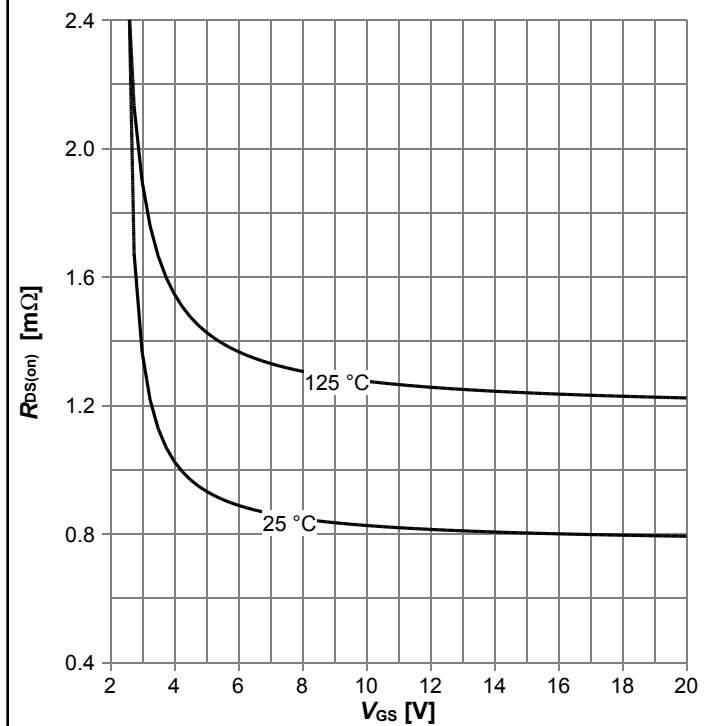
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



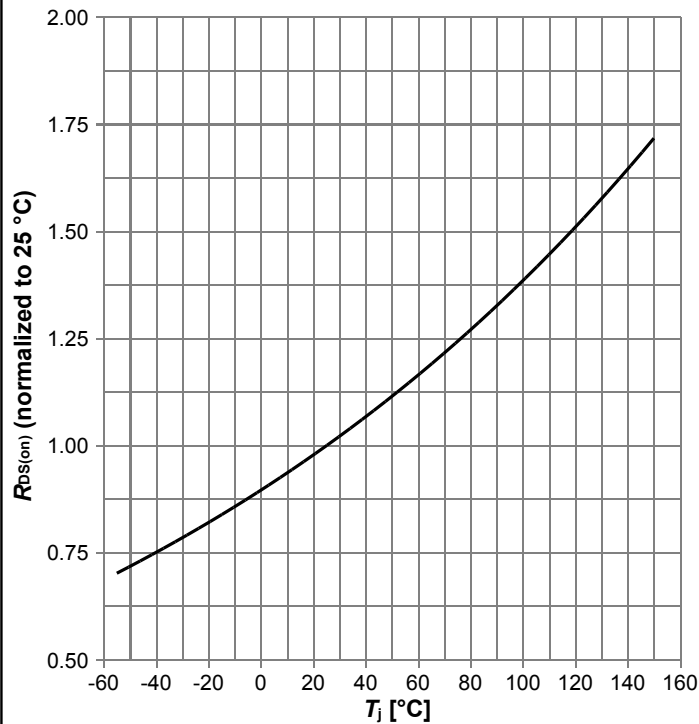
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\text{max}}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



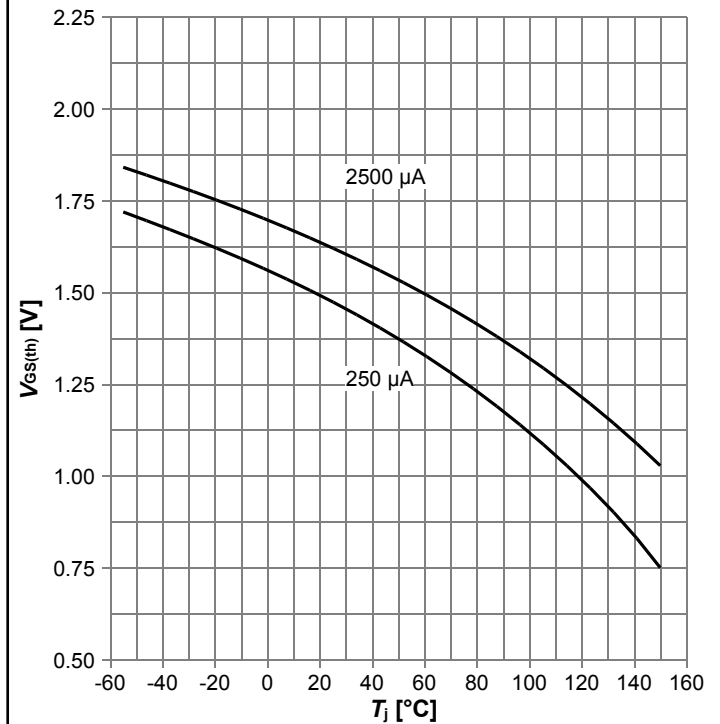
$R_{DS(on)} = f(V_{GS})$, $I_D = 50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



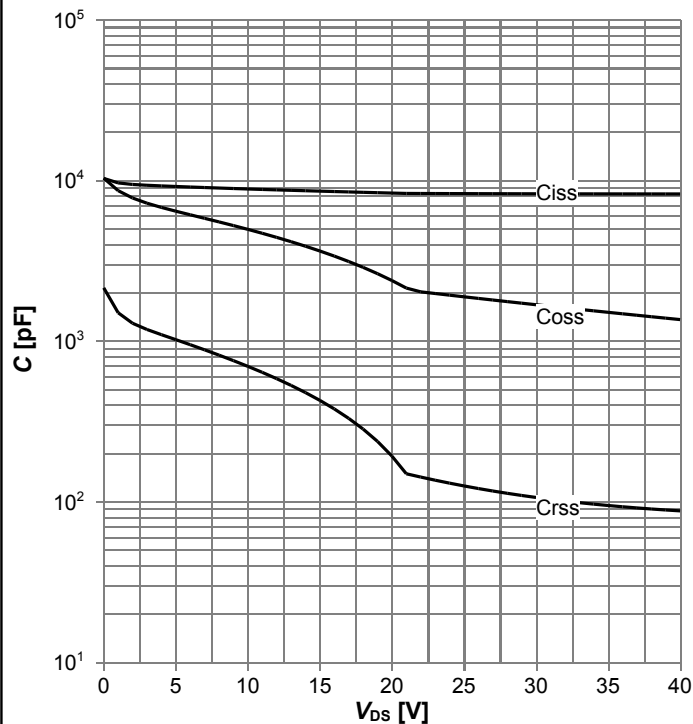
$R_{DS(on)} = f(T_j)$, $I_D = 50$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



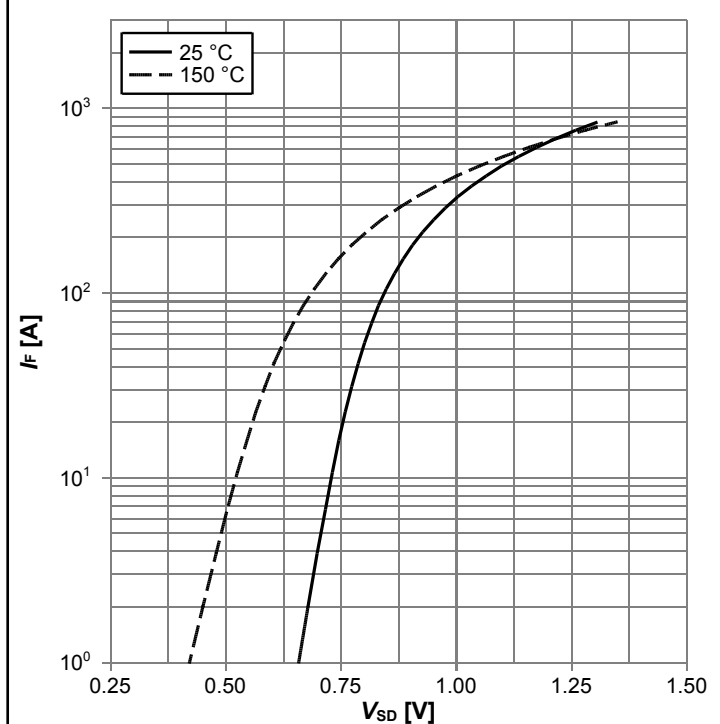
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



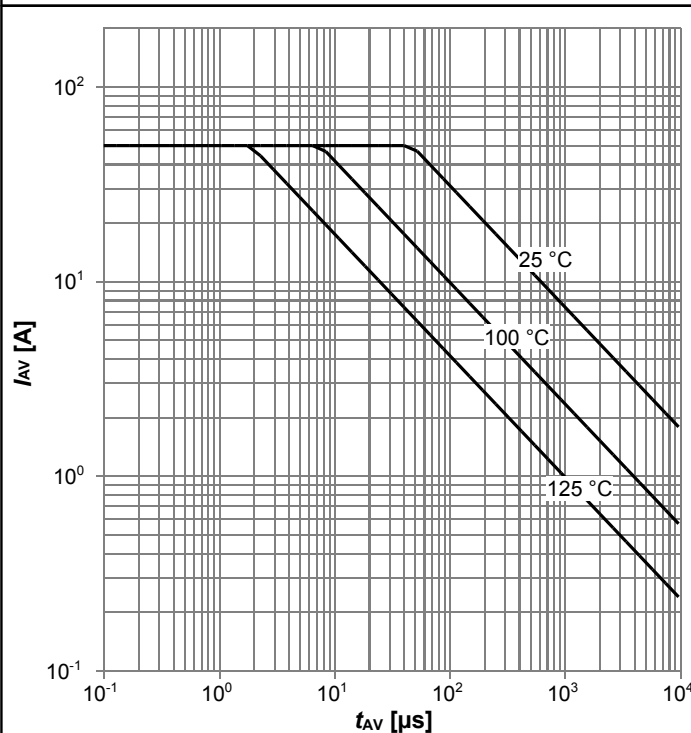
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



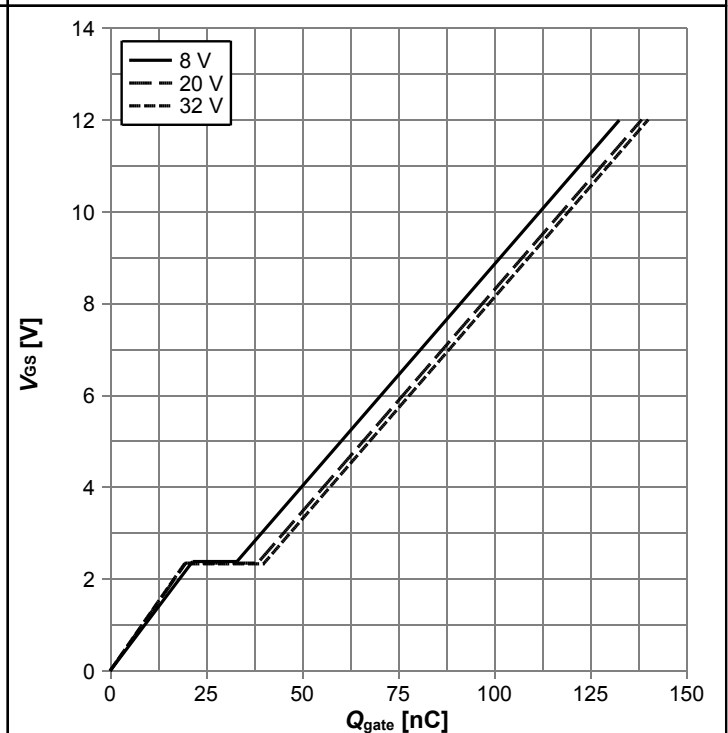
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



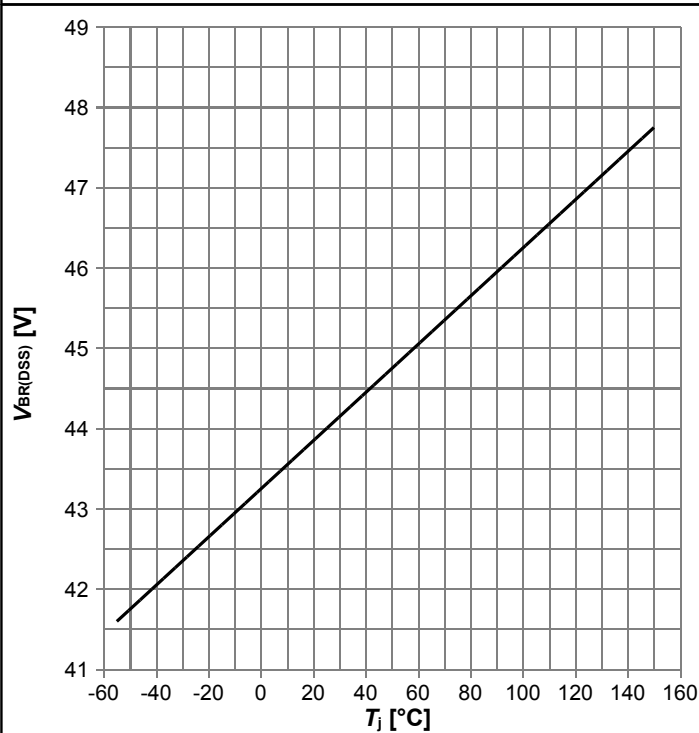
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



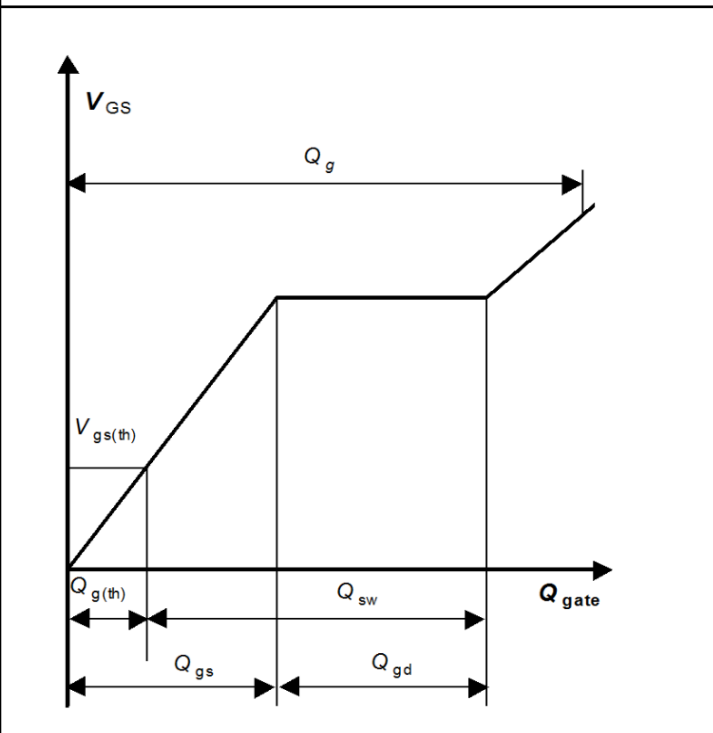
$V_{GS}=f(Q_{gate})$, $I_D=50\ A$ pulsed, $T_j=25\ ^\circ C$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



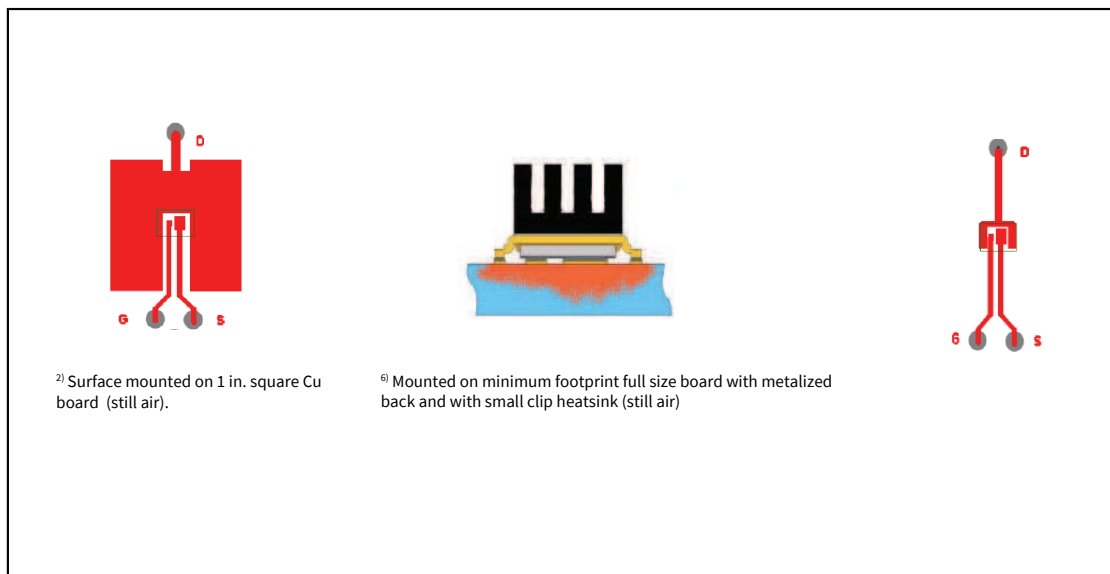
$V_{BR(DSS)}=f(T_j)$; $I_D=1\ mA$

Diagram Gate charge waveforms

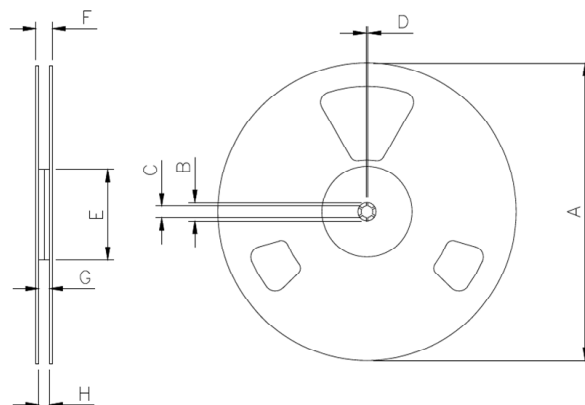


5 Test Circuits

Table 8 Rth/Zth measurement diagrams



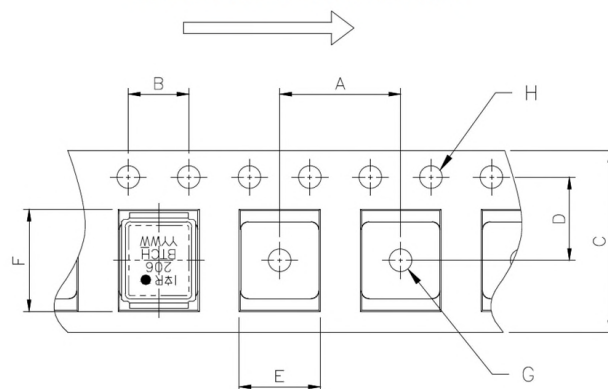
6 Package Outlines



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts, ordered as IRL40DM247

REEL DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606

LOADED TAPE FEED DIRECTION

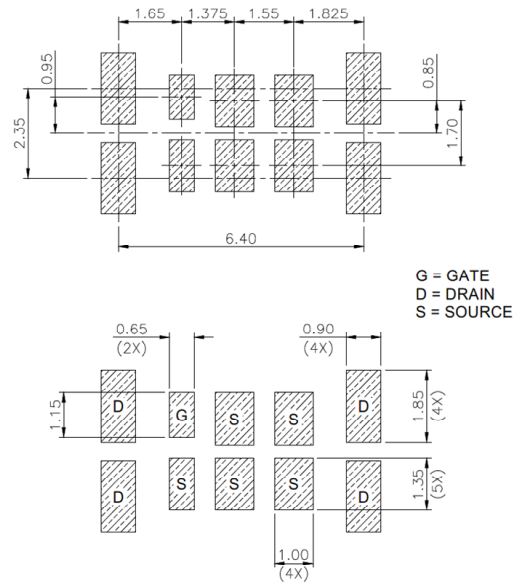


NOTE: CONTROLLING
DIMENSIONS IN MM

DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Figure 1 Outline Tape (MG-WDSO-8-904 (ME), dimensions in mm/inches

PCB Footprint



STENCIL Footprint

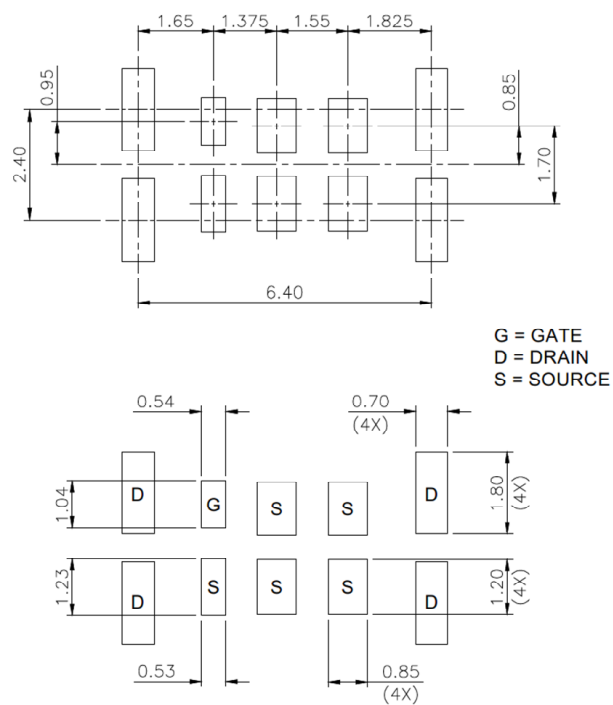
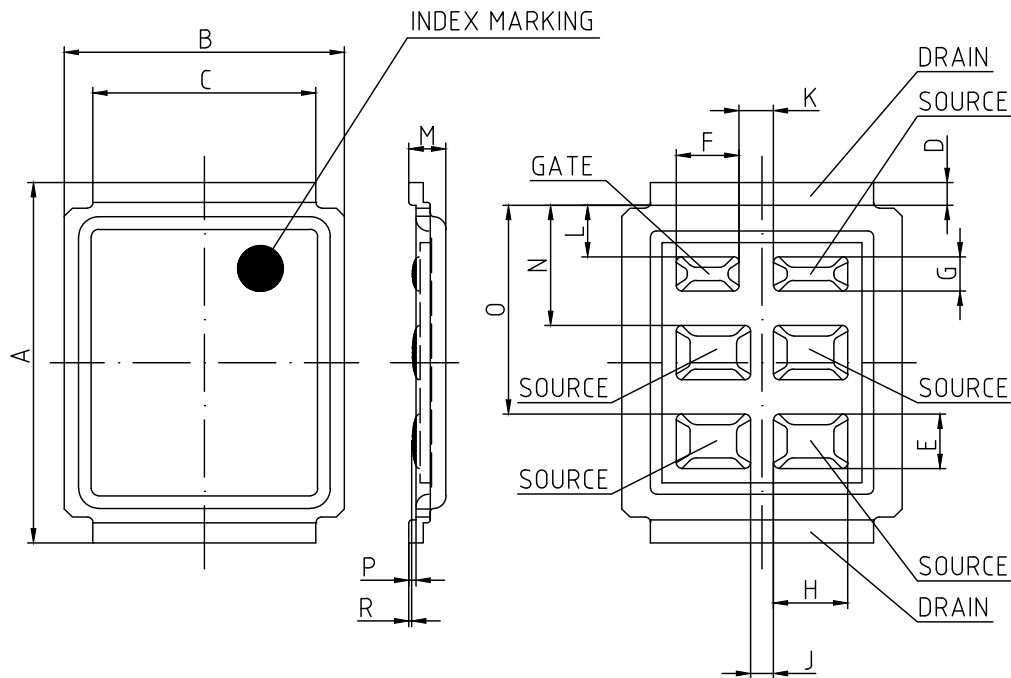


Figure 2 Outline Boardpad (MG-WDSO-8-904 (ME), dimensions in mm



DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	6.25	6.35
B	4.80	5.05
C	3.85	3.95
D	0.35	0.45
E	0.93	0.97
F	1.08	1.12
G	0.58	0.62
H	1.28	1.32
J	0.38	0.42
K	0.58	0.62
L	0.83	0.97
M	-	0.70
N	2.03	2.17
O	3.58	3.72
P	0.08	0.17
R	0.00	0.10

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Figure 3 Outline MG-WDSO-8-904 (ME), dimensions in mm/inches

Revision History

IRL40DM247

Revision: 2022-08-30, Rev. 2.5

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-10-30	Release of final version
2.1	2020-03-05	Update Max Qg- page 5
2.2	2020-03-05	Update Application
2.3	2020-09-21	Update Rth from 1.6C/W to 2.0C/W
2.4	2020-09-29	Rth symbol corrected from RTHJA to RTHJ-PCB in table 3
2.5	2022-08-30	Update the Storage and operating temperature and reflow MSL3

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