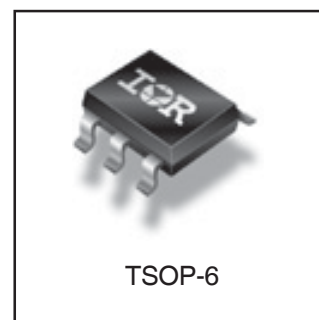
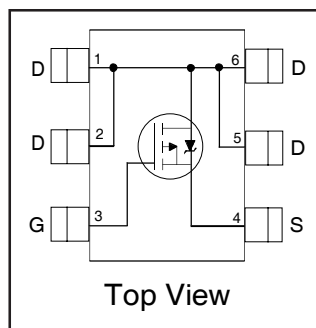


IRFTS9342PbF

HEXFET® Power MOSFET

V_{DS}	-30	V
$V_{GS\ max}$	±20	V
$R_{DS(on)\ max}$ (@ $V_{GS} = -10V$)	40	mΩ
$R_{DS(on)\ max}$ (@ $V_{GS} = -4.5V$)	66	mΩ
$Q_g\ typ$	12	nC
I_D (@ $T_A = 25^\circ C$)	-5.8	A



Applications

- Battery operated DC motor inverter MOSFET
- System/Load Switch

Features and Benefits

Features

Industry-Standard TSOP-6 Package
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Consumer Qualification

results in



Benefits

Multi-Vendor Compatibility
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFTS9342TRPbF	TSOP-6	Tape and Reel	3000	

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	±20	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	-5.8	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	-4.6	
I_{DM}	Pulsed Drain Current ①	-46	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.0	W
$P_D @ T_A = 70^\circ C$	Power Dissipation	1.3	
	Linear Derating Factor	0.02	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Notes ① through ④ are on page 2

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	19	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	32	40	m Ω	$V_{GS} = -10V, I_D = -5.8A$ ③
		—	53	66		$V_{GS} = -4.5V, I_D = -4.6A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.3	—	-2.4	V	$V_{DS} = V_{GS}, I_D = -25\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.5	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-150		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
g_{fs}	Forward Transconductance	6.8	—	—	S	$V_{DS} = -10V, I_D = -4.6A$
Q_g	Total Gate Charge	—	12	—	nC	$V_{DS} = -15V$
Q_{gs}	Gate-to-Source Charge	—	1.8	—		$V_{GS} = -10V$
Q_{gd}	Gate-to-Drain Charge	—	3.1	—		$I_D = -4.6A$
R_G	Gate Resistance	—	17	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	4.6	—	ns	$V_{DD} = -15V, V_{GS} = -10V$ $I_D = -4.6A$ $R_G = 6.8\Omega$
t_r	Rise Time	—	13	—		
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		
t_f	Fall Time	—	28	—		
C_{iss}	Input Capacitance	—	595	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	133	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	85	—		$f = 1.0\text{KHz}$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-46		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -4.6A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	20	30	ns	$T_J = 25^\circ\text{C}, I_F = -4.6A, V_{DD} = -24V$
Q_{rr}	Reverse Recovery Charge	—	11	17	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	62.5	$^\circ\text{C/W}$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
 ③ When mounted on 1 inch square copper board.

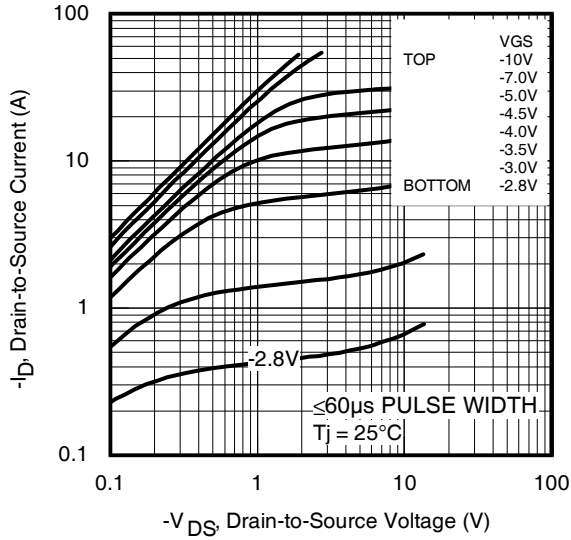


Fig 1. Typical Output Characteristics

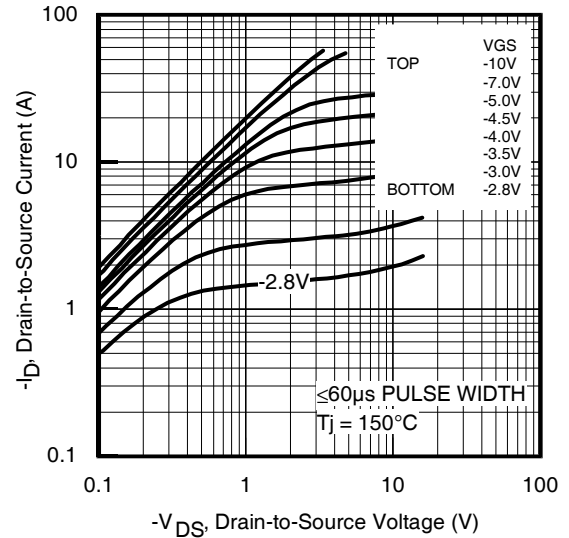


Fig 2. Typical Output Characteristics

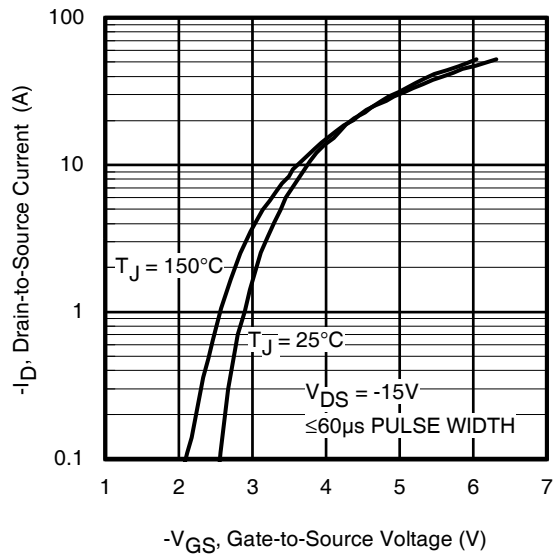


Fig 3. Typical Transfer Characteristics

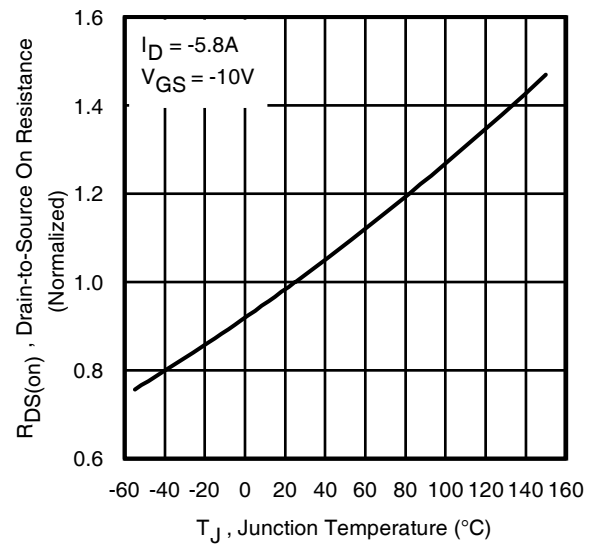


Fig 4. Normalized On-Resistance vs. Temperature

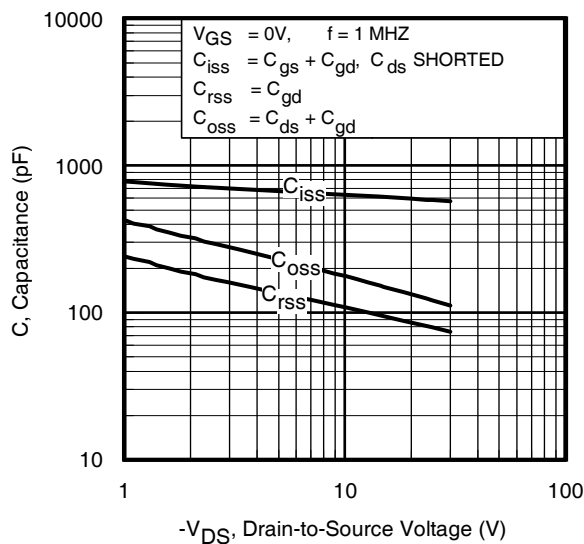


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
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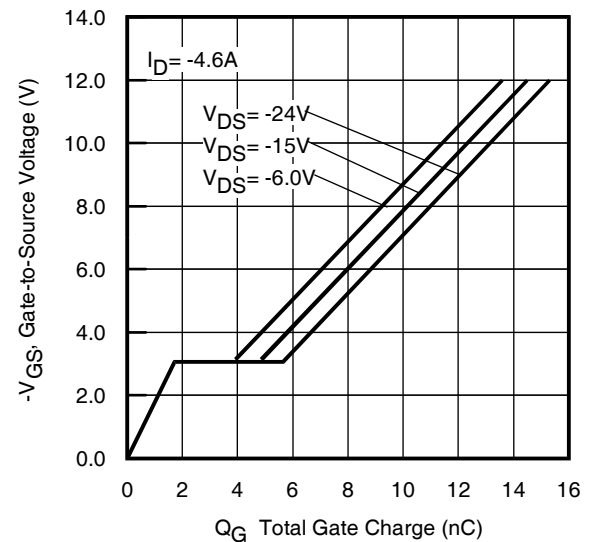


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

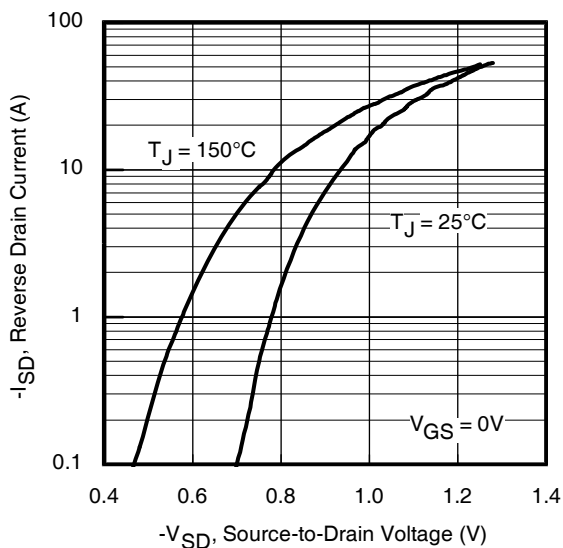


Fig 7. Typical Source-Drain Diode Forward Voltage

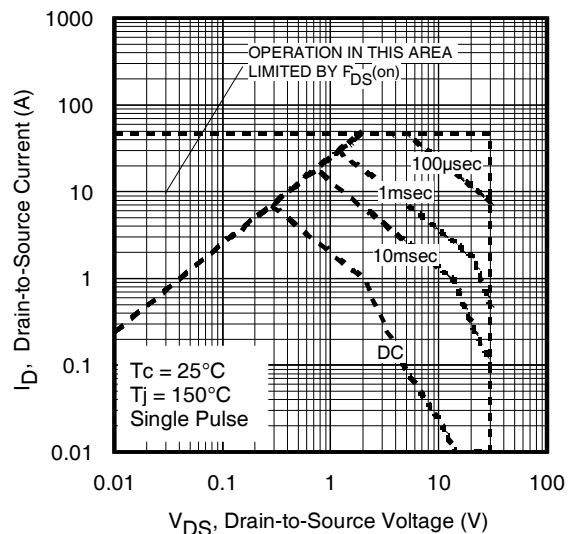


Fig 8. Maximum Safe Operating Area

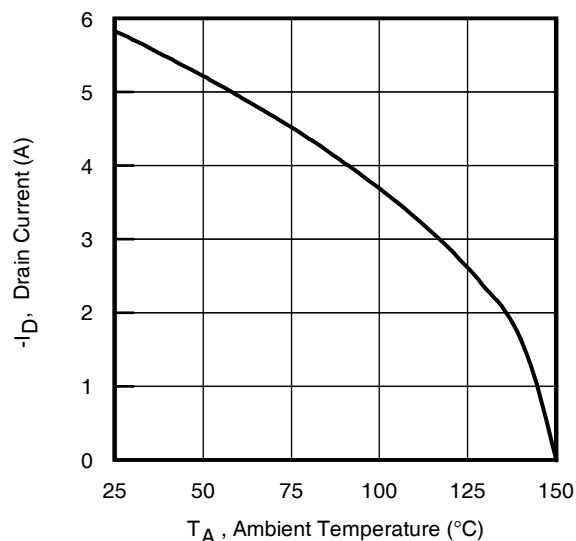


Fig 9. Maximum Drain Current vs. Case Temperature

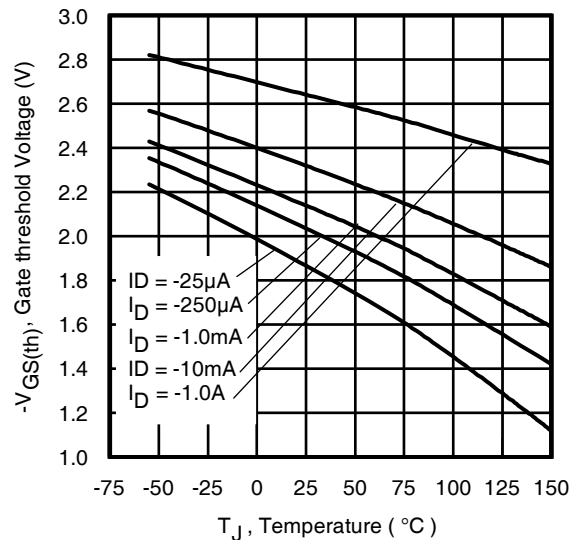


Fig 10. Threshold Voltage vs. Temperature

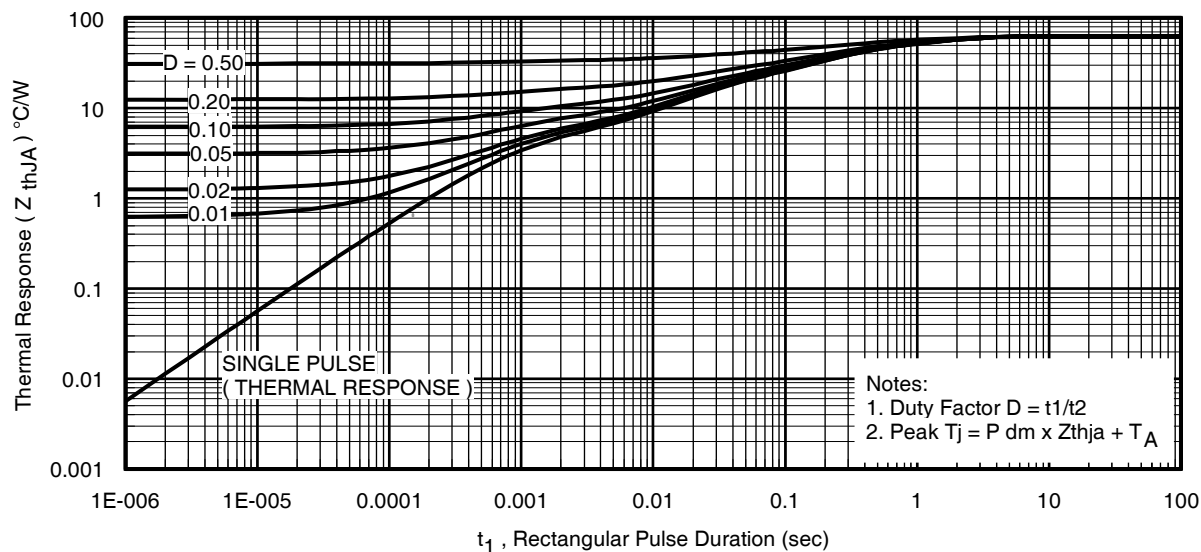


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

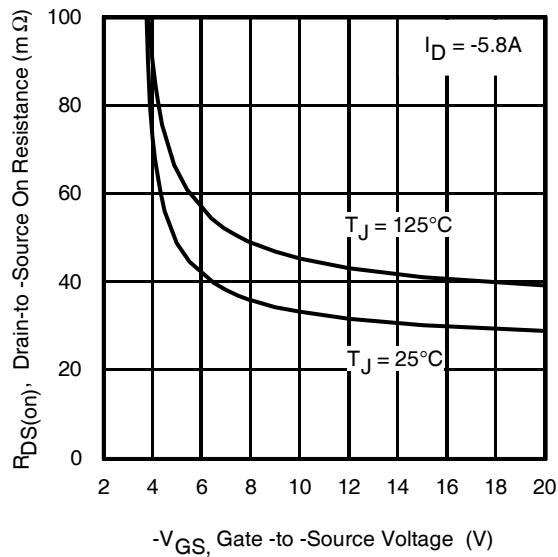


Fig 12. On-Resistance vs. Gate Voltage

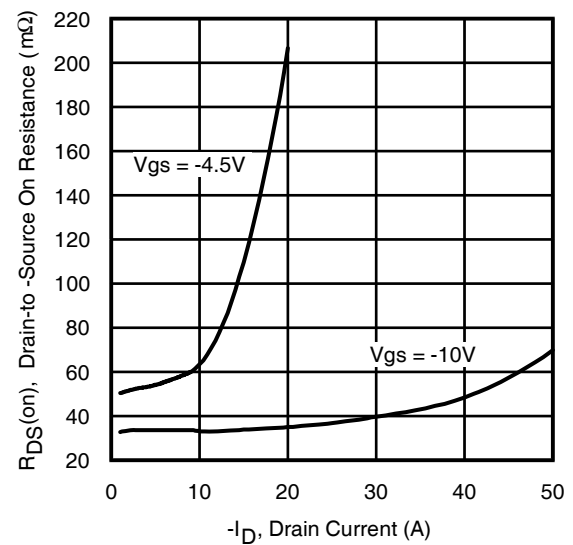


Fig 13. Typical On-Resistance vs. Drain Current

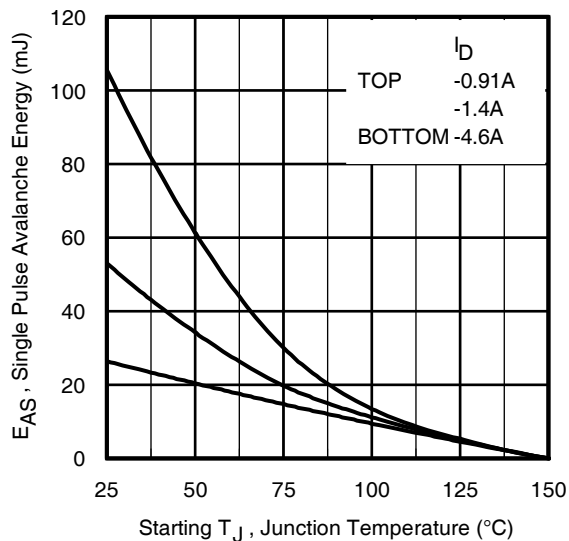


Fig 14. Maximum Avalanche Energy vs. Drain Current

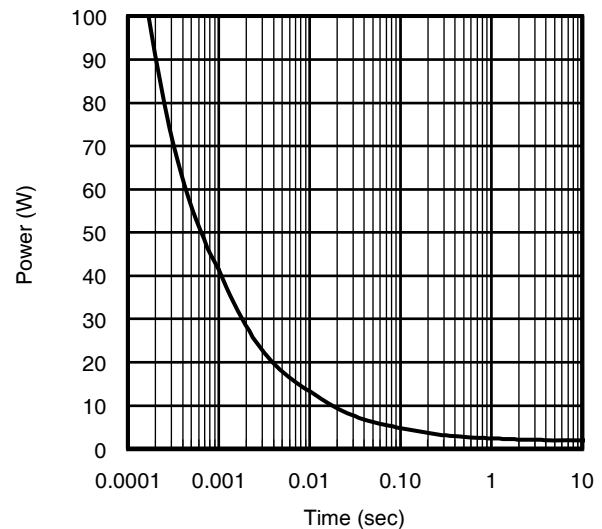
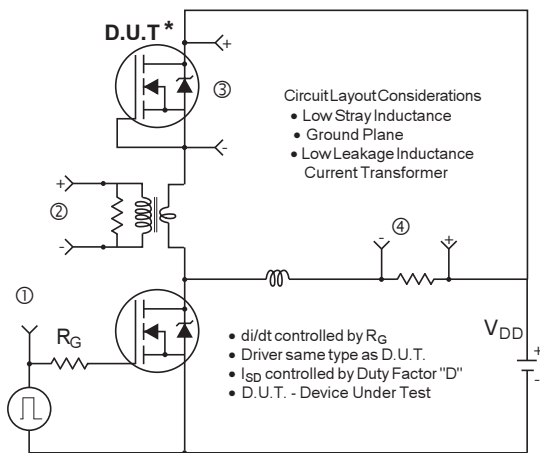
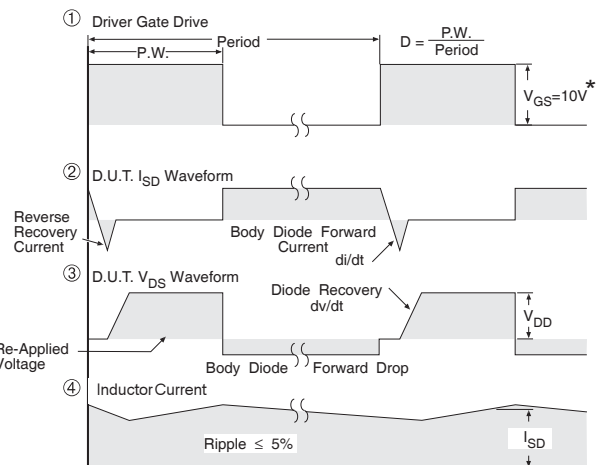


Fig 15. Typical Power vs. Time



* Reverse Polarity of D.U.T. for P-Channel



* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. Diode Reverse Recovery Test Circuit for P-Channel HEXFET® Power MOSFETs

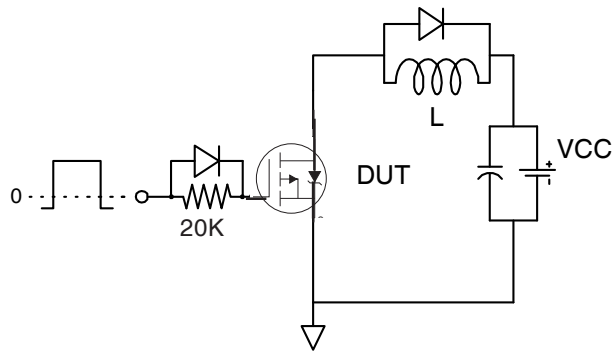


Fig 17a. Gate Charge Test Circuit

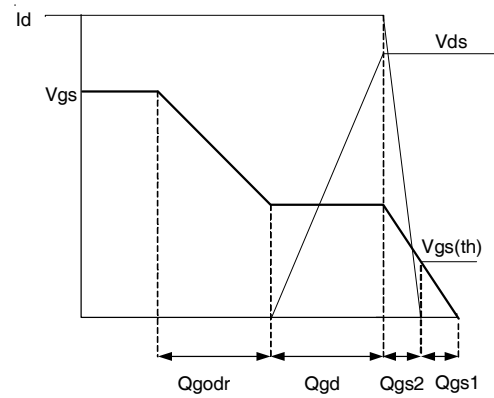


Fig 17b. Gate Charge Waveform

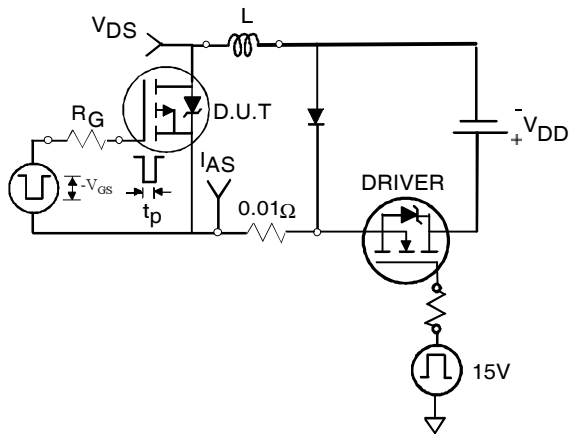


Fig 18a. Unclamped Inductive Test Circuit

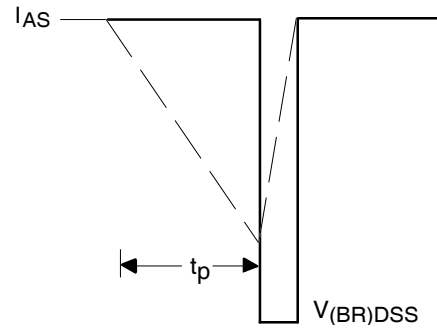


Fig 18b. Unclamped Inductive Waveforms

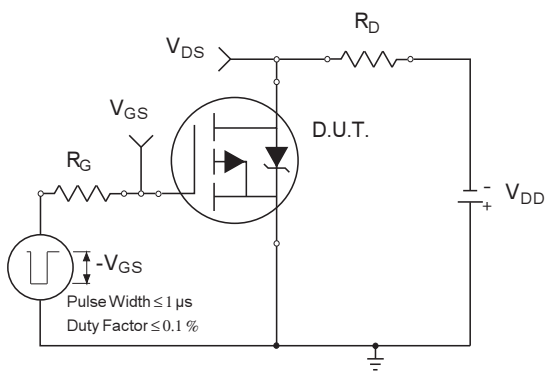


Fig 19a. Switching Time Test Circuit

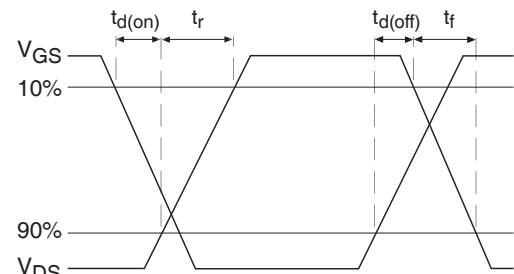


Fig 19b. Switching Time Waveforms

Technical drawing of a mechanical part showing two views: a top view and a side view.

Top View Dimensions:

- Overall width: 3.00 (118)
- Overall height: 2.80 (111)
- Slot widths (top): 1.75 (.068) and 1.50 (.060)
- Slot widths (bottom): 0.95 (.0375) 2X
- Slot depths: 0.50 (.019) and 0.35 (.014) 6X
- Surface finish: 0.15 (.006) (M) C A (S) B (S)

Side View Dimensions:

- Overall width: 3.00 (118)
- Overall height: 2.60 (103)
- Slot widths (top): 1.30 (.051) and 0.90 (.036)
- Slot widths (bottom): 1.45 (.057) and 0.90 (.036)
- Slot depths: 0.15 (.006) MAX.
- Surface finish: 0.10 (.006) 6 SURFA

A diagram of a 3x3 grid. The top row contains the letters D, D, S. The middle row contains the numbers 6, 5, 4. The bottom row contains the numbers .1, 2, 3. The letters D, D, G are positioned below the bottom row of the grid.

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

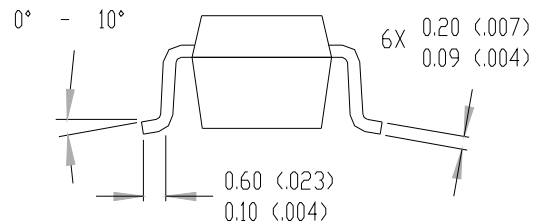


Diagram illustrating the marking layout on a component. The marking is **AYWLC**, where:

- A**: PART NUMBER
- Y**: YEAR
- W**: WEEK
- LC**: LOT CODE

The diagram shows the component from the **TOP** view.

A = SI3443DV	O = IRLTS6342TRPBF
B = IRF5800	P = IRF5800
C = IRF5850	R = IRF5850
D = IRF5851	S = Not applicable
E = IRF5852	T = IRLTS2242TRPBF
F = IRF5801	
G = IRF5803	
H = IRF5804	
I = IRF5805	
J = IRF5806	
K = IRF5810	
N = IRF5802	

WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

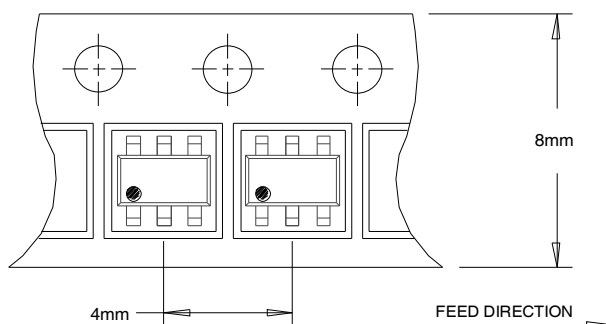
YEAR		Y	WORK WEEK	W
2011	2001	1	01	A
2012	2002	2	02	B
2013	2003	3	03	C
2014	2004	4	04	D
2015	2005	5		
2016	2006	6		
2017	2007	7		
2018	2008	8		
2019	2009	9		
2020	2010	0	24	X
			25	Y
			26	Z

WW = (27-52) IF PRECEDED BY A LETTER

YEAR		Y	WORK WEEK	W
2011	2001	A	27	A
2012	2002	B	28	B
2013	2003	C	29	C
2014	2004	D	30	D
2015	2005	E		
2016	2006	F		
2017	2007	G		
2018	2008	H		
2019	2009	J		
2020	2010	K	50	X
			51	Y
			52	Z

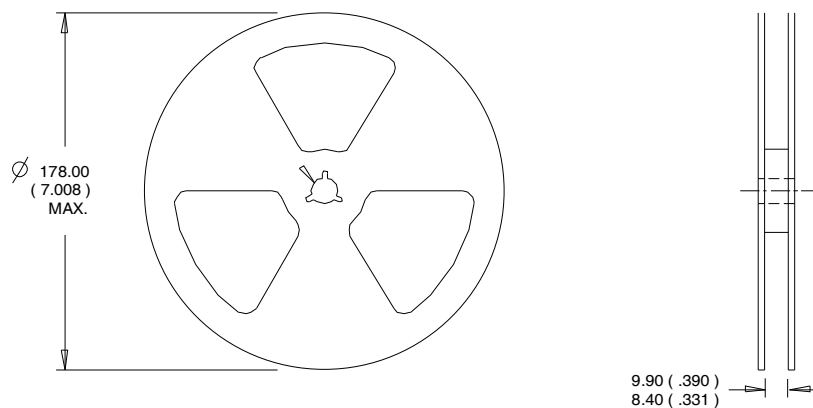
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TSOP-6 Tape and Reel Information



NOTES :

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification information[†]

Qualification level	Consumer ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	TSOP-6	MSL1 (per IPC/JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

International
IR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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