

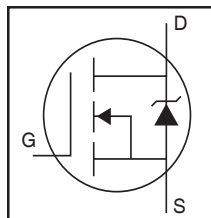
# IRFR4510PbF

# IRFU4510PbF

HEXFET® Power MOSFET

## Applications

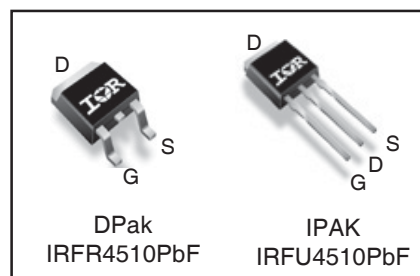
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



|                                        |               |
|----------------------------------------|---------------|
| <b>V<sub>DSS</sub></b>                 | <b>100V</b>   |
| <b>R<sub>DS(on)</sub> typ.</b>         | <b>11.1mΩ</b> |
| <b>max.</b>                            | <b>13.9mΩ</b> |
| <b>I<sub>D</sub> (Silicon Limited)</b> | <b>63A</b>    |
| <b>I<sub>D</sub> (Package Limited)</b> | <b>56A</b>    |

## Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



|          |          |          |
|----------|----------|----------|
| <b>G</b> | <b>D</b> | <b>S</b> |
| Gate     | Drain    | Source   |

## Absolute Maximum Ratings

| Symbol                                  | Parameter                                                         | Max.         | Units |
|-----------------------------------------|-------------------------------------------------------------------|--------------|-------|
| I <sub>D</sub> @ T <sub>C</sub> = 25°C  | Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited) | 63           | A     |
| I <sub>D</sub> @ T <sub>C</sub> = 100°C | Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited) | 45           |       |
| I <sub>D</sub> @ T <sub>C</sub> = 25°C  | Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited) | 56           |       |
| I <sub>DM</sub>                         | Pulsed Drain Current ①                                            | 252          |       |
| P <sub>D</sub> @ T <sub>C</sub> = 25°C  | Maximum Power Dissipation                                         | 143          | W     |
|                                         | Linear Derating Factor                                            | 0.95         | W/°C  |
| V <sub>GS</sub>                         | Gate-to-Source Voltage                                            | ± 20         | V     |
| T <sub>J</sub>                          | Operating Junction and                                            | -55 to + 175 | °C    |
| T <sub>STG</sub>                        | Storage Temperature Range                                         |              |       |
|                                         | Soldering Temperature, for 10 seconds<br>(1.6mm from case)        | 300          |       |

## Avalanche Characteristics

|                                     |                                 |                           |    |
|-------------------------------------|---------------------------------|---------------------------|----|
| E <sub>AS</sub> (Thermally limited) | Single Pulse Avalanche Energy ② | 127                       | mJ |
| I <sub>AR</sub>                     | Avalanche Current ①             | See Fig. 14, 15, 22a, 22b | A  |
| E <sub>AR</sub>                     | Repetitive Avalanche Energy ①   |                           | mJ |

## Thermal Resistance

| Symbol           | Parameter                         | Typ. | Max. | Units |
|------------------|-----------------------------------|------|------|-------|
| R <sub>θJC</sub> | Junction-to-Case ③                | ---  | 1.05 | °C/W  |
| R <sub>θJA</sub> | Junction-to-Ambient (PCB Mount) ⑦ | ---  | 50   |       |
| R <sub>θJA</sub> | Junction-to-Ambient               | ---  | 110  |       |

## ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.

Notes ① through ⑧ are on page 11

www.irf.com

Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

| Symbol                          | Parameter                            | Min. | Typ. | Max. | Units               | Conditions                                            |
|---------------------------------|--------------------------------------|------|------|------|---------------------|-------------------------------------------------------|
| $V_{(BR)DSS}$                   | Drain-to-Source Breakdown Voltage    | 100  | —    | —    | V                   | $V_{GS} = 0V, I_D = 250\mu A$                         |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient  | —    | 0.10 | —    | V/ $^\circ\text{C}$ | Reference to $25^\circ\text{C}$ , $I_D = 5mA$ ①       |
| $R_{DS(on)}$                    | Static Drain-to-Source On-Resistance | —    | 11.1 | 13.9 | m $\Omega$          | $V_{GS} = 10V, I_D = 38A$ ④                           |
| $V_{GS(th)}$                    | Gate Threshold Voltage               | 2.0  | 3.0  | 4.0  | V                   | $V_{DS} = V_{GS}, I_D = 100\mu A$                     |
| $I_{DSS}$                       | Drain-to-Source Leakage Current      | —    | —    | 20   | $\mu A$             | $V_{DS} = 100V, V_{GS} = 0V$                          |
|                                 |                                      | —    | —    | 250  |                     | $V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| $I_{GSS}$                       | Gate-to-Source Forward Leakage       | —    | —    | 100  | nA                  | $V_{GS} = 20V$                                        |
|                                 | Gate-to-Source Reverse Leakage       | —    | —    | -100 |                     | $V_{GS} = -20V$                                       |
| $R_{G(int)}$                    | Internal Gate Resistance             | —    | 0.61 | —    | $\Omega$            |                                                       |

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

| Symbol                      | Parameter                                     | Min. | Typ. | Max. | Units | Conditions                                   |
|-----------------------------|-----------------------------------------------|------|------|------|-------|----------------------------------------------|
| $g_{fs}$                    | Forward Transconductance                      | 62   | —    | —    | S     | $V_{DS} = 25V, I_D = 38A$                    |
| $Q_g$                       | Total Gate Charge                             | —    | 54   | 81   | nC    | $I_D = 38A$                                  |
| $Q_{gs}$                    | Gate-to-Source Charge                         | —    | 14   | —    |       | $V_{DS} = 50V$                               |
| $Q_{gd}$                    | Gate-to-Drain ("Miller") Charge               | —    | 15   | —    |       | $V_{GS} = 10V$ ④                             |
| $Q_{sync}$                  | Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )    | —    | 39   | —    |       | $I_D = 38A, V_{DS} = 0V, V_{GS} = 10V$       |
| $t_{d(on)}$                 | Turn-On Delay Time                            | —    | 18   | —    | ns    | $V_{DD} = 65V$                               |
| $t_r$                       | Rise Time                                     | —    | 42   | —    |       | $I_D = 38A$                                  |
| $t_{d(off)}$                | Turn-Off Delay Time                           | —    | 42   | —    |       | $R_G = 7.5\Omega$                            |
| $t_f$                       | Fall Time                                     | —    | 34   | —    |       | $V_{GS} = 10V$ ④                             |
| $C_{iss}$                   | Input Capacitance                             | —    | 3031 | —    | pF    | $V_{GS} = 0V$                                |
| $C_{oss}$                   | Output Capacitance                            | —    | 213  | —    |       | $V_{DS} = 50V$                               |
| $C_{rss}$                   | Reverse Transfer Capacitance                  | —    | 104  | —    |       | $f = 1.0MHz$                                 |
| $C_{oss \text{ eff. (ER)}}$ | Effective Output Capacitance (Energy Related) | —    | 255  | —    |       | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑥ |
| $C_{oss \text{ eff. (TR)}}$ | Effective Output Capacitance (Time Related)   | —    | 478  | —    |       | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑤ |

## Diode Characteristics

| Symbol    | Parameter                                 | Min.                                                                 | Typ. | Max. | Units | Conditions                                                              |
|-----------|-------------------------------------------|----------------------------------------------------------------------|------|------|-------|-------------------------------------------------------------------------|
| $I_S$     | Continuous Source Current<br>(Body Diode) | —                                                                    | —    | 56   | A     | MOSFET symbol<br>showing the<br>integral reverse<br>p-n junction diode. |
| $I_{SM}$  | Pulsed Source Current<br>(Body Diode) ①   | —                                                                    | —    | 252  |       |                                                                         |
| $V_{SD}$  | Diode Forward Voltage                     | —                                                                    | —    | 1.3  | V     | $T_J = 25^\circ\text{C}, I_S = 38A, V_{GS} = 0V$ ④                      |
| $dv/dt$   | Peak Diode Recovery                       | —                                                                    | 7.0  | —    | V/ns  | $T_J = 175^\circ\text{C}, I_S = 38A, V_{DS} = 100V$ ③                   |
| $t_{rr}$  | Reverse Recovery Time                     | —                                                                    | 34   | —    | ns    | $T_J = 25^\circ\text{C}$ $V_R = 86V$                                    |
|           |                                           | —                                                                    | 39   | —    |       | $T_J = 125^\circ\text{C}$ $I_F = 38A$                                   |
| $Q_{rr}$  | Reverse Recovery Charge                   | —                                                                    | 47   | —    | nC    | $T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ④                         |
|           |                                           | —                                                                    | 61   | —    |       | $T_J = 125^\circ\text{C}$                                               |
| $I_{RRM}$ | Reverse Recovery Current                  | —                                                                    | 2.4  | —    | A     | $T_J = 25^\circ\text{C}$                                                |
| $t_{on}$  | Forward Turn-On Time                      | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) |      |      |       |                                                                         |

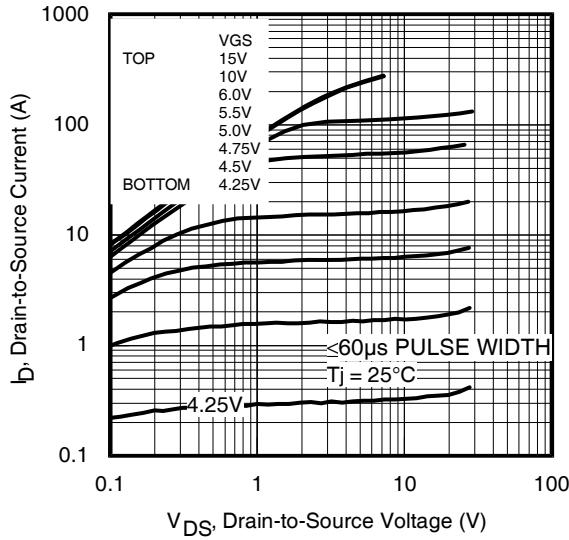


Fig 1. Typical Output Characteristics

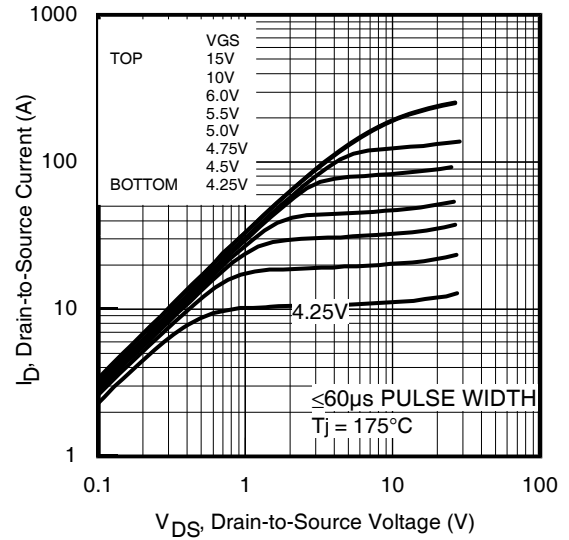


Fig 2. Typical Output Characteristics

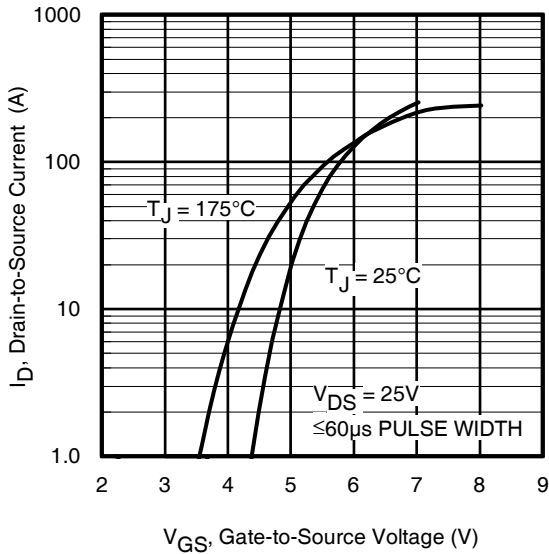


Fig 3. Typical Transfer Characteristics

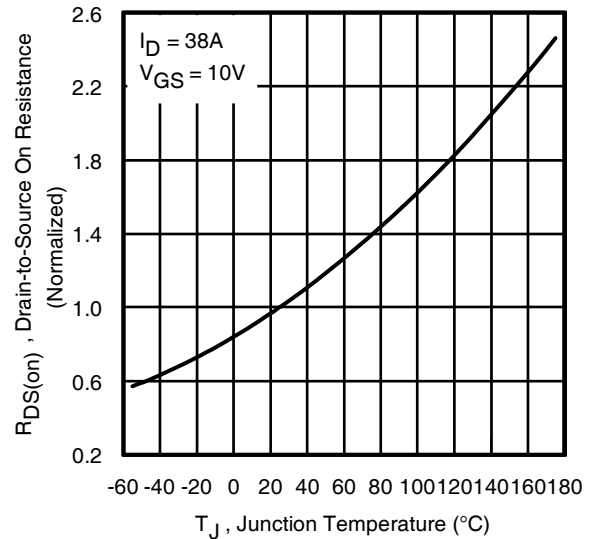


Fig 4. Normalized On-Resistance vs. Temperature

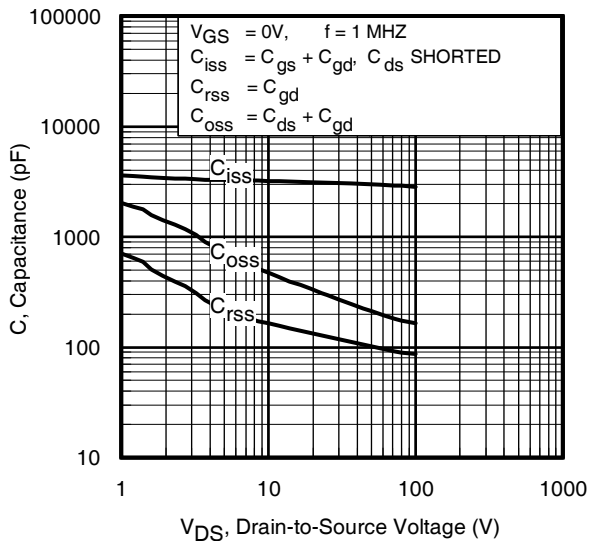


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

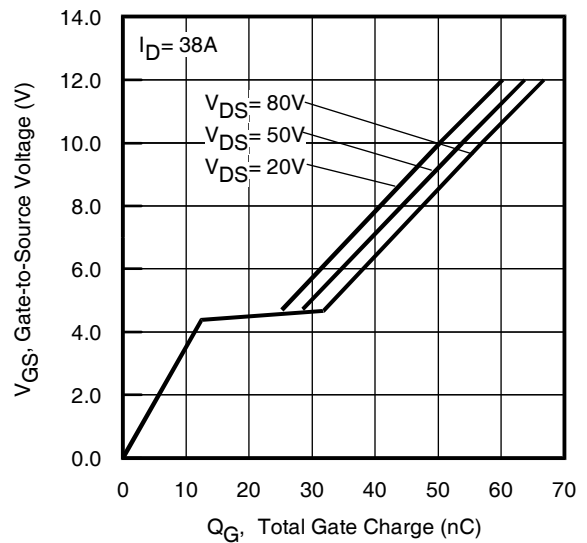
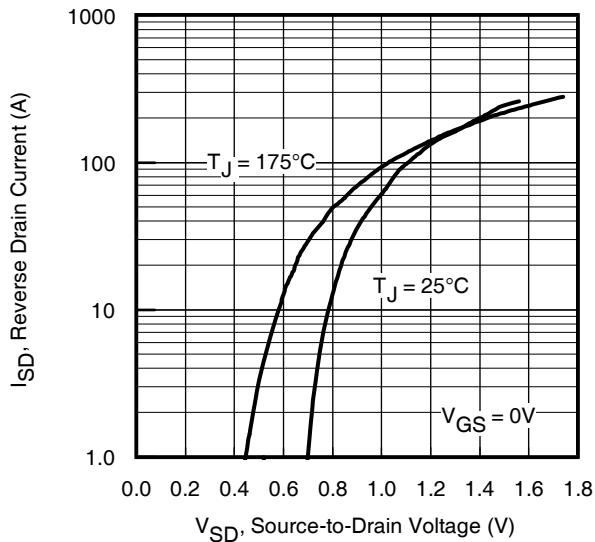
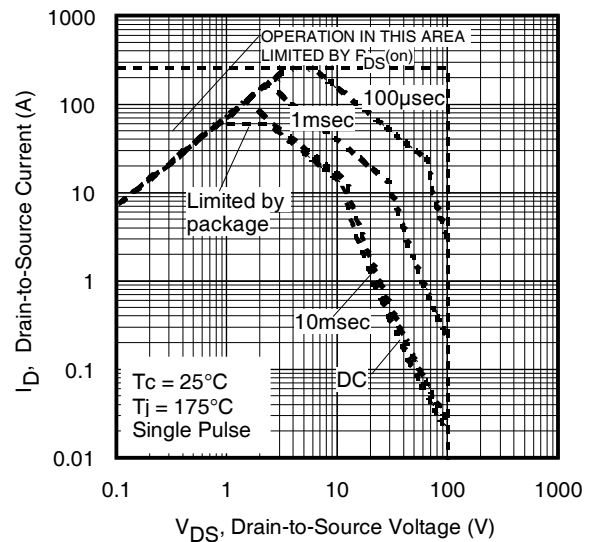


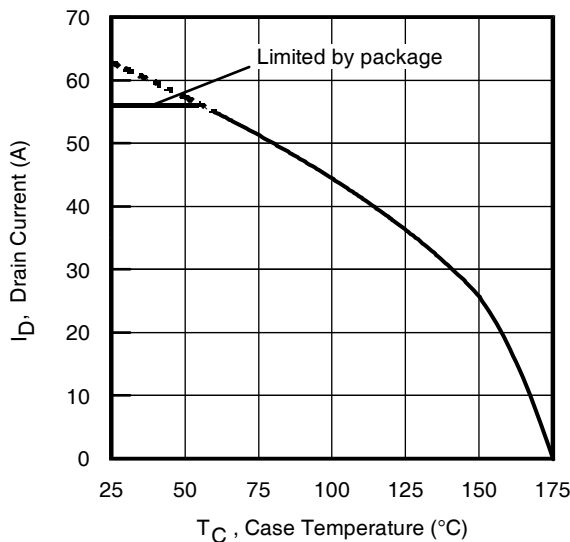
Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



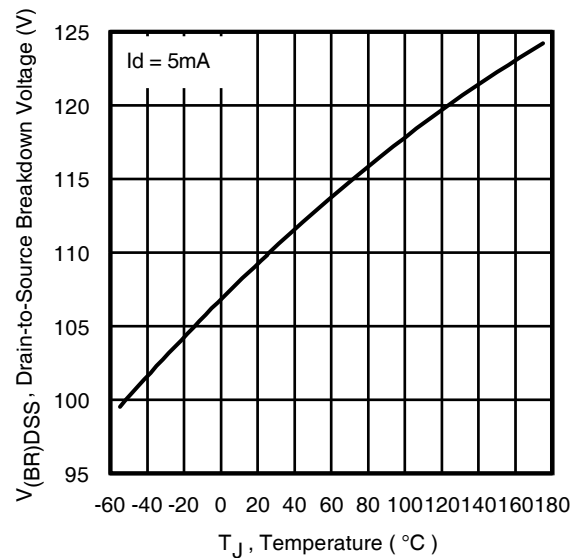
**Fig 7.** Typical Source-Drain Diode Forward Voltage



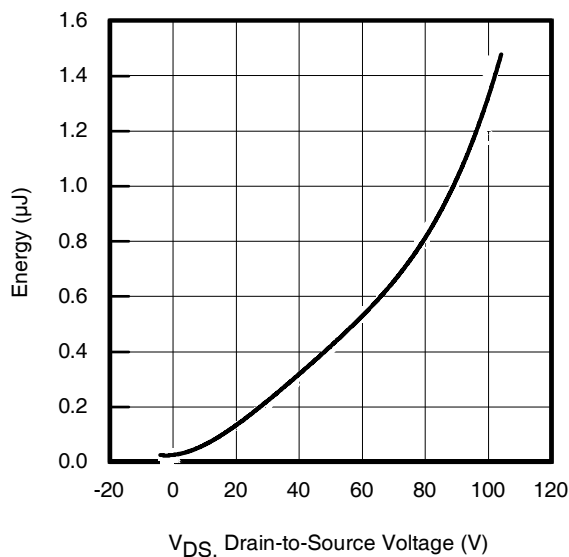
**Fig 8.** Maximum Safe Operating Area



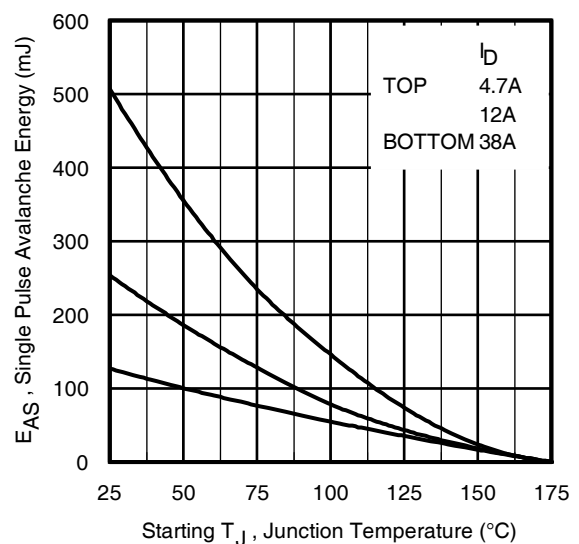
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

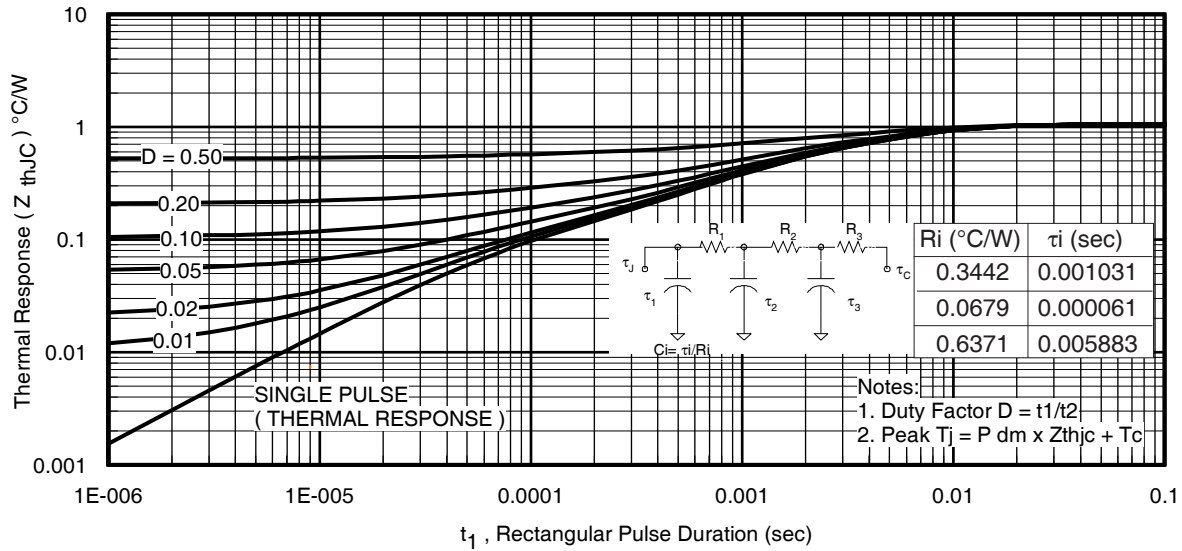


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

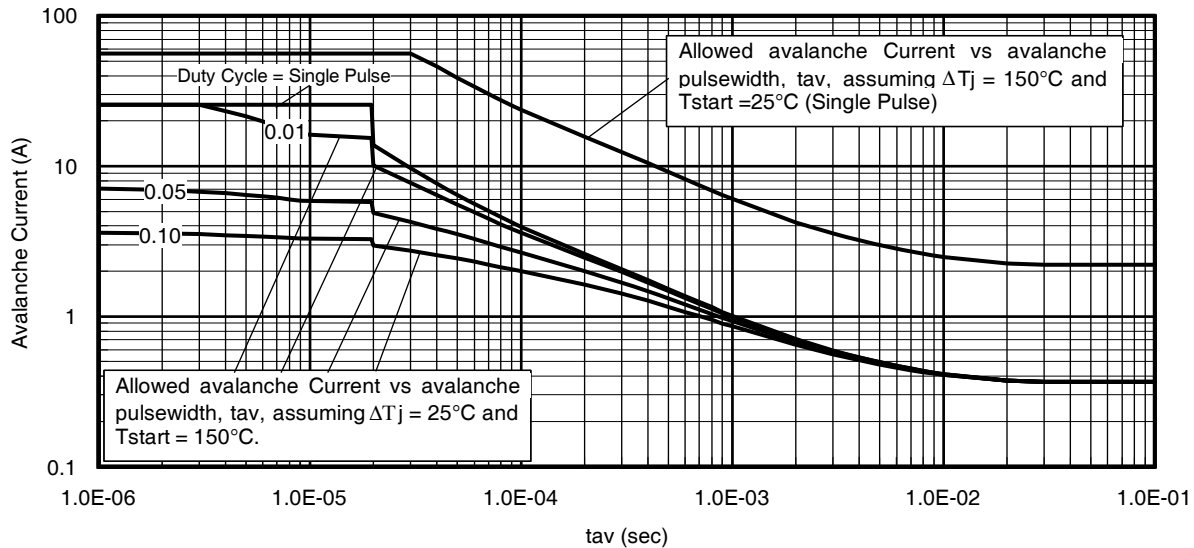


Fig 14. Typical Avalanche Current vs. Pulsewidth

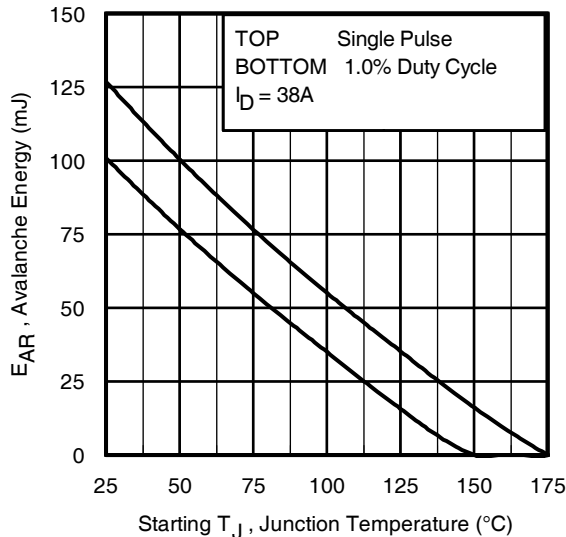


Fig 15. Maximum Avalanche Energy vs. Temperature

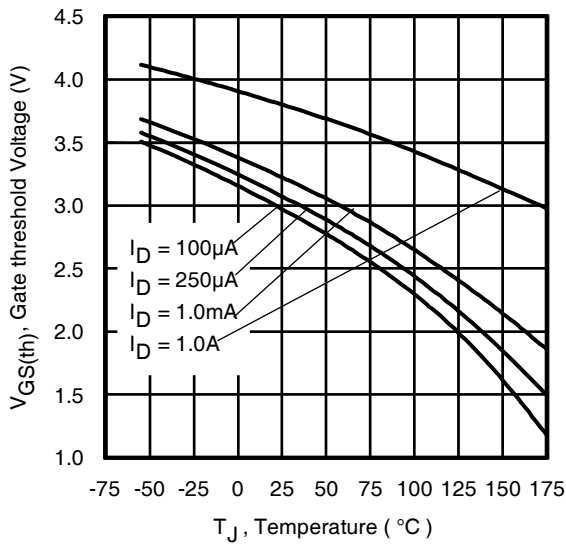
**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^{\circ}\text{C}$  in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

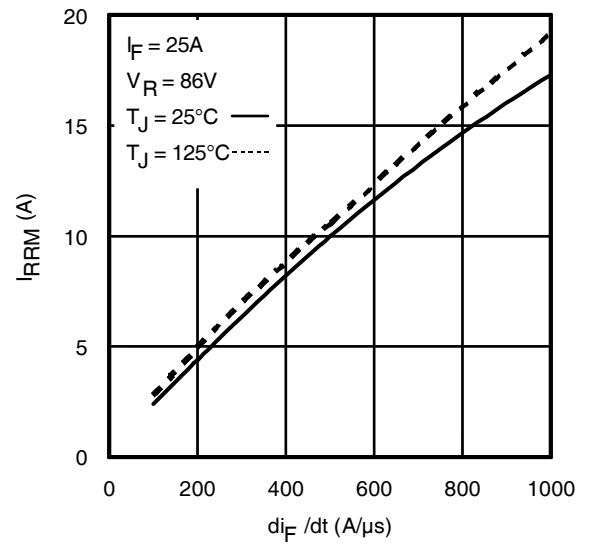
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

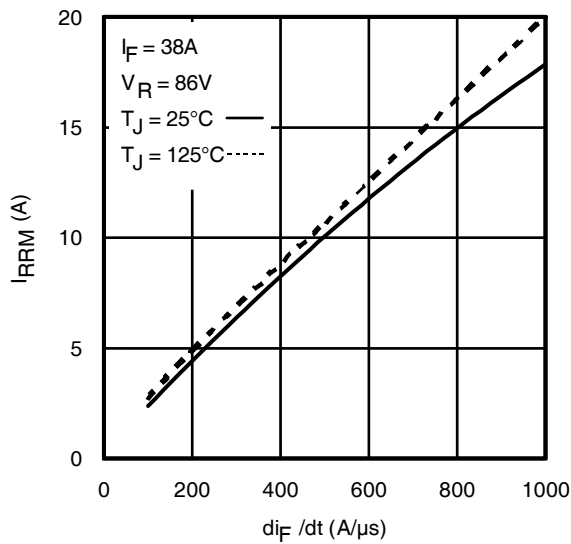
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



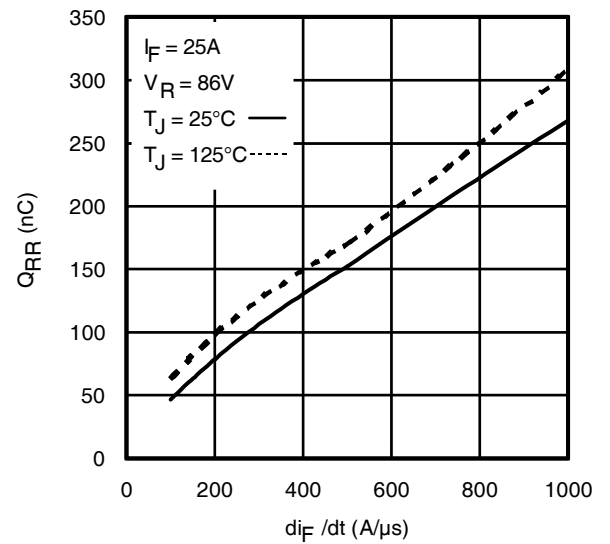
**Fig. 16.** Threshold Voltage vs. Temperature



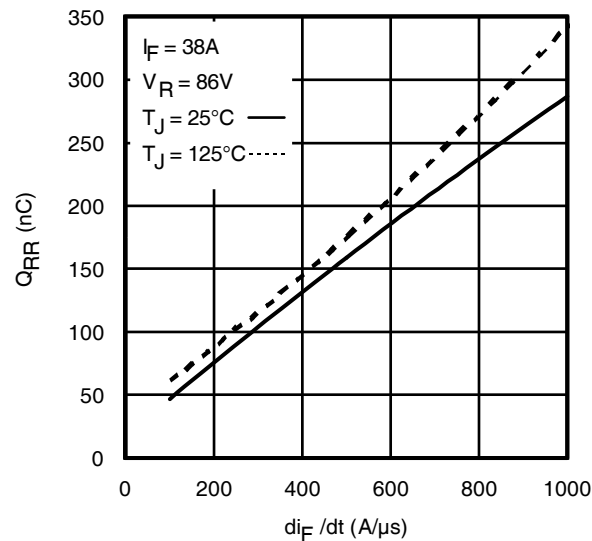
**Fig. 17 -** Typical Recovery Current vs.  $di_F/dt$



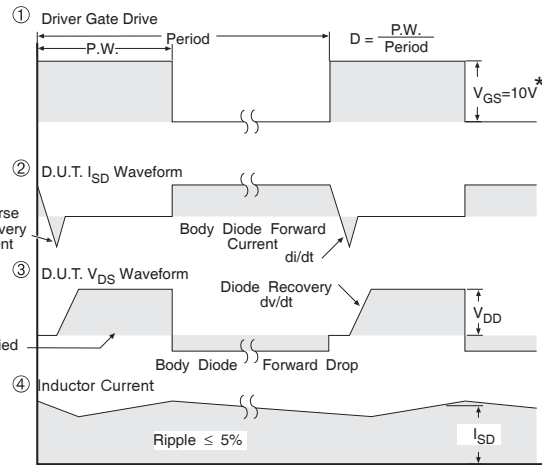
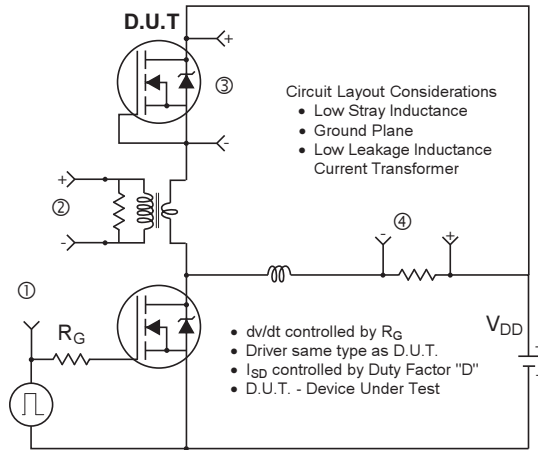
**Fig. 18 -** Typical Recovery Current vs.  $di_F/dt$



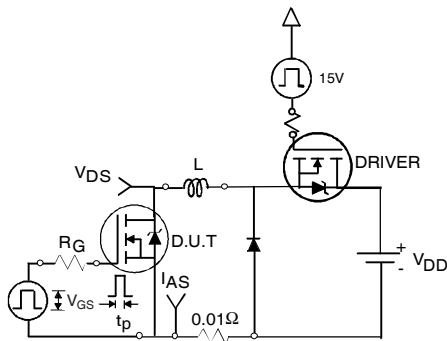
**Fig. 19 -** Typical Stored Charge vs.  $di_F/dt$



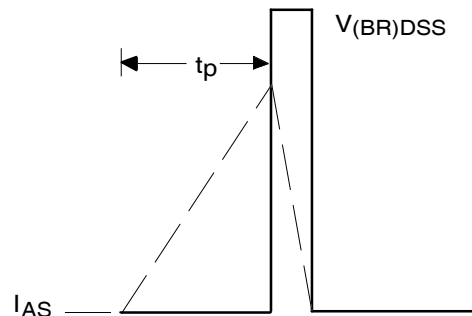
**Fig. 20 -** Typical Stored Charge vs.  $di_F/dt$



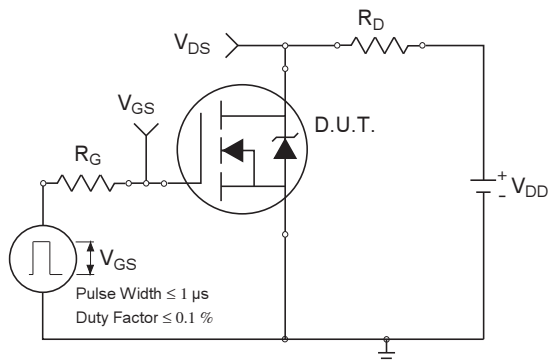
**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



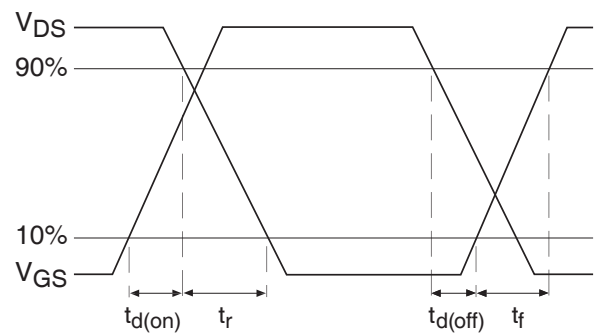
**Fig 22a. Unclamped Inductive Test Circuit**



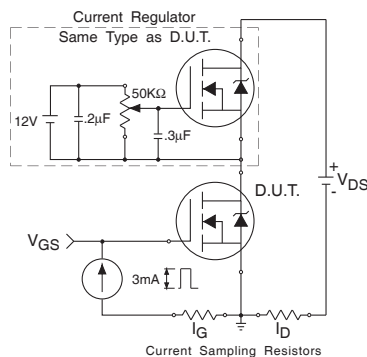
**Fig 22b. Unclamped Inductive Waveforms**



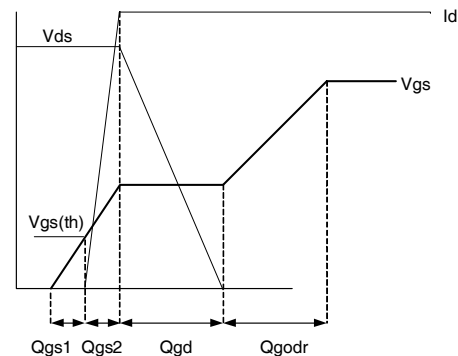
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



**Fig 24a. Gate Charge Test Circuit**



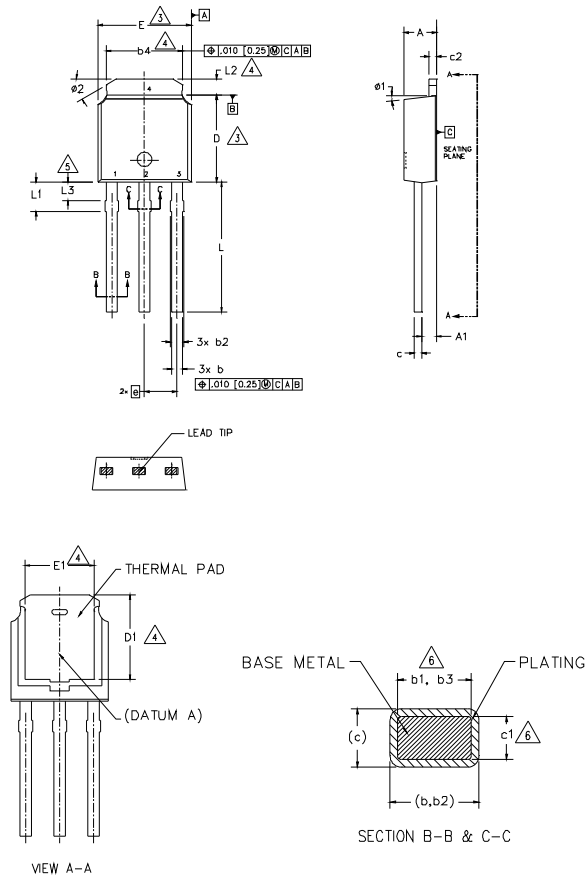
**Fig 24b. Gate Charge Waveform**





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5.- LEAD DIMENSION UNCONTROLLED IN L3.
- 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS  |      |          |      | NOTES |
|--------|-------------|------|----------|------|-------|
|        | MILLIMETERS |      | INCHES   |      |       |
|        | MIN.        | MAX. | MIN.     | MAX. |       |
|        |             |      |          |      |       |
| A      | 2.18        | 2.39 | .086     | .094 |       |
| A1     | 0.89        | 1.14 | .035     | .045 |       |
| b      | 0.64        | 0.89 | .025     | .035 |       |
| b1     | 0.65        | 0.79 | .025     | .031 | 6     |
| b2     | 0.76        | 1.14 | .030     | .045 |       |
| b3     | 0.76        | 1.04 | .030     | .041 | 6     |
| b4     | 4.95        | 5.46 | .195     | .215 | 4     |
| c      | 0.46        | 0.61 | .018     | .024 |       |
| c1     | 0.41        | 0.56 | .016     | .022 | 6     |
| c2     | 0.46        | 0.89 | .018     | .035 |       |
| D      | 5.97        | 6.22 | .235     | .245 | 3     |
| D1     | 5.21        | —    | .205     | —    | 4     |
| E      | 6.35        | 6.73 | .250     | .265 | 3     |
| E1     | 4.32        | —    | .170     | —    | 4     |
| e      | 2.29 BSC    |      | .090 BSC |      |       |
| L      | 8.89        | 9.65 | .350     | .380 |       |
| L1     | 1.91        | 2.29 | .045     | .090 |       |
| L2     | 0.89        | 1.27 | .035     | .050 | 4     |
| L3     | 1.14        | 1.52 | .045     | .060 | 5     |
| ø1     | 0°          | 15°  | 0°       | 15°  |       |
| ø2     | 25°         | 35°  | 25°      | 35°  |       |

### LEAD ASSIGNMENTS

### HEXFET

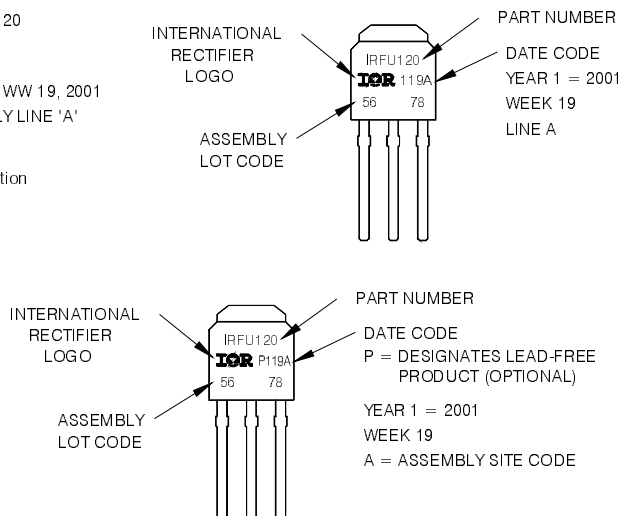
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position  
indicates Lead-Free'

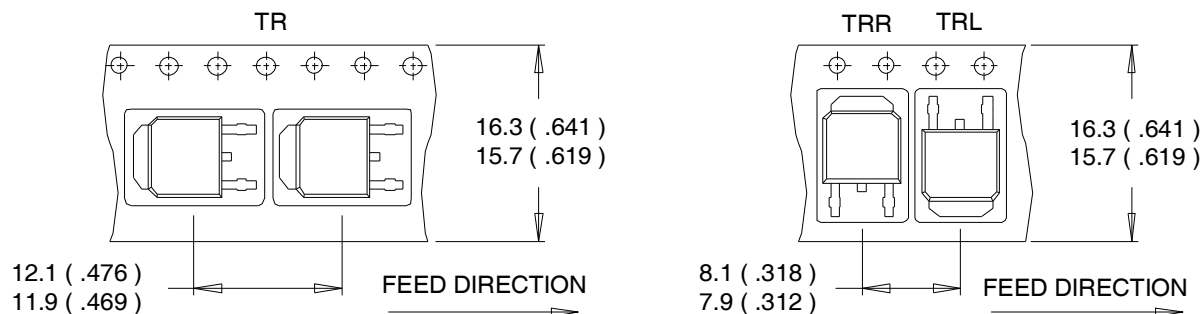
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>  
[www.irf.com](http://www.irf.com)

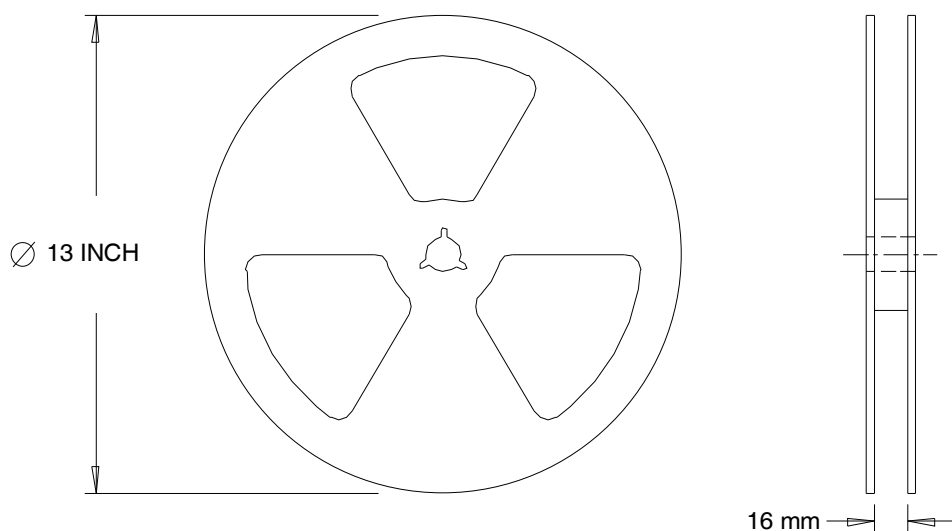
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



### NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



### NOTES :

1. OUTLINE CONFORMS TO EIA-481.

| Orderable part number | Package Type | Standard Pack |          | Note |
|-----------------------|--------------|---------------|----------|------|
|                       |              | Form          | Quantity |      |
| IRFR4510PbF           | D-PAK        | Tube/Bulk     | 75       |      |
| IRFR4510TRPbF         | D-PAK        | Tape and Reel | 2000     |      |
| IRFU4510PbF           | I-PAK        | Tube/Bulk     | 75       |      |

### Qualification Information<sup>†</sup>

|                            |                                                                                                                                                                          |                                                |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|
| Qualification level        | Industrial <sup>††</sup>                                                                                                                                                 |                                                |
|                            | (per JEDEC JESD47F <sup>†††</sup> guidelines)                                                                                                                            |                                                |
|                            | Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. |                                                |
| Moisture Sensitivity Level | D-PAK                                                                                                                                                                    | MSL1<br>(per JEDEC J-STD-020D <sup>†††</sup> ) |
|                            | I-PAK                                                                                                                                                                    | Not applicable                                 |
| RoHS Compliant             | Yes                                                                                                                                                                      |                                                |

<sup>†</sup> Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

<sup>††</sup> Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

<sup>†††</sup> Applicable version of JEDEC standard at the time of product release.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.18\text{mH}$   
 $R_G = 50\Omega$ ,  $I_{AS} = 38\text{A}$ ,  $V_{GS} = 10\text{V}$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 38\text{A}$ ,  $di/dt \leq 2031\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

- ⑤  $C_{OSS}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{OSS}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice

International  
IR Rectifier

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